nature COMMUNICATIONS

ARTICLE

Received 12 Aug 2013 | Accepted 12 Mar 2014 | Published 4 Apr 2014

DOI: 10.1038/ncomms4637

Fabrication and operation of a two-dimensional ion-trap lattice on a high-voltage microchip

R.C. Sterling[1], H. Rattanasonti[2], S. Weidt[1], K. Lake[1], P. Srinivasan[2], S.C. Webster[1], M. Kraft[2,3] & W.K. Hensinger[1]

Microfabricated ion traps are a major advancement towards scalable quantum computing with trapped ions. The development of more versatile ion-trap designs, in which tailored arrays of ions are positioned in two dimensions above a microfabricated surface, will lead to applications in fields as varied as quantum simulation, metrology and atom–ion interactions. Current surface ion traps often have low trap depths and high heating rates, because of the size of the voltages that can be applied to them, limiting the fidelity of quantum gates. Here we report on a fabrication process that allows for the application of very high voltages to microfabricated devices in general and use this advance to fabricate a two-dimensional ion-trap lattice on a microchip. Our microfabricated architecture allows for reliable trapping of two-dimensional ion lattices, long ion lifetimes, rudimentary shuttling between lattice sites and the ability to deterministically introduce defects into the ion lattice.

[1] Department of Physics and Astronomy, University of Sussex, Brighton BN1 9QH, UK. [2] School of Electronics and Computer Science, University of Southampton, Southampton SO17 1BJ, UK. [3] University of Duisburg-Essen, Faculty of Engineering Sciences, Bismarkstrasse 81, Duisburg D-47059, Germany. Correspondence and requests for materials should be addressed to W.K.H. (email: W.K.Hensinger@sussex.ac.uk).

© 2014 Macmillan Publishers Limited. All rights reserved.

The introduction of microfabrication techniques to the field of ion trapping has lead to the development of impressive microfabricated radio-frequency (RF) ion-trap devices[1]. Using such devices, many of the building blocks for scalable quantum computing have been demonstrated[2], including ion combination and separation and junction shuttling[3,4] as well as two-qubit gate operations[5,6].

A drawback of current microfabricated ion traps stems from the ions at the RF null naturally forming a one-dimensional string, so far, limiting their usefulness for applications that require the formation of arbitrary two-dimensional (2D) ion lattices. Penning traps offer a platform for a 2D lattice of ions, but the rotating crystal makes individual ion addressing and readout experimentally challenging, and the lattice geometry is limited to the naturally forming Wigner crystal[7].

The applications for a 2D ion lattice are numerous and far reaching, including, among others, spatial magnetic and electric field sensing[8–10], force detection[11], interactions between neutral atoms and ions[12] and cluster state quantum computing[13].

A further exciting application for a 2D ion lattice is in the field of analogue quantum simulation where the Hamiltonian of a complicated many-body system can be realized and its properties measured[14,15]. A promising approach to realizing a 2D quantum simulator is the proposal to use a 2D lattice of individual RF ion traps[16–18]. Each lattice site contains a single ion, which interacts with neighbouring ions via the Coulomb force. The current challenge lies in developing microfabrication techniques that allow for a tightly spaced ion lattice to be obtained where the ion–ion separation is small enough for coherent interactions to be measured. To date, experimental progress towards such a lattice has been limited to trapping dust particles and ion clouds above printed circuit boards[19] or wire meshes[20]. The optimum trap geometry of such a device has been well studied[21,22].

In operating a microfabricated ion surface trap, restrictions on the RF voltage that can be applied because of low flashover voltages exist[1,23] and prohibit a large trap depth and ion–electrode distance, d. This limits the achievable ion lifetime and secular frequencies and results in large rates of heating of the ion motion, which scales as d^{-4} (ref. 24), where heating has adverse effects on the fidelity of motion-dependant qubit gate operations[25]. The ability to apply large voltages to microfabricated and microelectromechanical system devices also has applications in nanoelectrospray thruster arrays for spacecraft[26–29], where high-electric fields are desirable and may also be useful in microfabricated mass spectrometry[30] as well as particle and cell sorting[31].

Here, we report on a general microfabrication process to achieve large breakdown voltages in microfabricated devices and use this process to fabricate a 2D lattice of ion traps on a microchip. This process could also be used for other surface electrode ion-trap geometries. Using this chip, we demonstrate trapping of a 2D lattice of single Yb^{+} ions, the deterministic trapping of multiple ions at lattice sites and rudimentary ion shuttling between lattice sites. The device presented is suitable for 2D sensing applications. The ion–ion distance for this device is, however, too large to be used for quantum simulation. We discuss how a minor modification to the microchip design would allow for simulation of 2D spin lattices. This modified design would also offer possible architectures for 2D cluster state generation[13] and general quantum information processing[16]. As the device presented in this article is an integrated ion-trap chip[1] it is potentially scalable to much larger ion lattices.

Results

Fabrication of the microchip. The layered structure of a commercial silicon-on-insulator (SOI) wafer was used by Britton *et al.*[32] to fabricate a linear ion trap permitting the application of voltages of up to 150 V. We have developed a different fabrication process using an SOI wafer to fabricate a planar ion trap with a significantly increased trap depth while maintaining large ion–electrode separations. This was achieved by a combination of recessed electrodes and the application of voltages in excess of 1 kV. We describe both of these fabrication advances in more detail below.

We utilize the layered SOI wafer to form a planar trap electrode structure with a 2D electrode pattern, shown in Fig. 1a. However, instead of the ground electrodes lying on the same plane as the RF electrodes, they are recessed from the chip surface. This recess was achieved by using the SOI handle layer as RF ground, shown in Fig. 1b. By using recessed electrodes, the trap depth for a given ion–electrode separation and voltage can be substantially increased. Each recess in the RF electrode corresponds to a single-trap site and is hexagonal in shape, the recessed hexagonal dimensions are shown in Fig. 1c.

To ensure ions can be trapped at a large ion height while maintaining a deep trapping potential using microfabricated ion traps in general, and our lattice ion trap specifically, a fabrication process that allows for high voltages to be applied was developed. This process not only has use for ion-trap fabrication but also for other microfabricated and microelectromechanical systems devices in general. We chose a thick oxide layer thus increasing the path length between the electrodes and the handle layer as well as reducing capacitance between the RF electrode and ground. However, this would typically only result in a modest increase in breakdown voltage. We were able to obtain a much larger increase by using a specialized fabrication process. In order to explain this process, it is important to note that voltage breakdown will usually occur via insulator surfaces connecting two conductors rather than through the insulator bulk. We selected a particular SOI structure that was fabricated by wafer bonding two wafers with 5 μm thick oxide surfaces to form a 10 μm thick buried oxide layer (see Methods). Using a buffered hydrofluoric acid etch, lasting 130–140 min, the oxide layer was etched to expose the handle layer. As there is an increased etch rate on the interface where the two oxide layers were bonded together, a highly anisotropic etch results laterally under the electrodes. Rather than obtaining the usual approximately straight etch profile, we were able to obtain the V-shaped undercut as shown in Fig. 1d. This V-shaped etch profile substantially increases the path length between the electrodes and ground resulting in extremely high-breakdown voltages as it increases the effective distance for surface flashover from 10 μm to 120 μm. Because of the depth of the undercut, the hexagon structure becomes completely detached from the handle layer, supported by the thick surrounding RF edge. This greatly reduces the number of potential flashover initiation points, such as sharp points and defects, and aids the improvement in the flashover voltage. The finished trap structure can be seen in Fig. 2a, with the undercut shown in Fig. 2b. Electrical flashover measurements were performed on SOI test samples to determine the voltage that can be applied (see Methods). The mean flashover voltages were measured to be $V_{\rm dc}=1{,}300(80)$ V and $V_{\rm RF}=1{,}061(10)$ V, where the error is the standard deviation. These values are one or two orders of magnitude higher than in previously fabricated microfabricated ion traps[1,32]. In fact, these voltages correspond to typical values applied in traditional ion traps made using large metallic rods illustrating the impressive performance of our microchip.

The microchip consists of 29 traps arranged in a triangular lattice, with each ion having up to six nearest neighbours with an ion–ion separation of 270.5 μm. The ion–electrode separation is 156 μm. Because of the recessed ground electrodes, the ion height

© 2014 Macmillan Publishers Limited. All rights reserved.

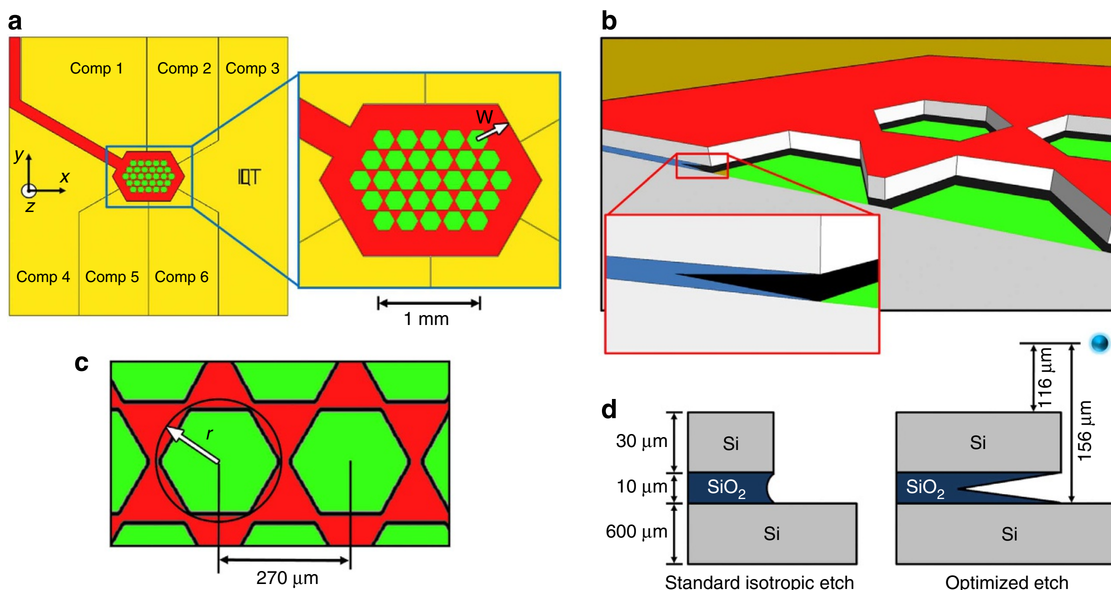

Figure 1 | Design of the lattice microchip electrode geometry and electrode undercut. (**a**) The electrode design for the microchip. There are 29 trapping sites, one above the centre of each hexagon of ground electrode. The radio-frequency (RF) electrode is shown in red, compensation electrodes are shown in gold and the ground electrode is shown in green. The distance from the outer polygon centre to the RF edge, labeled W, is 410 μm. (**b**) Cross-section drawing of the trap geometry, showing the silicon-on-insulator layered geometry. The close-up inset shows the deep V undercut achievable with our fabrication process. (**c**) Close-up of the hexagonal trap geometry with a polygon radius $r = 125$ μm and neighbouring traps separated by 270.5 μm. (**d**) Two schematics of the etch profile, a typical isotropic etch is shown on the left, showing a slight undercut into the buried oxide. The right picture shows the profile of our optimized etch. The preferential etch rate along the bond face results in a deep V-shaped undercut. The ion height relative to the trap electrodes is also shown.

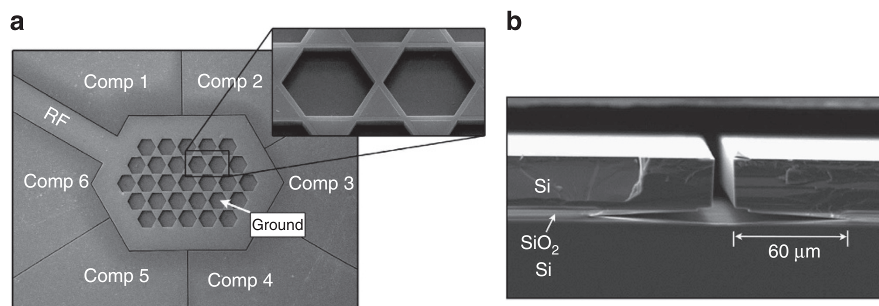

Figure 2 | Scanning electron micrographs of the fabricated microchip. (**a**) A scanning electron microscopy (SEM) image of a finished microchip. The inset shows a close up of two of the hexagonal traps, this shows the recessed ground electrode. (**b**) An SEM image of the cross-section of the layered silicon-on-insulator structure at the interface between two compensation electrodes. The deep V-shaped undercut into the oxide layer is clearly visible extending 60 μm into the SiO_2 layer.

from the top of the trap surface is 116 μm, as seen in Fig. 1d. A three-dimensional contour plot of the trap potential relating to the chip in Fig. 3a, for the central 11 trap sites, is shown in Fig. 3b. A 2D contour plot is projected below showing the potential at the ion height. To adjust the position of the ions to compensate for stray electric fields and perform shuttling operations, quasi-static voltages can be applied to six electrodes (Comp 1–6), which surround the RF electrode.

Trapping and manipulation of ions on the microchip. An RF voltage $V_0 = 455(3)$ V at a frequency $\Omega/2\pi = 32.2$ MHz was applied to the RF electrode to produce a trapping potential. All other electrodes were initially held at ground. A flux of neutral ytterbium atoms travelling parallel to the trap surface was produced by ohmically heating a natural abundance ytterbium oven from which ^{174}Yb atoms were resonantly ionized using a two-colour photoionization process with light at 399 and 369 nm. Trapped ions were then Doppler cooled by the 369 nm light, with 935 nm light used to repump the ion from a long-lived D-state[33]. The cooling and ionization laser beams were highly elliptical, forming a light sheet co-propagating parallel to the trap surface. An image plane co-incident with the plane of trap centres above the microchip was imaged onto an electron multiplying CCD array to view the ions.

The ion secular frequencies along the trap principle axes were measured to be $(\omega_{x'}, \omega_{y'}, \omega_{z'})/2\pi = (1.58, 1.47, 3.30) \pm 0.01$ MHz, respectively, for a single ion trapped in the top right corner of the array. Using these measurements, numerical simulations of the trap predict a trap depth of 0.42(2) eV. The lifetime of a single laser cooled ion was $\sim$90 min, likely limited by background collisions and $\gtrsim$5 min without cooling light.

A 2D ion lattice can be seen in Fig. 3a, six ions are trapped in adjacent lattice sites, with the viewable area limited by our

© 2014 Macmillan Publishers Limited. All rights reserved.

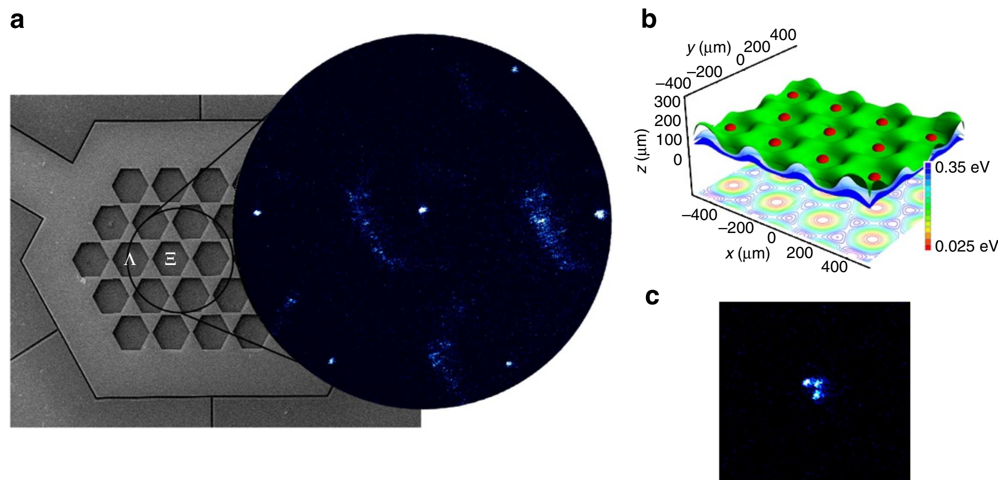

Figure 3 | Image of trapped ion lattice on the microchip. (**a**) An image of six ions trapped simultaneously on the lattice is shown, the hexagonal-shaped electrodes are also visible because of laser scatter. The area imaged was limited by our current imaging system and marked by a black circle over an scanning electron micrography (SEM) image of the trap. (**b**) A three-dimensional contour plot of the lattice potential for the central 11 trap sites with a radio-frequency voltage of 455 V. The equipotential surfaces correspond to: red = 0.04 eV, green = 0.4 eV, light blue = 0.5 eV and blue = 0.6 eV. A two-dimensional contour plot of the potential at the ion height is projected below, the equipotential lines are separated by 0.04 eV. (**c**) An image of a single-lattice site containing a three-ion Coulomb crystal.

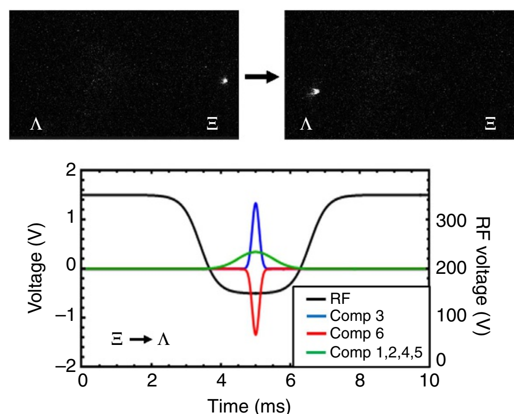

Figure 4 | Ion shuttling on the microchip. Two images are shown before and after shuttling an ion from lattice site Ξ to Λ. The shuttling voltage profile for this shuttling operation is shown. To shuttle the ion back to Ξ, the polarity of the voltages on Comp 3 and 6 is reversed.

imaging system. Because of the stochastic nature of ion loading, trapping a uniform lattice is difficult when uniformly illuminating all trap sites. However, by steering the 399 nm ionization laser to address individual sites, we can controllably fill the lattice. We can also introduce defects, either empty sites or multiple ions per site, in the same manner. A three-ion defect is shown in Fig. 3c. Such lattice defects may be of interest when investigating Bose–Hubbard physics, such as superfluid-Mott insulator transitions or simulations of spin models with spin greater than 1/2.

We have also demonstrated shuttling of ions between different sites of the lattice. An ion is initially trapped at site Ξ, as marked in Fig. 3a. By lowering the RF voltage to minimize the potential barrier and applying control voltages to the surrounding electrodes, the ion is shuttled to position Λ. Figure 4 shows two images of the ion before and after shuttling, also shown are the typical shuttling voltages. To shuttle the ion back to Ξ the polarity of the voltage on Comp 3 and Comp 6 is reversed. Although this shuttling was performed using global control electrodes, enhancing the trap design by adding local control electrodes to the handle layer around each trapping site using backside etches and depositions would allow the distribution of ions over the lattice sites to be changed after the ions are loaded. This would enable separate loading and experiment zones, and for the lattice to be repaired if an ion is lost because of a background collision. Any heating of the ions because of such shuttling can be removed by laser cooling before temperature-sensitive operations. Such local control would also enable precise control of the micromotion at each site.

Discussion

A 2D lattice such as we demonstrate here has many potential future applications. The use of single ions for highly sensitive magnetic-field sensing has been demonstrated[8], and the use of a lattice would allow for spatial as well as temporal measurements[10]. Single ions have been proposed to be used as point imperfections inside Bose–Einstein condensates[12], and ion lattices would allow the effect of precisely tailored arrays of imperfections, both regular and irregular depending on microchip design, to be studied.

One important future application for a 2D ion lattice is in the field of quantum simulation, where trapped ions represent spins in solid-state systems. Interactions between spins can be tailored to create analogues of different 2D systems (such as Ising or Heisenberg spin lattices) in a clean and controllable manner, whose properties can be determined by measurement of the state of all the ions in the array using a light sheet and a CCD array, something that is difficult or impossible to perform in actual solid-state systems.

In simulating these systems, interactions between ions trapped in adjacent sites a and b would be mediated by the Coulomb interaction. The coupling between motional states $H_{\mathrm{Coul}} = -\hbar\Omega_{\mathrm{ex}}/2(a^{\dagger}b + ab^{\dagger})$, where a, $a^{\dagger}$, b, $b^{\dagger}$ are the phonon annihilation and creation operators for the two sites, and the coupling strength

$$\Omega_{\mathrm{ex}} = \frac{e^2}{2\pi\varepsilon_0 m\omega}\frac{1}{s^3} \quad (1)$$

for a pair of singly-charged ions of mass m confined in traps with secular frequency ω separated by distance s (refs 34, 35).

© 2014 Macmillan Publishers Limited. All rights reserved.

For the lattice we have presented here, where $s = 270.5\,\mu m$ and with a trap frequency $\omega/2\pi$ of 1 MHz, the coupling strength $\Omega_{ex}/2\pi$ would be only 2 Hz, impractical for performing simulations and very small compared with the strengths already experimentally demonstrated using linear surface traps[34,35]. The coupling strength has a very strong dependence on the ion–ion separation ($\Omega_{ex} \propto s^{-3}$) and reducing this distance would be key to obtaining useful couplings. A lattice based on smaller ion–ion distances can easily be designed and produced using the fabrication method presented in this paper.

Using an SOI wafer with a 2.5 µm device layer and a 2.5 µm oxide layer fabricated by wafer bonding two 1.25 µm oxide layers together would reduce the depth of the ground plane beneath the surface of the microchip to 5 µm, and a trap electrode design with a hexagon radius of 13 µm and hexagon centre separation of 32 µm fabricated on such a wafer would produce a lattice of traps 15 µm above the surface of the microchip. To reduce scatter from tightly focused laser beams, an etch would be performed outside the trapping area to lower the surface by 100 µm. For a trap frequency $\omega/2\pi$ of 1 MHz, the motional coupling strength $\Omega_{ex}/2\pi$ would then be 1.3 kHz, almost a thousandfold increase compared with our current chip design. This value is comparable to previously achieved coupling strengths between individual wells in linear traps[34,35].

If this trap were used to simulate a 2D spin lattice using the scheme proposed by Porras and Cirac[17,36] a spin–spin coupling strength $J = 2\pi \times 1.2$ kHz would be obtainable using a pulsed 355 nm laser with an average power of 920 mW (see Methods). It is also important to consider possible sources of decoherence to evaluate if a successful quantum simulation would be expected for this prospective trap. We consider both heating of the motion of the trapped ions and photon scattering due to the laser driving the gate. These rates should be low compared with the spin–spin coupling strength J. At such small ion–electrode distance, heating rates at room temperature will be many orders of magnitude greater than J, necessitating cooling of the chip. Although estimating heating rates is imprecise, based on previous measurements in gold traps[37] an estimate for a trap of this design operating cryogenically at 7 K is $\dot{n} = 180\,s^{-1}$ (see Methods). The photon scattering due to the coupling laser is estimated to be $27\,s^{-1}$. Both these rates are significantly less than J, indicating that this type of quantum simulation should be possible with this combination of chip and driving laser.

We have demonstrated a 2D ion lattice integrated on a microchip along with a fabrication process to significantly increase the voltage that can be applied to microfabricated devices. By increasing the breakdown voltage, both 2D lattice and linear surface traps with higher trap depth and lower heating rates (by making use of larger ion–electrode distances) can be fabricated. For surface traps built to perform quantum information processing this reduces the effects of motional heating on gate fidelities[25]. In addition, we have used this advance to demonstrate the operation of a 2D lattice of ytterbium ions on a chip which offers many potential uses including spatially resolved force measurement in two dimensions and magnetic and electric field sensing, and with modifications may offer a platform for quantum simulations.

Methods

Wafer fabrication. The SOI wafers are produced by Ultrasil Corporation who use room temperature fusion bonding to bond the oxide surfaces before the substrate is annealed at 980 °C. X-ray reflection studies of bonded SOI wafers show that even after annealing several monolayers of water molecules remain at the bond-interface in the structure of the SiO_2 (ref. 38). This results in the V-shaped undercut caused by the anisotropic preferential etch along this interface.

Surface flashover measurements. Surface flashover measurements were performed on test chips consisting of gold-coated silicon islands surrounded by the exposed handle layer. The chips were glued, using conductive silver glue, onto a ceramic chip carrier and placed in high vacuum at a pressure of 6×10^{-4} Pa. RF voltage was applied by connecting a quarter-wave helical coil resonator to the vacuum feedthrough. This ensured >90% coupling between the RF amplifier and chip at a resonant frequency of 28.0 ± 0.5 MHz with $Q = 210 \pm 15$. The RF voltage was steadily increased while observing the sample. Upon breakdown, the voltage was measured using a capacitively coupled probe.

RF flashover was observed to occur ~20% lower than static flashover. The exact cause for this is not known, however, it is likely a result of local heating on the chip and outgassing from the surface when the RF voltage is applied. To apply sufficient voltage to trigger flashover, up to 30 W of RF power was applied to the chip. This power would be predominately dissipated on chip, which has the largest impedance. This would result in significant heating of the chip and the release of gases previously adsorbed to the surface.

Ultrahigh vacuum microchip mounting and high-voltage application. The trap was mounted onto a ceramic chip carrier, with gold ribbon wire connecting the electrodes to the chip carrier bond pads. The chip capacitance was measured to be 19 ± 1 pF. The chip was mounted inside an ultrahigh vacuum system at a pressure of 8.0×10^{-8} Pa. To ensure good RF grounding, 820 pF capacitors were wire bonded to the static electrodes. The RF voltage was applied via an external helical coil resonator with $Q = 160$ to provide voltage amplification and filtering of unwanted frequencies[39].

Quantum simulation parameters for modified microchip design. The Porras and Cirac spin simulation scheme[17,36] requires a state-dependant force to be applied to the ions whose internal states encode the simulated spins. The effective spin–spin coupling rate is given by $J = \beta F^2/4\hbar m_i \omega_i^2$, where $\hbar = h/2\pi$, h is Planck's constant, $\beta = \Omega_{ex}/\omega_i$ and F is the magnitude of the state-dependant force applied to each ion[17]. For the proposed modified chip design, with its ion–ion separation of 32 µm and using a pulsed laser with a wavelength of 355 nm divided into counter propagating beams of total average power of 920 mW focused into light sheets of width 50 µm and depth 15 µm to address a 3 × 3 lattice of ions, a coupling strength $J = 2\pi \times 1.2$ kHz could be achieved. As the simulation is driven by the displacement of the ions because of the force F, the simulated spins are entangled with the motional state of the ions at the end of the simulation. This produces an error in the measured spin properties of the simulated system proportional to F^2 (ref. 36). For the proposed modified design, we calculate a simulation error due to this effect of ~25% for the measurement of single-particle properties of the simulated system. In addition to using lasers to produce the spin–spin coupling, magnetic field gradients could also be used to generate the required spin-dependent forces[40] and would allow individual addressing of ions.

Motional heating of an ion is a result of electric field fluctuations at the trap secular frequency, and depends strongly on the ion–electrode distance, which in this case is 19 µm (the ion lies 15 µm above the surface of the chip, however, the electrode under the ion is recessed by 5 µm; the closest points to the ion lie on the edges of the hexagonal cutout). For the proposed modified chip, we assume that the electric-field noise density is the same as measured previously for a gold-electroplated trap at a temperature of 7 K (ref. 37), after adjusting for the different ion–electrode distance d and trap frequency ω using a scaling of $d^{-4}\omega^{-1}$. For our ion–electrode distance of 19 µm and trap frequency $2\pi \times 1$ MHz, we estimate an electric-field noise density $S_E(\omega) = 5.3 \times 10^{-12}\,V^2\,m^{-2}\,Hz^{-1}$. This corresponds to a heating rate $\dot{n} = 180\,s^{-1}$ for an $^{171}Yb^{+}$ ion.

References

1. Hughes, M. D., Lekitsch, B., Broersma, J. A. & Hensinger, W. K. Microfabricated ion traps. *Contemp. Phys.* **52,** 505–529 (2011).
2. Home, J. P. *et al.* Complete methods set for scalable ion trap quantum information processing. *Science* **325,** 1227–1230 (2009).
3. Hensinger, W. K. *et al.* T-junction ion trap array for two-dimensional ion shuttling, storage, and manipulation. *Appl. Phys. Lett.* **88,** 034101 (2006).
4. Amini, J. M. *et al.* Toward scalable ion traps for quantum information processing. *New J. Phys.* **12,** 033031 (2010).
5. Ospelkaus, C. *et al.* Microwave quantum logic gates for trapped ions. *Nature* **476,** 181–185 (2011).
6. Leibfried, D. *et al.* Experimental demonstration of a robust, high-fidelity geometric two ion-qubit phase gate. *Nature* **422,** 412–415 (2003).
7. Britton, J. W. *et al.* Engineered two-dimensional Ising interactions in a trapped-ion quantum simulator with hundreds of spins. *Nature* **484,** 489–492 (2012).
8. Kotler, S., Akerman, N., Glickman, Y., Keselman, A. & Ozeri, R. Single-ion quantum lock-in amplifier. *Nature* **473,** 61–65 (2011).
9. Narayanan, S. *et al.* Electric field compensation and sensing with a single ion in a planar trap. *J. Appl. Phys.* **110,** 114909 (2011).
10. Brownnutt, M., Harlander, M., Hänsel, W. & Blatt, R. Spatially-resolved potential measurement with ion crystals. *Appl. Phys. B* **107,** 1125–1130 (2012).

© 2014 Macmillan Publishers Limited. All rights reserved.

11. Biercuk, M. J., Uys, H., Britton, J. W., VanDevender, A. P. & Bollinger, J. J. Ultrasensitive detection of force and displacement using trapped ions. *Nat. Nanotechnol.* **5,** 646–650 (2010).
12. Zipkes, C., Palzer, S., Sias, C. & Köhl, M. A trapped single ion inside a Bose-Einstein condensate. *Nature* **464,** 388–391 (2010).
13. Raussendorf, R. & Briegel, H. J. A one-way quantum computer. *Phys. Rev. Lett.* **86,** 5188–5191 (2001).
14. Schneider, C., Porras, D. & Schaetz, T. Experimental quantum simulations of many-body physics with trapped ions. *Rep. Prog. Phys.* **75,** 024401 (2012).
15. Blatt, R. & Roos, C. F. Quantum simulations with trapped ions. *Nat. Phys.* **8,** 277–284 (2012).
16. Cirac, J. I. & Zoller, P. A scalable quantum computer with ions in an array of microtraps. *Nature* **404,** 579–581 (2000).
17. Porras, D. & Cirac, J. I. Effective quantum spin systems with trapped ions. *Phys. Rev. Lett.* **92,** 207901 (2004).
18. Chiaverini, J. & Lybarger, W. E. Laserless trapped-ion quantum simulations without spontaneous scattering using microtrap arrays. *Phys. Rev. A* **77,** 022324 (2008).
19. Kumph, M., Brownnutt, M. & Blatt, R. Two-dimensional arrays of radio-frequency ion traps with addresable interactions. *New J. Phys.* **13,** 073043 (2011).
20. Clark, R. J., Lin, T., Brown, K. R. & Chuang, I. L. A two-dimensional lattice ion trap for quantum simulation. *J. Appl. Phys.* **105,** 013114 (2009).
21. Siverns, J. D. *et al.* Optimization of two-dimensional ion trap arrays for quantum simulation. *New J. Phys* **14,** 085009 (2012).
22. Schmied, R., Wesenberg, J. H. & Leibfried, D. Optimal surface-electrode trap lattices for quantum simulation with trapped ions. *Phys. Rev. Lett.* **102,** 233002 (2009).
23. Stick, D. *et al.* Ion trap in semiconductor chip. *Nat. Phys.* **2,** 36–39 (2006).
24. Deslauriers, L. *et al.* Scaling and suppression of anomalous heating in ion traps. *Phys. Rev. Lett.* **97,** 103007 (2006).
25. Sørensen, A. & Mølmer, K. Entanglement and quantum computation with ions in thermal motion. *Phys. Rev. A* **62,** 022311 (2000).
26. Paine, M. D., Gabriel, S., Schabmueller, C. G. J. & Evans, A. G. R. Realisation of very high voltage electrode-nozzle systems for MEMS. *Sens. Actuators A Phys.* **114,** 112 (2004).
27. Krpoun, R. & Shea, H. R. Integrated out-of-plane nanoelectrospray thruster arrays for spacecraft propulsion. *J. Micromech. Microeng.* **19,** 045019 (2009).
28. Krpoun, R., Rdber, M. & Shea, H. in *Micro Electro Mechanical Systems, 2008. MEMS 2008. IEEE 21st International Conference on* 964; 13–17 January (2008).
29. Gassend, B., Velasquez-Garcia, L., Akinwande, A. & Martinez-Sanchez, M. A microfabricated planar electrospray array ionic liquid ion source with integrated extractor. *J. Microelectromech. S.* **18,** 679–694 (2009).
30. Syms, R. R. A. Advances in microfabricated mass spectrometers. *Anal. Bioanal. Chem.* **393,** 427–429 (2009).
31. Grujic, K., Helleso, O. G., Hole, J. P. & Wilkinson, J. S. Sorting of polystyrene microspheres using a Y-branched optical waveguide. *Opt. Express* **13,** 1–7 (2005).
32. Britton, J. *et al.* Scalable arrays of rf Paul traps in degenerate Si. *Appl. Phys. Lett.* **95,** 173102 (2009).
33. McLoughlin, J. J. *et al.* Versatile ytterbium ion trap experiment for operation of scalable ion-trap chips with motional heating and transition-frequency measurements. *Phys. Rev. A* **83,** 013406 (2011).
34. Brown, K. R. *et al.* Coupled quantized mechanical oscillators. *Nature* **471,** 196–199 (2010).
35. Harlander, M., Lechner, R., Brownnutt, M., Blatt, R. & Hänsel, W. Trapped-ion antennae for the transmission of quantum information. *Nature* **471,** 200–203 (2010).
36. Deng, X.-L., Porras, D. & Cirac, J. I. Effective spin quantum phases in systems of trapped ions. *Phys. Rev. A* **72,** 063407 (2005).
37. Labaziewicz, J. *et al.* Temperature dependence of electric field noise above gold surfaces. *Phys. Rev. Lett.* **101,** 180602 (2008).
38. Rieutord, F. *et al.* High-energy X-ray reflectivity of buried interfaces created by wafer bonding. *Phys. Rev. B* **63,** 125408 (2001).
39. Siverns, J. D., Simkins, L. R., Weidt, S. & Hensinger, W. K. On the application of radio frequency voltages to ion traps via helical resonators. *Appl. Phys. B* **107,** 921–934 (2012).
40. Minert, F. & Wunderlich, C. Ion-trap quantum logic using long-wavelength radiation. *Phys. Rev. Lett.* **87,** 257904 (2001).

Acknowledgements

We acknowledge helpful discussions with D. Porras and J. D. Siverns. This work is supported by the UK Engineering and Physical Sciences Research Council (EP/E011136/1, EP/G007276/1), European Commission's Seventh Framework Programme (FP7/2007-2013) under grant agreement no. 270843 (iQIT), the European Commission's Sixth Framework Marie Curie International Reintegration Programme (MIRG-CT-2007-046432), the Nuffield Foundation and the University of Sussex.

Author contributions

R.C.S. planned the experiment, designed the microchip and the fabrication process, performed the experiment and wrote the manuscript, H.R. fabricated the microchip, S.W., K.L. and S.C.W. performed the experiment and assisted in writing the manuscript, P.S. and M.K. assisted in the development of the fabrication process and W.K.H. planned the experiment, coordinated the work, helped design the microchip and fabrication process and assisted in writing the manuscript.

Additional information

Competing financial interests: The authors declare no competing financial interests.

Reprints and permission information is available online at http://npg.nature.com/reprintsandpermissions/

How to cite this article: Sterling, R.C. *et al.* Fabrication and operation of a two-dimensional ion-trap lattice on a high-voltage microchip. *Nat. Commun.* 5:3637 doi: 10.1038/ncomms4637 (2014).

© 2014 Macmillan Publishers Limited. All rights reserved.