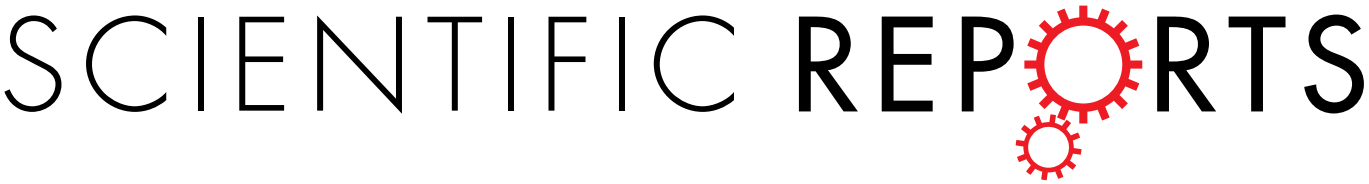

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Fabrication-constrained nanophotonic inverse design

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Received: 3 January 2017
Accepted: 4 April 2017
Published online: 11 May 2017

A major difficulty in applying computational design methods to nanophotonic devices is ensuring that the resulting designs are fabricable. Here, we describe a general inverse design algorithm for nanophotonic devices that directly incorporates fabrication constraints. To demonstrate the capabilities of our method, we designed a spatial-mode demultiplexer, wavelength demultiplexer, and directional coupler. We also designed and experimentally demonstrated a compact, broadband 1×3 power splitter on a silicon photonics platform. The splitter has a footprint of only $3.8 \times 2.5\ \mu$m, and is well within the design rules of a typical silicon photonics process, with a minimum radius of curvature of 100 nm. Averaged over the designed wavelength range of 1400–1700 nm, our splitter has a measured insertion loss of 0.642 ± 0.057 dB and power uniformity of 0.641 ± 0.054 dB.

Nanophotonic devices are typically designed by starting with an analytically designed structure, and hand-tuning a few parameters[1]. In recent years, it has become increasingly popular to automate this process with the use of powerful optimization algorithms. In particular, by searching the full space of possible structures, it is possible to design devices with higher performance and smaller footprints than traditional devices[2–8].

A major challenge when designing devices with arbitrary topologies is ensuring that the structures remain fabricable. Many of these computationally designed structures have excellent performance when fabricated using high-resolution electron-beam lithography, but they have features which are difficult to resolve with industry-standard optical lithography[3,7,8].

Building on our previous work[5,7,9], we propose an inverse design method for nanophotonic devices that incorporates fabrication constraints. Our algorithm achieves an approximate minimum feature size by imposing curvature constraints on dielectric boundaries in the structure. We then demonstrate the capabilities of our method by designing a spatial-mode demultiplexer, wavelength demultiplexer, and directional coupler, and experimentally demonstrating an ultra-broadband 1×3 power splitter. All of our designs are compact, have no small features, and should be resolvable using modern photolithography. Additionally, with the exception of the wavelength demultiplexer, all of our devices are well within the design rules of existing silicon photonics processes.

Design Method

Due to the complexity of accurately modelling lithography and etching processes, most attempts to incorporate fabrication constraints into computational nanophotonic design have focused on heuristic methods. One approach is to restrict the design to rectangular pixels which are larger than the mininum allowable feature size[10]. The resulting Manhattan geometry, however, is restrictive and likely not optimal for optical devices. Another method involves applying a convolutional filter to the design followed by thresholding[11–13], which can introduce artifacts smaller than the desired feature size. The approach used in this work is to impose curvature constraints on the device boundaries, which avoids the aforementioned issues. Curvature limits have been successfully applied in earlier work[4], but were not described in detail nor validated with experimental demonstrations.

Level Set Formulation. We assume that our device is planar and consists of only two materials. We can represent our structure by constructing a continuous function $\phi(x, y)$: $\mathbb{R}^2 \rightarrow \mathbb{R}$ over our design region, and letting the boundaries between the materials lie on the level set $\phi = 0$. The permittivity ε is then given by

$$\varepsilon(x, y) = \begin{cases} \varepsilon_1 & \text{for } \phi(x, y) \leq 0 \\ \varepsilon_2 & \text{for } \phi(x, y) > 0. \end{cases} \quad (1)$$

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The advantage of this implicit representation is that changes in topology, such as the merging and splitting of holes, are trivial to handle. We can also manipulate our structure by adding a time dependence, and evolving $\phi(x, y, t)$ as a function of time t with a variety of partial differential equations collectively known as level set methods[14,15].

To design a device, we first choose some objective function $f[\varepsilon]$ which describes how well the structure matches our electromagnetic performance constraints[5,7]. We then evolve our structure, represented by ϕ, in such a way that we minimize our objective f. We can achieve this by adapting gradient descent optimization to our level set representation. The level set equation for moving boundaries in the normal direction is

$$\phi_t + v(x, y)|\nabla\phi| = 0 \tag{2}$$

where $\nabla\phi = \phi_x + \phi_y$ is the spatial gradient of ϕ, and $v(x, y)$ is the local velocity. To implement gradient descent, we choose the velocity field $v(x, y)$ to correspond to the gradient of the objective function $f[\varepsilon]$[15]. The gradient can be efficiently computed using adjoint sensitivity analysis[3,4,6,9]. As $t \to \infty$, ϕ converges to a locally optimal structure.

Unfortunately, this approach tends to result in the formation of extremely small features. We can avoid this problem by periodically enforcing curvature constraints. The level set equation for smoothing out curved regions is

$$\phi_t - \kappa|\nabla\phi| = 0 \tag{3}$$

where the local curvature κ is given by

$$\kappa = \nabla \cdot \left(\frac{\nabla\phi}{|\nabla\phi|}\right) = \frac{\phi_x^2\phi_{yy} - 2\phi_x\phi_y\phi_{xy} + \phi_{xx}\phi_y^2}{|\nabla\phi|^3}. \tag{4}$$

Although equation (3) removes highly curved regions more quickly[14], the boundaries are eventually reduced to a set of straight lines with zero curvature as $t \to \infty$.

From a fabrication perspective, we only need to smooth regions which are above some maximum allowable curvature κ_0. We can do this by introducing a weighting function

$$b(\kappa) = \begin{cases} 1 & \text{for } |\kappa| > \kappa_0 \\ 0 & \text{otherwise} \end{cases} \tag{5}$$

and modifying equation (3) to be

$$\phi_t - b(\kappa)\kappa|\nabla\phi| = 0. \tag{6}$$

If we evolve ϕ with equation (6) until it reaches steady state, the maximum curvature will be less than or equal to κ_0.

Although curvature limiting will eliminate the formation of most small features, it does not prevent the formation of narrow gaps or bridges. We detect these features by applying morphological dilation and erosion operations to the set $\phi > 0$, and checking for changes in topology. Once detected, these narrow gaps and bridges can be eliminated by "cutting" them in half, and then applying curvature filtering to round out the sharp edges.

The final design algorithm is as follows:

1. Initialize ϕ and δt.
2. Repeat until $\delta t < \delta t_{min}$.

   (a) Let $\phi' \leftarrow \phi$.
   (b) **Gradient descent**: evolve ϕ' with eqn. (2) for time δt.
   (c) **Gap and bridge removal**: detect any small gaps or bridges, and modify ϕ' to remove them.
   (d) **Curvature limit**: evolve ϕ' with eqn. (6) until convergence.
   (e) **If** $f[\varepsilon[\phi']] < f[\varepsilon[\phi]]$, **then** let $\phi \leftarrow \phi'$ and increase δt.

   Otherwise, decrease δt.

A detailed description of the objective function $f[\varepsilon]$ and implementation details can be found in the supplementary information.

Designed Devices

To demonstrate the capabilities of our design method, we designed a variety of three-dimensional waveguide-coupled devices on a silicon photonics platform. All of the structures we show here consist of a single fully-etched 220 nm thick Si layer with SiO_2 cladding. Refractive indices of $n_{Si} = 3.48$ and $n_{SiO_2} = 1.44$ were used.

1×3 splitter. Our first device is a broadband 1×3 power splitter with 500 nm wide input and output waveguides. We constrained the minimum radius of curvature to be 100 nm, well within the typical design rules of a silicon photonics process, and enforced bilateral symmetry. To design the splitter, we specified that power in the fundamental traverse-electric (TE) mode of the input waveguide should be equally split into the fundamental TE mode of the three output waveguides, with at least 95% efficiency. Broadband performance was achieved by simultaneously optimizing at 6 equally spaced wavelengths from 1400–1700 nm.

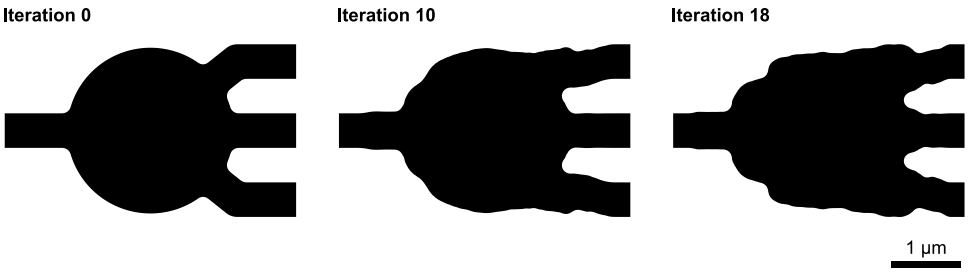

Figure 1. Intermediate steps in the optimization process for the 1×3 splitter. Starting with a star-shaped geometry, the optimization converged in 18 iterations. The minimum radius of curvature in the design was set to 100 nm. Regions with Si are denoted in black, and SiO_2 is denoted in white.

The optimization process is illustrated in Fig. 1; the simulated fields and performance are presented later in this paper alongside experimental results. Starting with a star-shaped geometry, the optimization process converged in 18 iterations. Each iteration required two electromagnetic simulations per design frequency (see supplementary information), resulting in a total of 216 simulations. The device was designed in approximately 2 hours on a single server with an Intel Core i7-5820 K processor, 64 GB of RAM, and three Nvidia Titan Z graphics cards. Since the computational cost of optimization is dominated by the electromagnetic simulations, we performed them using a graphical processing unit (GPU) accelerated implementation of the finite-difference frequency-domain (FDFD) method[16,17], with a spatial step size of 40 nm. A single FDFD solve is considerably faster and less computationally expensive than a finite-difference time-domain (FDTD) simulation.

Interestingly, the splitter appears to be operate using the multi-mode interferometer (MMI) principle[18], with a geometry that resembles a boundary-optimized MMI. This was without any human input or intervention throughout the design process, suggesting that MMI-based devices may be optimal for this particular application.

Spatial mode demultiplexer. Our second device is a spatial-mode demultiplexer that takes the TE_{10} and TE_{20} modes of a 750 nm wide input waveguide, and routes them to the fundamental TE mode of two 400 nm wide output waveguides. To design this device, we specified that $>$90% of the input power should be transmitted to the desired output port, and $<$1% should be coupled into the other output. As with the 1×3 splitter, this device was designed to be broadband by optimizing at six evenly spaced wavelengths between 1400 nm and 1700 nm. To obtain an initial structure for the level set optimization, we started with a uniform permittivity in the design region, allowed the permittivity to vary continuously in the initial stage of optimization, and applied thresholding to obtain a binary structure[5]. We used a minimum radius of curvature of 70 nm, and a minimum gap or bridge width of 90 nm.

The final design and simulated performance are illustrated in Fig. 2. The spatial mode multiplexer has an average insertion loss of 0.826 dB, and a contrast better than 16 dB over the design bandwidth of 1400–1700 nm.

Wavelength demultiplexer. Our third device is a 3-channel wavelength demultiplexer with a 40 nm channel spacing with 500 nm wide input and output waveguides. To design this device, we specified that $>$80% of the input power should be transmitted to the desired output port, and $<$1% should be coupled into the remaining outputs. The initial structure was a rectangular slab of silicon with a regular array of holes, which had a pitch of 400 nm and a diameter of 250 nm. We enforced a minimum radius of curvature of 40 nm, and a minimum gap or bridge width of 90 nm.

The final design and simulated performance are illustrated in Fig. 3. At the center of each channel, the insertion loss is approximately 1.5 dB, and the contrast is better than 16 dB. Each channel has a usable bandwidth $>$10 nm.

Directional coupler. Our final device is a relatively compact 50-50 directional coupler, with 400 nm input and output waveguides. This device was designed by specifying that half the power in fundamental mode of the input waveguide should be coupled into each of the outputs, with $>$90% efficiency. As in the design of the spatial mode demultiplexer, we obtained an initial structure by starting with a uniform permittivity in the design region, allowing the permittivity to vary continuously in the initial stage of optimization, and applying thresholding. To achieve moderate broadband performance, the device was simultaneously optimized for 6 wavelengths between 1470–1630 nm. We enforced a minimum radius of curvature of 70 nm, and a minimum bridge width of 90 nm.

The final device and simulated performance are illustrated in Fig. 4. At the optimal operating point of 1520 nm, the device couples 90% of the input power into the desired output waveguides. The device structure appears to be a grating-assisted directional coupler.

Experimental Realization of 1×3 Splitter

Robust and efficient power splitters are essential building blocks for integrated photonics. A variety of 1×2 splitters with attractive performance have been demonstrated on the silicon photonics platform, ranging from conventional devices[19,20] to those designed using advanced optimization techniques[4,21,22]. However, it is not possible to split power equally into an arbitrary number of waveguides by cascading 1×2 splitters, and efficient and compact devices that fill this gap are lacking in the literature. To help fill this gap, we fabricated and experimentally

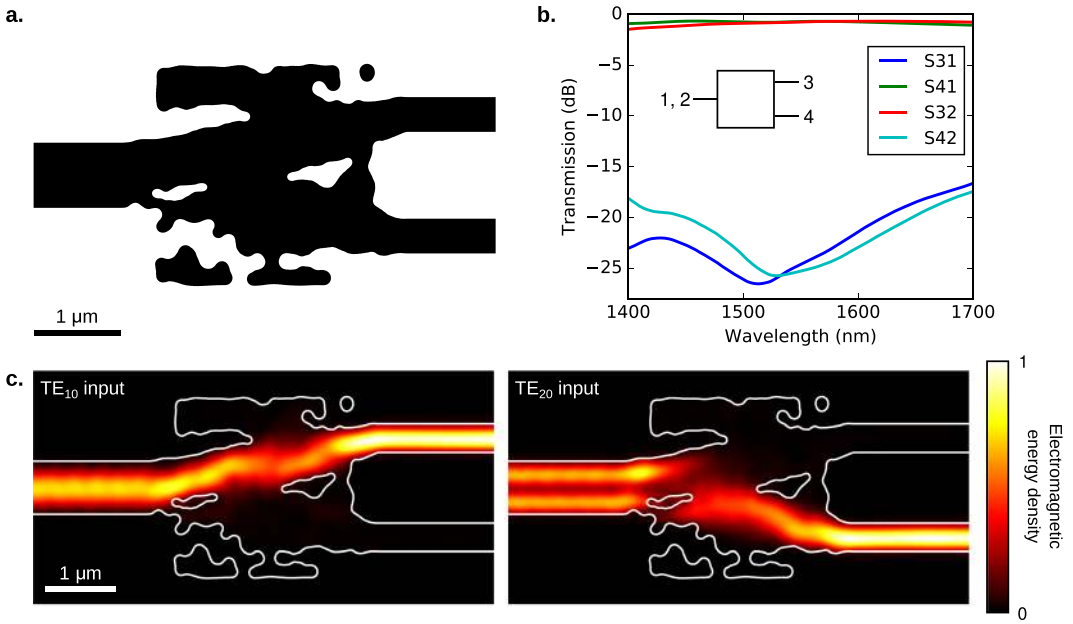

Figure 2. A spatial mode demultiplexer that takes the TE_{10} and TE_{20} modes of a 750 nm wide input waveguide, and routes them to the TE_{10} mode of two 400 nm wide output waveguides. Here, we present (**a**) the final design, (**b**) simulated S-parameters, and (**c**) the electromagnetic energy density $U = \frac{1}{2}\varepsilon E^2 + \frac{1}{2}\mu H^2$ at 1550 nm, where ε and μ are the permittivity and permeability, and E and H are the electric and magnetic fields respectively. The fields and S-parameters were calculated using finite-difference time-domain (FDTD) simulations. The boundaries of the device are outlined in white.

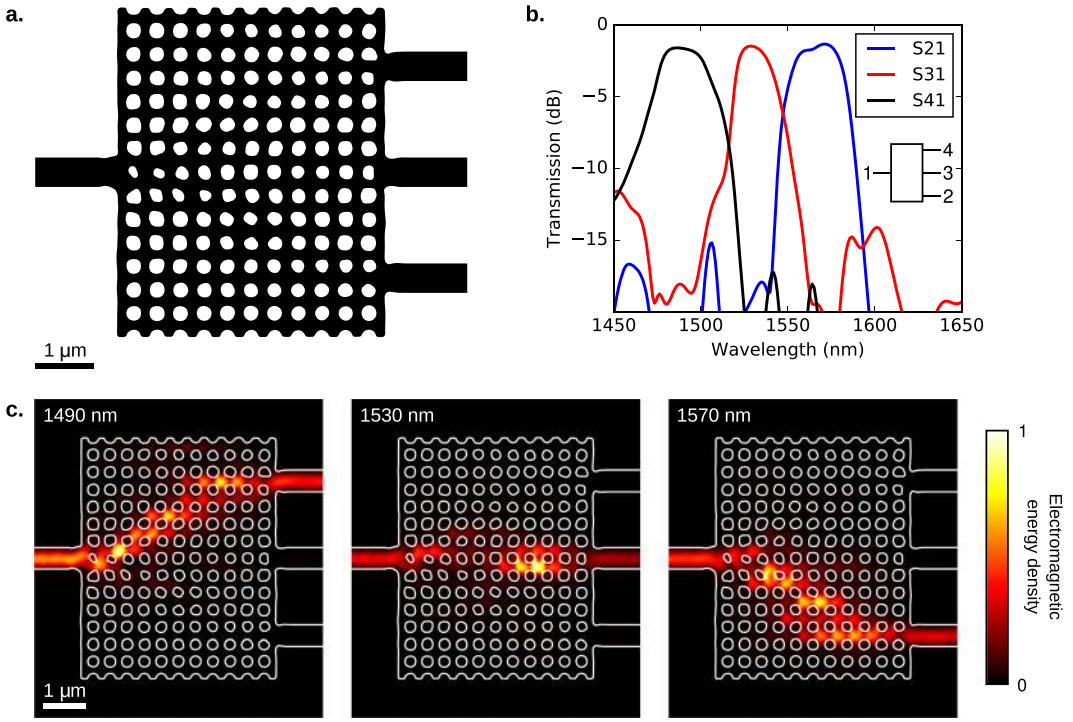

Figure 3. A compact 3-channel wavelength demultiplexer with a 40 nm channel spacing. The input and output waveguides are all 500 nm wide. Here, we present (**a**) the final design, (**b**) simulated S-parameters, and (**c**) the electromagnetic energy density at the three operating wavelengths.

demonstrated the 1×3 splitter we presented in the previous section. Our 1×3 splitter is considerably smaller and more broadband than any existing device in the literature[23,24].

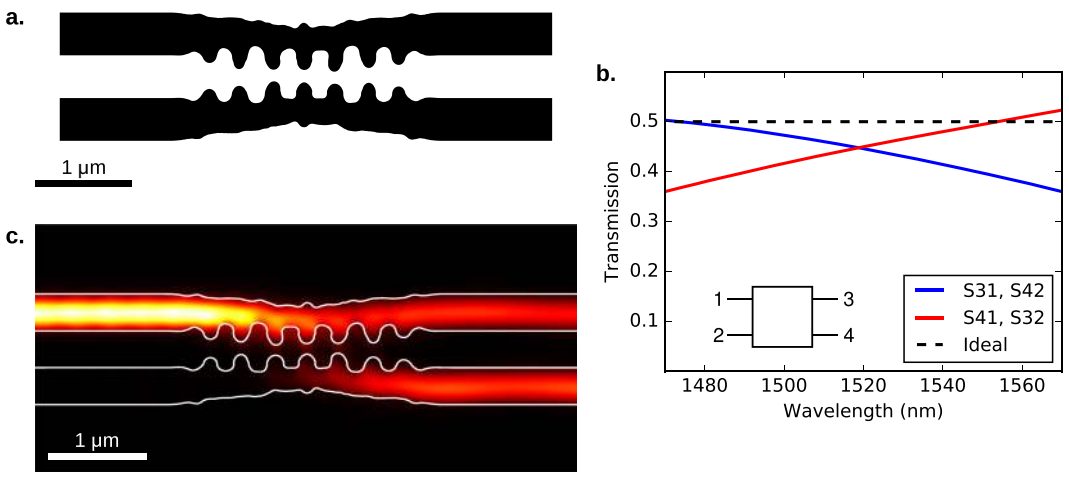

Figure 4. A relatively compact and broadband 50–50 directional coupler with 400 nm input and output waveguides. The device resembles a grating-assisted directional coupler. Here, we present (**a**) the final design, (**b**) simulated S-parameters, and (**c**) the electromagnetic energy density at 1550 nm.

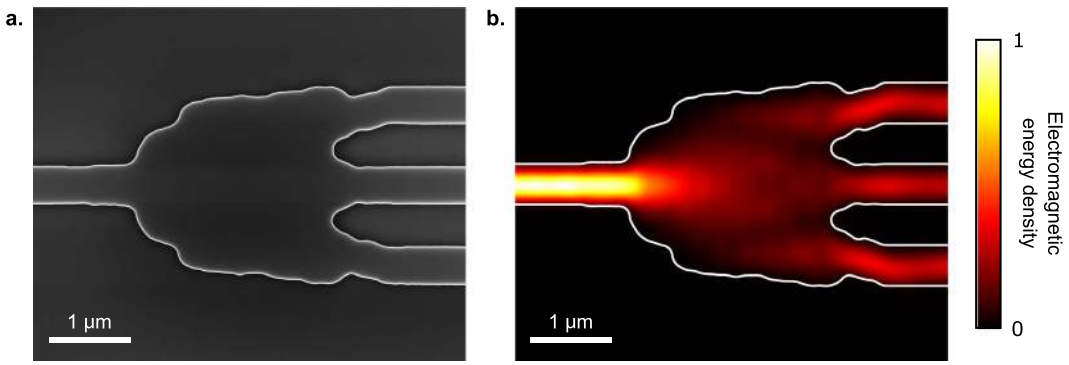

Figure 5. The broadband 1×3 splitter. (**a**) SEM image of the fabricated splitter. The device was made by fully etching the 220 nm device layer of an SOI wafer. The total footprint is $3.8 \times 2.5\,\mu$m. This image was taken before the devices were capped with oxide. (**b**) Electromagnetic energy density in the device at 1550 nm.

Fabrication. The power splitters were fabricated on Unibond SmartCut silicon-on-insulator (SOI) wafers obtained from SOITEC, with a nominal 220 nm device layer, and 3.0 μm buried oxide layer. A JEOL JBX-6300FS electron-beam lithography system was used to pattern a 330 nm thick layer of ZEP-520A resist spun on the samples. A transformer-coupled plasma etcher was used to transfer the pattern to the device layer, using a C_2F_6 breakthrough step and $BCl_3/Cl_2/O_2$ main etch. The mask was stripped by soaking in solvents, followed by a piranha (H_2SO_4/H_2O_2) clean. Finally, the devices were capped with 1.6 μm of LPCVD (low pressure chemical vapour deposition) oxide.

A multi-step etch-based process was used to expose waveguide facets for edge coupling. First, a chrome mask was deposited using liftoff to protect the devices. Next, the oxide cladding, device layer, and buried oxide layer were etched in a inductively-coupled plasma etcher using a C_4F_8/ArO_2 chemistry. To provide mechanical clearance for the optical fibers, the silicon substrate was then etched to a depth of ~100 μm using the Bosch process in a deep reactive-ion etcher (DRIE). Finally, the chrome mask was chemically stripped, and the samples were diced into conveniently-sized pieces.

Characterization. The final splitter is illustrated in Fig. 5, showing both an scanning-electron micrograph (SEM) of the fabricated device, and simulated electromagnetic energy density at the center wavelength of 1550 nm. The simulated electric energy density $U_E = \frac{1}{2}\varepsilon E^2$ as a function of wavelength is shown in the supplementary video.

Transmission through the device was measured by edge-coupling to the input and output waveguides using lensed fibers. A polarization-maintaining fiber was used on the input side to ensure that only the TE mode of the waveguide was excited. To obtain consistent coupling regardless of the transmission spectra of the devices, the fibers were aligned by optimizing the transmitted power of a 1570 nm laser. The transmission spectrum was then measured by using a supercontinuum source and a spectrum analyzer. The device characteristics were obtained by normalizing the transmission with respect to a waveguide running parallel to the device.

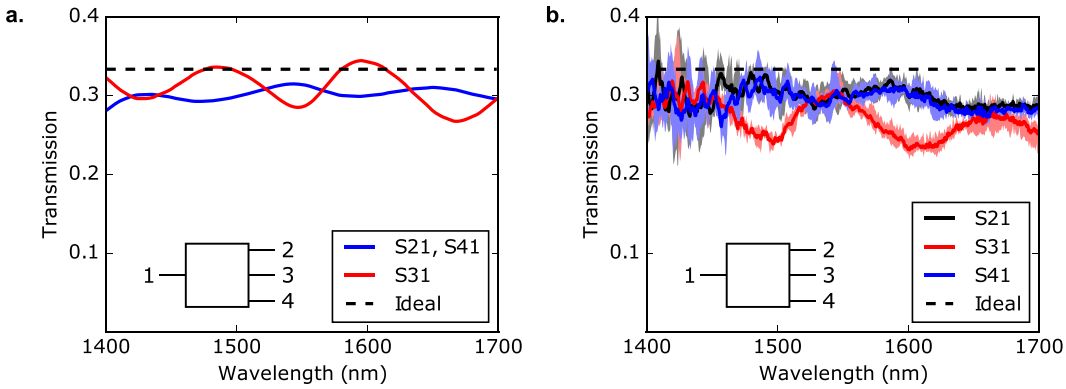

Figure 6. Simulated and measured S-parameters for the broadband 1×3 splitter, where *Sij* is the transmission from port *i* to port *j*. (**a**) Simulated performance, calculated using finite-difference time-domain (FDTD) simulations. Due to bilateral symmetry in the structure, S21 and S41 are equal to each other. (**b**) Measured device performance. Here, we have overlaid the measurements for 4 identically fabricated devices. The average values are denoted by the solid lines, and the minimum and maximum values are denoted by the shaded areas.

The simulated and measured transmission spectra of the device are plotted in Fig. 6. The simulations and measurements match reasonably well, although the measured devices have slightly higher losses and exhibit a spectral shift with respect to simulations. The device performance is highly consistent across all 4 measured devices, indicating that they are robust to fabrication error. The spectral shifts are likely due to slight over-etching or under-etching errors, as indicated by simulations we present in the supplementary information.

The two key criteria for a power splitter are low insertion loss, and excellent power uniformity. The power uniformity is defined as the ratio between the maximum and minimum output powers. Averaged over the designed wavelength range of 1400–1700 nm, our 1×3 splitter has a measured insertion loss of 0.642 ± 0.057 dB, and a power uniformity of 0.641 ± 0.054 dB. Here, the uncertainty refers to the variability between different measured devices.

Conclusion

In summary, we have incorporated fabrication constraints into an inverse design algorithm for nanophotonic devices. Using this method, we designed a spatial mode demultiplexer, a 3-channel wavelength demultiplexer, and 50–50 directional coupler. We also designed and experimentally demonstrated a broadband 1×3 splitter. Critically, our devices have no small features which would be difficult to resolve with photolithography, paving the way for inverse designed structures to become practical components of integrated photonics systems.

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Acknowledgements

This work was funded by the AFOSR MURI for Aperiodic Silicon Photonics, grant number FA9550-15-1-0335, the Gordon and Betty Moore Foundation, and GlobalFoundries Inc. All devices were fabricated at the Stanford Nanofabrication Facility (SNF) and Stanford Nano Shared Facilities (SNSF).

Author Contributions

A.Y.P. designed, simulated, fabricated and measured the devices. A.Y.P., J.P., and L.S. developed the design and simulation software. J.V. supervised the project. All members contributed to the discussion and analysis of the results.

Additional Information

Supplementary information accompanies this paper at doi:10.1038/s41598-017-01939-2

Competing Interests: The authors declare that they have no competing interests.

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