

Fabrication of Injectable Micro-Scale Opto-Electronically Transduced Electrodes (MOTEs) for Physiological Monitoring

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Abstract—*In vivo*, chronic neural recording is critical to understand the nervous system, while a tetherless, miniaturized recording unit can render such recording minimally invasive. We present a tetherless, injectable micro-scale opto-electronically transduced electrode (MOTE) that is $\sim 60\mu\text{m} \times 30\mu\text{m} \times 330\mu\text{m}$, the smallest neural recording unit to date. The MOTEs consist of an AlGaAs micro-scale light emitting diode (μLED) heterogeneously integrated on top of conventional 180nm complementary metal-oxide-semiconductor (CMOS) circuit. The MOTEs combine the merits of optics (AlGaAs μLED for power and data uplink), and of electronics (CMOS for signal amplification and encoding). The optical powering and communication enable the extreme scaling while the electrical circuits provide a high temporal resolution ($<100\mu\text{s}$). This paper elaborates on the heterogeneous integration in MOTEs, a topic that has been touted without much demonstration on feasibility or scalability. Based on photolithography, we demonstrate how to build heterogeneous systems that are scalable as well as biologically stable – the MOTEs can function in saline water for more than six months, and in a mouse brain for two months (and counting). We also

present handling/insertion techniques for users (*i.e.* biologists) to deploy MOTEs with little or no extra training. [2020-0080]

Index Terms—CMOS post processing, electrophysiology, heterogenous integration, physiological monitoring, tetherless neural recording.

I. INTRODUCTION

CHRONIC neural recording is crucial in gaining a better understanding of the brain and could provide insights in neurological disorders such as Alzheimer’s Disease [1]. Although multi-electrode shanks are widely employed [2]–[4], they tend to generate ongoing damage and irritation due to relative motion between the implant and surrounding tissue [5]. Therefore, recent efforts have focused on building micro-scale, tetherless implants. While microscale RF [6]–[8] and ultrasonic [9]–[11] systems have shown promise, their transduction mechanisms make scaling below a millimeter challenging. On the other extreme, optical imaging based on calcium/voltage sensitive dyes/proteins allows noninvasive imaging at cell-scale resolution [1]. However, such optical imaging is limited by genetics to certain neurons and species, is impeded by scattering, and has a low temporal resolution. We present tetherless, injectable micro-scale opto-electronically transduced electrodes (MOTEs) which combine the merits of optical and electronic modalities to enable a) extreme scaling down to $60\mu\text{m}$ in cross-sectional diameter and b) direct electrical measurement with a high temporal resolution ($<100\mu\text{s}$). While circuit aspects of MOTEs have been present before [12], the challenges associated with heterogeneous integration and encapsulation are also significant in developing MOTEs, and are discussed here.

II. THEORY

Heating in the brain dictates the maximum available optical power, where we have chosen infrared (IR) based on photo-voltaic (PV) efficiency and minimal absorption in the brain. Reference [13] has shown $160\text{mW}/\text{mm}^2$ at the IR range to be the damage threshold. Our previous work has shown [12], [14] that a MOTEs can function on a few microwatts of delivered power, so that it can function few

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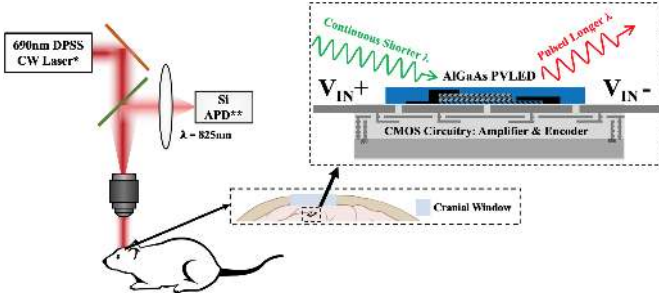


Fig. 1. A simplified schematic of MOTEs-based neural recording [12], [14]. *DPSS CW Laser: Diode-Pumped Solid-State Continuous Wavelength Laser. **Si APD: Silicon Avalanche Photodiode.

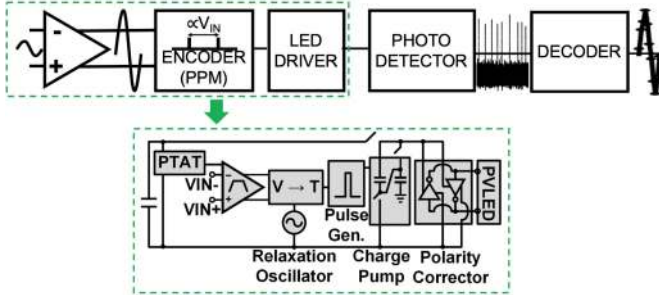


Fig. 2. System Block Diagram of a MOTE [12], [14].

millimeters deep in the brain through a transcranial window without exceeding $160\text{mW}/\text{mm}^2$. The same work has shown that it is possible to build a circuit that can provide $>10\text{kHz}$ bandwidth and $\sim 15\mu\text{V}_{\text{RMS}}$ noise floor, using pulse-position-modulation (PPM) encoding, often used in energy starved systems such as satellites [15].

Fig. 1 shows a proof-of-concept illustration of the MOTE. The proposed system comprises of two parts: a) an optical component, a micro-scale (μ) AIGaAs diode that acts as both a PV for power transfer and as a light emitting diode (LED) for data communication (hence often referred as PVLED [16], [17]), and b) an electrical component, a complementary metal-oxide-semiconductor (CMOS) circuitry for electrical signal amplification and subsequent signal processing. We have chosen $\lambda_{\text{Emission}} = 825\text{nm}$ and $\lambda_{\text{Power}} = 690\text{nm}$ to optimize the PV efficiency while minimizing the brain absorption.

Fig. 2 shows a system-level block diagram for the MOTE circuitry [12], [14], and Fig. 3 illustrates an example of a MOTE operation – 500Hz , $500\mu\text{V}_{\text{PP}}$ test signal is applied at the input differential electrodes, amplified and encoded into optical pulses, and finally detected by a photodetector (PD). The detected pulses' timing, namely their spacing (Δt), can then be used to recover the original sinusoid input.

While the MOTE's two main pillars, PVLED and the CMOS have individually been studied in detail [12], [14], [18], discussion of the associated integration challenges has been lacking. Given the MOTE's size scale, wire-bonding is out of the question for interconnecting PVLED and MOS: a single wire-bond-pad footprint is larger than the MOTE. Furthermore, such bendable wire-bonds jeopardize the insulation needed for chronic recording inside a biological medium. We have instead

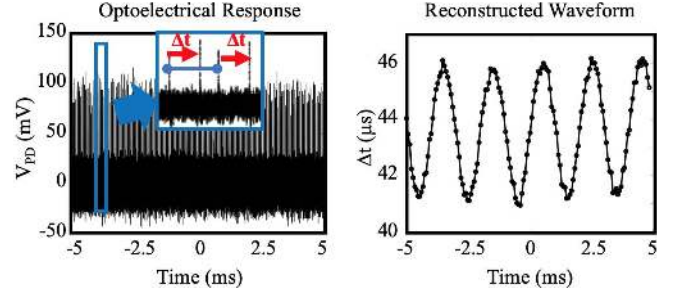


Fig. 3. A MOTE decoding example [12].

photolithographically integrated the PVLED and the CMOS to result in a scalable and robust system. We have optimized the polymer-based transfer method [18], [19] and dielectric cladding to allow MOTEs to survive in a mouse brain for two months (and counting). We also discuss a practical insertion method that has been lacking – a μ -pipette approach to allow users to manipulate and insert the MOTEs with a minimal learning curve.

III. RESULTS

A. PVLED Transfer on CMOS

The following integration process is based on a 180nm foundry CMOS process, whose top metal is aluminum. A MOTE has four contact points: $V_{\text{IN}+}$, $V_{\text{IN}-}$, V_{DD} , and V_{SS} . The V_{DD} and V_{SS} are to be connected to the PVLED (*i.e.* anode and cathode) while the two input electrodes are to be coated with platinum for biocompatibility. Although it is crucial to have a planar surface for a successful PVLED transfer and its adhesion to the CMOS, a CMOS die is not chemical-mechanically polished (CMP) after its final dielectric deposition (*i.e.* the dielectric on top of the top metal) – instead, there is $1\sim 2\mu\text{m}$ of relief in the $\text{Si}_x\text{O}_y\text{N}_z$ dielectric on top of the top metal layer. Hence, we start the integration fabrication with CF_4 reactive ion etch (RIE) on the CMOS (Oxford 80: 150W , 40mTorr , 30sccm CF_4) for about 30 minutes in total. This etch removes all the dielectric above the top metal while the aluminum acts as an etch stop (high selectivity against the CF_4 etch). It should be noted that 'pad opening' designation (the foundry selectively removes dielectric on top of the top metal for bondpads) is not used as the pad opening designation incurs $100\sim 200\text{nm}$ of unremovable (by the CF_4 etch) residues at the opening boundaries (suspected to originate from techniques used to make the openings at the foundry), detrimental to the subsequent PVLED transfer.

Following the dielectric removal, we transfer an AIGaAs μLEDs array that have been tailored to match the CMOS layout, using poly (methyl methacrylate) (PMMA) transfer techniques often used in 2D materials transfers [18], [19], while both the V_{DD} and the V_{SS} aluminum pads are directly below the cathodic layer of the PVLED, they do not form ohmic contacts alleviating leakage concerns.

B. CMOS Integration

The transfer results in PVLED on CMOS with the PMMA still intact. To cleanly remove the PMMA, we employ a high

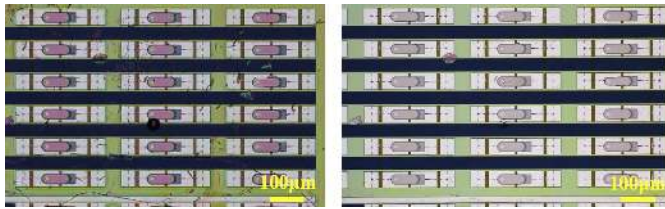


Fig. 4. AlGaAs μ LEDs transferred on top of the MOTE CMOS die, before annealing (left) and after annealing (right).

vacuum annealing (Custom-built: 320°C for 2 hours at less than 10^{-6} Torr, 30-minute ramp from room temperature, and natural cool-down). This anneal not only removes the PMMA better than oxygen plasma it also enhances the adhesion between the CMOS and the μ LEDs (simply using solvent to remove PMMA also washes the μ LEDs off the CMOS surface). Post annealing, it is possible to rinse with solvent as well as deionized water (DI) to better remove polar residues for more than 15 minutes, further reducing the transfer process residues. Fig. 4 compares the before and the after the anneal. Importantly, any excess residues will later inhibit the cladding layer deposition and cause biological media to leak in.

After the annealing and the residue cleaning, $\sim 90\text{nm}$ SiO_2 is deposited using atomic layer deposition (ALD) (Oxford FlexAL: 200°C, Plasma enhanced) to fill micro-cracks and voids, and further the adhesion of the PVLEDs on CMOS. We have found that a temperature lower than 200 °C results in SiO_2 with inadequate quality for cladding. Fig. 5 illustrates the ensuing fabrication steps based on four-mask contact lithography.

1) *Contact*: AZ® nLOF 2002 resist is used with ABM contact aligner to define contact openings. CHF_3/O_2 reactive ion etch (RIE) (Oxford 80: 200 W, 50 mTorr, 50 sccm CHF_3 , 2 sccm O_2 , 9 minutes) removes the ALD SiO_2 in the openings. Then buffered oxide etch (BOE, 6:1, 60 seconds) is used to remove naturally forming aluminum oxide, and form undercuts beneath the nLOF resist. Shortly after the BOE etch, the MOTE is placed inside a sputter for RF sputtering [20] (AJA: Base Pressure $< 10^{-6}$ Torr, RF = 50W, Ti $\sim 5\text{nm}$ for adhesion, Pt $\sim 50\text{nm}$ at 20mTorr), and lifted off in Shipley MICROPOSIT® REMOVER 1165.

2) *Routing*: AZ® nLOF 2002 resist is used again with the ABM contact aligner as in 1) *contact openings*. Because there is no undercut this time, DC sputtering is used (AJA: Base Pressure $< 10^{-6}$ Torr, Ti $\sim 10\text{nm}$ for adhesion, Pt $\sim 90\text{nm}$ at 20mTorr) and it is lifted off in the 1165 as before. There is a trade-off between the thickness of Pt (lower resistance) and the film stress & lift-off viability – we have found that $\sim 100\text{nm}$ to be an optimal point. Also, because the routing metal has to cover uneven topologies, electron beam (e-beam) evaporation is not suitable for this step. Following the routing, $\sim 10\text{nm}$ ALD Si_3N_4 (Oxford FlexAL: 350°C, Plasma enhanced) and $\sim 90\text{nm}$ ALD SiO_2 (Oxford FlexAL: 200°C, Plasma enhanced) are deposited to insulate the routing metals. We find that the performance of MOTEs typically improves post the ALD deposition, likely owing to the thermal annealing effect during the step.

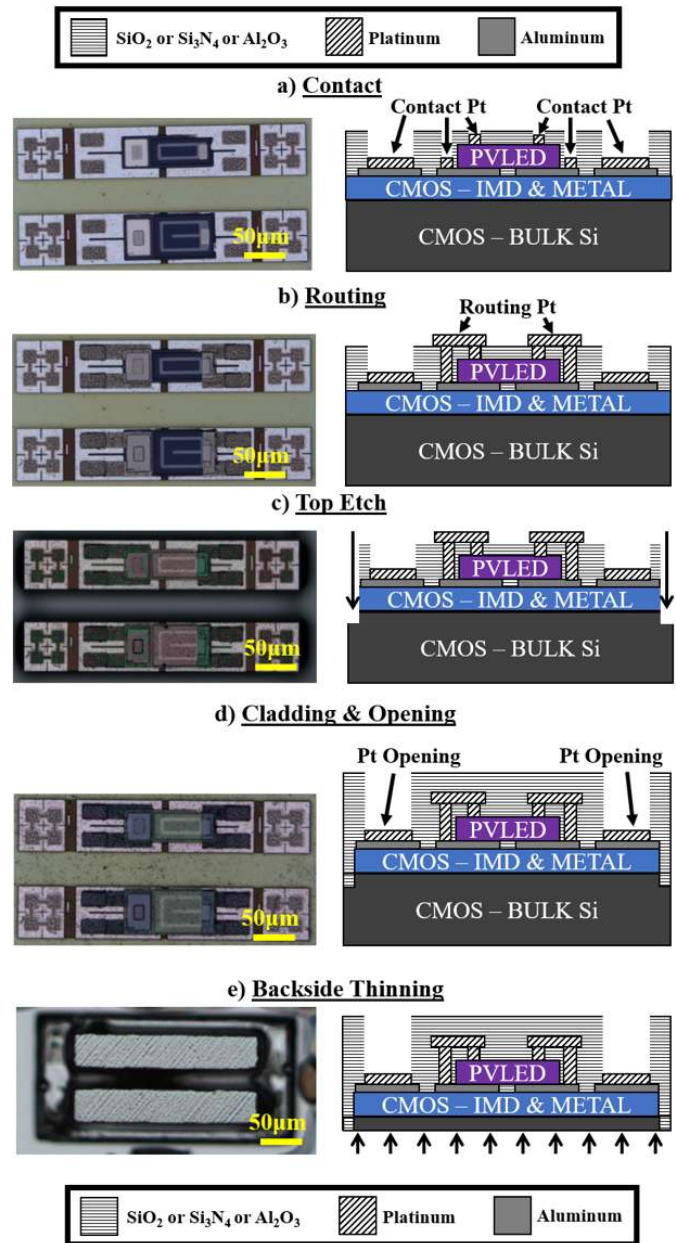


Fig. 5. MOTEs integration fabrication flow.

3) *Top Etch*: This step separates each MOTE in the array. Because we must etch through inter-metal dielectric (IMD) and into the bulk silicon, we use Cr hard mask to withstand the required prolonged etch. RF sputtering is used to deposit the Cr (AJA: Base Pressure $< 10^{-6}$ Torr, RF = 50W, Cr $\sim 100\text{nm}$ at 30mTorr). MEGAPOSIT™ SPR™220-3.0 resist is used with the ABM contact aligner, and the Cr is selectively etched away using TRANSENE CHROMIUM ETCHANT 1020AC. After the Cr etch, the remaining resist is not stripped to serve as an additional etch mask to the Cr.

Inductively coupled plasma (ICP) RIE plasma etch is then used to etch the IMD (Oxford PlasmaPro 100 RIE: ICP = 3000W, RF = 60W, 4mTorr, 20sccm CH_2F_2 , 80sccm He). While the ICP RIE provides excellent etch rate and vertical etch profile, it is difficult to guarantee sufficient

thermal cooling because the tool is made for four-inch wafers and larger, whereas CMOS die are typically on the order of millimeters. Therefore, we have employed a Si carrier wafer that is as thin as possible without being too fragile (four-inch, 400 μ m thick, double side polish (DSP) wafer) and attached our die using AI Technology, Inc. COOL-GREASE™(CGR7016). We have also programmed the etcher to cycle the etch (30s etch followed by 60s cooling). Even with the high power of the ICP RIE, \sim 1hr of etching time is required to remove the IMD, which is \sim 10 μ m of Si_xO_yN_z.

We have noticed that the IMD color differs depending on whether the underlying bulk silicon is defined as diffusion layer or not during the tapeout. Hence, we have defined a section of the etch area to contain both the diffusion and non-diffusion area, so that it is optically apparent when the IMD is all etched away, and Si is exposed.

Following the IMD etch, we used deep-RIE (DRIE) (Unaxis 770 Deep Silicon Etcher) to etch away \sim 25 μ m of the bulk silicon. Together with the IMD thickness (\sim 10 μ m), this defines the maximum thickness of MOTES. This is because subsequent fabrication steps include thinning the backside silicon until the \sim 25 μ m deep trenches appear.

4) *Cladding and Opening*: Following 3) *Top Etch*, both the remaining resist and the Cr are removed by oxygen plasma and the Cr Etch, respectively. Then, plasma enhanced chemical vapor deposition (PECVD) (OXFORD PlasmaPro 100 PECVD) is used to deposit \sim 200nm low stress Si_xN_y (139MPa, Tensile) followed by \sim 900nm tetraethyl orthosilicate (TEOS) SiO₂. Furthermore, \sim 50nm ALD Al₂O₃ (Oxford FlexAL: 200°C, Plasma enhanced) is additionally deposited. While this cladding is needed to ensure longevity of the MOTES inside biological media, input electrodes must be exposed. The photolithographic step is similar to the one shown in c) *Top Etch* – SPR330-2.0 atop sputtered Cr.

For the opening etch, the 3000W ICP RIE cannot be used as the extreme plasma density seems to damage the input capacitor in the CMOS circuitry. Therefore, we resorted to a lower power ICP RIE and a regular RIE which, while slower, are less damaging. We first etched away the Al₂O₃ using BCl₃/Ar ICP RIE (PlasmaTherm 770: ICP = 800W, RF = 15W, 7mTorr, 45sccm BCl₃, 5sccm Ar), followed by CHF₃/O₂ RIE etch (Oxford 80: 240W, 40mTorr, 50sccm CHF₃, 2sccm O₂) to remove the remaining dielectric. The same etching is then repeated on the backside of the MOTES chip as the conformal nature of the ALD and PECVD often leads to the unwanted dielectric deposition on the backside. Then the SPR220 photoresist and Cr are removed as in 3) *Top Etch*.

5) *Backside Thinning*: The final step, thinning, is done through DRIE (Unaxis 770 Deep Silicon Etcher), which while being efficient in terms of the etch rate, suffers from the same issues as the ICP RIE during IMD etch – heating and handling. While Cornell NanoScale Facility (CNF) possesses higher power (hence faster etch) DRIE (PlasmaTherm Deep Silicon Etcher: 3000W vs. 800W of the Unaxis), we opted for the lower power Unaxis due to heating concerns. Therefore, we first spun the SPR 330-2.0 resist on a 400 μ m thick DSP wafer, and before the resist bake, the MOTES die is placed

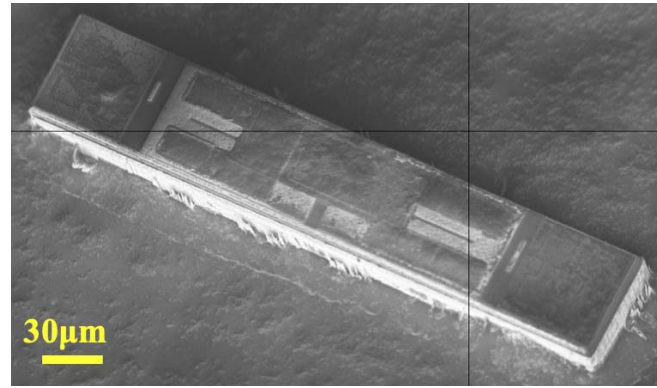


Fig. 6. A scanning electron microscope (SEM) image of a fully released MOTE.

TABLE I
A YIELD TABLE OF MOTES FABRICATION

MOTE V5_C24	1	2	3	4	5	6	7	8	9
1	Green	Red	Green	Green	Green	Red	Green	Red	Green
2	Green	Green	Green	Green	Green	Red	Green	Green	Green
3	Green	Green	Red	Green	Green	Green	Red	Red	Green
4	Green	Green	Green	Green	Green	Green	Green	Red	Green
5	Red	Green	Green	Green	Green	Green	Green	Green	Green
6	Green	Green	Green	Green	Green	Green	Green	Green	Green
7	Green	Green	Green	Green	Green	Green	Green	Green	Green
8	Green	Green	Green	Green	Green	Green	Green	Green	Green
9	Green	Red	Green	Green	Green	Green	Green	Green	Green
10	Green	Green	Green	Green	Green	Green	Green	Green	Green

CMOS Platform	90	Dead Devices	14.00
μ LED Transferred on	90	Alive Devices	76.00
Transfer Yield (%)	100	Total Yield (%)	84.44

upside down against the freshly spun resist, and gently pressed before being baked for twice the typical soft-bake time. Lastly, DRIE (Unaxis 770 Deep Silicon Etcher) is used in cycles, 40 loops at a time (follow by 30 seconds of cooling on a room temperature chill plate) to minimize the excess heating, until the trenches defined in the c) *Top Etch* appear.

It is important to note that if there are any residues present in between the CMOS and the μ LEDs, then the heating is exacerbated and the MOTES can be destroyed during this DRIE or ICP RIE etching for 3) *Top Etch*, as the authors found, painfully, prior to the adaptation of the high vacuum annealing.

Once the trenches appear, we immerse the MOTES on the carrier wafer in acetone, and through medium exchange, the MOTES are transferred to isopropanol, and finally to sterile water. Fig. 6 shows a fully released MOTE post the integration fabrication.

Table 1 describes the yield of the integration fabrication from the latest run. As shown, the μ LEDs transfer is often perfect (the transfer yield rarely drops below 90%), and most failures are likely incurred during the integration fabrication. Though μ LEDs may get damaged (*i.e.* micro cracks) during the transfer, this is hard to ascertain at the time of transfer.

An interesting phenomenon we have noticed is that once the MOTES are released, and in a solution (*i.e.* saline), if there are any cracks in the encapsulation, inorganic ‘black mold’ quickly appears upon exposure to light. We speculate that this is likely due to an unwanted electrochemical interactions powered by the PVLED. Micro-bubbles near the cracks can

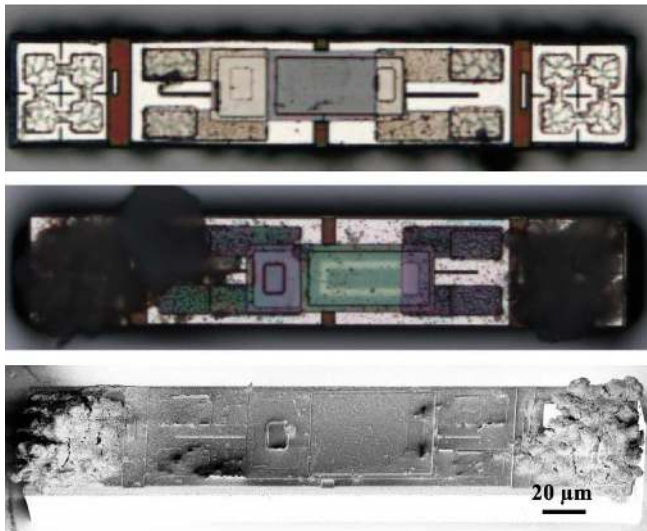


Fig. 7. Successful encapsulation (top) vs. defective encapsulation (middle). The bottom is a SEM image of the middle.

also be observed during such failure processes – typically the micro-bubble sites quickly turn into ‘black mold’ sites. Fig. 7 compares a successful MOTE against its defective counterpart.

IV. HANDLING AND INSERTION

Once the MOTEs are in a sterile solution, individual MOTEs are nearly invisible to a naked eye, making them extremely difficult to handle. We have found using μ -pipettes (with fiber) under a stereoscope (Thermo Fisher Scientific Fisher Stereomaster F1411-D830-002) to be the most straightforward method to handle and insert MOTEs. Once a μ -pipette is inserted near a MOTE in solution, capillary forces draw solution into the pipette, along with a MOTE. The μ -pipette tip can then be placed in contact with a paper wipe (we have used Kimberly-Clark Kimtech Science Kimwipes), and as the wipe absorbs solution inside the μ -pipette, the MOTE will be brought to the tip of the pipette. Thanks to the light weight of the MOTE ($\sim 1\mu\text{g}$), the van der Waals attraction between the μ -pipette and the MOTE is enough to keep the MOTE intact inside the now-dry μ -pipette while moving.

To insert the MOTE into the brain, we have affixed the MOTE-containing μ -pipette to a X-Y-Z micro-positioner and inserted a stainless-steel wire into the μ -pipette as a push mechanism. Once the cranial opening is made, the μ -pipette is brought to touch down on dura. Because a MOTE is similar to a razorblade in its dimensions, it is possible to puncture the dura with the MOTE (*i.e.* the μ -pipette, which is bigger than the MOTE, stays outside dura, minimizing the insertion damage). Fig. 8 depicts the insertion scheme and a *in vivo* insertion into a mouse brain.

Each MOTE insertion can take as little as five minutes after a few practice sessions, and we have routinely implanted four to eight MOTEs each surgery. Once the MOTEs are inserted, a head bar window is installed to allowed for awake neural recording. Fig. 9 shows a mouse with the head bar and a typical *in vivo* measurement setup. While we have yet to obtain a

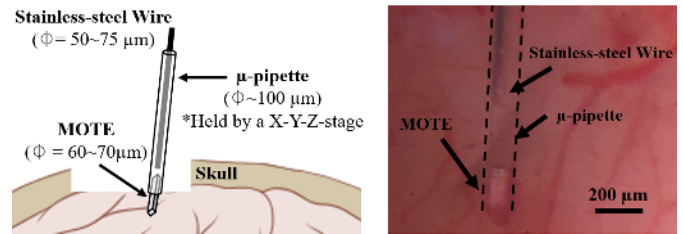


Fig. 8. A MOTE insertion using a pulled μ -pipette. The left shows a simplified insertion mechanism while the right shows an *in vivo* insertion.



Fig. 9. A mouse with a head bar window, ~ 2 months after the insertion surgery (left). The right shows the mouse (awake) under measurement using a head-bar fix apparatus.

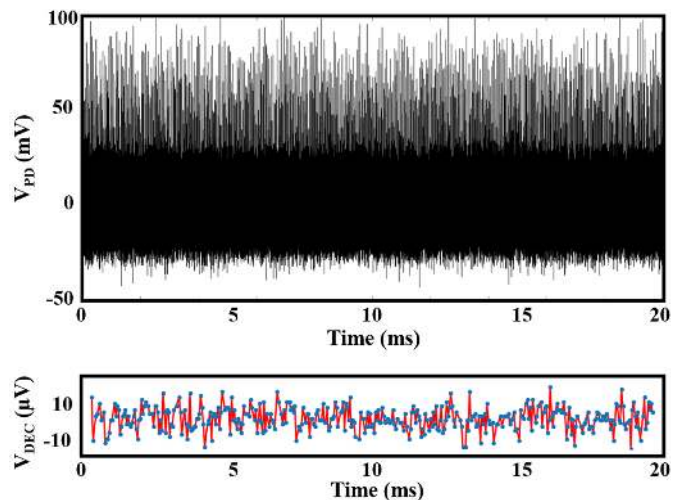


Fig. 10. A MOTE measurement *in vivo*. While the decoded signal (bottom) did not show a neural response, the observed optical pulses (top) indicate that the MOTE is functioning as designed.

neural signal from the MOTE (as inserting MOTEs near active neurons is largely chance based), Fig. 10 demonstrates that the inserted MOTEs are functioning properly, outputting pulses (insertion depth $\sim 200\mu\text{m}$, optical power $\sim 23\text{mW}/\text{mm}^2$).

V. CONCLUSION

For chronic, tetherless neural recording, MOTEs provide a compelling alternative to existing modalities such as electrodes shanks and coils/ultrasound-based implants. The heterogenous integration described in this manuscript has not only enabled the MOTE to be scaled down below human hair width, but also enabled the MOTEs to be fabricated en masse with high yield, proving scalability of the technology. Table II compares the MOTEs against state-of-the-arts.

TABLE II
TABLE OF COMPARISON

	Integrated Neural Interface [6]	Microwave Backscattering [21]	Neural Dust [11]	MOTE [This Work]
Wireless Power Source	RF Coil	RF	Ultrasonic	Optical
Technology (nm)	500	-	65	180
Gain (dB)	60		24	24
Bandwidth (kHz)	5	5	5	10
Noise Floor (μV_{RMS})	5.1	63	5.3	15
Power	135 μW	0	37.7	<1 μW
Cross-sectional Diameter	>300 μm	>10mm	>500 μm	>57 μm
Volume per Channel (mm^3)	>10	360	0.8	<1 $\times 10^{-7}$
Functional Depth (mm)	Surface Only	Surface Only	50	<5 (est.)
Functional Depth/Volume per Channel (mm^{-2})	-	-	61.7	<5 $\times 10^3$

MOTES can survive in biological media for months timescale, can easily be integrated with standard microscopy systems, and can be handled with μ -pipettes that many biologists are familiar with. Furthermore, the proposed fabrication and handling methodologies are applicable to other types of heterogeneously integrated CMOS systems.

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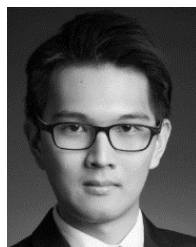


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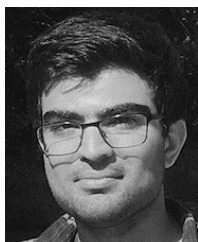
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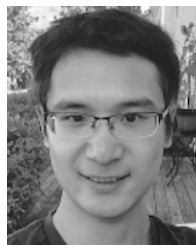
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