Fabrication of Photonic Wire and Crystal Circuits in Silicon-on-Insulator Using 193nm Optical Lithography

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***Abstract*—High-index contrast silicon-on-insulator technology enables wavelength-scale compact photonic circuits. We report fabrication of photonic circuits in silicon-on-insulator using complementary metal-oxide-semiconductor processing technology. By switching from advanced optical lithography at 248 nm to 193 nm, combined with improved dry etching, a substantial improvement in process window, linearity, and proximity effect is achieved. With the developed fabrication process, propagation and bending loss of photonic wires were characterized. Measurements indicate a propagation loss of 2.7 dB/cm for 500 nm photonic wire and an excess bending loss of 0.013 dB/ $90\,^{\circ}$bend of 5 μm radius. Through this paper, we demonstrate the suitability of high resolution optical lithography and dry etch processes for mass production of photonic integrated circuits.**

***Index Terms*—Nonophotonics, Waveguides, Silicon-on-Insulator (SOI), Photonic crystal.**

I. Introduction

High refractive index contrast and transparency at telecom wavelengths (1300 nm/1500 nm) make silicon (Si) an ideal material for integrated photonic applications. Exploiting this high refractive index contrast, researchers have demonstrated low-loss waveguides and small radius bends [1], [2], [3]. Active functionalities such as modulators have recently been proposed and successfully demonstrated [4], [5] ; aiming at compact components and circuits. However, as a consequence of the high index contrast and the waveguide dimensions being close to the diffraction limit, the device response is very sensitive to any dimensional variation. Therefore, we need an accurate dimensional control in the range of 1-5 nm. To achieve such requirement a high resolution fabrication process is needed.

In recent years, electron beam lithography was used extensively for making photonic integrated circuits by many research groups [1], [3], [4], [5], [6]. Even though e-beam steering can allow accurate dimensional control [7], it is tedious, slow and, due to the small writing area it is unsuitable for mass production. Though low propagation loss photonic wires were reported using high resolution e-beam resist (HSQ) [1], a number of works have noted a degree of instability and irreproducibility issues in this material [8], [9], [10]. Its insensitivity to deep ultra-violet wavelengths and these reliability issues render it unusefull for high volume manufacturing in its present state.

Alternatively, advanced optical lithography systems, which are used for present day electronic IC fabrication, can be exploited. Deep UV lithography at 248 nm and 193 nm offers high resolution and mass production capabilities. These fabrication tools can pattern $\geq$135 wafers/hr in a production environment, with an layer-to-layer alignment accuracy of $\leq$12 nm [11]. The use of 248 nm Deep UV lithography for fabricating nano-photonic integrated circuits was explored to great extent by Bogaerts et al [2]. His works [2], [12], [13] clearly demonstrates the feasibility of CMOS fabrication tools for fabricating photonic integrated circuits. However, with 248 nm DUV optical lithography issues such as optical proximity effect (OPE), resolution, process window, and uniformity can not meet the requirements for advanced nano-photonic integrated circuits. With 193 nm optical lithography, there should be an improvement in OPE [14], process window, uniformity, and resolution.

In this paper, we demonstrate fabrication of photonic wire and photonic crystals in SOI using 193 nm optical lithography and dry etching. All the processes were developed for CMOS compatibility and mass production.

This paper is organized as follows. A brief overview of the fabrication process is given in section II. Section III discusses the 193 nm optical lithography process and optimization for photonic wire and crystal structures. Various lithography issues, such as the proximity effect and process windows are also discussed. In section IV, we discuss the dry etching of Si and the results are presented. In section V, the developed fabrication process is assessed by measuring the propagation and bend loss in the photonic wire and conclusions are drawn in section VI.

II. Fabrication process overview

We use mono-crystalline Silicon-on-Insulator (SOI) for fabricating the nanophotonic circuits. The 200 mm SOI wafers were manufactured by SOITEC using the UNIBOND process [15] and have 220 nm of Si on top of 2 μm buried oxide (BOx). An overview of all the steps involved in fabricating a nanophotnoic device is depicted in Fig.1 and will be explained in detail in the following sections. To reduce the dry etch development cost, the expensive mono-crystalline silicon on insulator is replaced by poly-crystalline silicon-on-insulator

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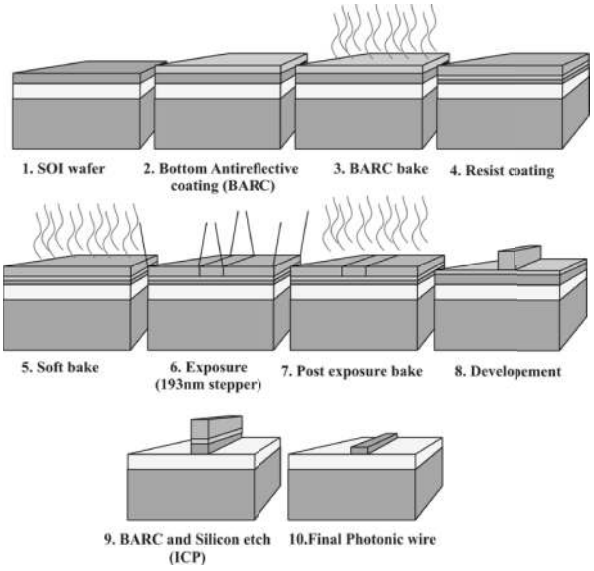

Fig. 1. Fabrication process overview of a photonic device in SOI using 193 nm optical lithography.

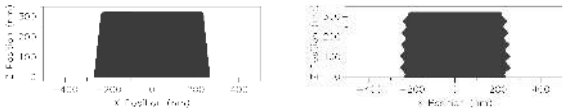

Fig. 2. Simulated photoresist profile with (left) and without (right) bottom anti-reflective coating.

for etch tests. We observed no difference in the etching properties when using poly-Si or mono-crystalline Si. All our experiments were performed in the pilot-line of the advanced microelectronics research facility of IMEC, Belgium.

III. Optical Lithography Process

For optical lithography, we used an ASML PAS5500/1100 step-and-scan system. The scanner uses an ArF laser at 193 nm for imaging. A TEL-ACT clean track system is attached to the stepper for resist processing (resist/antireflective coating, baking and development). The lithography steps involved in the fabrication process are summarized in Fig. 1(step1-8). The

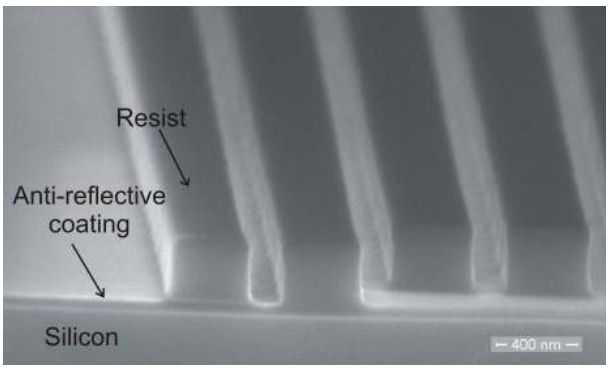

Fig. 3. Resist profile after exposure and development.

resolvable resolution (R) of an optical lithography system is given by [16],

$$R \propto \frac{\lambda}{NA} = k\frac{\lambda}{NA} \tag{1}$$

Where λ is the illumination wavelength, NA is the numerical aperture of the projection system and k is a proportionality constant determined by the resist process and the mask. Theoretically, there is no resolution limit for an isolated structure (e.g. photonic wire). But periodic structures, such as, photonic crystal and grating structures diffract finite spatial frequencies spaced at 2 λ/p, where p denotes the pitch. The image is formed on the wafer by capturing the diffracted light (at least 1^{st} order) from the mask and allowing them to interfere on the wafer. Therefore, the smallest resolvable pitch is determined by the illumination wavelength (λ) and capturing capacity (NA) of the projection system. Eq. 1 is valid for a perfectly coherent illumination source, but in practice the stepper uses a partially coherent light source [16], hence Eq. 1 should be rewritten as,

$$R = k\frac{\lambda}{NA(1+\sigma)} \tag{2}$$

Where σ is the the coherency factor, indicating the spatial coherence, or the angular distribution of the light source. This factor is defined by the size of the illuminating source compared to the pupil of the imaging system . When σ = 0, the source a perfectly collimated beam with zero diameter in the pupil, i.e. a coherent point source (Eq. 1). For $\sigma > 0$ the source has a definite size and hence is partially coherent. In our stepper, σ can be varied between 0.3 and 0.85.

A. Experiment

A 200 mm SOI wafer is coated with an organic anti-reflective coating and photoresist in a clean track. The thickness of the bottom anti-reflective coating (BARC) is chosen to be 77 nm to reduce reflection from the SOI layer stack. Without a BARC layer, the reflections from the substrate create standing waves in the resist resulting in an undesirable resist profile. Fig. 2 depicts the effect of the BARC layer on the resist profile.

After BARC (77 nm) and resist coating (330 nm), the wafer is baked to remove the solvent from the applied layers. After baking, the wafer is then illuminated with the desired mask pattern. The exposure parameters, namely, dose and focus are varied to find the optimum conditions. The conditions used in the experiment are shown in Table I. After exposure, the wafers are baked again and developed to remove the exposed part of the photoresist in a developer solution. Fig. 3 depicts the resist profile after development. As the BARC layer is insoluble in developer solution, it is removed during dry etching.

B. Process optimization

From lithography point of view, photonic circuits are different from CMOS circuits. In CMOS circuits, dense and isolated structures are printed at different lithography steps and the

TABLE I
LITHOGRAPHY PROCESS CONDITIONS

Parameters	Values
Illuminating wavelength	193 nm (ArF)
Numerical aperture (NA)	0.6 - 0.74
Coherence (σ)	0.6 - 0.85
Exposure dose (mJ/cm2)	16 - 40
Defocus (μm)	-0.5 - 0.5

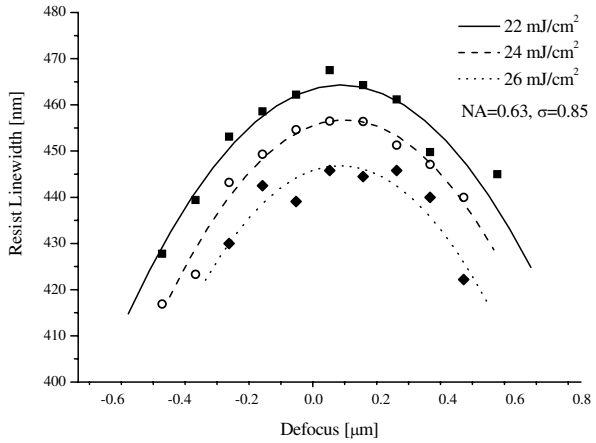

Fig. 4. Bossung curve for 450 nm photonic wire

tolerances are relaxed (range-10%). Therefore, processes can be optimized for dense and isolated structures separately. On the other hand, in photonic circuits, all waveguide structures must be accurately aligned with each other, so dense structures (photonic crystals) are printed together with isolated (photonic wires) structures and at the same time, nanometer accuracy is required (range 1%).Optimizing the lithography process for these two types of structures simultaneously is not straightforward.

To optimize the lithography process, we have divided the photonic circuits into two groups; photonic wire circuits and photonic crystal circuits. Circuits with wire structures, such as ring resonators, Mach-Zehnder interferometers and arrayed waveguide gratings are considers as photonic wire circuits. Circuits with holes in a triangular lattice are considered as photonic crystal circuits.

1) Photonic wire circuits: A 450 nm photonic wire, which is the basic component for a photonic wire circuit, is taken as the test structure for optimization. For the lithography, we used a fixed NA = 0.63 and σ = 0.85, while focus and dose are varied to find the optimum condition. On a 200mm Si wafer, the exposure dose is changed from west to east and focus from north to south resulting in a focus-exposure matrix (FEM). Fig. 4 depicts the measured line width as a function of focus and exposure dose (so-called Bossung curve)[17]. By changing the exposure dose, the photonic wire width can be varied from the design width (Fig. 5) resulting in a wealth of information from a single device design. With single illumination condition we were able to print line widths from 150-500 nm without any dimensional correction achieving a

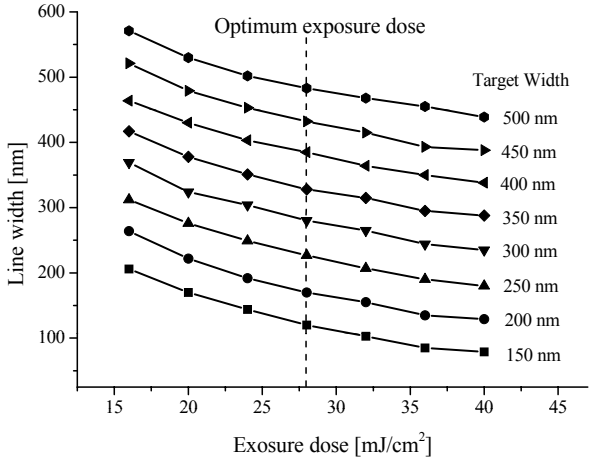

Fig. 5. Line width as a function of exposure dose at optimum focus (NA=0.6, σ=0.85).

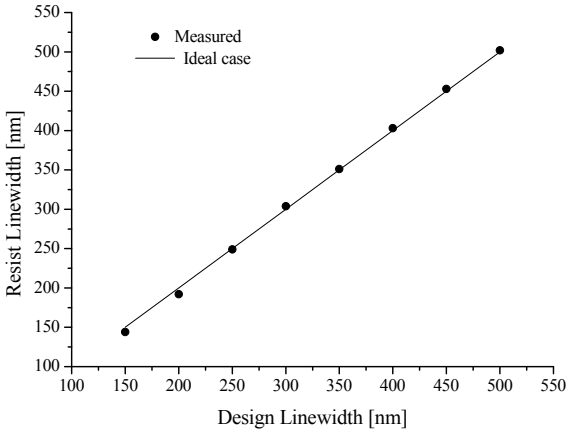

Fig. 6. Different line widths can be printed on target without individual optimization. The process is optimized for 450 nm photonic wire which shows high linearity.

linear response (Fig.6). From these measurements, we extract the process window, which can be defined as the area in the parameter space, where the dimensional variation is within an allowed tolerance. The illumination parameters, mainly, focus and exposure dose can vary due to various factors, such as, resist thickness, substrate reflectivity or lithography tool related issues. Hence an acceptable process window is necessary for a stable lithography process.

Fig. 7 shows the process window of a 450 nm photonic wire with 1% line width variation or 4.5 nm. Any variation of exposure dose or focus within the ellipse will not change the linewidth more than 1%. At optimum focus and exposure dose, we have achieved exposure latitude of 5% at 0.3um depth of focus.

2) Photonic crystal structure: Even more than photonic wire structures, photonic crystals are very challenging structures to fabricate by optical lithography. In CMOS circuits, two dimensional arrays of holes are used for contact holes. However, the density of such structures is typically much lower than for photonic crystals. In this paper, we consider densely packed photonic crystal with circular holes within a triangular

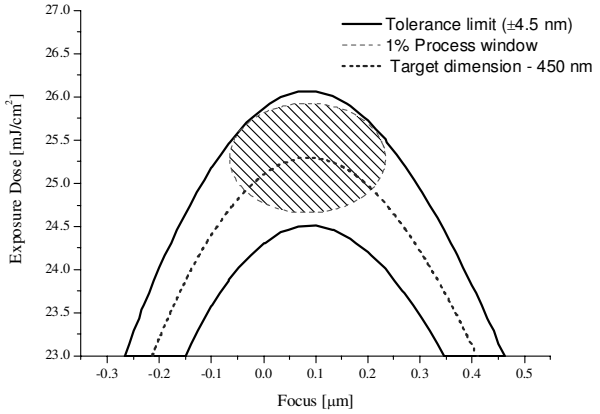

Fig. 7. Process window of a 450 nm photonic wire. Any change in the dose or focus with-in the ellipse will result in wire width variation within 1% or 4.5 nm.

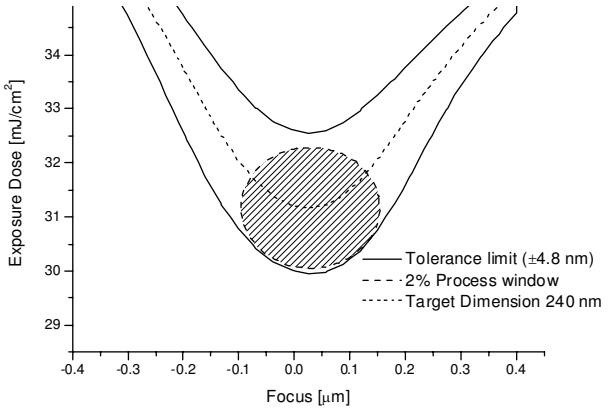

Fig. 8. Process window of photonic crystal of 400 nm pitch and 240 nm hole diameter. Any change in the dose or focus with-in the ellipse will result in hole diameter variation within 2% or 4.8 nm.

lattice.

Photonic crystals with different pitch and fill factors were fabricated with the lithography setting optimized for a photonic wire. Fig. 9 shows the fabricated hole diameter as a function of the exposure dose. The fill factor can be lithographically tuned by varying the exposure dose. Fig. 10a shows an overexposed photonic crystal structure with design pitch of 500 nm and 440 nm hole diameter (r/a= 0.44). By over exposure (higher dose) the hole diameter is increased to 490 nm resulting in a mere 50 nm vein of thin resist between the holes. This thin resist is still sufficient to etch a 220 nm hole in the Si layer (Fig.10b). With an optimized lithography process pitches as low as 300 nm can be defined (Fig. 10c and d), which was the minimum pitch available in our test mask. Fig. 8 shows the process window of photonic crystal with 400 nm pitch and 240 nm hole diameter. Any variation of exposure dose or focus within the ellipse will not change the linewidth more than 2%.

3) Overlapping process window : In order to fabricate photonic wires and photonic crystals in a single lithography step, one should have common illumination conditions (NA, σ, focus and exposure dose) to print them on target. From our experiments, we have found that with NA=0.63 and σ=0.85,

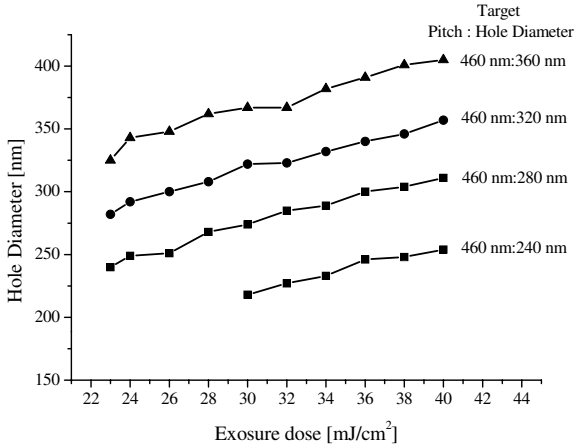

Fig. 9. Photonic crystal hole diameter as a function of exposure dose.

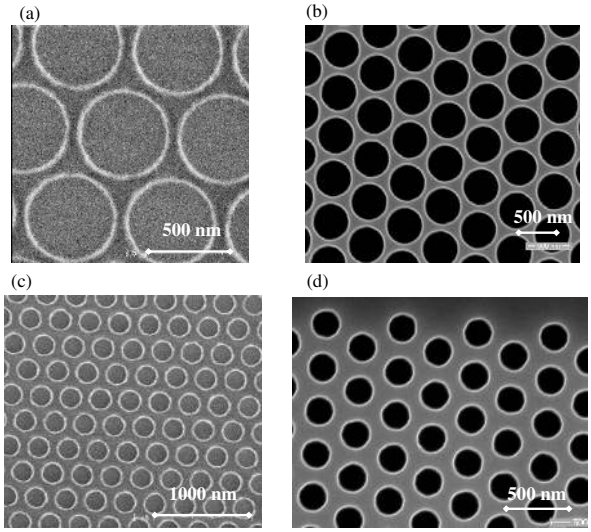

Fig. 10. Top-down SEM image of photonic crystals a) resist pattern pitch =550 nm, hole diameter = 450 nm , b) same patter on Si after etching, c) resist patter pitch =300 nm, hole diameter = 240 nm, d) same patter on Si after etching

at the dose of 33 mJ/cm^2, where 280 nm holes with 500 nm pitch print correctly, the 450 nm wide photonic wire was only 423 nm . Therefore, a bias of +27 nm has to be applied in the mask to photonic wires to print correctly. This bias can be tremendously reduced by changing the NA and σ however.

Fig. 11 depicts the hole diameter as a function of exposure dose for two different NA/σ settings. By increasing the NA and reducing σ the dose-to-target is reduced by 14%. As a consequence, the required bias for photonic wires is reduced from 27 nm to 8 nm (Table II). These corrections should be known in advance to apply them during mask fabrication; hence, an extensive characterization using suitable test structures is a must before designing masks for manufacturing photonic circuits.

C. Optical proximity effect

A superdense arrangement of holes in a photonic crystal gives rise to an optical proximity effect (OPE), which is

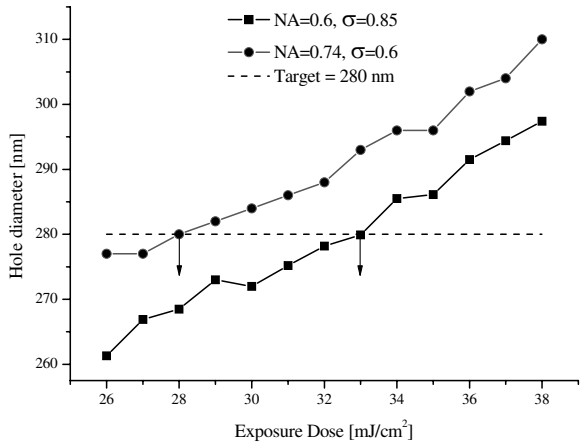

Fig. 11. Decrease in dose to target with higher NA and lower σ. For pitch=500 nm, hole dia.=280 nm the exposure dose is reduced from 33 mJ/cm2 to 28 mJ/cm2.

TABLE II
PHOTONIC WIRE BIAS CORRECTION FOR DIFFERENT ILLUMINATION SETTINGS.

Illumination setting	Photonic crystal Dose-to-traget	Photonic wire printed width	Photonic wire bias
NA=0.6, σ=0.85	33 mJ/cm^2	423 nm	27 nm
NA=0.74, σ=0.6	28.5 mJ/cm^2	442 nm	8 nm

defined as the change in feature size as a function of the proximity of other nearby features. OPE depends strongly on feature proximity, illumination settings (NA, σ, source shape) and wavelength. OPE can be partially corrected (optical proximity correction - OPC) at the mask level by adding sub-resolution assist features (SRAF), which is a standard procedure in mask design for microelectronics circuits [16].

Using 248 nm DUV optical lithography, Bogaerts et al [2] reported an OPE of 40 nm for the holes in a photonic crystal. By using 193 nm optical lithography, we observe a substantial reduction in OPE (Fig. 12). The difference between edge holes and bulk holes is reduced from 40 nm (248 nm Litho) to 5 nm (193 nm Litho). This reduction agrees with the results published by Settle at al [14]. These experiments clearly demonstrate that high resolution optical lithography can reduce OPE.

OPE not only affects superdense photonic crystals, but also photonic wire structures. When an isolated line comes in close proximity with another line (e.g. in an optical coupler), the line widths of both lines reduce as a function of the distance between them. Fig. 13 illustrates OPE in a double line configuration, the inset shows the arrangement of the double lines. A sharp drop in the line narrowing is observed for gap widths larger than the illuminating wavelength. Thus, the corrections required for $<$ 200 nm gap features are much more important than for the $>$ 200 nm features.

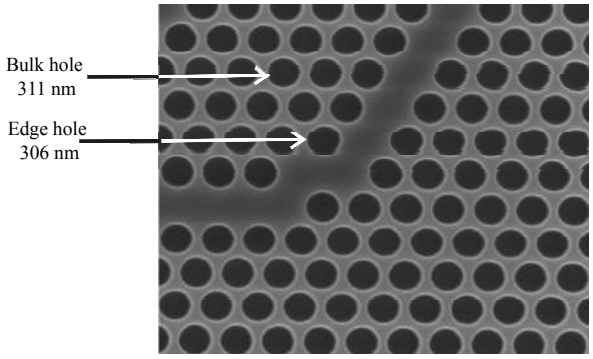

Fig. 12. Optical proximity effect in Photonic crystal circuit. The edge hole diameter is only 5 nm smaller than the bulk holes.

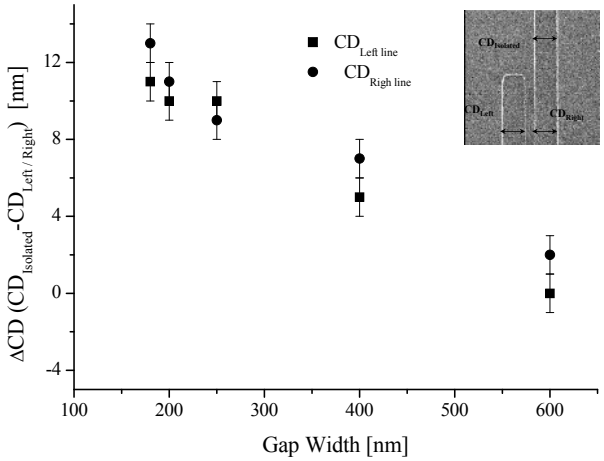

Fig. 13. Optical proximity effect in Photonic wires.

TABLE III
ETCH GAS MIXTURE USED FOR SI ETCH

Etch process	Gas	Reason
Break through (BT)	CF_2/CH_2F_2	Remove native oxide on Si
Main Etch 1 (ME1)	$CL_2/HBr/CF_4/O_2$	Reduce iso-dense CD bias
Main Etch 2 (ME2)	HBr/O_2	Highly selective Si etch
Over Etch (OE)	HBr/O_2	Remove Si foot

IV. ETCH PROCESS

Following lithography, the pattern defined in the photoresist is transferred into the underlying Si by dry etching. We use inductively coupled plasma-reactive ion etching (ICP-RIE) to etch Si. Photoresist is used as an etch mask. Two different gas chemistries (Table III) were used. The Si etch process is critical for photonic devices: it is well known that dry etching creates rough sidewalls resulting in scattering loss [18] and degrades the device performance (propagation loss, Q factor, etc.). Therefore, a suitable etch scheme with smooth sidewalls and better dimensional control is required.

To etch 200 nm of Si with a resist mask, we use six etch steps in total; two for the BARC and resist processing, and four for the Si etch. All the processing steps were done in sequence without removing the wafer from the etch chamber.

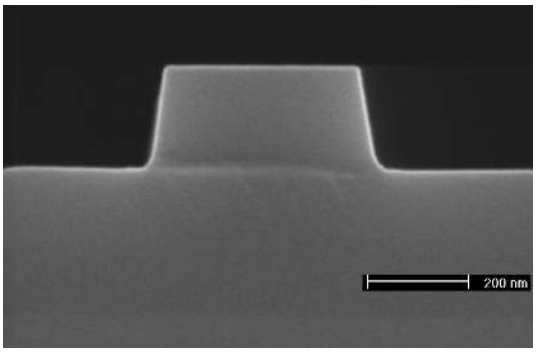

Fig. 14. Cross-section SEM image of a 500X220 nm photonic wire after Si etch and strip.

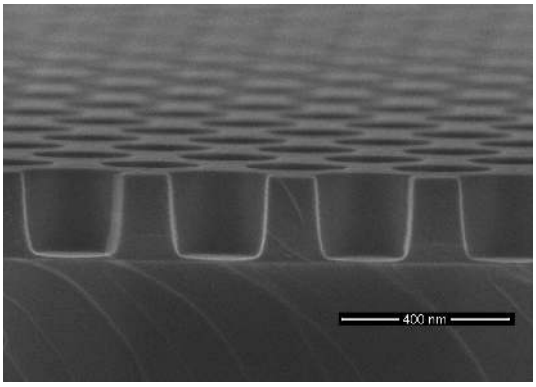

Fig. 15. Cross-section SEM image of a photonic crystal after Si etch and strip.

Before the Si etch, the BARC layer has to be removed to reach the Si layer (Fig.3). A Br/F based chemistry is used to etch this layer, followed by a Br plasma treatment. The Br plasma treatment is applied to make the photoresist more resistant to etch gases , which increases the etch selectivity and to reduce the roughness in the photoresist [19]. After Br treatment, the etch sequence switches to a four-step Si etch. The different steps are the break-through etch (BT), main etch 1 (ME1), main etch 2 (ME2) and over-etch (OE). Each step has different chemistry and purpose, Table III summarizes them.

One of the main requirements for a good etch process for a photonic device is good control over the critical dimension (CD) of the devices (i.e line width, hole diameter,). Therefore ME1 is tailored to decrease the lateral CD bias between isolated structures (wires) and dense structures (photonics crystals) [20]. After ME1, we switch to ME2, which uses HBr/O2 chemistry to etch the major part of Si. The etch rates of ME1 and ME2 were accurately controlled to reach an etch depth of 220 nm. ME2 is highly selective [21] to SiO2, etching will be stopped when it reaches the BOx layer.

Following Si etch the remaining photoresist and BARC is removed by a combination of dry and wet strip processes. Fig. 14 depicts a 500 nm wide fabricated photonic wire. Even though we used two different gas chemistries to etch, the etch profile does not show a discontinuity. ME1 and ME2 are accurately controlled to achieve a highly reproducible etch process. Due to the highly passivating nature of ME2, we observe a sloped sidewall angle of 8°. On the other hand, by using this passivating layer the sidewalls can be protected from the ion bombardment, thus reducing the roughness on the sidewalls. Fig. 15 depicts the cross section micrograph of a photonic crystal in Si.

V. Optical Measurements

The 193 nm optical lithography and dry etching process developed is evaluated through optical characterization. In order to measure propagation loss and bending loss, we have fabricated spiral photonic wires with different wire length and bending radius. Photonic wire lengths were varied from 0.5 mm to 5 mm, while the number of 90° bends was varied from 50 to 550 with a bending radius of 1, 2, 3 and 5 μm.

To characterize the photonic wires a broad band light source is used as the light source and the transmitted power is

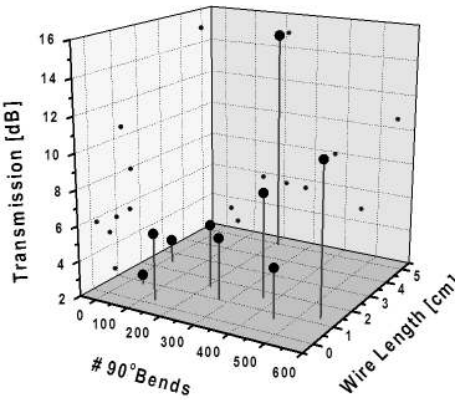

Fig. 16. Measured power as a function of photonic wire length and number of 90° bends of 5 μm radius for a 500 nm photonic wire.

measured using a spectrum analyzer with 0.1 nm spectral resolution. The input polarization (TE(E_x) - parallel to wafer plane) of the light is controlled using a polarization controller. Grating fiber couplers [22] were used to couple light in and out of the circuit. The output power measured from different photonic wire lengths and bends is projected in the parameter space as shown in Fig. 16. By fitting the measured power in the paramter space we can extract the propagation loss of the wire and the excess bend loss.

For a 500 nm wide photonic wire, we have extracted a propagation loss of 2.7 $\pm$0.06 dB/cm. Fig. 17 depicts the extracted excess bending loss for a 500 nm wide photonic wire. The excess bending loss includes mode mismatch at the straight-bend interface, coupling to TM and higher order modes in the bend section and propagation loss in the bends. We have also measured photonic wires with varying width (500 - 450 nm). The propagation loss did not change appreciably within this range, the maximum variation was limited to 0.2 dB/cm. Thus a flat propagation loss regime existed between 450 nm and 500 nm photonic wires.

VI. Conclusion

It has been shown that by using 193 nm optical lithography and an optimized dry etching process it is indeed possible to fabricate photonic devices with the required high resolution and excellent control of the critical dimensions. Moving from

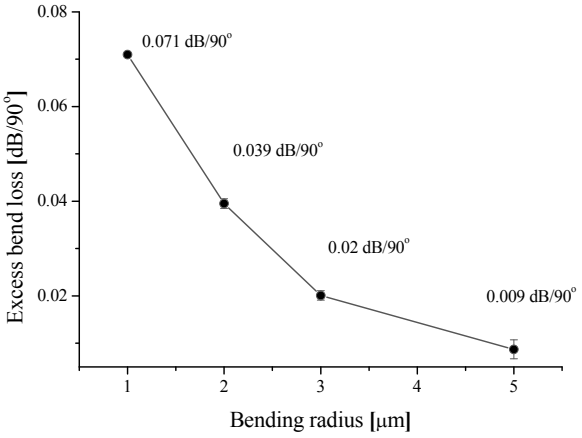

Fig. 17. Extracted excess bend loss of a 500 nm photonic wire.

248 nm to 193 nm optical lithography, we have observed a substantial improvement in process window, proximity effect and resolution. By optimizing the illumination conditions (NA and σ), we could print photonic crystals and wires with very small design bias (8 nm) to photonic wires. The proximity effects in photonic crystals were reduced from 40 nm with 248 nm process to only 5 nm with 193 nm optical lithography. Using photoresist as the etch mask, we have dry-etched 220 nm of Si using a process with two etch chemistries. The etch rates and profiles were accurately controlled to obtain a continuous sidewall. With this process we have made photonic wires with propagation loss of 2.7 dB/cm and excess bend loss of 0.009 dB/90 °bend of 5 μm radius.

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REFERENCES

[1] M. Gnan, S. Thoms, D. S. Macintyre, R. M. De La Rue, and M. Sorel, "Fabrication of low-loss photonic wires in silicon-on-insulator using hydrogen silsesquioxane electron-beam resist," Electron. Lett. , vol. 44, no. 2, pp. 115-116, 2008.

[2] W. Bogaerts, R. Baets, P. Dumon, V. Wiaux, S. Beckx, D. Taillaert, B. Luyssaert, J. Van Campenhout, P. Bienstman, and D. Van Thourhout, "Nanophotonic waveguides in silicon-on-insulator fabricated with CMOS technology," J. Lightw. Technol, vol. 23, no. 1, pp. 401-412, 2005.

[3] Y. A. Vlasov and S. J. McNab, "Losses in single-mode silicon-on-insulator strip waveguides and bends," Opt. Express, vol. 12, no. 8, pp. 1622-1631, 2004.

[4] B. Schmidt, Q. F. Xu, J. Shakya, S. Manipatruni, and M. Lipson, "Compact electro-optic modulator on silicon-on-insulator substrates using cavities with ultra-small modal volumes," Opt. Express, vol. 15, no. 6, pp. 3140-3148, 2007.

[5] L. J. Zhou and A. W. Poon, "Silicon electro-optic modulators using p-i-n diodes embedded 10-micron-diameter microdisk resonators," Opt. Express, vol. 14, no. 15, pp. 6851-6857, 2006.

[6] T. Tsuchizawa, K. Yamada, H. Fukuda, T. Watanabe, J. Takahashi, M. Takahashi, T. Shoji, E. Tamechika, S. Itabashi, and H. Morita, "Microphotonics devices based on silicon microfabrication technology," IEEE J. Sel. Topics. Quantum Electron., vol. 11, pp. no. 1, pp. 232-240, 2005.

[7] T. Barwicz, M. A. Popovic, M. R. Watts, P. T. Rakich, E. P. Ippen, and H. I. Smith, "Fabrication of add-drop filters based on frequency-matched microring resonators,"J. Lightw. Technol, vol. 24, no. 5, pp. 2207-2218, 2006.

[8] F. C. M. J. M. van Delft, J. P. Weterings, A. K. van Langen-Suurling, and H. Romijn, "Hydrogen silsesquioxane novolak bilayer resist for high aspect ratio nanoscale electron-beam lithography,"J. Vac. Sci. Technol. B, vol. 18, no. 6, pp. 3419-3423, 2000.

[9] W. Henschel, Y. M. Georgiev, and H. Kurz, "Study of a high contrast process for hydrogen silsesquioxane as a negative tone electron beam resist," J. Vac. Sci. Technol. B, vol. 21, no. 5,pp. 2018-2025, 2003.

[10] J. A. Liddle, F. Salmassi, P. P. Naulleau, and E. M. Gullikson, "Nanoscale topography control for the fabrication of advanced diffractive optics," J. Vac. Sci. Technol. B, vol. 21, no. 6, pp. 2980-2984, 2003.

[11] www.asml.com.

[12] W. Bogaerts, V. Wiaux, D. Taillaert, S. Beckx, B. Luyssaert, P. Bienstman, and R. Baets, "Fabrication of photonic crystals in silicon-on-insulator using 248-nm deep UV lithography," IEEE J. Sel. Topics. Quantum Electron, vol. 8, no. 4, pp. 928-934, 2002.

[13] W. Bogaerts, D. Taillaert, B. Luyssaert, P. Dumon, J. Van Campenhout, P. Bienstman, D. Van Thourhout, R. Baets, V. Wiaux, and S. Beckx, "Basic structures for photonic integrated circuits in silicon-on-insulator," Opt. Express, vol. 12, no. 8, pp. 1583-1591, 2004.

[14] M. Settle, M. Salib, A. Michaeli, and T. F. Krauss, "Low loss silicon on insulator photonic crystal waveguides made by 193nm optical lithography," Opt. Express, vol. 14, no. 6, pp. 2440-2445, 2006.

[15] SOITECs Unibond(R) process, Microelectron. J, vol. 27, no. 4/5, pp. R36, 1996.

[16] H. J. Levinson, Principles of Lithography: SPIE, Washington, DC, 2001.

[17] J.W. Bossung, "Projection printing characterization, Proc. SPIE, vol. 100, pp. 80-84, 1977.

[18] K. K. Lee, D. R. Lim, H. C. Luan, A. Agarwal, J. Foresi, and L. C. Kimerling, "Effect of size and roughness on light transmission in a SiSiO2 waveguide: Experiments and model," Appl. Phys. Lett. , vol. 77, no. 11, pp. 1617-1619, 2000.

[19] M. C. Kim, D. Shamiryan, Y. Jung, W. Boullart, C. J. Kang, and H. K. Cho, "Effects of various plasma pretreatments on 193 nm photoresist and linewidth roughness after etching," J. Vac. Sci. Technol. B, vol. 24, no. 6, pp. 2645-2652, 2006.

[20] X. Detter, R. Palla, I. Thomas Boutherin, E. Pargon, G. Cunge, O. Joubert, and L. Vallier, "Impact of chemistry on profile control of resist masked silicon gates etched in high density halogen-based plasmas," J. Vac. Sci. Technol. B, vol. 21, no. 5, pp. 2174-2183, 2003.

[21] T. Wahlbrink, T. Mollenhauer, Y. M. Georgiev, W. Henschel, J. K. Efavi, H. D. B. Gottlob, M. C. Lemme, H. Kurz, J. Niehusmann, and P. H. Bolivar, "Highly selective etch process for silicon-on-insulator nanodevices," Microelectron. Eng. , vol. 78-79, pp. 212-217, 2005.

[22] D. Taillaert, F. Van Laere, M. Ayre, W. Bogaerts, D. Van Thourhout, P. Bienstman, and R. Baets, "Grating couplers for coupling between optical fibers and nanophotonic waveguides," Jpn. J. Appl. Phys., Part 1, vol. 45, no. 8A, pp. 6071-6077, 2006.

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