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Fabrication of quantum point contacts by imprint lithography and transport studies

Ingo Martini,[a] Silke Kuhn, Martin Kamp, Lukas Worschech, and Alfred Forchel
Technische Physik, University of Wuerzburg, Am Hubland, D-97074 Wuerzburg, Germany

Dominik Eisert and Johannes Koeth
Nanoplus Nanosystems and Technologies GmbH, D-97074 Wuerzburg, Germany

Rint Sijbesma
Laboratory of Macromolecular and Organic Chemistry, Eindhoven University of Technology, 5600 MB Eindhoven, The Netherlands

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This article demonstrates the integration of imprint lithography into nanoelectronic device fabrication. We present a quantum point contact (QPC) with split gates patterned by imprint lithography. The semiconductor substrate is a modulation-doped GaAs/AlGaAs heterostructure with the two-dimensional electron gas located about 90 nm below the surface. A Si mold with a split-gate pattern is embossed into a poly(methylmethacrylate) film located on top of the semiconductor. The Schottky gates are fabricated by metal evaporation and liftoff. The gate tip separation ranges from 120 to 600 nm. Transport studies performed at $T=2$ K show conductance quantization with varying gate voltages. Measurements performed on a reference QPC with gates defined by electron beam lithography show similar results. This indicates that the imprint does not affect the electronic performance of the semiconductor. © *2000 American Vacuum Society.* [S0734-211X(00)05306-3]

I. INTRODUCTION

Pattern transfer on nanometer scale is of increasing interest in many areas of science and technology. Optical lithography techniques with resolution up to about 200 nm are currently employed for pattern transfer on industrial scale. Other technologies, such as extreme ultraviolet lithography, x-ray lithography, electron projection lithography, and ion projection lithography are pushing towards the domain of 35 nm.

Chou *et al.*[1] proposed nanoimprint as an alternative process to conventional lithography. The pattern transfer process is based on embossing a mold with nanometer structures into a polymer [e.g., polymethylmethacrylate (PMMA)] film. Various groups have investigated the imprint on a nanometer scale with different structures,[2,3] using different polymer materials and layers,[4,5] and testing the imprint over large wafer areas.[6]

However, only a few applications of imprint technology in nanoelectronic device fabrication have been presented, e.g., the fabrication of silicon on insulator wires, dots and ring channels,[7] and gratings of distributed feedback lasers.[8] For integration of imprint lithography with conventional processing, issues like alignment and imprint on nonflat surfaces have to be addressed. Imprint lithography has the potential to replace optical lithography in industrial applications since no sophisticated tools are required and it shows potentially high throughput due to parallel processing.

We demonstrate the mix-and-match fabrication of a split-gate quantum point contact (QPC) by combining imprint lithography for the gate level with optical lithography for Hall bar and ohmic contact definition. The QPC constitutes an ideal test device for the applicability of a nanoimprint in nanoelectronic device fabrication. Although a QPC is a basic well understood device, its fabrication involves challenges typical for device fabrication by imprint, e.g., alignment, uniform pressure, and mold release.

II. SEMICONDUCTOR LAYER STRUCTURE

A schematic diagram of the QPC is displayed in Fig. 1. The device is based on a modulation doped GaAs/AlGaAs heterostructure grown by molecular beam epitaxy. The two-dimensional electron gas (2DEG) with a mobility $\mu=870\,000$ cm^2/V s and a carrier concentration $n=3.8\times10^{11}$ cm^{-2} is located about 90 nm below the surface. A negative gate voltage depletes the 2DEG below the gates leading to 1D channels for carrier transport.

Prior to the general processing, the backside of the heterostructure is polished with Br_2/methanol. The advantage of this step will become obvious when the alignment of struc-

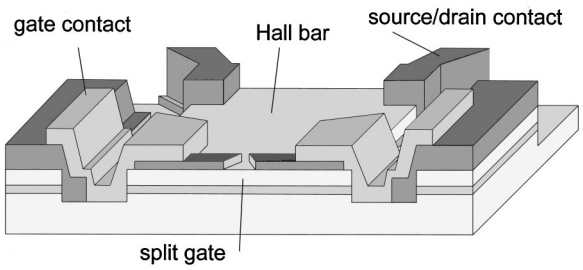

FIG. 1. Schematic of the quantum point contact showing Hall bar, ohmic contacts, split gates, and a metal bridge to connect the gate with a contact pad.

[a]Electronic mail: martini@physik.uni-wuerzburg.de

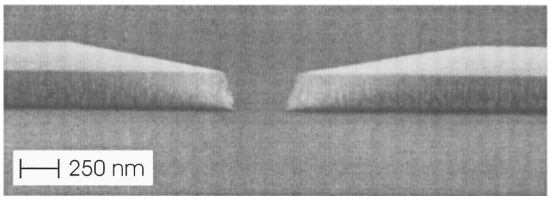

FIG. 2. SEM micrograph showing the gate pattern of the Si mold.

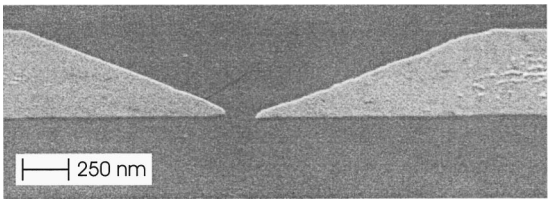

FIG. 4. Schottky gate defined by imprint lithography, Ti/Au evaporation, and liftoff. The gate tip separation is about 180 nm.

ture and mold will be discussed. The preparation of the basic transport structure consists of two major steps. First, the Hall bar is defined by wet etching with $0.5\,NH_4OH+0.5\,H_2O_2+50\,H_2O$ using photoresist patterned by optical lithography as an etch mask. The second step is the deposition of the AuGe/Ni/Au for ohmic contacts. The metal of the ohmic contact layer is also used to form alignment marks for the imprint step. Prior to the metal evaporation, the sample is dipped into a NH_3 solution to remove the native oxide from the semiconductor. After a lift-off procedure, the contacts are annealed at 480 °C for 60 s. For the subsequent imprint process, the transport structure is spin coated with PMMA 50 K (200 nm thickness).

III. MOLD FABRICATION

Imprint on nonplanar surfaces is crucial for device fabrication. From the schematic in Fig. 1 one can see the topography of the semiconductor structure. The contact pads on the Hall bar have a thickness of about 400 nm. To compensate for this, the split-gate pattern on the mold is placed on a pedestal. The mold is fabricated from a double side polished Si $p\langle 100\rangle$ wafer with a thickness of 525 μm. The pedestal is defined by optical lithography, deposition of a BaF_2/Cr mask, and reactive ion etching with CHF_3/Ar gas. Since the split gates will be defined on this pedestal a complete removal of the mask is essential for the subsequent process steps. Next, Cr alignment marks for the imprint step are fabricated by optical lithography, metal deposition, and liftoff. The split-gate patterns centered on the pedestal are defined by high resolution electron beam lithography at 100 kV into PMMA 950 K. After the evaporation of a 30 nm chromium layer and liftoff, the gate patterns are transferred into the Si by reactive ion etching with CHF_3/Ar gas.

Figure 2 shows a scanning electron micrography (SEM) image of a split-gate mold. The height is about 260 nm, the wire width about 1000 nm, and the taper separation ranges from 120 to 600 nm. In order to prevent polymer adhesion during the imprint process, the mold is immersed into an octadecyltrichlorosilane (OTS) $CH_3(CH_2)_{17}SiCl_3$–toluene solution. OTS forms a stable monolayer on the Si, leading to a passive surface because of its long alkylic chain. The passivation process occurred in a water free environment. The passivation layer lasts many imprint cycles and is resistant to mold cleaning with pyrrolidon.

IV. ALIGNMENT AND IMPRINT

The alignment of substrate and mold is achieved by using an optical mask aligner. The metal marks of the contact level on the QPC sample and the Cr marks on the mold are aligned under backside infrared illumination as illustrated in Fig. 3, with an accuracy of about ± 2 μm. Without backside polished wafers the alignment marks do not provide sufficient contrast. Then, mold and substrate are brought into soft contact, i.e., the mold is slightly pressed into the polymer. A crucial step is the manual transfer of the aligned samples into the press. The samples are placed on a polytetrafluoroethylene foil to account for the possible unevenness of the backside of the sample introduced by foregoing processing. After pressure build up to about 100 bar the press is heated up to 165 °C for 20 min. By heating up the PMMA above its glass transition temperature ($T_G=105\,°C$) the split-gate pattern is transferred into the polymer. The PMMA layer is chosen to be slightly thicker than the height of the gate mold so that damage on the mold and semiconductor substrate are avoided.

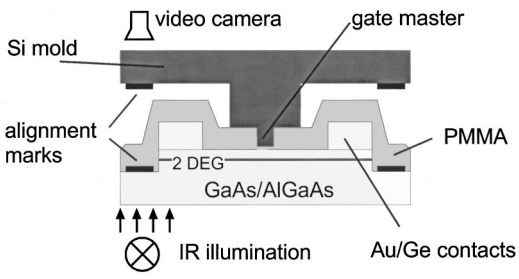

FIG. 3. Schematic to illustrate the topography during alignment and imprint procedure.

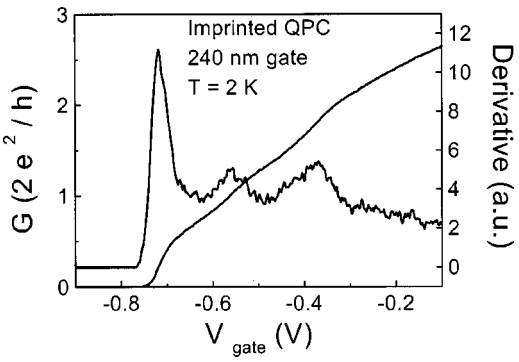

FIG. 5. Conductance as a function of the gate voltage. The split gate defined by imprint technology is a taper with a nominal tip separation of 240 nm.

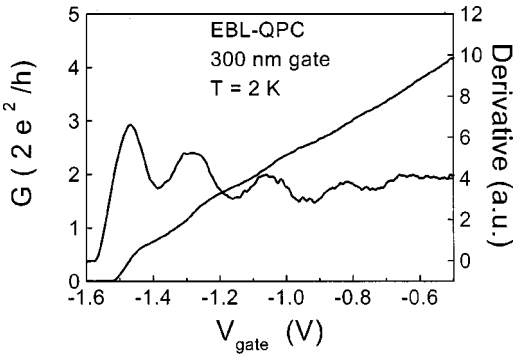

FIG. 6. Conductance as a function of the gate voltage for the reference QPC. The split gate defined by EBL is a taper with a nominal tip separation of 300 nm.

The pressure is released after the press has reached room temperature. If the mold was passivated prior to the imprint, the mold release occurs reclusively. The thin residual PMMA film in the gate structure is removed by reactive ion etching with Ar/O_2 gas. The Schottky gates are fabricated by evaporation of a Ti/Au layer and liftoff. An imprinted gate with a tip separation of 180 nm is shown in Fig. 4. In a last step, the split gates have to be connected with the contact pads. The bridges (also shown in Fig. 1) are fabricated by optical lithography, evaporation of 100 nm Al and liftoff. The process above describes the processing of an array of 4×4 QPCs located on a 1 cm^2 large wafer. To test the electronic properties, the QPCs are separated and bonded on chip carriers.

V. TRANSPORT MEASUREMENTS

Transport measurements on the QPCs with imprinted gates were performed at $T=2$ K. By applying a negative voltage to the Schottky gates, the electron gas is laterally confined to a small channel below the gate tips. In order to increase the signal to noise ratio, a lock-in technique is employed. The conductivity modulation with varying gate voltage of a QPC with a nominal tip separation of 240 nm is displayed in Fig. 5. For a gate voltage $V_g<-0.75$ V, the electron gas is completely depleted and no conductance occurs. Evaluating the derivative of the curve, the plateau in the conductance become visible indicating quantized charge transport through a one-dimensional channel in agreement with standard literature.[9,10] To determine the possible influence of the imprint process on the electronic properties of the semiconductor layer, quantum point contacts with split gates patterned by high resolution electron beam lithography (EBL) at 100 keV were processed. Figure 6 displays conductance measurements performed on an EBL reference QPC with a nominal tip separation of 300 nm. The result is comparable to that obtained from the imprinted device. This indicates that the imprint process is capable of replacing electron beam lithography for nanoelectronic device fabrication.

VI. CONCLUSION

In conclusion, we have demonstrated mix-and-match fabrication of a basic nanoelectronic device by integration of nanoimprint lithography with conventional processing. The processing of a quantum point contact included three optical lithography steps and the imprint of the split-gate pattern. The gate was fabricated by metal evaporation and liftoff. Transport measurements performed at $T=2$ K have shown quantized charge transport with varying gate voltage. The conductance properties of the imprinted device are similar to those from a reference QPC with gates patterned by EBL, showing no detrimental effect of the imprint on the device performance.

ACKNOWLEDGMENTS

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