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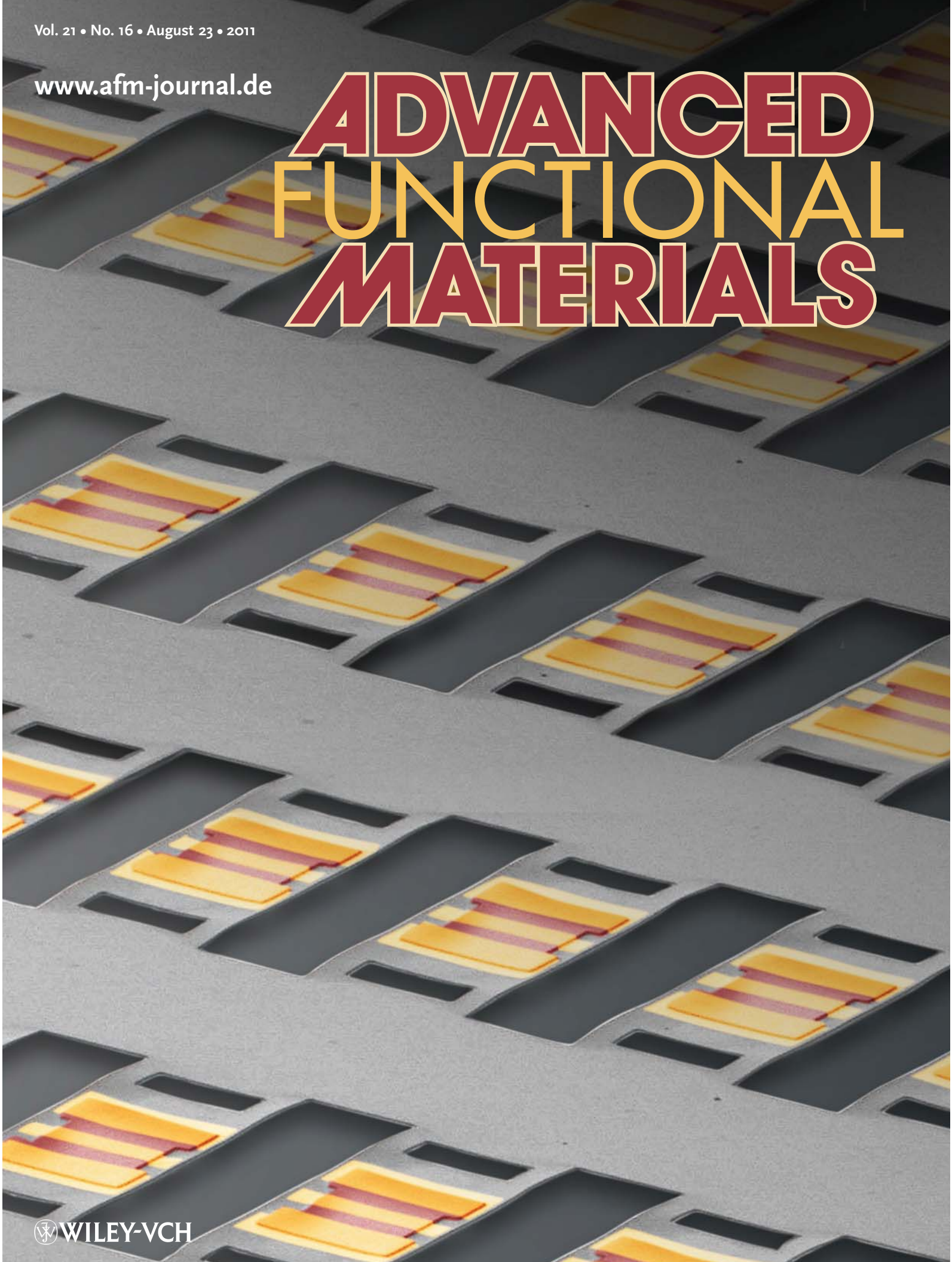

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Fabrication of Releasable Single-Crystal Silicon–Metal Oxide Field-Effect Devices and Their Deterministic Assembly on Foreign Substrates

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A new class of thin, releasable single-crystal silicon semiconductor device is presented that enables integration of high-performance electronics on nearly any type of substrate. Fully formed metal oxide–semiconductor field–effect transistors with thermally grown gate oxides and integrated circuits constructed with them demonstrate the ideas in devices mounted on substrates ranging from flexible sheets of plastic, to plates of glass and pieces of aluminum foil. Systematic study of the electrical properties indicates field-effect mobilities of ≈710 $cm^2 V^{-1} s^{-1}$, subthreshold slopes of less than 0.2 V $decade^{-1}$ and minimal hysteresis, all with little to no dependence on the properties of the substrate due to bottom silicon surfaces that are passivated with thermal oxide. The schemes reported here require only interconnect metallization to be performed on the final device substrate, which thereby minimizes the need for any specialized processing technology, with important consequences in large-area electronics for display systems, flexible/stretchable electronics, or other non-wafer-based devices.

1. Introduction

Single-crystal silicon holds a dominant position in microelectronics, due to its remarkably attractive set of properties for transistors and other semiconductor devices. This circumstance continues to motivate research into methods for using silicon in ways that avoid constraints in size, geometry, mechanics, and/or cost structures set by conventional, wafer-based implementations. The most prominent example is in thin-film electronics on glass, where amorphous silicon serves as the semiconductor for switching transistors in large-area backplanes for liquid-crystal displays, or as the precursor to large-grained polycrystalline silicon for similar, but more demanding, applications.[1] In these cases, deposition and related processing steps occur at temperatures that are compatible with glass, sometimes in ways that can also be extended for use with flexible sheets of plastic or other more unusual substrates.[2] A second, and conceptually different approach uses micro/nanostructures of monocrystalline silicon formed at high temperatures, and then subsequently assembled into organized arrays at low temperatures on substrates of interest.[3–7] Although many important systems can be achieved with these two schemes, neither has been used to produce high-performance devices that incorporate gate dielectrics formed by thermal oxidation, due to the constraints associated with the high temperatures required for this process (>1000 °C). This limitation represents a serious shortcoming because it precludes the use of the exceptionally high-quality interfaces between silicon and thermal oxide (tg-SiO_2). The electronic defect density at and near this interface is, in fact, lower than that for any other known gate dielectric for silicon, resulting in optimal transistor performance.[8–11] Another drawback of previous approaches is that most of the device and circuit processing occurs on the final substrate, thereby adding cost and complexity in tooling, especially for large-area applications.

Here we report ideas that enable silicon electronics with tg-SiO_2 dielectrics to be integrated onto arbitrary substrates, in a manner that also separates all aspects of individual device fabrication (e.g., contact doping, metallization, interconnection for small-scale circuit blocks, etc.) from their incorporation into systems. The approach extends schemes that use micro/

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nanostructures of silicon released from wafers as a starting point for device/circuit processing,[6,7] by replacing the silicon with thin, specialized silicon–metal oxide semiconductor field-effect transistors (MOSFETs) and microscale circuit elements, all with tg-SiO_2 dielectrics. Transfer printing allows these microcomponents to be distributed into arbitrary layouts over large or small areas, on nearly any substrate type or size. A final interconnection step yields functional systems. The field-effect mobilities, densities of interface traps, subthreshold behaviors, and other characteristics of MOSFETs achieved on thin plastic substrates in this manner significantly exceed those of previous demonstrations. This fabrication sequence has some conceptual similarities with ones that rely on fluidic assembly,[3,4] and robotic pick-and-place manipulation of miniature integrated circuit blocks and of assembly of chiplets derived from foundry-processed silicon-on-insulator (SOI) wafers.[12] A key difference is that the devices reported here have thicknesses several to more than ten times smaller than those required for circuit blocks or chiplets, which thereby renders them compatible with the techniques of transfer printing and with simple, planar processes for interconnect metallization. The schemes reported here also terminate all exposed silicon surfaces with tg-SiO_2, thereby imparting robust operation and performance that is nearly independent of device substrate.

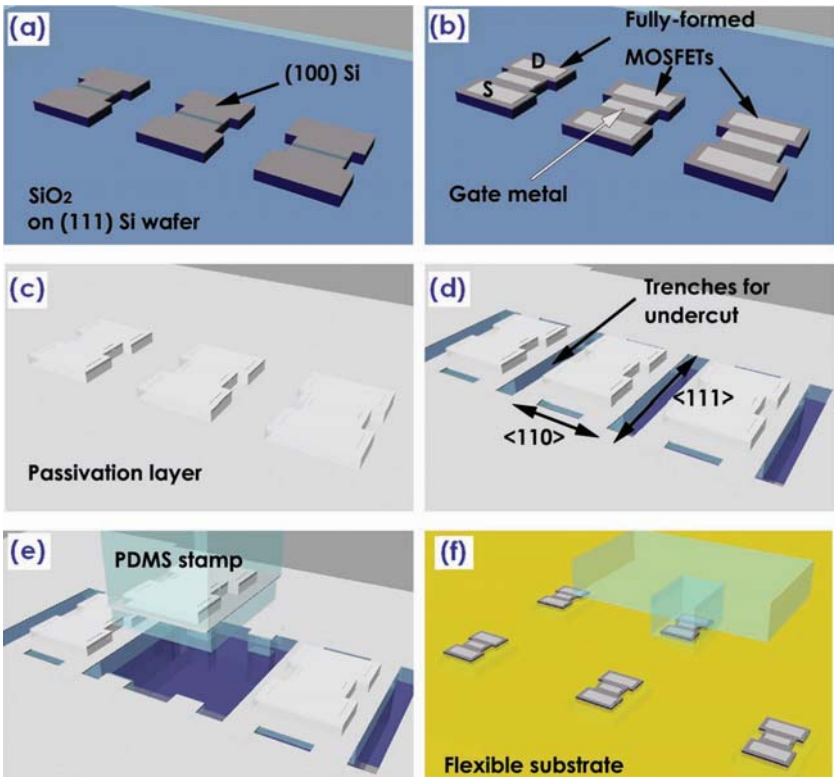

Figure 1. Schematic illustration of steps for fabricating thin, microscale MOSFETs, releasing them from the wafer substrate and then assembling them onto a flexible substrate by transfer printing, including a) forming and isolating n^+-p-n^+ junctions on the top device layer of an SOI wafer; b) growing a thermal oxide as a gate dielectric, followed by defining source, drain and gate metallization to complete the MOSFETs; c) depositing a uniform, protecting (i.e., passivation) layer on top of the devices; d) RIE etching to define anchors and supporting structures, followed by anisotropic, wet-chemical undercut etching (TMAH) to release the structures in a suspended state above the underlying substrate; e) selectively releasing a single device onto the surface of a PDMS stamp; f) transfer printing onto a flexible substrate, followed by the removal of the passivation layer.

2. Results and Discussion

2.1. Techniques for Fabrication and Assembly of Silicon Devices

The schematic illustrations in **Figure 1**a–f show steps for fabricating thin MOSFETs on an SOI wafer, followed by deterministic assembly onto a receiver substrate by transfer printing. The SOI consists of a handle wafer with (111) orientation, a buried layer of silicon dioxide (BOx; 1 μm thick), and a top layer of p-type Si with (100) orientation (≈2 μm thick). This type of wafer is unusual, and designed specially for the present purposes due to its favorable characteristics for 1) electronic transport in (100) silicon for MOSFETs and 2) anisotropic etching of (111) silicon for release. The first step in the fabrication involves heavy n-type doping (n^+) with a solid source of phosphorus (1000 °C, 10 min) in lithographically patterned geometries to define n^+–p–n^+ junctions for arrays of transistors or collections of them designed for logic gates. Reactive-ion etching (RIE) then removes unwanted regions of the top silicon layer to isolate the devices. Dry oxidation at 1100 °C for 1 hour induces conformal growth of a layer of SiO_2 (≈90 nm thick) on the exposed surfaces of the silicon (Figure 1a). Etching openings through this layer in the n^+ regions with HF provides electrical access for source and drain (S and D) electrodes patterned on top. The metals for S, D, and gate (Cr; 250 nm thick) are then deposited and patterned in a single step to form a coplanar transistor structure (Figure 1b). Next, plasma-enhanced chemical-vapor deposition (PECVD) forms a conformal layer of Si_3N_4 (800 nm) uniformly across the area of the wafer (Figure 1c). A photopatterned metal layer (Cr; 200 nm thick) serves as a hard mask for dry etching to form openings through the Si_3N_4 and BOx layers and to expose the underlying (111) handle wafer to a depth of ≈2 μm (Figure 1d). This process defines the lateral geometries of the devices/logic gates as well as structures (i.e., anchors) at their edges to maintain contact with the handle wafer even after complete undercut etching. After removing the sacrificial metal layer, immersion of the wafer in a boiling aqueous solution of tetramethyl ammonium hydroxide (TMAH; 25% diluted in water) etches the handle anisotropically, such that the etch front proceeds along the Si <110> directions. A complete undercut prepares the devices for release, and assembly by transfer printing. The long axes of the anchors lie along the <111> direction of the handling wafer, to leave the devices freely suspended, with edges tethered to the handle only at selected

locations. The etch time depends on the widths of the devices; ≈90 minutes is sufficient for 180-μm widths.

An important feature of the device design is that the bottom surfaces of the silicon are passivated with the BOx. As a result, the electronic properties are insensitive to the characteristics of the final substrate. The assembly involves transfer-printing procedures described elsewhere,[7] in which contact of the devices with a patterned stamp (polydimethylsiloxane; PDMS) and then rapid retraction of the stamp leads to fracture at the anchors (Figure 1e; shown in Supporting Information S1) and removal of the devices from the SOI wafer. Bringing the stamp, with devices supported on its surface, into contact with a target substrate that has an adhesive material coated on its surface, followed by removal of the stamp and etching the Si_3N_4 completes the assembly process (Figure 1f). As a final step, metal interconnects and/or probing pads to these devices can be formed using conventional, planar processing or printing techniques. Details are in the Supporting Information (Figure S2 and movie M1, M2).

Optical microscopy images appear in **Figure 2**a–d. Figure 2a shows two isolated n^+-p-n^+ junctions after oxidation, which corresponds to the cartoon in Figure 1a. Figure 2b reveals the structure after etching the vertical trenches (Figure 1d). The black regions reveal the etched (111) handle wafer. The S/D and gate metals cover part of the n^+-Si regions and the entire p-Si areas, respectively. The four small squares in the S/D metal are the contact holes etched through the gate oxide layer. Figure 2c shows two suspended devices spanning over the handle wafer, after etching with TMAH (cf. Figure 1e). The variation in color across the <110> axis arises from slight bowing of the devices. Finally, Figure 2d shows two devices after transfer printing onto a polyimide (PI) substrate (Figure 1f).

The anisotropic TMAH etching process is a critically important aspect of the fabrication. Cross-sectional scanning electron microscopy (SEM) images in Figure 2e reveal additional features. Here, the etch fronts propagate through the <110> direction of the (111) handle wafer (trench depth appears larger than the one defined by RIE (≈2 μm) due to i) misorientation in the handle wafer and ii) weak anisotropy of TMAH; the ratios of etching rates for the (111) and (100) planes are ≈0.02 – 0.08[13]). The BOx layer serves as a barrier to the etchant, thereby protecting the undersides of the devices; the Si_3N_4 protects the top surface. The anisotropy of the etch leaves the anchor structures connected to the handle wafer along straight, unetched regions of silicon. The tilted view in Figure 2f shows suspended, fully undercut devices ready for release onto a stamp.

Devices formed in this way incorporate a high quality, thermal oxide as the gate dielectric. Alternative schemes can retain this advantage, and at the same time provide other processing options. For example, anisotropic etching and transfer printing steps can occur immediately after thermal oxidation. In this case, the S, D, and gate metallization can be defined on the target, device substrate, after printing. This method corresponds to performing the processes in Figure 1b after finishing steps through Figure 1f. This sequence has the advantage that the choice of metal is not limited by its compatibility with other steps, thereby offering potential value in specialized applications, such as those in biomedical devices or high-speed circuits, where the selection of metal can be critically important. A disadvantage, of course, is that the processing must be compatible, in terms of both materials and cost considerations, with the final device substrate.

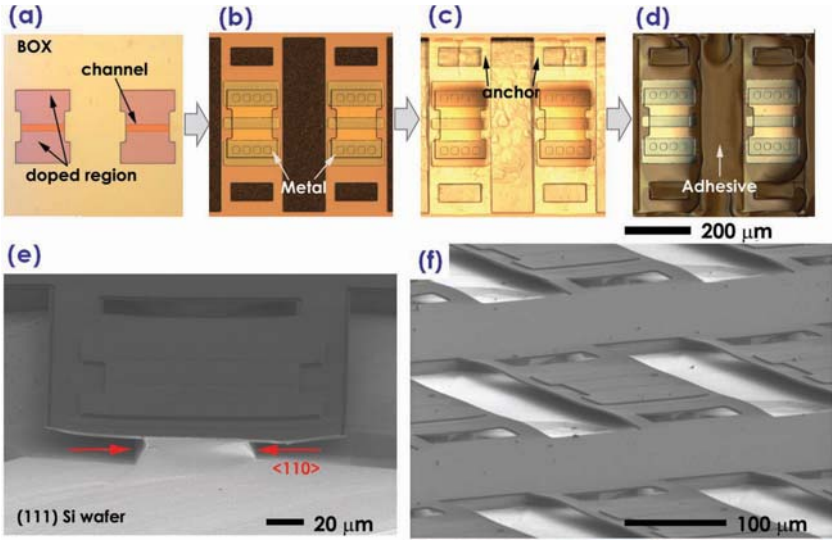

Figure 2. a–d) Optical microscopy images at various stages of the device fabrication, including (from left) a) after oxidation and doping, b) after defining the anchors and supporting device platforms, c) after TMAH undercut etching, and d) after transfer printing. e) Cross-sectional SEM image of a representative device after partial anisotropic undercut etching with TMAH. g) Angled SEM image of an array of suspended structures after complete undercut etching, showing anchors at the four corners of each element.

2.2. Transferred MOSFET Properties

Figure 3 provides electrical characterization data for a representative n-type MOSFET printed onto a PI substrate (KAPTON; 25 μm thick). The nominal channel length (L) and width (W) are 20 and 150 μm, respectively, as defined by the photolithography. The transfer characteristics, consisting of output drain current (I_D) as a function of input gate bias (V_G) for drain voltage (V_D) values of 0.1, 2.1, and 4.1 V, appear in both logarithmic (solid) and linear (short dash) scales in Figure 3a. The transconductance, $g_m = (\partial I_D/\partial V_G)|_{V_D}$, is also plotted for V_D = 0.1 V. The field-effect mobility μ_{FE} can be obtained from the g_m according to Equation (1)[14]

$$\mu_{FE} = \left.\frac{L_{eff} g_m}{W C_{ox} V_D}\right|_{V_D \to 0} \quad (1)$$

where C_{ox} is the capacitance of the gate oxide and L_{eff} is the effective channel length. By using the measured thickness of 90 nm and known dielectric coefficient of SiO_2, 3.9, the value of C_{ox} is 38.4 nF cm^{-2}. The μ_{FE} values are a function of V_G because the electron mobility in the inversion layer depends on the vertical electrical field. For the present purposes, we use the mobility obtained from the maximum g_m, 27.2 μS, as

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a representative parameter. With the nominal values of L and W in Equation (1), μ_{FE} is determined to be ≈950 cm^2 V^{-1} s^{-1}. This value corresponds to 85% of the bulk electron mobility and is unphysical.[15] The error arises from reductions in L by thermal diffusion of dopants during the processing, to yield a value of L_{eff} that is ca. 4.45 μm shorter than the photodefined value (L), according to detailed analysis presented in Section 2.3. The corrected value of μ_{FE} is ≈740 cm^2 V^{-1} s^{-1}. The saturation mobility, $\mu_{sat} = (2L_{eff}/WC_{ox})\left[(\partial I_D^{1/2}/\partial V_G)\big|_{V_D}\right]^2$ is ≈580 cm^2 V^{-1} s^{-1} at V_D = 4.1 V.[14] The on/off ratio is >5 × 10^6 and the gate leakage current is less than 7 pA throughout the measured range. The threshold voltage (V_{th}) and subthreshold swing (S) at V_D = 0.1 V are +0.60 V and 0.14 V decade^{-1}, respectively. The output characteristics appear in Figure 3b. Here, the curves exhibit sharp saturation behavior at high V_D and the saturated I_D values show good agreement with a parabolic fit to $(V_G - V_{th})$, consistent with nearly ideal MOSFET behavior under square-law theory.[16] In addition, the device is free from hysteresis behavior when the gate voltage sweeps from –10 V to +10 V, then back to –10 V at V_D = 0.3 V in Figure 3c. These parameters are representative of those observed in other devices; additional data appears in the context of scaling behavior described subsequently and in statistical information in the Supporting Information (S3). Here, the average and standard deviation values for μ_{FE}, V_{th}, and S are 710 ± 40 cm^2 V^{-1} s^{-1}, 0.47 ± 0.24 V, and 0.18 ± 0.04 V decade^{-1}, respectively.

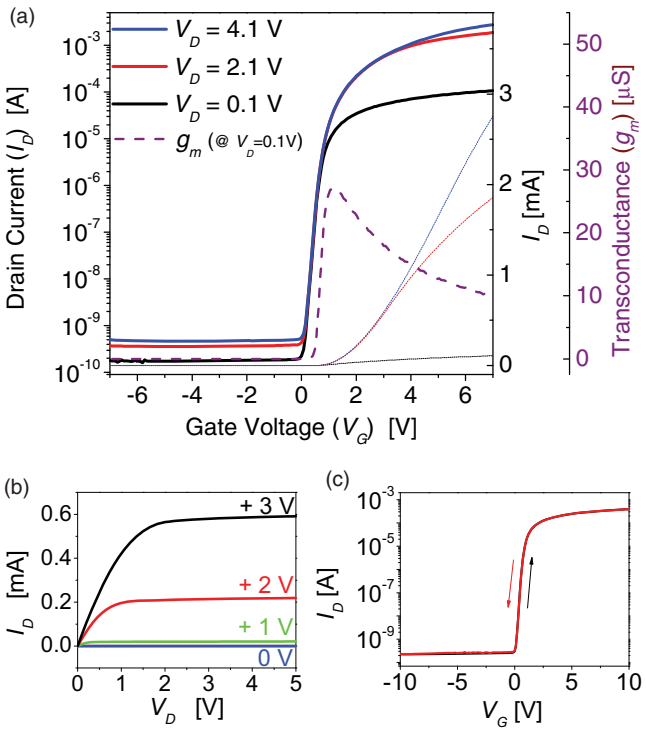


Figure 3. a) Typical transfer characteristics of a thin, microscale MOSFET printed onto a PI substrate, with W/L = 150/20 μm. Solid and short dashed lines correspond to the drain current plotted in logarithmic and linear scales, respectively. The curve indicated by the long dashed line shows g_m values, evaluated in the linear regime. b) Output characteristics (at gate voltages labeled in colored text in the plot) and c) hysteresis properties (V_D = 0.3 V; up and back sweeps shown in black and red) of the same device presented in (a).

The quality of the interface between Si and SiO_2 governs the key performance aspects of the MOSFET. The properties of this interface can be estimated by analysis of device parameters such as μ_{FE} and S. When the MOSFET operates in inversion mode, the electron channel lies within a slab of thickness less than 10 nm.[15] Thus, the maximum mobility μ_{FE} is typically lower than the bulk mobility because of electron scattering by charge centers near the Si/SiO_2 interface, namely the positive fixed-oxide charge (Q_f) and the interface-state charge (N_{it}).[15] Because the relaxation time is inversely proportional to the density of the charges, an empirical relation for μ_{FE} can be defined as

$$\mu_{FE} = \frac{\mu_0}{1 + \alpha\,(Q_f + N_{it})} \tag{2}$$

where μ_0 and α are experimentally determined fitting parameters that depend on the average impurity concentration in the bulk Si (N_A).[15] Because boron-doped (100) Si with a resistivity of 10–20 Ω·cm is used in this study, N_A for the devices reported here is ca. 10^{15}.[16] The relationship between the μ_{FE} and the density of electrostatic scattering centers $(Q_f + N_{it})$ is quantitatively well established. Therefore, by using the fitting parameters (μ_0 and α),[15] the $(Q_f + N_{it})$ value can be determined to be ≈2.2 × 10^{11} cm^{-2}. The equivalent maximum density of states (N_{ss}^{max}) at the Si/SiO_2 interface can be extracted from S, using the following equation,

$$N_{ss}^{max} = \left(\frac{S\log(e)}{kT/q} - 1\right)\frac{C_{ox}}{q} \tag{3}$$

where q is the electron charge, k is the Boltzman constant, and T is the absolute temperature.[17] From Equation (3), N_{ss}^{max} is ≈3.2 × 10^{11} cm^{-2}, which is consistent with the result from Equation (2). Whereas the state-of-art MOSFETs may reach μ_{FE} and $(Q_f + N_{it})$ values >800 cm^2 V^{-1} s^{-1}, and <10^{11} cm^{-2} respectively,[9,15] the parameters of the devices reported here exceed those produced in other ways on plastic or other nonwafer substrates.

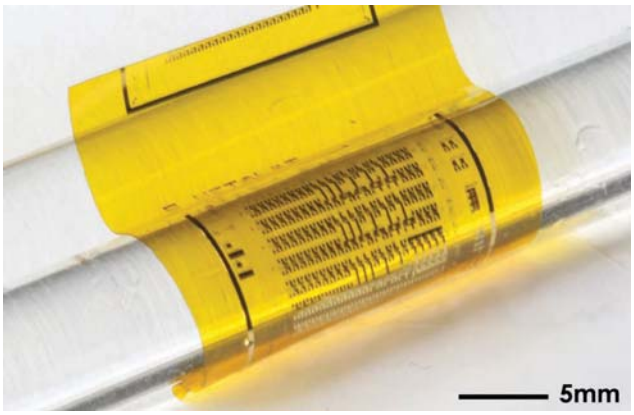
2.3. Effective Channel Length and Mobility

The fabrication processes of Section 2.1 involve two high-temperature steps: solid-state doping (1000 °C, 10 min) and thermal oxidation (1100 °C, 1 hour). By defining the phosphorus diffusion length as the point where the phosphorus concentration is outnumbered by that of the background boron, this thermal history leads to a ≈2 μm diffusion of the phosphorus dopants into the boron-doped channel area,[18] resulting in a ≈4 μm reduction of the channel length. The consequences of this diffusion, and the quality of the contacts, can be examined in additional detailed by using the gated transmission-line method (g-TLM).[19] In g-TLM, the total resistance of the MOSFET at an on-state (R_{on}) is the sum of the intrinsic channel resistance (R_{ch}) and a parasitic resistance (R_p) according to,

$$R_{on} = \left.\frac{\partial V_D}{\partial I_D}\right|_{V_{DS}\to 0}^{V_G} = R_{ch} + R_p = \frac{L}{W\mu_i C_{ox}(V_G - V_{th,i})} + R_p \quad (4)$$

where μ_i and $V_{th,i}$ are the intrinsic mobility and threshold voltage, respectively. This expression is only valid in the linear response regime, where V_{DS} is near 0, because R_{ch} is not proportional to L in the saturation regime, due to pinch-off of the channel. In an ideal case, a plot of R_{on} versus L for various values of V_G exhibits a single crossing point at (0, R_p), where R_p is a resistance, typically the contact resistance, that does not depend on L. If the effective channel length (L_{eff}) is different from the photodefined (L) value, then the crossing point will be shifted. In this case, the x-axis value at the crossing point, $L_0 = L - L_{eff}$, defines the shrinkage of the channel length induced by diffusion.[19]

Figure 4 provides an optical image, electrical measurements, and g-TLM analysis data for a series of MOSFET devices with L = 10, 15, 20, 30, and 40 µm. For all of these devices W is 150 µm. Figure 4a shows the array of MOSFETs with patterned metal pads on a polyimide substrate. Figure 4b presents the transfer curves of the five MOSFETs used in this analysis at V_D = 0.1 V. The threshold voltages are all uniform, with V_{th} = +0.42 ± 0.05 V (Figure 4d), which makes the devices suitable for g-TLM analysis. Figure 4c shows $R_{on}W$ plotted against L for various V_G values. Here, the linear fits (lines) to the raw data (solid marks) cross at a single point at L_0 = 4.45 µm. The value is consistent with the estimation based on diffusion considerations discussed previously, 4 µm. The y coordinate of the crossing point, $(R_{on}W)_0$ is often referred as a minimum effective contact resistance. The value of 0.4 Ω·cm is typical for single-crystal silicon-based n-type MOSFET devices.[19] In addition, from the variation of sheet conductance plotted against V_G in the Figure 4d, the values of μ_i and $V_{th,i}$ are derived to be ≈500 cm^2 V^{-1} s^{-1} and –0.56 V, respectively. The value of μ_i is lower than μ_{FE} because these quantities are determined $4 \le V_G \le 7$ V and $V_G \approx 1$ V, respectively. The electron mobility within the inversion layer decreases with increasing vertical electric field because of the effects of Coulomb scattering. Lastly, the field-effect mobility (μ_{FE}) must be invariant over a wide range of gate lengths if a correct value of L_0 is derived. The μ_{FE} values plotted in Figure 4e validate this hypothesis.



(a)

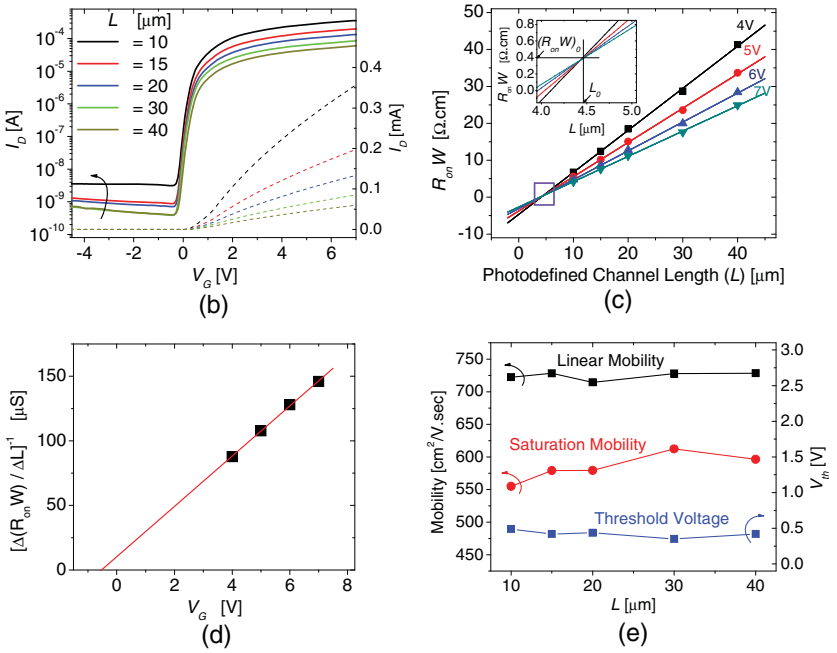


Figure 4. a) Image of an array of MOSFETs containing various W/L values and a set of logic gates printed onto a PI substrate. b) Transfer curves (V_D = 0.1 V) of devices with various L, all with W = 150 µm. Solid and dashed lines correspond to logarithmic and linear scales, respectively. c) Width-normalized ON resistance ($R_{on}W$) as a function of channel length at different gate voltages. The solid lines represent linear least-square fits to the data (symbols). The inset shows the region corresponding to the blue box in the main frame, with parameters for the channel-length reduction (L_0) and the minimum effective contact resistance $(R_{on}W)_0$ of 4.45 µm and 0.4 Ω·cm indicated. d) Variation of the sheet conductance, determined from the reciprocal of the slopes in the linear fitting in the main panel, as a function of V_G. e) Threshold voltage and corrected mobility values plotted against channel length.

2.4. Logic Gates

Extensions of the concepts described previously can be used to form and assemble not only isolated MOSFETs but also small-scale integrated circuits. **Figure 5**a shows optical images of the three examples, in the form of inverters, NOR, and NAND logic gates, along with equivalent circuit diagrams. Figures 5b and 5c show operational characteristics of such devices. Here,

W/L geometry of the load and the drive devices are 30/40 and 120/20 µm, respectively, and supply voltages (V_{dd}) are 1 V for all cases. The inverter in Figure 5b exhibits well-defined transfer characteristics with gains of ≈2.1. The output voltages (V_{out}) at inputs (V_{in}) of 0 and 1 V are 0.885 and 0.035 V, respectively. The NOR and NAND gates in Figure 5c show well-defined "0" and "1" output voltages of 0.01–0.04 V and 0.93–0.96 V, respectively, for input signals of –1 V and +1 V, respectively. All the circuits operate at small V_{dd} of 1 V and V_{in} of –1 to +1 V, due to the small subthreshold voltages (0.2 V decade^{-1}) of the constituent MOSFETs and the sufficient on/off ratios (1.2×10^4 at $V_G = \pm 1$ V) of the drive devices (see inset in Figure 5b). These characteristics can further improved by optimizing the values of W/L. Also, more complex circuits can be envisioned.

2.5. Assembly Onto Unusual Substrates

Figure 6a shows released devices on an SOI wafer, ready for assembly by transfer printing. The printing equipment consists of a charge-coupled device (CCD) camera, precision motion stages, and a PDMS stamp in a mounting fixture, all designed for automated operation as described in detail elsewhere (Figure 6b and Supporting Information S2). These techniques and tools allow densely arrayed devices on the SOI wafer to be distributed over large areas on nearly any type of target substrate. Movies in the Supporting Information show the printing process. As examples, we formed large-area arrays on sheets of polyethylene terephthalate (PET; Figure 6c), on aluminum foil (Figure 6d), on a piece of fabric (Figure 6e), and on a sheet of paper (Figure 6f). Furthermore, these procedures allow printing on highly nonplanar surfaces, for example, on the lens of a pair of eyeglasses (Figure 6g) and on the sharp edges of glass slides (Figure 6h).

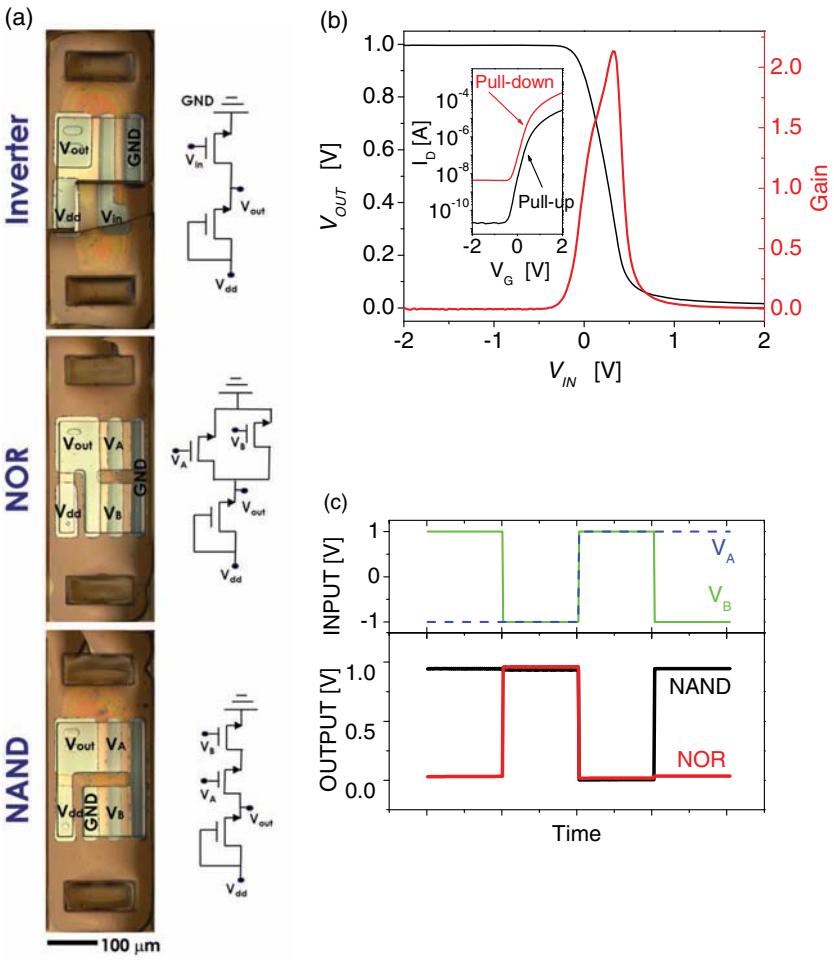


Figure 5. a) Optical microscopy images of inverter, NOR, and NAND logic gates printed on a PI substrate, with respective equivalent circuit diagrams. b) Current–voltage characteristics of an inverter with $V_{dd} = 1$ V. The inset shows transfer curves ($V_D = 1$ V) from adjacent MOSFETs that have identical W/L geometries as the load (30/40 µm) and the drive (120/20 µm) devices in the inverter. c) Input–output characteristics of the NAND and NOR gates.

3. Conclusion and Outlook

The ideas presented here enable integration of high-quality, distributed silicon electronics with thermal oxide dielectrics on various classes of substrates that are incompatible with critical steps (e.g., thermal oxidation and many others) in conventional semiconductor manufacturing. A key feature is that, except for interconnection, the device-fabrication steps are completely separated from the target substrate. Also, the bottom surfaces of the devices are passivated with thermal oxide, thereby minimizing any influence of the substrate on their performance. When implemented using foundry wafer fabrication facilities for the devices and advanced inkjet,[20] electrohydrodynamic,[21,22] direct-write,[23] or alternative printing techniques[24] for the interconnect, these procedures have the potential to bypass the need for any additional specialized processing technology for large-area electronics, or other nonwafer applications such as those that demand flexible, stretchable, or curvilinear substrates.

4. Experimental Section

MOSFET Fabrication: The SOI wafer was custom designed (Silicon Quest Inc.) with a (100) device layer (2 ± 0.5 µm; boron doped; 10–20 Ω·cm) and BOx layer (1 ± 0.05 µm) supported on a (111) handle wafer. These substrates were cleaved and cleaned with SC-1 ($NH_4OH:H_2O_2:H_2O$ = 1:1:5) and SC-2 ($HCl:H_2O_2:H_2O$ = 1:1:6). Dry oxidation formed a 300-nm oxide layer as a mask for the doping process. To pattern this oxide, a layer of photoresist (PR; AZ5214) was spin-coated at 4000 rpm for 40 s and soft-baked at 110 °C for 2 min. An ultraviolet (UV) exposure followed by developing (MIF327) defined the photoresist in an appropriate pattern. A combination of CH_4/O_2 RIE and 6:1 BOE wet-etching removed the oxide to expose areas for n^+ doping. After cleaning the wafer again with SC-1 and SC-2, doping was performed in a tube

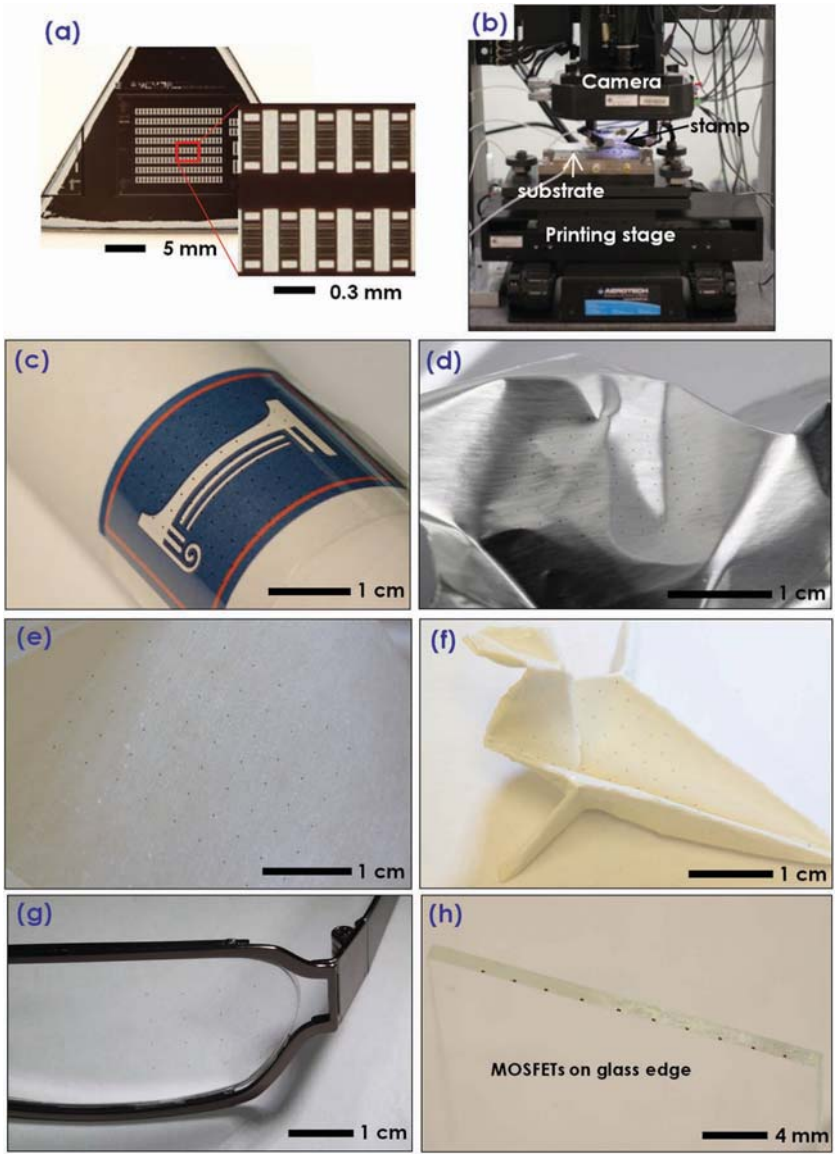


Figure 6. a) Image of arrays of fully formed MOSFETs on an SOI wafer. The inset image provides a magnified view. b) Printing equipment, consisting of a moving stage and CCD camera for automated transfer of selected MOSFETs from the source wafer to a target substrate. c) 77 MOSFETs and 33 NAND, NOR logic-gate devices assembled in a sparse array by printing onto a PET substrate of 50-μm thickness, shown here bent to a 1.5-cm radius of curvature. d) 80 MOSFETs printed onto aluminum foil of 100-μm thickness, e) 56 MOSFETs printed onto a piece of fabric, and f) 80 MOSFETs printed onto glossy paper. The spacing between the devices is 2 mm in (c) and (d), 4 mm in (e), and 3 mm in (f). Examples of MOSFETs printed (g) on the lens of a pair of eyeglasses and (h) on the rough edge of a glass slide.

furnace with phosphorus source (Saint-Gobain Ceramics) at 1000 °C for 10 minutes. The oxide was removed in concentrated HF, and then RIE was performed with SF_6 through a photopatterned mask (AZ5214) to isolate the devices. After cleaning the wafer with SC-1, dry oxidation was performed in a clean oxidation tube furnace at 1100 °C for 60 minutes to form the gate dielectric. Contact holes were patterned with AZ nLoF 2070 photoresist, spin-cast at 4000 rpm for 40 s, soft-baked at 110 °C for 90 s, exposed with UV, hard-baked at 110 °C for 2 minutes, and then developed in MIF327 for 60 s. A combination of CH_4/O_2 RIE and 6:1 BOE wet-etching defined areas for S/D metals. These electrodes and the gates were patterned with AZ nLoF 2070, followed by sputter-deposition of chromium (250 nm) and lift-off in acetone.

Passivation and Device Delineation: A film of Si_3N_4 (800 nm) deposited by plasma-enhanced chemical vapor deposition (PECVD) onto the entire wafer served as a passivation, or protecting, layer for the devices against further processing. The anchor regions were patterned by first defining patterns in AZ 4620 PR, spin-cast at 3000 rpm for 30 s, soft-baked at 110 °C for 3 min 30 s, exposed to UV, and then developed in diluted AZ400K (1:3). Next, a hard mask consisting of a layer of metal (Cr; 200-nm thick) was formed by sputter-deposition and lift-off. Etching by RIE with CF_4/O_2 defined openings in the Si_3N_4 and BOx layers, down into the underlying handle wafer to a depth of ≈2 μm. After removing the hard mask with Cr etchant (CR-7; Cyantek), the wafer was immersed in a boiling aqueous solution of tetramethyl ammonium hydroxide (TMAH; 25%) for anisotropic etching. A complete undercut through the <110> axis required ca. 90 minutes for 180-μm wide devices.

Transfer Printing: A PDMS stamp (Sylgard 184, Dow Corning, 10:1 mixture of base to curing agent) was formed by casting and curing against a pattern of a negative photoresist (SU-8 100, MicroChem Corp., 100-μm thickness) on a silicon wafer. For experiments reported here, this resist provided a single 100-μm tall post with a contact area of 200 μm^2. With this stamp and the automated printer system presented in Figure 6b, MOSFETs and logic-gate circuits were printed onto thin films of UV-curable adhesive coated on various substrates including PET, aluminum foil, PI, and pieces of fabric and paper coated with thin layers of PDMS (see movie clips in Supporting Information M1, 2). When performing transfer printing, each device was placed onto a designated coordinate of target substrate without any noticeable tilt or dislocation. During automated printing, ca. 100% transfer yield was observed for the MOSFET devices in Figure 2a–f, whereas logic-gate devices (Figure 5a) exhibited, on rare occasions (≈5%) unwanted fractures near the regions where silicon narrows. Regions where metal interconnects rest on isolated, undercut layers of BOx were particularly vulnerable. The results indicate the importance of structural design. The adhesive consisted of a composition of bisphenol A glycerolate (1 glycerol/phenol) diacrylate (Sigma-Aldrich), 3-(trimethoxysilyl)propyl methacrylate (Sigma-Aldrich), SOG (spin-on-glass, SpinTronics Inc.), and photointiator mixed, by weight, to a ratio of 55:35:10. Spin-coating this material at 3000 rpm for 30 s, and then annealing the substrate for 30 s at 110 °C yielded the proper level of tackiness for high-yield printing. After printing MOSFETs on PET or Al foil, exposing to UV light and then annealing at temperatures between 110–210 °C, the adhesive layer was fully cured. For printing on rough surfaces, such as fabric and paper, thin coatings of PDMS (≈100 nm), activated by exposure to UV, served as adhesive layers.

Metal Interconnects and Probing Pads: On top of the printed devices, an adhesion promoter [1:100 diluted VM651 (HD Microsystems) in methanol] was spin-cast at 3000 rpm for 30 s and then soft-baked at 110 °C for 1 min. Next, diluted PI-2525 [HD Microsystems; 4:1 (weight) mixed with *N*-methyl-2-pyrrolidone (NMP)] was spin-cast at 3000 rpm for 60 s, as a planarization layer (1.5- μm thick). This PI layer was baked at 250 °C in a globe box with argon atmosphere for 2 hours. Holes were

defined by oxygen RIE through a mask of AZ4620 PR. The S/D and gate metals Cr/Au (30/200 nm) layers were then sputter-deposited. Metal pads were photopatterned with AZ4620 PR, and then wet-etched using Au (TFA; Transene Inc.) and Cr etchants (CR-7; Cyantek).

Scanning Electron Microscopy (SEM) and Optical Microscopy (OM) Imaging: SEM images were obtained with a high-resolution instrument (Hitachi S4800). OM images were obtained with an Ultraplan Model FS100 (Mitutoyo Corp., Japan).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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