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COMMUNICATIONS

Published on Web 04/09/2003

Fabrication of Silica Nanotube Arrays from Vertical Silicon Nanowire Templates

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Hollow inorganic nanotubes are attracting a great deal of attention due to their fundamental significance and potential applications in bioanalysis and catalysis.[1] Among them, silica nanotubes are of special interest because of their hydrophilic nature, easy colloidal suspension formation, and surface functionalization accessibility for both inner and outer walls. These modified silica nanotubes and nanotube membrane have shown potential applications for bioseparation and biocatalysis.[2] Recently, bright visible photoluminescence from sol−gel template synthesized silica nanotubes was observed by Zhang et al.[3] In addition, the study of the physical and chemical nature of molecules or ions confined within the inorganic nanotubes is of great current interest.

Silica nanotubes have been synthesized typically within the pores of porous alumina membrane templates using the sol−gel coating technique.[4] Alumina templates can be dissolved to liberate single silica nanotubes. These nanotubes prepared at low temperature[5−7] have porous walls and are relatively fragile. Once the templates are removed, the silica nanotubes will generally bundle up and become less oriented. The same applied to the silica nanotubes prepared at low temperature using other templates.[5−7] The fabrication of oriented, robust silica nanotube arrays is of interest for their potential use in nanoscale fluidic bioseparation, sensing, and catalysis. Here, we developed a well-controlled process to translate vertical silicon nanowire arrays into silica nanotube arrays through a thermal oxidation-etching approach. The obtained nanotubes perfectly retain the orientation of original silicon nanowire arrays. High-temperature oxidation (800−1000 °C) produces relative thick and rigid walls that are made of condensed silica. This method could be useful for fabrication of single nanotube sensors and nanofluidic systems.

Silicon nanowire arrays were prepared using chemical vapor deposition (CVD) epitaxial growth employing silicon tetrachloride ($SiCl_4$, Aldrich, 99.99%) as the silicon source. Hydrogen (10% balanced by argon) is used to reduce $SiCl_4$ at high temperature (900−950 °C). Gold thin film was coated on Si (111) substrates to initiate the growth of silicon nanowires via the vapor−liquid−solid growth mechanism. This approach was developed recently and has been used for the synthesis of vertical Si/SiGe superlattice nanowire arrays in our lab.[8,9] The silicon nanowire array samples are loaded into a tube furnace and heated at 800−1000 °C for 1 h under the continuous flow of pure O_2. These nanowires are uniformly oxidized to give SiO_2 sheaths with continuous silicon wire cores inside. We then leave the SiO_2 sheath intact and try to remove the thin silicon cores to create SiO_2 nanotubes. The processing details are presented in Figure 1. During the oxidation, the nanowire tips are also oxidized to give an oxide cap on each vertical wire, which could prevent the selective etching of silicon cores. Therefore, the first step after thermal oxidation is to selectively remove the SiO_2 caps from the Si/SiO_2 core-sheath nanowires. Our strategy is to deposit polymer

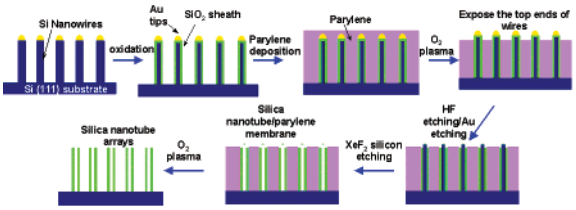

Figure 1. Flowchart of the fabrication process for making silica nanotube arrays from vertical silicon nanowire templates.

to fill in the space between nanowires such that the side wall of SiO_2 is protected by the matrix polymer. Here, parylene dimer (di-para-xylylene) was thermally evaporated at 160 °C, dissociated at 650 °C, and then deposited onto the Si/SiO_2 core-sheath nanowire array sample for 5 h to give a continuous coating of parylene (poly-para-xylylene) polymer. This parylene deposition is conformal, starting from thin layer coating on the surface of nanowires and then filling all of the interval space between nanowires. This process leads to a highly conformal wrapping of the nanowires without pinholes or cracks. Oxygen plasma was then employed to etch the parylene surface to expose the tips of the Si/SiO_2 nanowires, after which the sample was immersed in a buffered hydrofluoric acid solution for 2 min to selectively remove the SiO_2 caps and expose the silicon cores. To remove the silicon nanowire cores, XeF_2 etchant gas was used. Detailed parameters for silicon etch are presented in ref 10. Thus far, we obtained a silica nanotube array embedded parylene membrane in which the continuous pores run through the entire film. As a final step, the parylene matrix was completely etched away using high power oxygen plasma treatment for 30 min to give a vertically oriented, robust silica nanotube array.

Figure 2 shows the scanning electron micrographs (SEM) for the silicon nanowire array, the silica nanotube embedded parylene membrane, and the silica nanotube array. The Si nanowires are vertically orientated to form a perfect array as shown in Figure 2A. Typical sizes of the silicon nanowires are 50−200 nm, and the length is around 8 μm. On the top of each nanowire, there is a bright gold tip indicative of the vapor−liquid−solid growth.[9] After the parylene deposition, the SiO_2 cap removal, and the etching of the silicon cores, we obtained the silica nanotube embedded parylene membrane as shown in Figure 2B. The pores can be readily seen on the polymer surface. The bright spots correspond to the gold nanoparticle tips, which nearly take the shape of half spheres. The membrane has a relatively flat surface. The inset in Figure 2B clearly shows the hollow pores with silica walls. After the O_2 plasma etching of parylene, a free-standing silica nanotube array is obtained (Figure 2C). The nanotubes are well aligned and retain the vertical orientation of the starting silicon nanowire templates. The inset of Figure 2C is a high magnification SEM image showing clearly the morphology of the vertical nanotube array. The average length of the nanotubes is about 5 μm. The average size of the resulting silica nanotubes is larger than that of the template silicon nanowires

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10.1021/ja034163+ CCC: $25.00

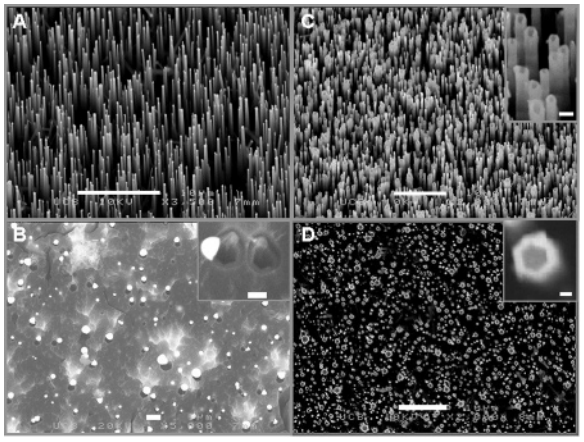

Figure 2. Scanning electron micrographs of the silicon nanowire array (A), the silica nanotube/parylene membrane (B), and the free-standing silica nanotube array (C). The scale bars for (A), (B), and (C) are 10, 1, and 10 μm, respectively. The inset in (B) is a high magnification SEM image for two silica nanotubes embedded in a parylene membrane with a scale bar of 200 nm. The inset in (C) shows the zoom in view of vertical silica nanotubes with a scale bar of 200 nm. (D) is a top view of the silica nanotube arrays. The scale bar corresponds to 10 μm. The inset of (D) shows the open end of a single silica nanotube. The scale bar represents 100 nm.

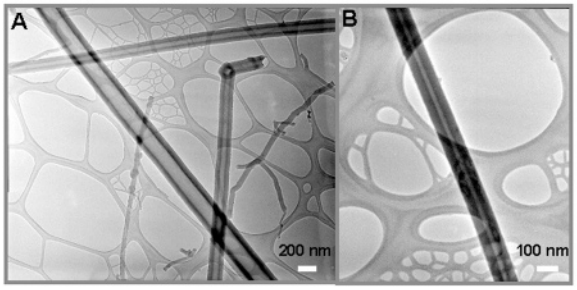

Figure 3. Transmission electron micrographs for the as-prepared silica nanotubes.

because of the structural expansion caused by the thermal oxidation. Figure 2D is a top view of the silica nanotube array. It also confirms the vertical orientation of these silica nanotubes and clearly shows their pore and the walls. Interestingly, the pore and silica wall exhibit a well-defined hexagonal shape (inset of Figure 2D) indicative of the ⟨111⟩ orientation of the original Si nanowires and the anisotropic in-plane etching rates.

Transmission electron microscopy (TEM) further proves the formation of high-quality silica nanotubes. The nanotubes as shown in Figure 3A have uniform inner diameters along the entire nanotubes. The pore sizes for the nanotubes ranges from 10 to 200 nm. The inner and the outer wall surfaces are rather smooth. It is observed that the thicknesses of the nanotubes are nearly identical (∼70 nm for 1000 °C thermal treatment) for all of the nanotubes with different pore sizes. This is reasonable because the oxidation layer thickness is expected to be the same for the nanowires under a constant thermal treatment condition because the thermal oxidation of the silicon is a self-limiting process. Taking advantage of this phenomenon, we can precisely control the tube size and the wall thickness simply by adjusting the thermal treatment temperature. For example, the sample oxidized at 900 °C has a typical wall thickness around 55−65 nm, and the thickness is 30−35 nm for the 800 °C sample. Figure 3B shows a typical thin tube with pore size of ∼20 nm. The pore is continuous and has a smooth inner wall. Occasionally, we have also observed branched nanotubes which could provide interesting implications in fluidic applications (see Supporting Information). This multistep approach of making silica nanotube arrays templated from silicon nanowire arrays is a well-controlled process capable of controlling the pore size and the array height, and the tubes can be readily subjected to different surface modification on inner and outer walls. The respective surface modification of inner and outer walls is critical for further application in bioseparation and the smart molecule transport. In addition, the walls of these nanotubes are made of pinhole-free condensed thermal oxide, which would be advantageous in terms of their mechanical robustness and fluidic stability.

In summary, silica nanotube arrays were fabricated using a multistep oxidation-etching process from vertical silicon nanowire array templates. These silica nanotubes are uniform in morphology and have similar wall thickness. Formed through high temperature thermal oxidation, they are rigid, robust, and could be used as building blocks for fabricating the nanofluidic system. The vertical silica nanotube array as well as the nanotube/polymer membranes might find applications in catalysis, chemical/biological separation, and sensing.

Acknowledgment. This work was supported by the Camille and Henry Dreyfus Foundation, Beckman Foundation, and National Science Foundation. P.Y. is an Alfred P. Sloan Research Fellow. Work at the Lawrence Berkeley National Laboratory (A.M., P.Y.) was supported by the Office of Science, Basic Energy Sciences, Division of Materials Science of the U.S. Department of Energy. We thank the National Center of Electron Microscopy for the use of their facilities.

Supporting Information Available: TEM images of branched silica nanotubes (PDF). This material is available free of charge via the Internet at http://pubs.acs.org.

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(10) The Si/SiO_2 core-sheath nanowire sample after removing oxide caps was loaded into the XeF_2 etching chamber. The chamber temperature is adjusted at 40 °C. After the chamber was purged and flushed with nitrogen, the XeF_2 vapor was introduced together with N_2 (XeF_2:N_2 = 4:5) to conduct etching for 30 s at a total pressure of 9 Torr. The chamber is then evacuated and flushed with nitrogen, and the etching is carried out for a second cycle. Eight cycles were carried out for complete etching of the silicon cores.

JA034163+