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Fabrication of thick silicon dioxide layers for thermal isolation

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Abstract
This paper reports a method of fabricating very thick (10–100 μm) silicon dioxide layers for thermal isolation without the need for very long deposition or oxidation. Deep reactive ion etching (DRIE) is used to create high-aspect-ratio trenches and silicon pillars, which are then oxidized and/or refilled with LPCVD oxide to create oxide layers as thick as the DRIE allows. Stiffeners are used to provide support for the pillars during oxidation. Thermal tests show that such thick silicon dioxide layers can effectively thermally isolate heated structures from neighboring structures within a distance of hundreds of microns. The thermal conductivity of the thick SiO_2 is measured to be $\sim$1.1 W (m K)$^{-1}$. Such SiO_2 diaphragms of thickness 50–60 μm can sustain an extrinsic shear stress up to 3–5 MPa.

1. Introduction

Good thermal isolation is very desirable in small-scale high-temperature devices. Examples include micro hotplates [1], infrared detectors [2] and infrared thermal sources [3], ultrasonic transducers for high-temperature applications [4], micromachined reactor [5] and combustion-based micro power generators [6–10]. Of the commonly used MEMS materials, silicon dioxide is preferred because of its low thermal conductivity. It also has good mechanical strength and low thermal expansion coefficient. Therefore, it is an excellent material for both supporting the hot regions of high-temperature devices and achieving good thermal isolation. For sufficient mechanical support, there is certain requirement for the silicon dioxide thickness, and in many cases the thickness is in the order of 10 μm or larger.

Because of diffusion/deposition rate limitations, it is not very practical to produce thick SiO_2(>5 μm) using standard high-temperature oxidation or deposition. One reported approach for fabricating thick SiO_2 involves converting a portion of a silicon substrate to porous silicon by anodization [11], and then oxidizing the porous silicon [12, 13] to create SiO_2 of $\sim$25 μm thickness. Because pores exist inside the SiO_2, this method may not be suitable for fabricating an impermeable SiO_2 layer for applications that need to maintain a pressure difference between the two sides of the layer or contain liquid or gas within the layer. Another approach uses a spin-on glass method (sol–gel technique) [14, 15] to produce firm and crack-free SiO_2 films as thick as 200 μm. However, these films may not be strong enough for mechanical support.

This paper presents a method of fabricating silicon dioxide layers of 10–100 μm thickness [16] without the need for very long deposition or oxidation. As illustrated in figure 1, the technique uses deep reactive ion etching (DRIE) to create high-aspect-ratio trenches and silicon pillars, which are then oxidized and/or refilled with LPCVD oxide to create layers as thick as the DRIE allows. The high-aspect-ratio trenches are realized in a STS DRIE etcher by a Bosch process using SF_6 and C_4F_8. Because the trenches are refilled by oxidation and/or LPCVD oxide deposition, the resulting SiO_2 layer is impermeable and can sustain a large pressure difference. Although a similar approach has been used to produce a SiO_2 layer of thickness $\sim$20 μm [17, 18] for electrical isolation of passive components such as coils, this paper reports thicker silicon dioxide layers (thickness 10–100 μm, 40–60 μm in general) and their application for thermal isolation at high temperatures and for mechanical strength and isolation.

Other than its use for thermal isolation in emerging high-temperature systems, very thick (10–100 μm) SiO_2 layers have a variety of applications for mechanical support of suspend elements in integrated circuits and MEMS and for micropackaging.

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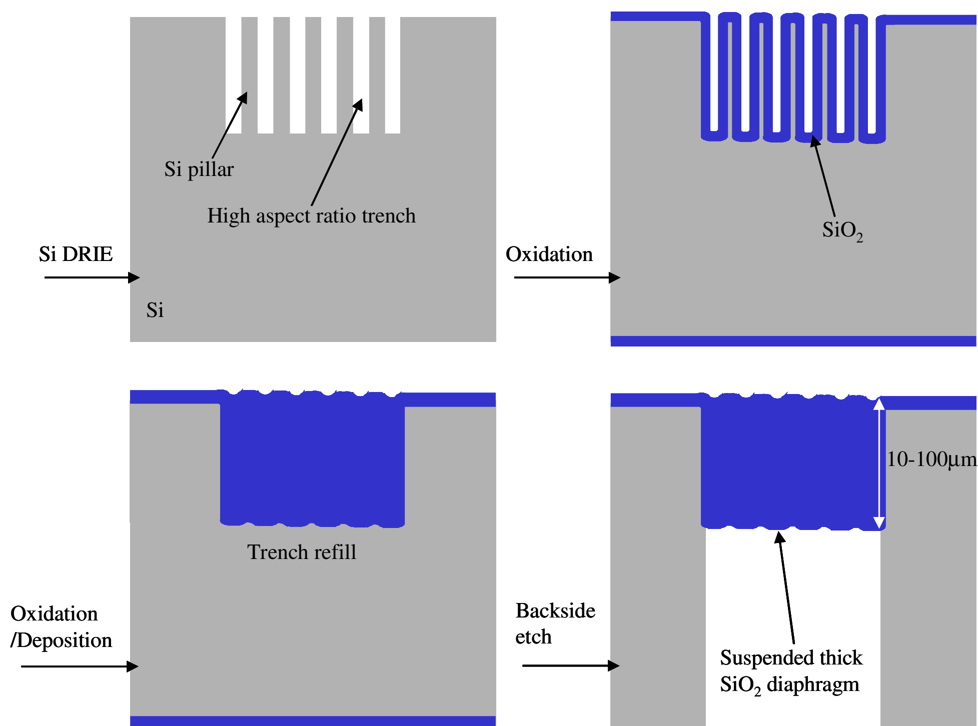


Figure 1. DRIE etched pillars are oxidized and the trenches are refilled by oxidation and/or LPCVD oxide deposition to create a thick oxide layer, which can be released by removing the silicon from backside etching.

2. Fabrication of thick silicon dioxide

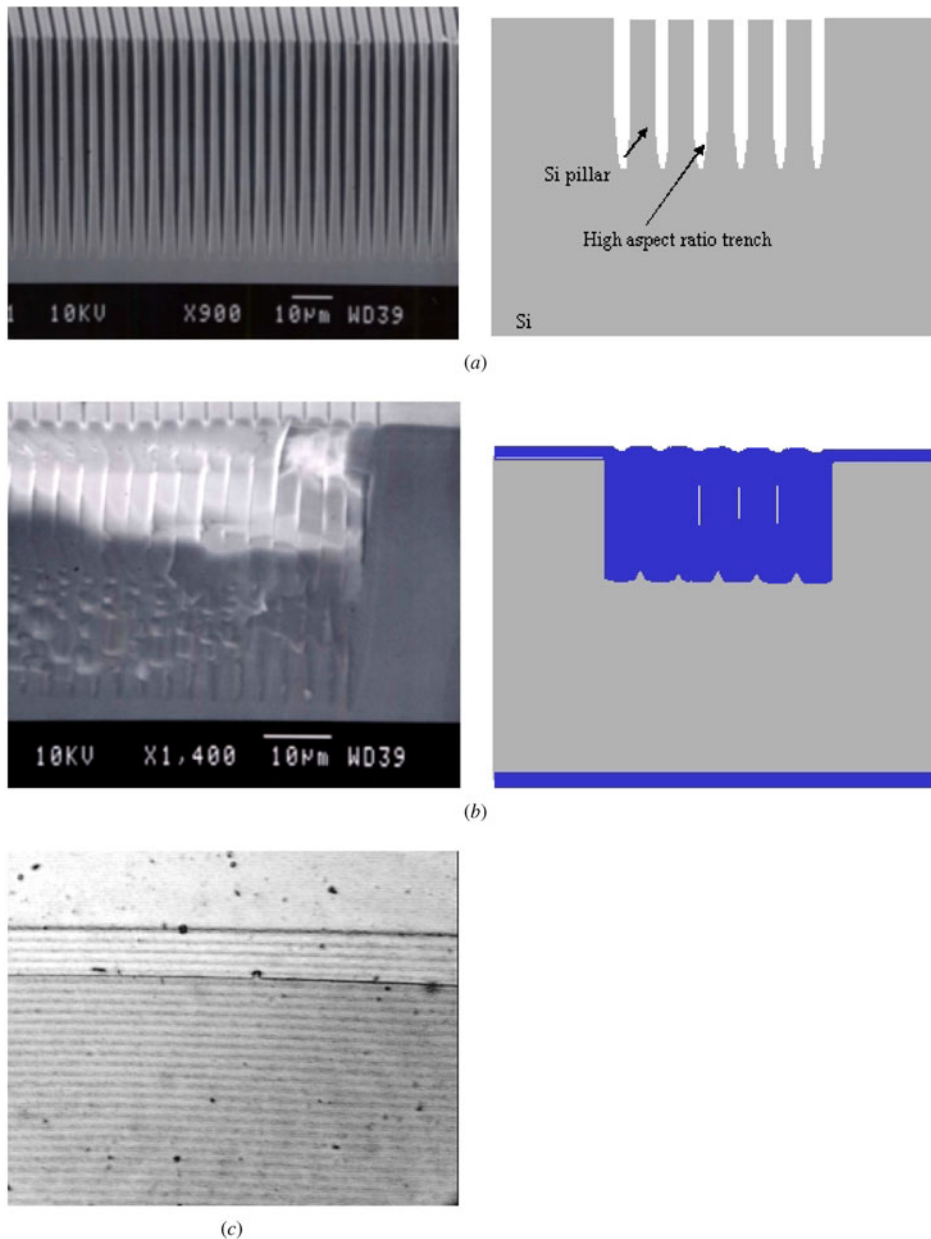
The trench refill process illustrated in figure 1 is not complicated and can be achieved by two methods: trench refill by oxidation only or by oxidation and LPCVD oxide. However, a complete refill is difficult and strongly depends on the sidewall profile of the trenches, the ratio of trench width to silicon pillar width, and the stress resulting from the oxidation, as will be discussed below.

2.1. Trench refill by oxidation only

In the process illustrated in figure 2, the trench is refilled by consuming the Si pillars through oxidation and outgrowth of the oxide into the trench. In figure 2, the left side shows the SEM and optical photographs and the right side shows the corresponding drawings illustrating the process. When Si is oxidized, the larger volume of the oxide fills a region approximately 54% above and 46% below the original silicon surface of the wafer. Therefore, to obtain an exact refill by oxidation only, the ratio of silicon pillar width to trench opening should be ~0.85. In practice, the ratio should be made larger than this to ensure a complete refill. Furthermore, to minimize the time needed for oxidizing the silicon, a narrow layer is preferred. However, a wide silicon pillar is also required to resist damage and stress during processing. As a trade-off, a mask where the width of Si pillars is ~2.0 μm and the trench opening is ~1.5 μm was fabricated. These dimensions were chosen to accommodate the undercut of trenches by DRIE. After DRIE to create the high-aspect-ratio straight trenches in Si (figure 2(*a*)), the wafer is wet oxidized for 10 h at 1100 °C to refill the trench (figures 2(*b*, *c*)) and join all the SiO_2 layers together to form a thick layer with a small amount of un-oxidized Si enclosed inside the top SiO_2. It can be seen from figure 2(*b*) that because of the non-ideal sidewall profile formed by the bowing effect of DRIE (figure 2(*a*)), the top and the bottom of the thick oxide layer join together, but voids are formed in the middle. For many applications this is acceptable, and for thermal isolation purposes this is even preferred since the voids reduce thermal conductance, but for some applications requiring excellent mechanical strength it is preferred that the entire layer be of solid material.

2.2. Trench refill by oxidation and LPCVD oxide

To avoid the formation of voids, we can use both oxidation of Si pillars and further refilling of the trenches using LPCVD oxide. Figure 3 shows the fabrication results of oxidation and LPCVD oxide trench refill. In order to achieve complete refill, one needs to change the sidewall profile during trench etching. Using the same mask used to fabricate structures shown in figure 2(*a*) but adjusting the sidewall profile mainly by tuning the DRIE etch/passivation ratio, a trench with larger width at the top and gradually narrower width going towards the bottom can be obtained (figure 3(*a*)). After 10 h of wet oxidation at 1100 °C, the trench bottom gets refilled by lateral growth of oxide, but the top is still open (figure 3(*b*)). 1–2 μm of LPCVD oxide is then deposited to refill and seal the opening (figure 3(*c*)). In these SEM photographs, the oxide regions are shown as lighter regions because of charging effect (figures 3(*b*), (*c*)). The thick oxide layer so produced does not have voids in the middle. However, as shown in figures 3(*c*) and (*d*), the large stress in the narrow Si pillars bends the oxide pillars and produces some openings between adjacent areas that cannot be completely filled by LPCVD oxide.



(*a*)

(*b*)

(*c*)

Figure 2. SEM and optical photographs (left) and drawings (right) showing trenches refilled only by oxidation of Si pillars: (*a*) DRIE etched trenches, (*b*) oxidized Si pillars refill the trenches and (*c*) top view of 2(*b*).

This stress problem can be overcome by adding periodic stiffeners (figure 4) perpendicular to the direction of the trenches to provide support for the pillars and by using thicker Si pillars (as shown in figure 3(*a*), the lateral etch during DRIE makes Si pillars too narrow). A new mask was then designed, where the width of stiffeners is ~1.4 μm with a pitch of 20 μm along the trench direction (at junction regions the pitch is as small as 5 μm to further strengthen these particularly stressed regions). On the new mask, the width of Si pillars was increased to ~2.8 μm and the trench opening to ~1.2 μm. Correspondingly, the wet-oxidation time was increased to 15–20 h at 1100 °C to fully oxidize the wider bottom of the resulting Si pillars. Figure 5 shows one preliminary result using stiffeners. It can be seen that the top is totally refilled without bending the opening (stiffeners with pitch 50 μm have also been tried and it is found that for this pitch, openings larger than 8 μm are produced in some regions). Although the top surface is not perfectly smooth, metal lines of thickness about 1000 Å can still be deposited on the top surface by evaporation. Voids are formed at the bottom of this layer. One reason may be that the transfer of LPCVD reactants to the bottom of the trenches is hindered by the stiffeners. Another reason may be that the DRIE etch did not produce the desired sidewall profile. Further characterization of DRIE and modification of stiffeners will improve overall yield and reproducibility.

3. Thermal isolation using thick oxide

A structure with a SiO_2 square ring (300 μm wide, 53 μm thick) surrounding a Si island (5 mm × 5 mm × 0.5 mm) has

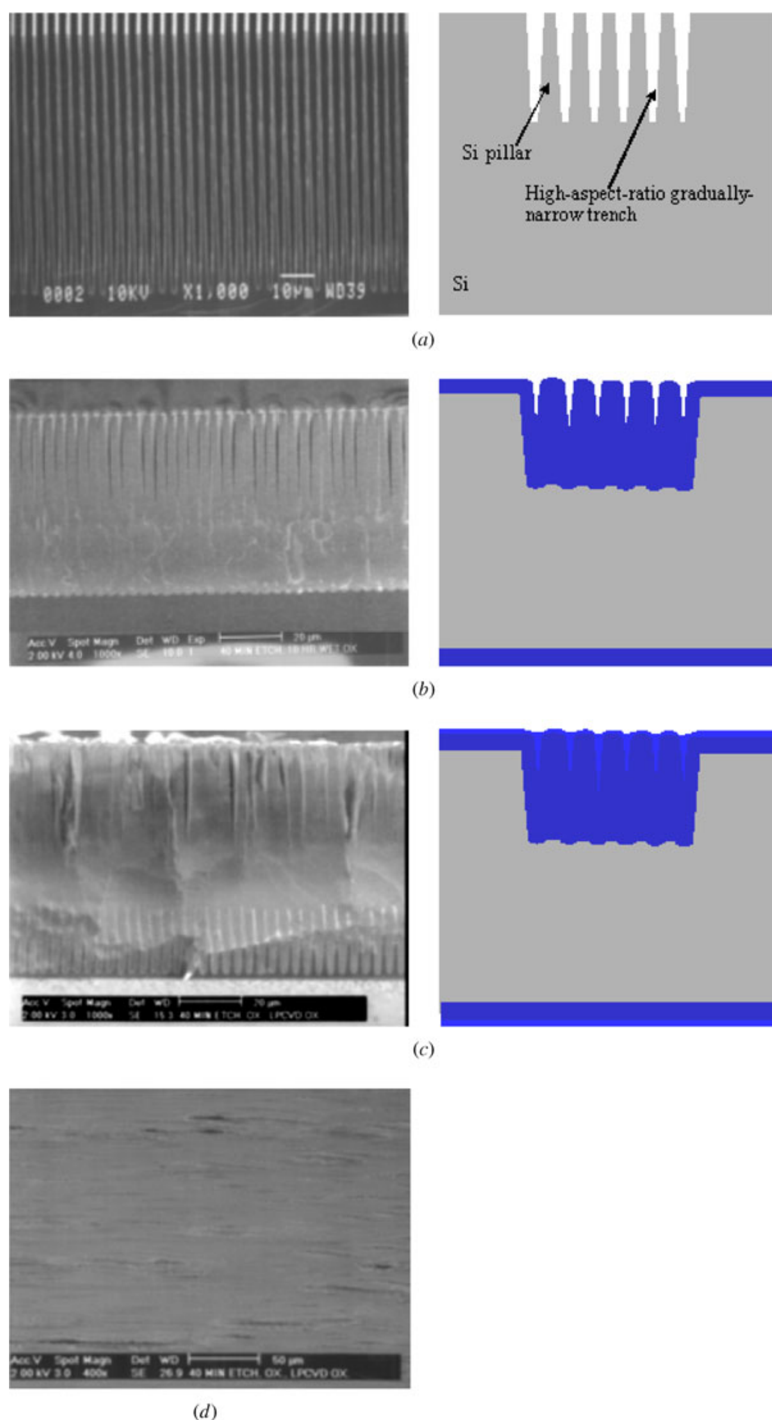


Figure 3. SEM pictures (left) and drawings (right) showing trenches refilled by oxidation plus LPCVD oxide deposition. Stiffeners are not used in the structures corresponding to this set of SEMs: (*a*) DRIE etched trenches, (*b*) trenches refilled by oxidation, (*c*) further refill by LPCVD oxide and (*d*) top view of 3(*c*).

been fabricated for thermal and mechanical tests (figure 6), where trenches are formed along the ring direction and stiffeners go from the Si island to the outside perimeter. The heater and thermoresistors are fabricated on the island and on the two sides of the ring, respectively, by evaporation of Ti/Pt (200 Å/1000 Å).

The Si island is heated up by passing current through the heater, and the temperature difference between the two sides of the ring is measured at steady state using the thermoresistors. Assuming all input power is dissipated through the thick SiO_2 layer (ignore convection and radiation losses under the conditions of small power input and small temperature difference across the SiO_2 layer), the thermal conductivity of the thick SiO_2 is measured to be $\sim$1.1 W $(\mathrm{m\,K})^{-1}$, which is slightly smaller than that of the bulk fused SiO_2: $\sim$1.38 W $(\mathrm{m\,K})^{-1}$ [19]. The major reason for the difference may be that the voids inside the thick SiO_2 reduce thermal conductance of the thick SiO_2 structure.

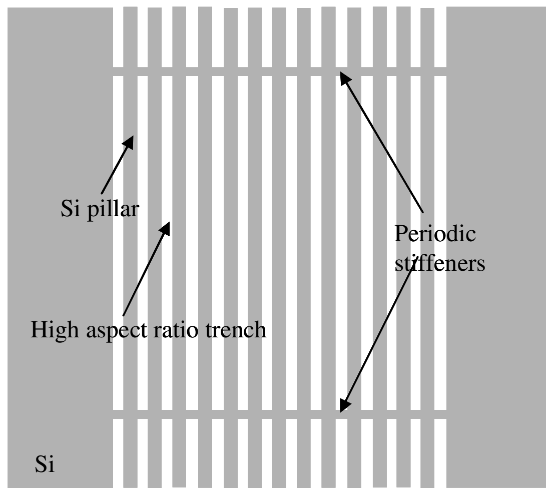


Figure 4. Top view illustration of the high-aspect-ratio trenches using stiffeners.

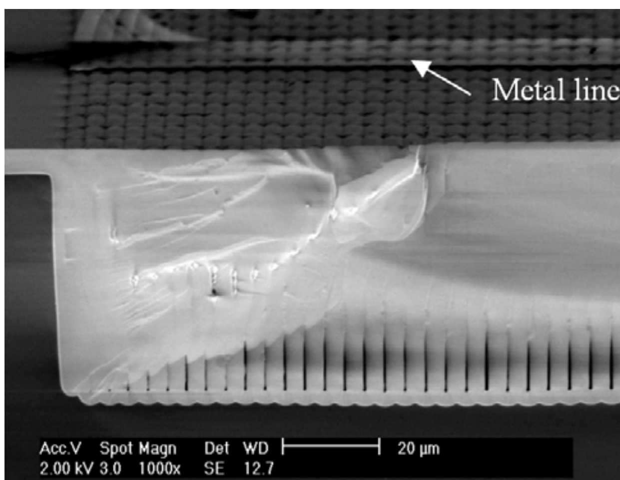


Figure 5. Thick oxide layer using stiffeners. The cross section is perpendicular to trench direction.

Figure 7 shows the temperature distribution of the heated silicon island and the surrounding area measured by an infrared imager. It is seen that the SiO_2 ring can effectively thermally isolate the island from the support ring with a temperature difference of $\sim$190 °C when the silicon island is $\sim$440 °C at an input power of 1 W. It should be pointed out that figure 7 is not a direct image from the infrared imager but a temperature distribution obtained from infrared data. Since there is a large emissivity difference between the Pt heater surface and the rest of the top surface, an emissivity correction has been made to the Si island based on thermoresistor measurement. But no correction has been made to the SiO_2 ring and the rest of the metal lines. In the measurement, most of the structure is suspended in air and only the two far edges (top and bottom of figure 7) are supported by thermal isolation material. Because of the excellent thermal isolation by the thick SiO_2 layer within the small distance of 300 μm, the test structure is actually an excellent low-power high-temperature micro-heater. It should be pointed out that the substrate is at a temperature of $\sim$250 °C during the test because of the thermal isolation material used to support the far edges. The tests were set up so to achieve

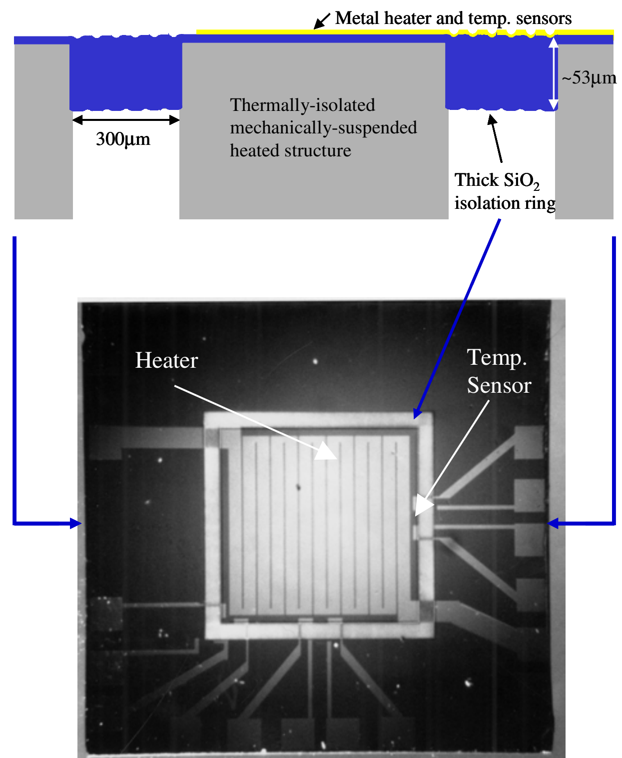


Figure 6. Test structure: a 5 mm $\times$ 5 mm $\times$ 0.5 mm Si island suspended on a 300 μm wide and 53 μm thick oxide ring. Heater and temperature sensors are built to characterize thermal conductivity of SiO_2.

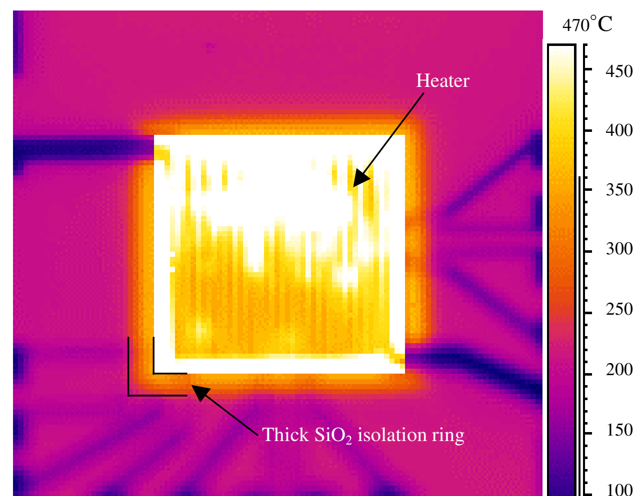


Figure 7. Infrared measurement of temperature distribution across the thick oxide diaphragm. The thick SiO_2 ring surrounds the hot region in the middle. Emissivity correction has been made for hot and cold regions.

(This figure is in colour only in the electronic version)

a high temperature in the Si island with low input power. In many applications, the substrates/chips cannot be used at a temperature as high as $\sim$250 °C. A thermally conductive supporting material or a substrate-cooling method can be used for these substrates/chips to maintain a low temperature. While the ring structure can still be used to thermally isolate a

high-temperature region in the substrates/chips effectively by taking advantage of the low thermal conductance of the ring.

The thick silicon dioxide layer also provides excellent mechanical support. The test structure with a SiO_2 thickness of 50–60 μm has been subjected to an applied differential pressure where the Si island is only supported by the SiO_2 ring. Results show that the ring breaks at a pressure difference of about 22–32 psi. This indicates that the SiO_2 layer has excellent mechanical strength and can sustain an extrinsic shear stress of up to 3–5 MPa.

The intrinsic stress inside the refilled trenches not only causes the problem of oxide pillar bending as described above in the fabrication, but also makes it very difficult to fabricate large membrane made of the thick oxide. An attempt was made to fabricate such square or circular membranes with a size of ~5 mm. Most of the membranes were broken after their release.

4. Conclusion

This paper presented a method of fabricating very thick (10–100 μm) silicon dioxide layers for thermal isolation without the need for very long deposition or oxidation. DRIE is used to create high-aspect-ratio trenches and silicon pillars, which are then oxidized and/or refilled with LPCVD oxide to create layers as thick as the DRIE allows. Stiffeners are used to provide support for the pillars during oxidation. A test structure using a thick SiO_2 ring as thermal isolation and mechanical support to the hot region is fabricated. Thermal tests show that such thick silicon dioxide layers can effectively thermally isolate heated structures from neighboring structures within a distance of hundreds of microns. The thermal conductivity of thick SiO_2 is measured to be $\sim$1.1 W $(\mathrm{m\,K})^{-1}$. The SiO_2 layer has excellent mechanical strength and can sustain large extrinsic shear stress. The thick silicon dioxide can be used in emerging high-temperature MEMS devices for excellent thermal isolation.

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