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Failure modes and FEM analysis of power electronic packaging

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Abstract

The development of power electronics technology is driven by the insatiate demand to control electrical power. The new power electronics devices reduce the volume of the converters by three to four orders of magnitude compared to their mercury arc predecessor. And the turn-on and turn-off time has decreased from milliseconds to the microseconds and even nanoseconds, depending on power level. The power range commanded by converters now extends from micro-VA to several hundreds of mega-MVA. Among the new power devices, insulated gate bipolar transistor (IGBT) devices are being more accepted and increasingly used in traction application such as locomotive, elevator, tram and subway. Thus the long-term reliability of IGBT is highly demanded. In this paper the failure modes of power electronics devices especially IGBTs are reviewed. A FEM analysis of a multilayered IGBT packaging module under cyclic thermal loading is presented.

Keywords: Failure modes; Electronic packaging; Power electronic packaging; Finite element analysis; Reliability; IGBT

1. Failure modes of power electronics packaging

The insulated gate bipolar transistor (IGBT) modules are developed with increasing power capability, high voltage and high current (up to several kV and kA). All devices have finite on-state voltage drops when conducting the on-state currents and finite switching times during turn-on and turn-off. These effects result in significant power dissipation in the system. These power dissipations need to be removed through electronic packaging. As reported, in a typical IGBT-based motor drive, 4% of the controlled power is dissipated as heat within the device [3].

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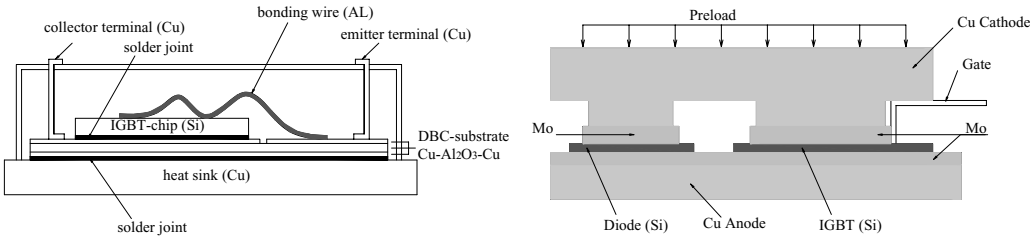

(a) Scheme of Wire Bonding IGBT module (b) Scheme of Press-Pack IGBT module

Fig. 1. Schemes of wire bonding and press pack packaging.

Thus thermal and thermal–mechanical management is critical for power electronics modules. The failure mechanisms that limit the number of power cycles are caused by the coefficient of thermal expansion mismatch between the materials used in the IGBT modules. All interfaces in the module could be locations for potential failures [4]. Several researchers conducted experiments to estimate the long-term reliability and the failure modes of power semiconductor modules [5–8].

The failure modes of IGBT modules are dependent on the mounting technology used. Wire bonding (Fig. 1a) and press pack (Fig. 1b) are two different mounting techniques, and the failure modes are thus different. Press pack or flat pack techniques are relatively new in IGBT, thus most literatures are focused on wire bonding IGBTs.

1.1. Emitter bonding wire lifting failure

For wire bonding IGBT modules, the emitter bonding wire lifting is reported as the most important failure mode [5]. In Wu's research [5], more than forty 300 A/400 A 1200 V IGBT modules were subjected to power cycling test. It was reported that no tested modules could pass 10^6 power cycles in the test. Wire lifting failure occurred in about 70% of the tested modules. Wu and partner [5] believe that the poor bonding pressure and contamination may lead to low fracture strength at the bonding interface. Moreover, bonding wires are subjected to a tensile stress due to the temperature fluctuation during power cycling. Longer wire is subjected to higher tensile stress. This tensile strength also affects the bonding strength. Lambilly and Keser [9] tested the reliability of power IGBT modules with power cycling method. Lifted wire bonds were observed in their test. The Al wire has much larger CTE and expands during heating. They conclude that when the stiffness of the wire and potting material prevent the deformation of the wire, the whole strains are converted to large stresses on the bond area, causing it to get sheared from silicon. This can be amplified by the stiffness and the large CTE of potting material. They indicate that with less stiff potting material better performance of bonding wire can be achieved. In Cova and Fantini's research [10], some medium power devices were subjected to power cycles. The module was placed in a thermally controlled chamber to establish the ambient temperature by forced air ventilation, from 0°C to 150°C. Emitter bonding lift-off was observed as the main failure mechanism. Cova and Fantini claim that the degradation of the die attach was probably the root cause of the failure mechanism. They also claim that the

thermal excursion ΔT may be the cause for damage of the soldering layers and bond wires and the power cycling lifetime was exponentially related to ΔT. Another research by Auerbach and Lenniger [4] also indicates the predominant failure mechanism as lift-off of the bonding wires. The solder degradation between the substrate and copper baseplate as well as the solder degradation between chip and substrate are also important failure mechanism. Their conclusion is similar to that of Auerbach and Lenniger's, that maximum number of power cycles decreases with increasing temperature swing. They also found that the medium junction temperature is very important for the maximum number of power cycles that a module can stand. Lower medium temperature leads to higher power cycling stability.

1.2. Solder degradation

Solder degradation may cause different types of failure. IGBT modules are multilayered structures. Silicon die is soldered to the DCB substrate, and DCB is soldered to the copper heat sink. The substrate and heat sink have much larger CTE than silicon die. This CTE mismatch requires the die bond to be compliant to prevent large stress in the silicon die. Soft solder is more suitable to be used here, since it has low modulus of elasticity, low yield strength, and relatively high ductility. Thus it allows plastic deformation of the bond. Alternatively, less compliant solder may be used if a buffer (such as molybdenum) is used between the substrate and die [11].

Significant amount of heat dissipated by the IGBT modules needs to be removed through this sandwiched structure. Solder degradation at any location increases the thermal resistance from the silicon module to the heat sink. Cyclic temperature shifts during operation produce cyclic shear strains in the die bond due to the CTE mismatch between layers and the spatial temperature gradients. This eventually produces cracking due to fatigue, which lower the critical capability of the bond to transfer heat generated in the die [12–14]. Evans [11] states spatial temperature gradients and transient thermal effects play significant roles in die bond fatigue failure. Fatigue cracks initiate rapidly in solder. They generally initiate at the corner or edge of the die (the point of maximum shear strain) and grow through the die bond. In a die bond of uniform thickness, the crack growth is expected to proceed toward the neutral point or center of the die. The loss of die bonds will increase the die temperature, and effectively reduce the safe operating area of IGBT. Thus the power transistor will eventually fail by catastrophic burn-out or secondary breakdown. Evans and Evans [11] used 133 power transistors in power cycling intermittent operating life test. Their analysis shows that increasing die bond thickness has a significant role in improving the cyclic life of the die bond. The die bond thickness varies substantially between devices and may not be uniform under a single die. This nonuniformity influences the device life by increasing strain concentration and influencing cracks growth. In the test by Wu et al. [6], with SEM image, the forming and growing process of voids and cracks in the solder layer of fine-prepared IGBT cross-sectional samples was quasi-dynamically observed during thermal cycling test. It indicates that void-free solder material is important to produce high reliable power modules. In another power cycling test by Wu et al. [5], the local overheat burn-out failure due to big voids in the solder layer was observed. In the thermal cycling test by Shaw et al. [15], each test article was inspected by a high-frequency ultrasonic C-scan imaging technique. The crack initiation and subsequent

growth were observed. Since the voids are almost unavoidable in any solder joints, Zhu [16] discussed the thermal impact of different types of solder voids using finite element method. Influences of such voids on mechanical characteristics of solder joints are not discussed in this paper.

1.3. Cracks in silicon die and substrate

Large semiconductor devices can be subjected to significant mechanical stress resulting from the CTE mismatch between different layers of devices. In these layers, silicon die and Al_2O_3 or AlN (used as insulator in DCB substrate) have small CTE. On the other hand, the CTE of most metals is several times larger. Due to the bimetal effect, when this multilayer structure is subjected to temperature changes, thermal stresses are developed, resulting in bending deformation. These stresses may cause the brittle silicon and alumina to crack.

Thermal stress-induced IGBT chip crack failure was observed in the power cycling test by Wu et al. [5]. The cracks in silicon chip and alumina were also observed in Wu and partner's [6] thermal cycling test of cross-sectional samples of IGBT module. A simple simulation by Wu et al. [6] showed that the stresses in copper substrate and copper heat sink are compressive, and the silicon chip and alumina layer are subjected to high tension stresses, which cause them to crack.

It is also reported that the residual stress during manufacturing may cause mechanical failure or change the operational characteristics of power modules [17].

Manufacturing requires heating the components above the melting point of solders. Because of the different CTE between layers, significant residual stresses are developed during cooling back to ambient temperature. This affects the reliability of the power module during operation. By using the piezospectroscopic techniques, the absolute magnitudes and spatial distributions of time-dependent thermal residual stress on the surface of silicon die were measured by several researchers [3,18,19].

1.4. Electro-migration in bonding wires

The electro-migration failure in bonding wires is reported by Wu et al. [5]. The high temperature plays an important role in thick wire electro-migration even when the current density is low.

1.5. Surface degradation in emitter bonding pads

Surface degradation in emitter bonding pads was observed in Wu and et al.s test [5], and it could be accelerated by thermo-mechanical stress due to the different CTE of Al and Si. It was found that the metallization surface became rough and hillocks were formed because of recrystallization and electro-migration during power cycling. This process could be accelerated by thermo-mechanical stress due to the CTE mismatch. Wu et al. found chip passivation or polyimide coating could improve IGBT Al metallization degradation.

2. FEM analysis of IGBT modules under cyclic thermal loading

In order to understand the solder joints degradation in IGBT modules, an IGBT module is analyzed with the FEM package ANSYS. The bonding wires are not included in the model since only solder joint layers are the focus in this analysis. The geometry of the module is basically a multilayered structure (shown in Fig. 2), which are bonded together with solder joint layers. The purpose of the FEM analysis is to find the stress–strain distribution at the solder joints under cyclic thermal loading. Since Pb/Sn eutectic and near eutectic solders are highly viscoplastic in nature, a nonlinear viscoplastic material is used for solder in the analysis, whereas the silicon chip, aluminum substrate and copper heat sink are considered to be elastic. Due to the CTE mismatch of laminated materials, under the cyclic thermal loading, the stress and strain development in the free edge of the solder layer will be the main concern in the design and fabrication of semiconductor device packaging [20].

The viscoplastic model used in this study to describe the solder's behavior is Anand's model implemented in ANSYS general purpose FEA program. Anand's constitutive model incorporates viscoplastic, time-dependent plastic phenomenon where the development of plastic strain is dependent on the rate of loading. Viscoplasticity is defined by unifying plastic and creep deformations. There are two basic features in Anand's model. First, there is no explicit yield surface, rather the instantaneous response of the material is dependent on its current state; secondly, a single scalar variable 's' called the deformation resistance, is used to represent the isotropic resistance to the inelastic flow of the material. The main equations of this constitutive model are

$$\text{flow equation}: \quad \dot{\varepsilon}_v = A\mathrm{e}^{-Q/RT}\left[\sinh\left(\xi\frac{\sigma}{S}\right)\right]^{1/m},$$

$$\text{evolution equation}: \quad \dot{s} = \left[h_0|x|^a\frac{B}{|B|}\right]\dot{\varepsilon}_v,\ a>1,$$

where $B = 1 - s/s^*$ with $s^* = \hat{s}[\dot{\varepsilon}_v/A\mathrm{e}^{Q/RT}]^n$.

This equation allows modeling not only strain hardening but also strain softening. where $\dot{\varepsilon}_v = \mathrm{d}\varepsilon_v/\mathrm{d}t$ is the effective inelastic deformation rate; A is a pre-exponential factor, Q is the activation energy, R is the universal gas constant, T is the current absolute temperature, σ is the current tensile stress, n is the strain rate sensitivity of saturation (deformation resistance)

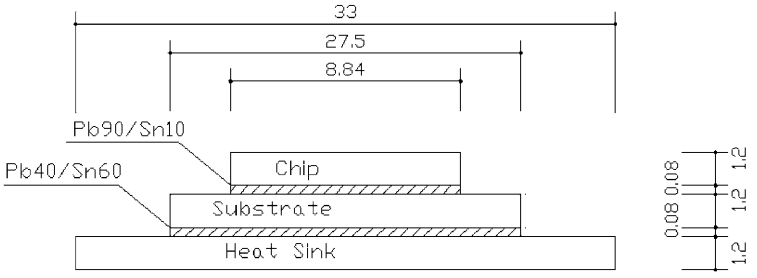

Fig. 2. Schematic layout of structure (mm).

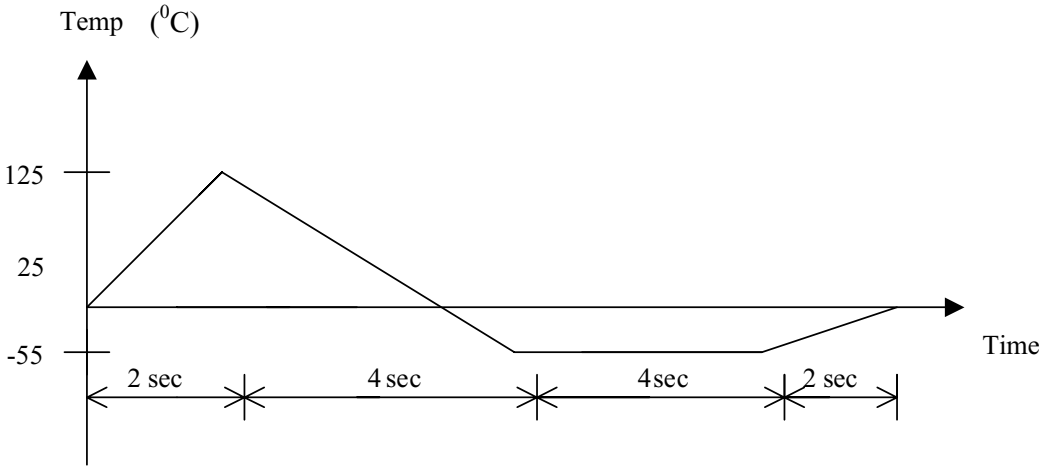

Fig. 3. Thermal time history.

value, $\hat{s}$ is the coefficient for saturation, ξ is the multiplier of stress, m is the strain rate sensitivity of stress, $\dot{s}$ is the time derivative of deformation resistance, s^* is the saturation value of deformation resistance, h_0 is the hardening/softening constant, a is strain rate sensitivity of hardening or softening.

Since bending strength of very thin layers is negligible, it is common to neglect bending moment in the adhesive layer. It is acceptable to simplify the 3-D laminated microelectronic structure to 2-D plane strain problem. It should be pointed out that a more accurate stress analysis would require modeling the assembly with plate and 3-D interface elements. Experimental and 3-D numerical stress analysis of laminated structures is an area that needs further research [21].

Fig. 3 shows the temperature time history used in the analysis. The range of the frequency of a typical semiconductor device is 5 cpm, thus we took the loading situation effectively one thermal cycle of the temperature range from -55°C–125°C (Fig. 3). The finite element mesh of the structure is shown in Fig. 4.

The models have been broken into regions of adjustable element densities. The boundary condition is that the nodes at the base are fixed in both X and Y directions. Due to the symmetry of the structure and load, we only analyzed half of the structure. The points in the symmetric plane are fixed in X direction and free in Y direction.

Material properties for the adherent layers are given in Table 1 [21]. Material properties for the Pb 90/Sn 10 and Pb 40/Sn 60 solders are shown in Table 2 [21]. The solder layers are considered to be viscoplastic material and the material parameters are shown in Table 3 [22].

Thermal analysis has been performed using ANSYS. The stress distribution after one thermal cycle is shown in Fig. 4. In Figs. 5 and 6, xy-strain contour results of Pb 90/Sn 10 are shown. Finite element analysis results indicate that the outer edge element is the critical point for delamination initiation. It is observed that there is significant plasticity in the solder layer mainly

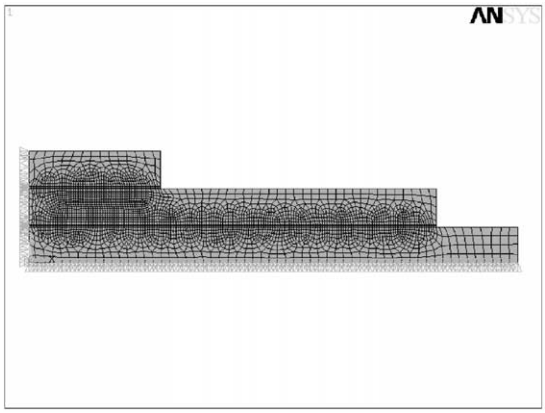

Fig. 4. Finite element mesh.

Table 1

Properties	Chip	Substrate	Heat sink
E (Gpa)	124.13	322.04	117.22
v	0.2	0.25	0.3
ρ (gm/cm^3)	2.33	0.9	8.69
α^T ($/^\circ$c)	3×10^{-6}	4×10^{-6}	16.1×10^{-6}

Table 2
T is the absolute Kelvin temperature

Pb 40/Sn 60	Pb 90/Sn 10
$E = 62.0–0.067$ T Gpa	$E = 68.95 \times (T/300)^{-2.95}$ Gpa
$G = 24.3–0.029$ T Gpa	$v = 0.3\ (T/300)^{0.14}$
$\alpha^T = 21.6 \times 10^{-6}/^\circ$C	$\alpha^T = 24.0 \times 10^{-6}/^\circ$C
$\rho = 8.52$ gm/cm^3	$\rho = 10.9$ gm/cm^3

Table 3
Parameters used in Anand's model

Parameters	Value
A	3.862×10^4 s^{-1}
Q/R	6966 K
m	0.2845
h_0	30.11 Gpa
$S^\wedge$	122.7 Mpa
n	0.002
a	1.8
S_0	5040 Mpa
ξ	5.0

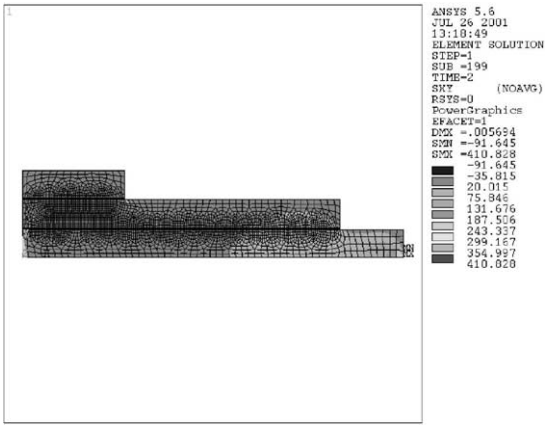

Fig. 5. Shear stress distribution (Pa).

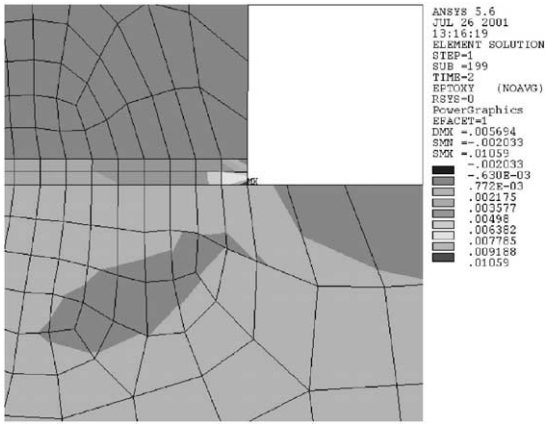

Fig. 6. Shear strain distribution.

due to the material properties of the adherends and the adhesive, and also due to the boundary condition. The distribution of the shear and normal stresses and strains of the solder joint layers Pb 40/Sn 60 and Pb 90/Sn 10 at temperature 125°C are shown, respectively, in Figs. 7 and 8. The distributions are from center point to free edge. The shear strains and stresses increase along the solder layer from the value of zero in the center to the highest value to the point near the free edge and drop down. The normal stresses are tension in the center of the solder layer and slowly decrease to the half of the length of the solder layer and changes to compression at the free edge. There are some differences in stress profile between the two solder layers, which we assumed due to the interaction of the upper and lower structures.

There is another problem that needs to be addressed, which is about the mesh size effect on repeatability and accuracy of the result from the ANSYS analysis. For viscoplastic model, the

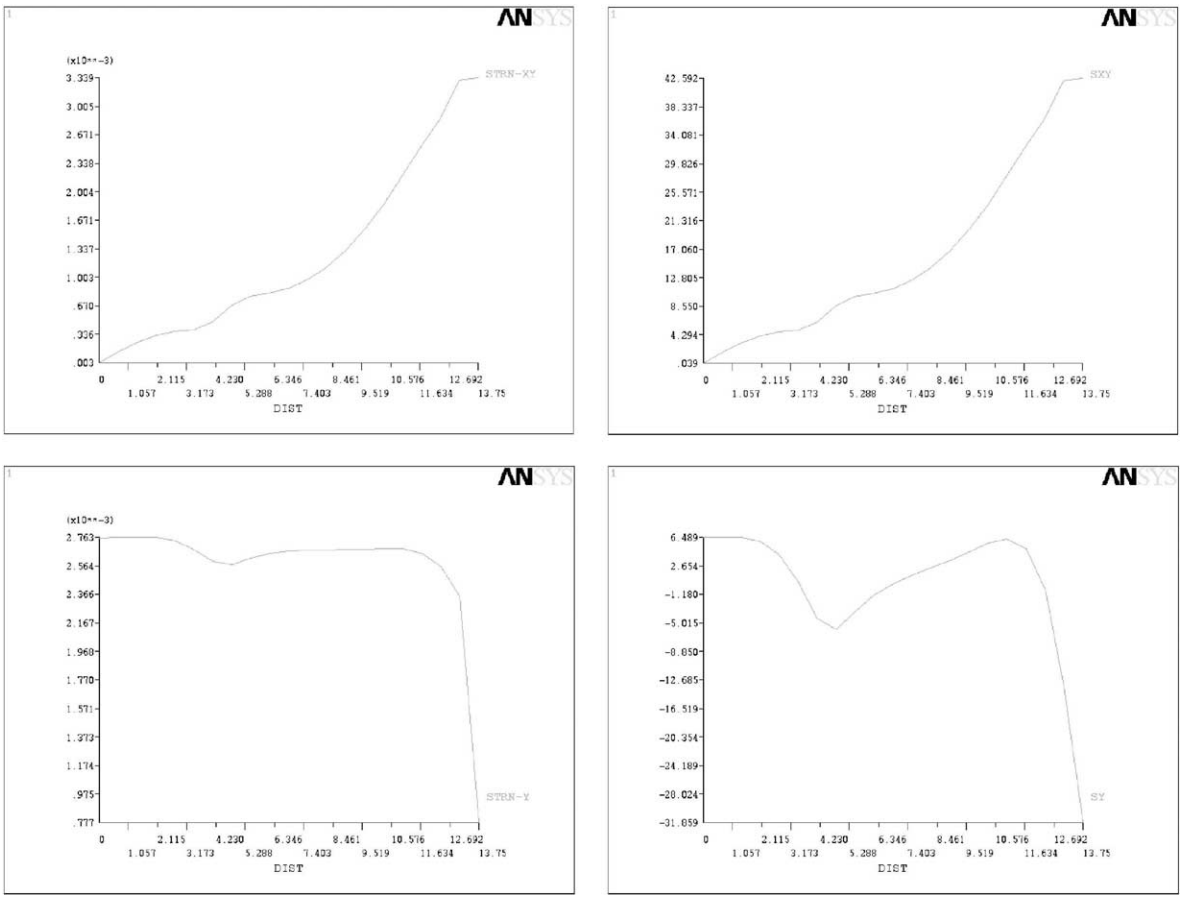

Fig. 7. Stress and strain distribution in Pb 40/Sn 60 solder layer: (a) shear strain; (b) shear stress; (c) normal strain; (d) normal stress, (MPa for stress, mm for the distance).

results are not sensitive to mesh refinement, especially for shear stresses. There is about 1–2% difference between the largest shear stress in the coarsest mesh and finest mesh [24].

3. Conclusions

In this paper we reviewed different failure modes in power electronic devices. With the development of power electronics technology, the research in this field will grow rapidly. Among the new power devices, IGBT devices are getting more popular in traction application, which require highly reliable packaging. Some failure modes have been researched intensively, but there are still many failure mechanisms, which need further research. In the second part of the paper we use ANSYS nonlinear program to analyze a simplified IGBT module and obtain the

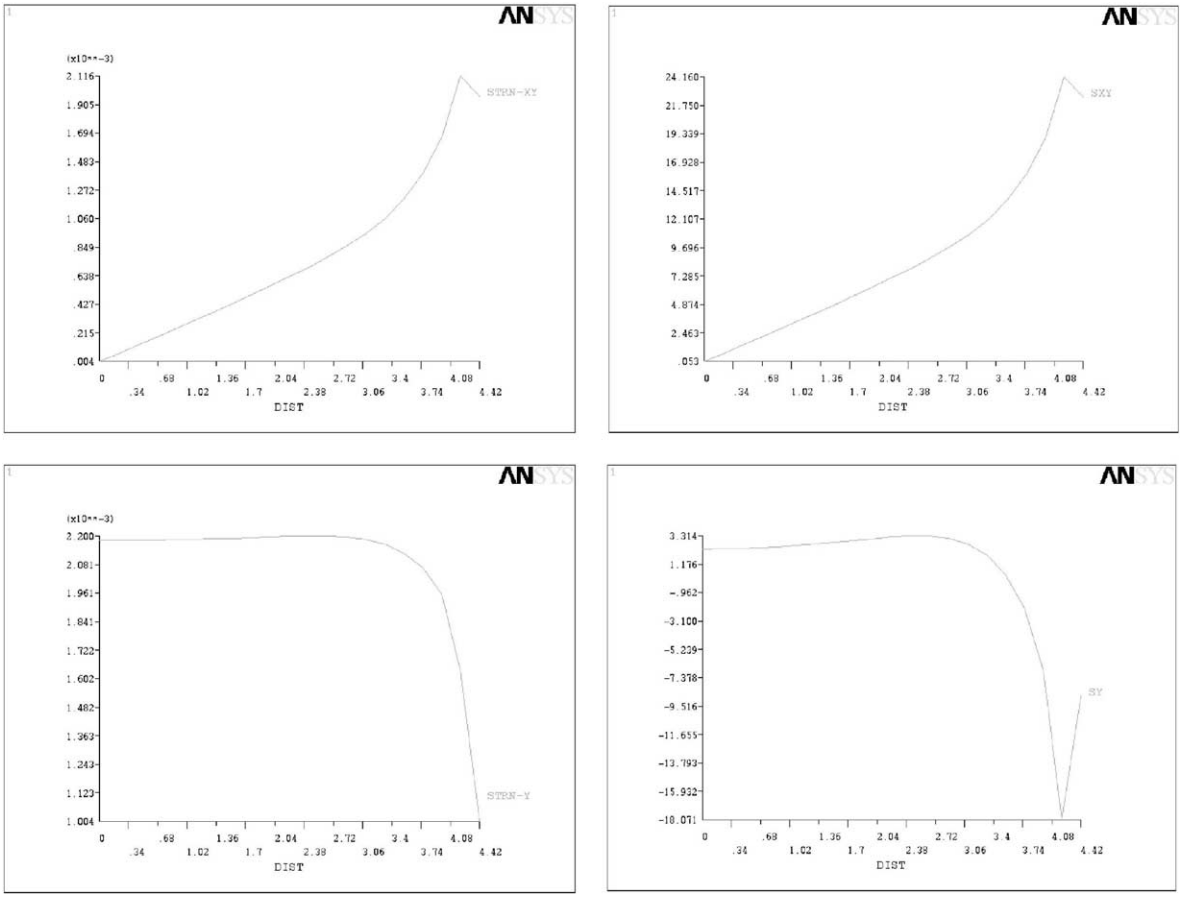

Fig. 8. Stress and strain distribution in Pb 10/Sn 90 solder layer: (a) shear strain; (b) shear stress; (c) normal strain; (d) normal stress, (MPa for stress, mm for the distance).

stress and strain in the solder layer. From these results we conclude that the thermal cycling has significant effect on the solder layer reliability.

Using finite element analysis and damage mechanics constitutive model it is possible to predict number of cycles to failure for solder layers [23]. Presently, we are working on a model to simulate damage degradation mechanism under electrical current. Combining electrical current induced damage evolution with thermal cycling damage will enable us to predict reliability of a power device in actual working conditions.

4. Uncited references

[1,2]

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