Slow-Scale Instability of Single-Stage Power-Factor-Correction Power Supplies

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***Abstract*—This paper reports slow-scale instability in a single-stage power-factor-correction (PFC) power supply, which is a popular design solution for low power applications. The circuit employs a cascade configuration of a boost converter and a forward converter, which share an active switch and operate in discontinuous-conduction mode (DCM), to provide input PFC and tight output regulation. Main results are given by "exact" cycle-by-cycle circuit simulations. The effect of the slow-scale instability on the attainable power factor is illustrated in terms of total harmonic distortion which can be found by taking the fast Fourier transform of the input current. The slow-scale instability usually manifests itself as local oscillations within a line cycle. Based on the critical condition of DCM for the buck converter, the underlying mechanism of such instability is further investigated. It has been found that border collision is the underlying cause of the phenomenon. Moreover, it has been shown that the border collision observed here is effectively a nonsmooth Neimark–Sacker bifurcation. Finally, experimental results are presented for verification purposes.**

***Index Terms*—Power-factor correction (PFC), single-stage PFC power supply, instability, border collision.**

I. Introduction

POWER-FACTOR correction (PFC) has become an important design consideration for switching power supplies [1], [2]. For low power applications (below 200 W), the single-stage isolated PFC power supply (SSIPP) proposed by Redl *et al.* [3] is a cost effective design solution to provide PFC and tight output regulation. Basically, the circuit of SSIPP employs a cascade structure consisting of a boost PFC converter and a forward converter for output regulation. Being a single-stage converter, the SSIPP uses only one active switch and mandatorily operates the PFC stage in discontinuous-conduction mode (DCM) to achieve automatic PFC function and to maintain a fixed (load-independent) voltage stress in the storage capacitor which sits between the two stages. Thanks to these advantages, the SSIPP has become a popular choice for low power applications, and hence has received a great deal of attention in the past decade [4]–[6].

Recently, studies of nonlinear dynamics of switching power converter circuits have identified various kinds of bifurcation behaviors in a number of simple dc-dc converters under some typical control configurations (see [7]–[10], and references therein). Such studies have also been extended to the PFC converters, which are actually ac-dc converters with a near unity input power factor. For the boost PFC preregulators operating in continuous-conduction mode (CCM), it has been found that both fast-scale and low-frequency instabilities can occur in some selected parameter regions [11]–[14]. For the SSIPP operating with DCM boost stage and DCM (or CCM) forward stage, it has also been reported that fast-scale instability may take place if the system parameters are chosen inappropriately [15], [16]. It has also been shown previously that the low-frequency instability problem may worsen the harmonic distortion of the input current, whereas the fast-scale instability problem may impose higher current stresses on the switching devices. Thus, the study of instability in PFC converters has a practical motivation and results arising from such study will be useful for practical design considerations. Slow-scale and fast-scale instabilities were first used to describe low-frequency oscillation and period-doubling bifurcation of a voltage-mode buck converter operating in CCM, respectively [17]. In the study of simple dc-dc converters, we focus on a time scale which commensurates with the switching period. In PFC converters, however, an additional time scale that commensurates with the line period becomes equally important. In practice, the line frequency is much lower than the switching frequency. Thus, in PFC converters, instability may be considered under two time scales. First, fast-scale instability/bifurcation refers mainly to bifurcations emerging from the switching-frequency orbits, such as the usual period-doubling bifurcation at the switching frequency [13]–[16]. Second, bifurcations emerging from line-frequency orbits are referred to as line-frequency instability/bifurcation [11], [12]. In this paper, we report a totally different type of instability observed in the complete single-stage PFC power supply, in which both the PFC boost preregulator and the forward output regulator are originally designed to operate in DCM. The instability reported in this paper usually manifests itself as a local oscillation within a line cycle. Hence, the observed instability seems to be "faster" than line-frequency instability, but "slower" than fast-scale instability. To consist with the technical terms used in the context of dc-dc converters, the instability observed here is called slow-scale instability/bifurcation. Strictly speaking, the slow-scale instability/bifurcation may also cover line-frequency

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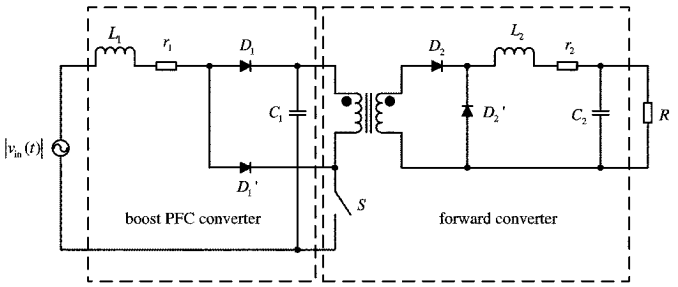

Fig. 1. SSIPP [3]. This circuit consists of a boost front-end PFC converter and a forward converter. Transformer isolation allows sharing of active switch by the two cascading stages [5], [6]. For the sake of simplicity, the core reset arrangement is not shown in this figure.

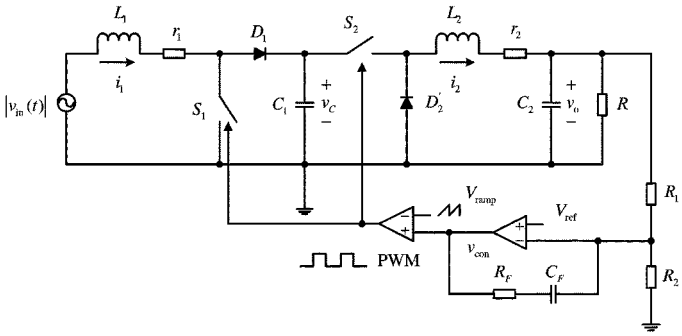

Fig. 2. Equivalent circuit model of the SSIPP under PI control.

instability/bifurcation mentioned above. However, in the study of PFC converters, we exclude line-frequency instability/bifurcation from slow-scale instability/bifurcation which only refers to bifurcation emerging from the low-frequency oscillation within the a line cycle.

We will present our main findings as follows. First, through "exact" cycle-by-cycle simulations, we will show that power factor can be drastically degraded when slow-scale instability occurs. This is very important in practice because it will seriously affect the performance of the SSIPP. We will then investigate the underlying mechanism of the degradation of power factor along with the occurrence of slow-scale instability by observing the operation mode of both the PFC boost preregulator and the forward output regulator. We find that the slow-scale instability is essentially caused by *border collision*, which involves alterations of operating mode within the line cycle. From the analysis, we can derive the boundary of normal operation in any suitably chosen parameter space. Finally, we will show some experimental results to verify our findings from simulations.

II. System Description

A. Operating Principle of SSIPP

Fig. 1 shows the simplified schematic of the SSIPP under study [3]. The system can be considered as a cascade connection of a boost converter and a forward converter. The two converters share the same active switch S. The duty cycle of switch S is used to regulate the output voltage via a voltage feedback loop. Moreover, by virtue of DCM operation, the boost preregulator can automatically achieve the PFC function.

The equivalent circuit model of the SSIPP under study is shown in Fig. 2. Here, a proportional-integral (PI) feedback

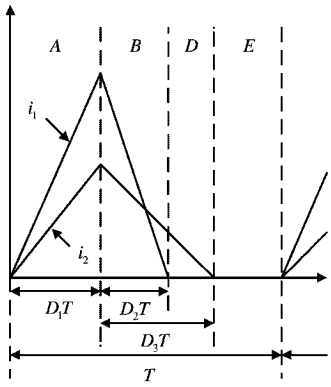

Fig. 3. Typical current waveforms of the SSIPP. Both the boost and the forward stages operate in DCM, and the corresponding equivalent circuit presents a sequence of switch states as "ABDE" in a switching cycle.

control loop is applied to synchronously drive the switches S_1 and S_2 via a pulsewidth-modulation (PWM) signal.[1] The PWM signal is generated by comparing the control voltage $v_{\rm con}$ and the ramp signal $V_{\rm ramp}$. The ramp signal is given by

$$V_{\rm ramp} = V_L + (V_U - V_L)\left(\frac{t}{T} \bmod 1\right) \tag{1}$$

where V_L and V_U are the lower and upper thresholds of the ramp, and T is the switching period. The switches are turned on when $v_{\rm con} > V_{\rm ramp}$, and turned off when $v_{\rm con} < V_{\rm ramp}$.

B. Exact State Equations

When both the boost and the forward stages operate in DCM, five switch states may appear during a switching cycle.

State A: S_1 and S_2 are on, D_1 and D_2' are off.
State B: S_1 and S_2 are off, D_1 and D_2' are on.
State C: S_1 and S_2 are off, D_1 is on and D_2' is off.
State D: S_1 and S_2 are off, D_1 is off and D_2' is on.
State E: S_1 and S_2 are off, D_1 and D_2' are off.

Generally, the sequence of switch states follow the order given above. However, State C and State D can not both appear in a switching cycle because exact synchronous switching of the diodes is not possible in practice. The typical current waveforms are illustrated in Fig. 3, in which State C does not exist as the forward stage has a relatively larger inductance. In addition, it should be noted that if the boost (forward) stage operates in CCM, State D (State C) and State E will not appear in the sequence of switch states. This must be taken care of in the cycle-by-cycle circuit simulations.

Now, we can give the exact state equation corresponding to each switch state as follows:

$$\dot{x} = \begin{cases} A_1 x + B_1, & \text{for state} A \\ A_2 x + B_2, & \text{for state} B \\ A_3 x + B_3, & \text{for state} C \\ A_4 x + B_4, & \text{for state} D \\ A_5 x + B_5, & \text{for state} E \end{cases} \tag{2}$$

where x is the state vector defined as

$$x = [i_1 v_C i_2 v_o v_{\rm con}]^T \tag{3}$$

[1]Different from the proportional control used in [15] and [16], PI control is employed in our study as it is more typical in industrial applications.

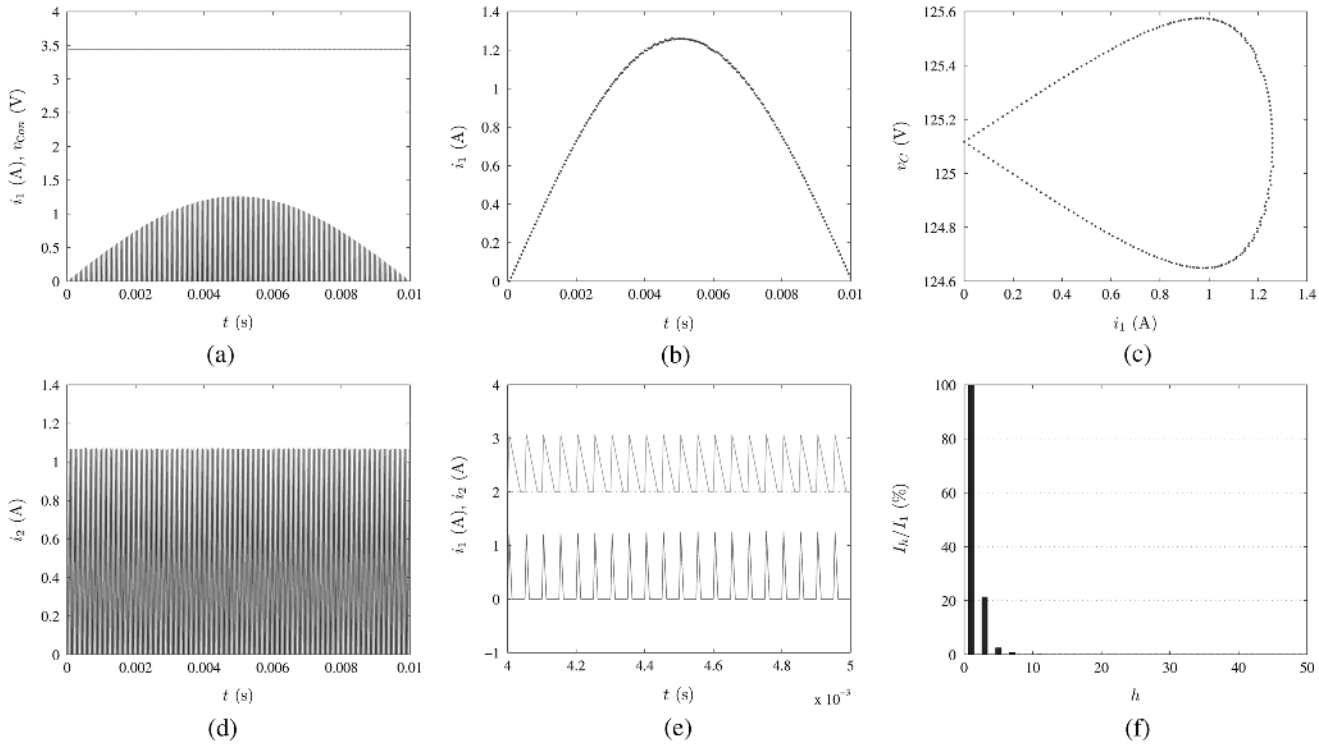

Fig. 4. Simulations for $R = 37.9\ \Omega$. (a) Waveforms of i_1 and $v_{\rm con}$. (b) Peak values of i_1. (c) Phase portrait of peak values of i_1 and v_C. (d) Waveform of i_2. (e) Enlarged waveforms of i_1 (lower) and i_2 (upper). (f) Harmonic spectrum of i_1.

and the system matrices As and Bs are given as

$$A_1 = \begin{bmatrix} -\frac{r_1}{L1} & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{C_1} & 0 & 0 \\ 0 & \frac{1}{L_2} & -\frac{r_2}{L_2} & -\frac{1}{L_2} & 0 \\ 0 & 0 & \frac{1}{C_2} & -\frac{1}{RC_2} & 0 \\ 0 & 0 & -\frac{K}{C_2} & \frac{K}{RC_2} - \frac{K}{\tau_F} & 0 \end{bmatrix} \tag{4}$$

$$A_2 = \begin{bmatrix} -\frac{r_1}{L1} & -\frac{1}{L_1} & 0 & 0 & 0 \\ \frac{1}{C_1} & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{r_2}{L_2} & -\frac{1}{L_2} & 0 \\ 0 & 0 & \frac{1}{C_2} & -\frac{1}{RC_2} & 0 \\ 0 & 0 & -\frac{K}{C_2} & \frac{K}{RC_2} - \frac{K}{\tau_F} & 0 \end{bmatrix} \tag{5}$$

$$A_3 = \begin{bmatrix} -\frac{r_1}{L1} & -\frac{1}{L_1} & 0 & 0 & 0 \\ \frac{1}{C_1} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{RC_2} & 0 \\ 0 & 0 & 0 & \frac{K}{RC_2} - \frac{K}{\tau_F} & 0 \end{bmatrix} \tag{6}$$

$$A_4 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{r_2}{L_2} & -\frac{1}{L_2} & 0 \\ 0 & 0 & \frac{1}{C_2} & -\frac{1}{RC_2} & 0 \\ 0 & 0 & -\frac{K}{C_2} & \frac{K}{RC_2} - \frac{K}{\tau_F} & 0 \end{bmatrix} \tag{7}$$

$$A_5 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{RC_2} & 0 \\ 0 & 0 & 0 & \frac{K}{RC_2} - \frac{K}{\tau_F} & 0 \end{bmatrix} \tag{8}$$

$$B_1 = B_2 = B_3 = \begin{bmatrix} \frac{|v_{\rm in}|}{L_1} \\ 0 \\ 0 \\ 0 \\ \frac{KV_{\rm ref}}{\tau_F}\left(1 + \frac{R_1}{R_2}\right) \end{bmatrix} \tag{9}$$

$$B_4 = B_5 = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ \frac{KV_{\rm ref}}{\tau_F}\left(1 + \frac{R_1}{R_2}\right) \end{bmatrix} \tag{10}$$

where $v_{\rm in}$ is the input sinusoidal voltage, $K = R_F/R_1$ is the dc gain of the PI controller, $\tau_F = R_F C_F$ is the time constant of the PI controller, and the other component symbols are as defined in Fig. 2.

III. Slow-Scale Instability From Circuit Simulations

In this section, we will present the observations of slow-scale instability of the SSIPP. Our simulation is based on the exact piecewise switched model described in the foregoing section. Since practicing engineers are usually interested in the performance of SSIPP as the output power varies, we will accordingly observe the dynamical behaviors as the output power is changed. In our study, we will only change the load resistor R and keep other circuit parameters fixed.[2] The circuit parameters used in our simulations are shown in Table I.

[2]The output power equals V_o^2/R, where $V_o = V_{\rm ref}(1 + R1/R2)$ is the expected regulated output voltage in the steady state.

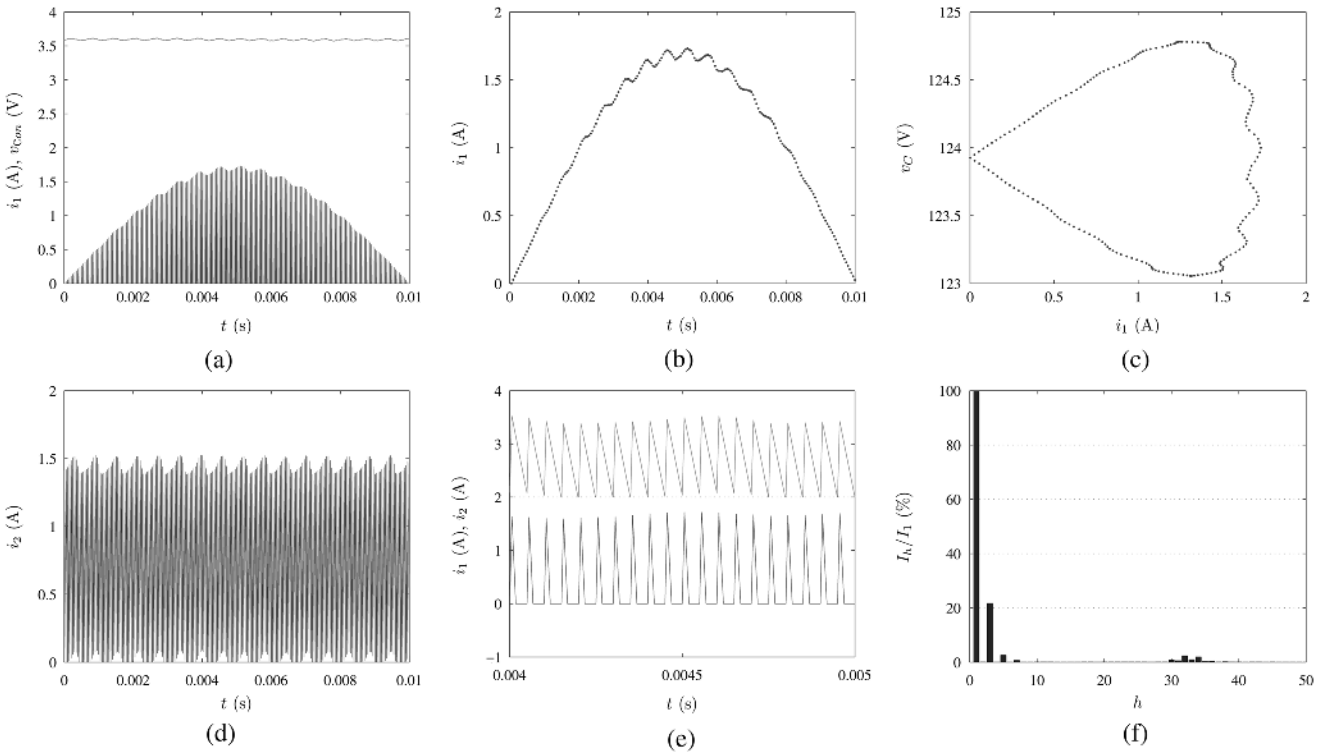

Fig. 5. Simulations for $R = 20.2\ \Omega$. (a) Waveforms of i_1 and $v_{\rm con}$. (b) Peak values of i_1. (c) Phase portrait of peak values of i_1 and v_C. (d) Waveform of i_2. (e) Enlarged waveforms of i_1 (lower) and i_2. (f) Harmonic spectrum of i_1.

TABLE I
CIRCUIT PARAMETERS USED IN SIMULATIONS

Circuit Component	Values
Switching Period T	50 μs
Input Voltage $v_{\rm in}$	60 V rms, 50 Hz
Inductance L_1, ESR r_1	300 μH, 0.01 Ω
Inductance L_2, ESR r_2	460 μH, 0.01 Ω
Capacitance C_1	200 μF
Capacitance C_2	47 μF
Load Resistor R	10 Ω-50 Ω
Reference Voltage $V_{\rm ref}$	1.5 V
V_L, V_U	3 V, 8 V
R_1, R_2	9 kΩ, 1 kΩ
DC Gain of Controller K	0.06
Time Constant of Controller τ_F	65 μs

A. Stable Operation

When the load resistor R is large, e.g., $37.9\ \Omega$ (i.e., the output power is 5.94 W), the SSIPP can work in stable operation. Fig. 4(a) shows the time-domain waveforms of i_1 and $v_{\rm con}$. In order to see the change in dynamical behavior clearly, we collect the sampled peak values for i_1 and the corresponding values for v_C during each switching period in the steady state. Fig. 4(b) shows the peak values of i_1 and Fig. 4(c) shows the phase portrait of the peak values of i_1 and v_C. To observe the operation mode of the inductor L_2, the time-domain waveform of i_2 is also given in Fig. 4(d). The enlargements of i_1 and i_2 are shown in Fig. 4(e), which clearly illustrate DCM operation of both i_1 and i_2.

Since the power factor is of practical importance in the SSIPP, we also calculate the total harmonic distortion (THD) using fast Fourier transform (FFT) [18]. Here, we make use of the function "fft" in Matlab environment, where the sampling frequency and the length of FFT are set to 2 MHz and 40000 points, respectively. In the calculation of FFT and THD, two points are worth mentioning.

1) In the calculation of FFT, the waveform of i_1 is purposely "un-rectified" such that its fundamental frequency equals the line frequency, i.e., 50 Hz.
2) In the calculation of THD, the frequency components higher than 10 kHz are ignored as a filter is always there to remove the switching ripples of the input current.

In our simulations, all FFT and THD calculations are obtained in the way described above.

Fig. 4(f) shows the harmonic spectrum of i_1. The power factor is 0.98, which is adequate for most practical applications.

B. Onset of Slow-Scale Instability

We now gradually decrease the load resistance to obtain a larger output power. When the load resistor R is adjusted to $20.2\ \Omega$ (i.e., the output power is 11.14 W), the slow-scale instability begins to develop with a very small amplitude of $v_{\rm con}$. Fig. 5(a) shows the time-domain waveforms of i_1 and $v_{\rm con}$. Fig. 5(b) and (c) also shows the distortion of the peak values of i_1. The time-domain waveform of i_2 is presented in Fig. 5(d) from which we observe CCM operation of i_2 in some time intervals. Fig. 5(e) shows the enlargements of i_1 and i_2, which illustrate DCM operation of i_1 and the appearance of CCM operation of i_2 in some time intervals. Nonetheless, the power factor still maintains to be as high as 0.97 since the small distortion of i_1 contributes little to the harmonic spectrum, as shown in Fig. 5(f).

The slow-scale instability occurs as the load resistance decreases. When the load resistor R reaches $18.6\ \Omega$ (i.e., the output power is 12.10 W), the oscillation of i_1 and $v_{\rm con}$ becomes significant, as shown in Fig. 6(a)–(c). Obviously, the magnitude of

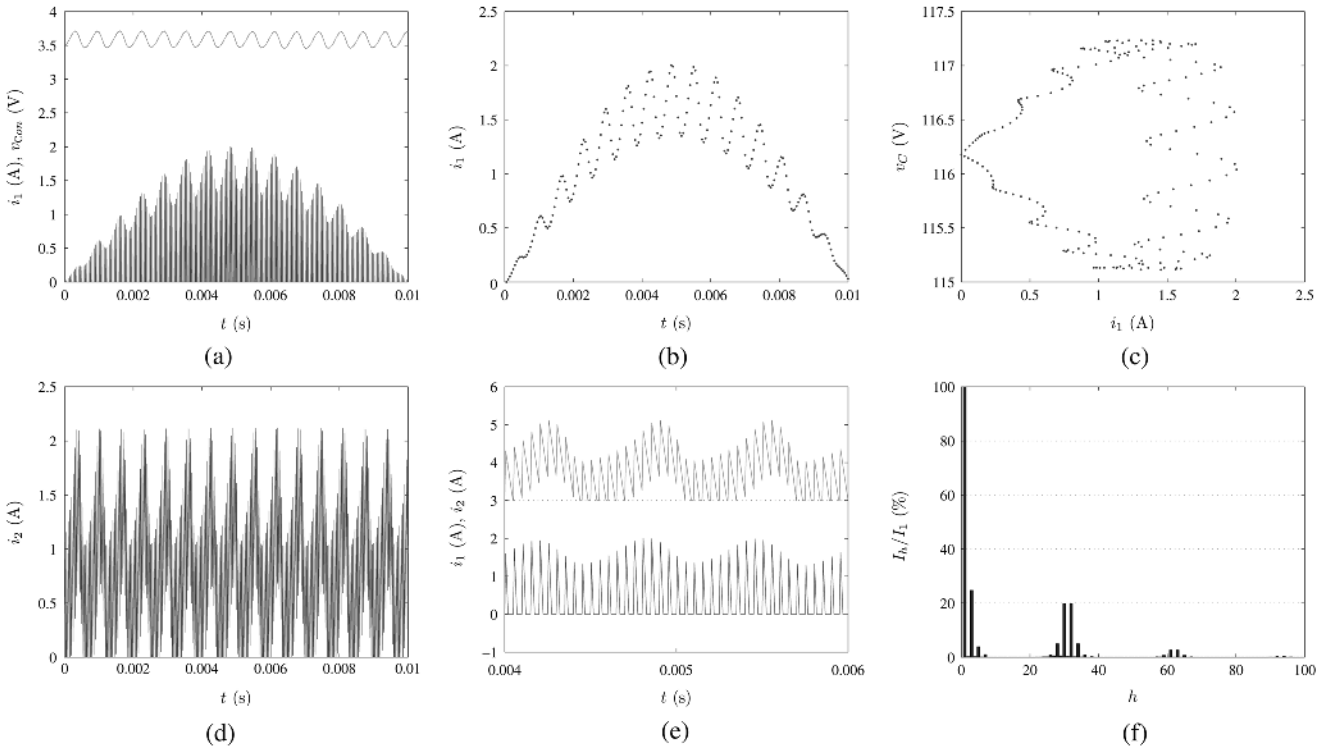

Fig. 6. Simulations for $R = 18.6\ \Omega$. (a) Waveforms of i_1 and $v_{\rm con}$. (b) Peak values of i_1. (c) Phase portrait of peak values of i_1 and v_C. (d) Waveform of i_2. (e) Enlarged waveforms of i_1 (lower) and i_2 (upper). (f) Harmonic spectrum of i_1.

the oscillation is larger than that for $R = 20.2\ \Omega$. Meanwhile, it can be readily recognized that there are approximately 31 oscillating periods included in a line cycle. Consequently, these local oscillations manifest as spectral spikes in the harmonic spectrum, as shown in Fig. 6(f), where the local oscillation around 31st harmonics can be clearly observed. As a result, the power factor decreases to 0.93. In addition, the time-domain waveform of i_2 is given in Fig. 6(d) and the enlargements of i_1 and i_2 are shown in Fig. 6(e), which clearly illustrate DCM operation of i_1 and the appearance of CCM operation of i_2 in some time intervals.

C. "Deep" Slow-Scale Instability

When the load resistance is decreased to $13.9\ \Omega$ (i.e., the output power is 16.19 W), the slow-scale instability becomes quite serious. As shown in Fig. 7(a)–(c), we can observe that the system oscillates with a very large amplitude. Consequently, the power factor falls drastically to 0.73. Obviously, the PFC function has failed completely. The time-domain waveform of i_2 is given in Fig. 7(d) and the enlargements of i_1 and i_2 are shown in Fig. 7(e), which clearly illustrate the entry into CCM operation of both i_1 and i_2 in some time intervals. Additionally, Fig. 7(f) shows the harmonic spectrum of i_1, where a large amount of harmonics is observed.

IV. Effect Of Slow-Scale Instability on Power Factor

In this section, we will look more closely at the effects of slow-scale instability on power factor. Fig. 8 shows the variation of the power factor as the load resistance decreases. To clearly investigate the influence of the slow-scale instability on the circuit operation, we specifically observe the variation of operating mode as the load resistance changes. For brevity, we denote the operating mode in which both the PFC boost preregulator and forward output regulator operate in DCM by DCM–DCM. Likewise, we denote the operating mode in which the PFC boost preregulator operates in DCM and the forward output regulator operates in mixed-conduction mode (MCM)[3] by DCM–MCM. Similarly, MCM–MCM means that both the PFC boost preregulator and the forward output regulator operate in MCM.

As mentioned in the previous section, the slow-scale instability appears around $R = 20.2\ \Omega$. From Fig. 8, we can see that the power factor begins to drop when the load resistance decreases below this critical point. Meanwhile, the operating mode is changed from DCM–DCM to DCM–MCM, which implies the occurrence of border collision due to the variation of operating mode of the system [19]. The power factor will further decrease as the load resistance continues to decrease. We can also observe another border collision which occurs around $R = 13.9\ \Omega$ with the operation mode changed from DCM–MCM to MCM–MCM. Clearly, the power factor is greatly affected by the load resistance (or the output power as the output voltage is fixed here) due to the occurrence of slow-scale instabilities.

V. Border Collision: Cause of Slow-Scale Instability

We have pointed out the occurrence of border collision when the load resistance decreases. Now, we will explain how it leads to slow-scale instability and the corresponding drop of the power factor. Moreover, we will also discuss some details on the border collision observed here.

[3]When the converter operates in MCM, both DCM and CCM exist in the line cycle.

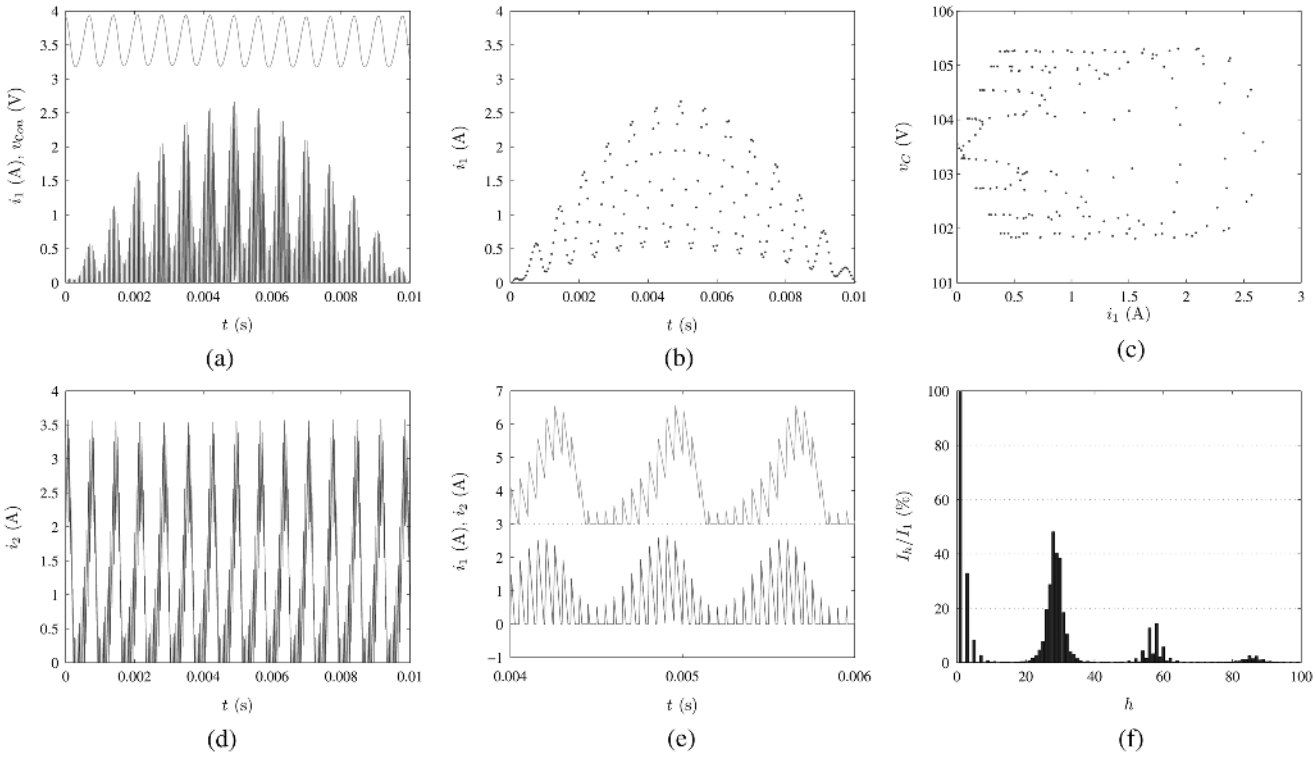

Fig. 7. Simulations for $R = 13.9\ \Omega$. (a) Waveforms of i_1 and $v_{\rm con}$. (b) Peak values of i_1. (c) Phase portrait of peak values of i_1 and v_C. (d) Waveform of i_2. (e) Enlarged waveforms of i_1 (lower) and i_2 (upper). (f) Harmonic spectrum of i_1.

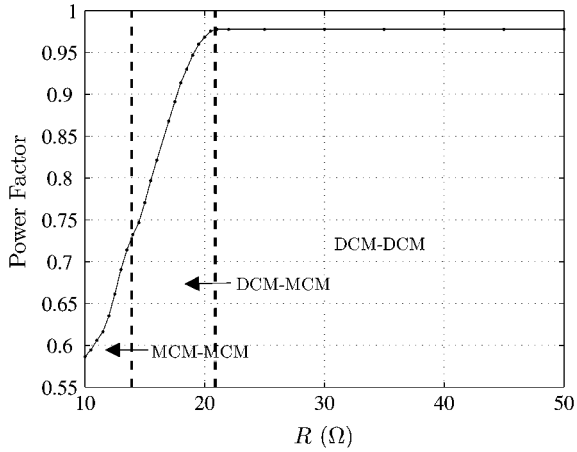

Fig. 8. Power factor of the SSIPP as the load resistance varies.

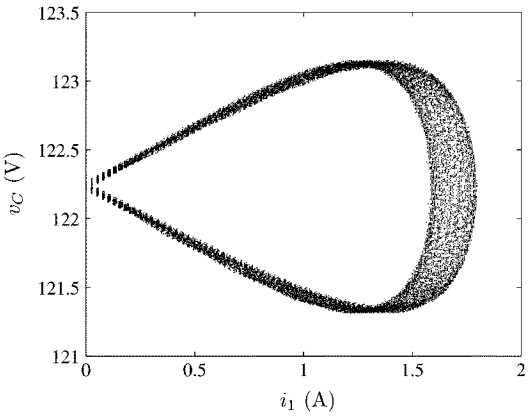

Fig. 9. Phase portrait of peak values of i_1 and v_C in many line cycles for $R = 20.2\ \Omega$.

According to the operating mechanism of SSIPP, when the boost PFC preregulator operates in DCM, we have

$$I_{\text{peak},i} = \frac{v_{\text{in}}}{L_1} d_i \tag{11}$$

where $I_{\text{peak},i}$ and d_i are the peak value of input current and the duty cycle in the ith switching period for a half line cycle, respectively. In the normal operation, the control voltage $v_{\rm con}$ within a half line cycle is approximately constant, as shown previously in Fig. 4. This implies that the duty cycle almost remains the same within a half line cycle since the duty cycle is determined by the intersection of the control voltage $v_{\rm con}$ and the ramp signal $V_{\rm ramp}$. Thus, from (11), the peak value of the input current can well track the variation of the input voltage, which guarantees unity power factor.

In our study, the forward output regulator is also designed to operate in DCM. From the equivalent circuit given in Fig. 2, the input of the forward output regulator is the output of the boost PFC preregulator, i.e., the voltage v_C across the storage capacitor C_1. Usually, v_C is only crudely regulated by the boost PFC preregulator, and thus can be considered as a dc voltage V_C superposed by a small ripple. If the capacitance of C_1 is sufficiently large, the ripple is negligible and v_C at steady state is approximately the dc voltage V_C. In Redl *et al.* [3], it has been shown that V_C is independent of the load variation for SSIPP operating in DCM–DCM. An equation for V_C, which can be solved numerically, was given in [3]. For the system considered

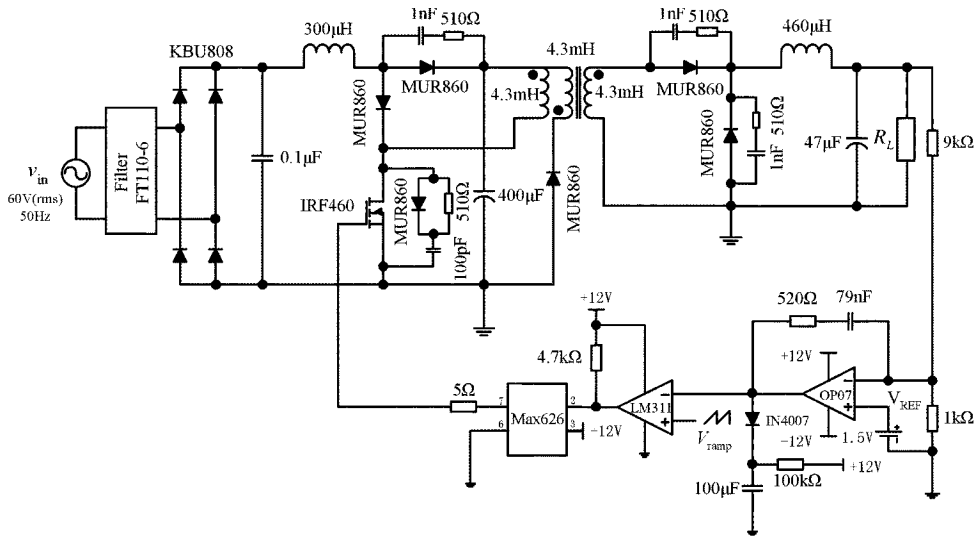

Fig. 10. Full schematic diagram of experimental circuit.

in our paper, a similar equation can be obtained and is given by (see Appendix for detailed derivation)

$$\int_0^{T_L/2} \frac{v_{\rm in}^2}{V_C - v_{\rm in}} dt = \frac{L_1 T_L}{2L_2}(V_C - V_o) \tag{12}$$

where T_L is the line period.[4]

It is important to point out that the DCM operation of the forward output regulator is only limited to the specific parameter regions. In the steady state, if we ignore the small ripple of v_C, the forward output regulator can be approximately regarded as a buck converter operating in DCM with a dc input voltage V_C. Hence, the inequality [24]

$$\frac{1-M}{2} > \frac{L_2}{RT} \tag{13}$$

must be satisfied to ensure the DCM operation. Here, M is the ratio of the steady-state output voltage V_o to input voltage V_C for the forward output regulator. Clearly, M is a constant since V_C is independent of load variation.

In the normal operation, when the load resistor R is decreased, i.e., the output power is increased, this inequality may be violated for some specific choice of parameter region. When it happens, the DCM operation of the forward output regulator cannot be maintained, and the MCM operation emerges. This is the so-called border collision which has been widely observed in dc-dc converters [19]. Specifically, this border collision is ignited by the change of the state-space dimension, which has been reported in the dc-dc boost converter [20], [21]. Here, the border collision results in a local oscillation of the control voltage within the line cycle, as shown earlier in Figs. 5–7. Therefore, the duty cycle d_i in a half line cycle will also oscillate, which leads to the oscillation of $I_{{\rm peak},i}$ as given in (11). Consequently, in this case, the peak value of the input current $I_{{\rm peak},i}$ cannot correctly track the variation of the input voltage, causing serious degradation of the power factor.

Unlike simple dc-dc converters, the SSIPP under study consists of two stages and has a time-varying input. Thus, it would be rather complicated to study the specific type of border collision via the analytical means proposed in Banerjee *et al.* [20], [22]. However, we observe that the border collision shown here is qualitatively similar to that studied in [23], where the border collision gives rise to the quasi-periodicity. In our study here, the periodic orbit also bifurcates to a quasi-periodic one as the system shifts its operation from DCM–DCM to DCM–MCM. Fig. 9 shows the phase portrait of peak values of i_1 and v_C in many line cycles for $R = 20.2\ \Omega$,[5] which may better illustrate the appearance of quasi-periodicity. As stated in [23], we further conjecture that the discrete map of the system (if derived) undergoes a nonsmooth Neimark–Sacker bifurcation, which means that a complex conjugate pair of eigenvalues jump discontinuously out of the unit circle when border collision occurs.

Remarks on Practical Design Previous studies on SSIPP have mainly focused on the steady-state design and control aspects. The detailed dynamical behavior as well as its potential adverse influence on the system's performance have seldom been investigated. Specifically, some conventional viewpoints can be re-examined in the light of this study. For instance, it has been considered that slipping into CCM at or close to full load for output regulator is not necessarily harmful [3]. However, it is clearly seen here that the change of operation mode as the load varies can result in slow-scale instability which will lead to degradation of PFC performance. Thus, it is desirable, by design, to make the system work in DCM–DCM in the whole load range such that slow-scale instability can be completely avoided.

VI. Experimental Verifications

To verify the observed slow-scale instability, an experimental circuit prototype of the SSIPP under study has been built. Fig. 10 shows the full schematic diagram of the experimental circuit with detailed specifications indicated. It should be noted that the dc gain K and time constant τ_F of the PI controller are found by direct measurement to be consistent with those used in the simulations.

[4]The SSIPP in [3] actually uses a flyback stage as the regulating stage, whereas a forward stage is used in our study here.

[5]To clearly illustrate the oscillation, all phase portraits in Section III are plotted only for a half line cycle

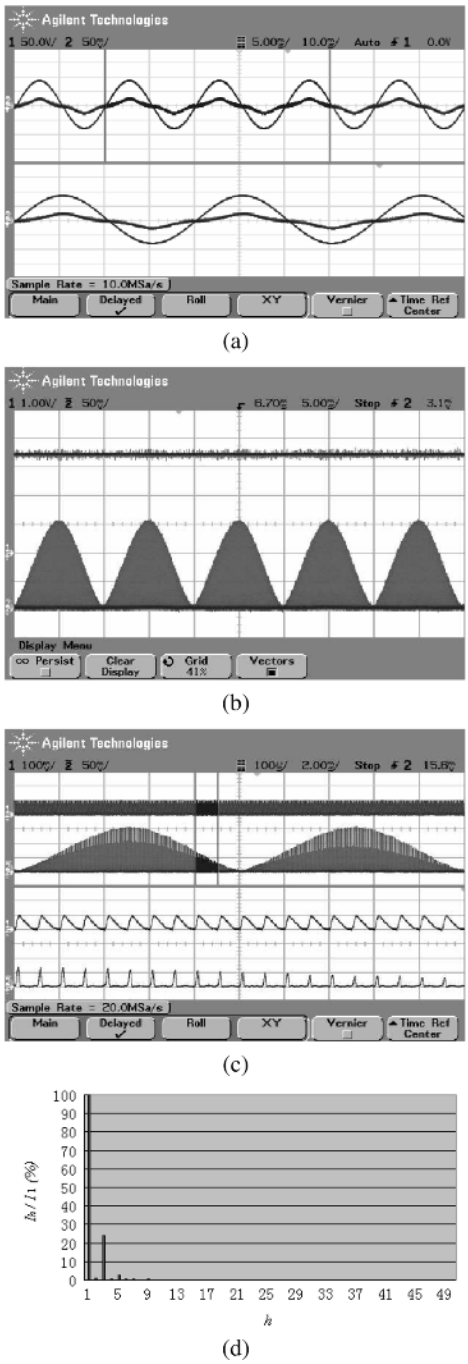

Fig. 11. Measured waveforms for $R = 37.9\ \Omega$. (a) Line voltage (50 V/div) and current (50 mV/div), time scale: 10 ms/div. (b) Control voltage (upper trace: 1 V/div) and current of L_1 (lower trace: 50 mV/div), time scale: 5 ms/div. (c) Current of L_1 (lower trace: 50 mV/div) and current of L_2 (upper trace: 100 mV/div), time scale: 2 ms/div. (d) Harmonic spectrum of line current. The lower part of (a) and (c) also shows the enlargement of the selected waveforms.

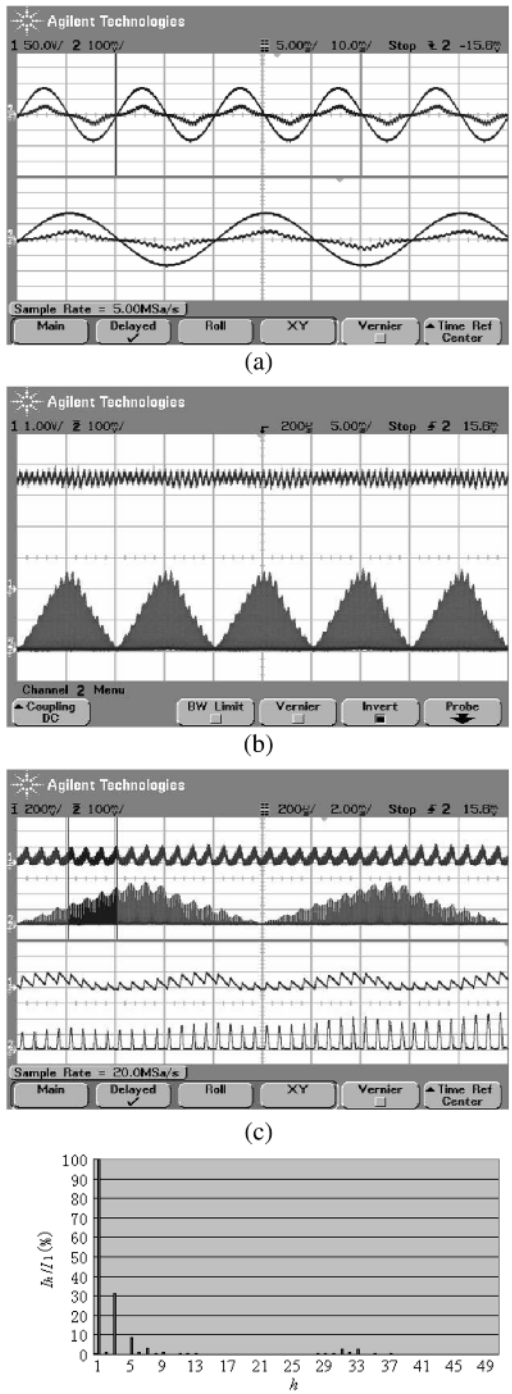

Fig. 12. Measured waveforms for $R = 20.2\ \Omega$. (a) Line voltage (50 V/div) and current (100 mV/div), time scale: 10 ms/div. (b) Control voltage (upper trace: 1 V/div) and current of L_1 (lower trace: 100 mV/div), time scale: 5 ms/div. (c) Current of L_1 (lower trace: 100 mV/div) and current of L_2 (upper trace: 200 mV/div), time scale: 2 ms/div. (d) Harmonic spectrum of line current. The lower part of (a) and (c) also shows the enlargement of the selected waveforms.

In our experiment, digital oscilloscope Agilent 54622D and current probe Tektronix A622 (100 mV/A) are used to capture the measured waveforms. Also, power analyzer module Tektronix TPS2PWR1 is employed to measure the harmonics of line current up to the 50th order.

Fig. 11 shows the measured waveforms for $R = 37.9\ \Omega$, where the system works in stable operation. Fig. 11(a) shows the line voltage and current waveforms. It can be observed that there is no distortion in the line current. Fig. 11(b) shows the control voltage and the current of L_1. It can be clearly observed that the control voltage is approximately constant and there is no oscillation in the current of L_1. Fig. 11(c) shows the currents in both L_1 and L_2, from which we observe that the system operates in DCM–DCM operation mode. Fig. 11(d) shows the spectrum of the line current.

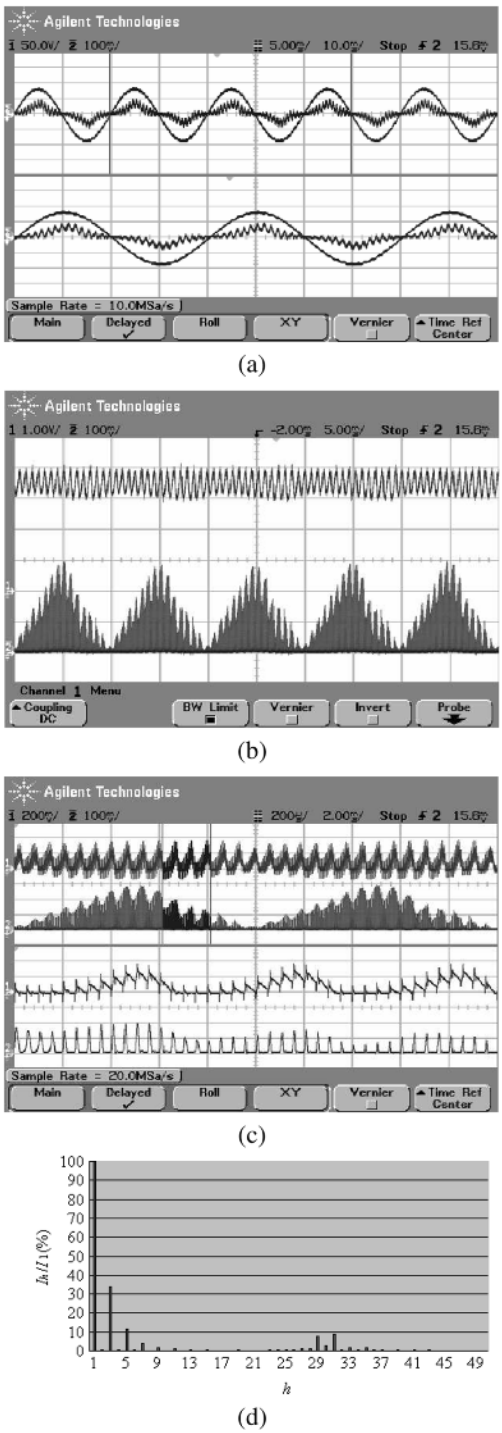

Fig. 13. Measured waveforms for $R = 18.6\ \Omega$. (a) Line voltage (50 V/div) and current (100 mV/div), time scale: 10 ms/div. (b) control voltage (upper trace: 1 V/div) and current of L_1 (lower trace: 100 mV/div), time scale: 5 ms/div. (c) Current of L_1 (lower trace: 100 mV/div) and current of L_2 (upper trace: 200 mV/div), time scale: 2 ms/div. (d) Harmonic spectrum of line current. The lower part of (a) and (c) also shows the enlargement of the selected waveforms.

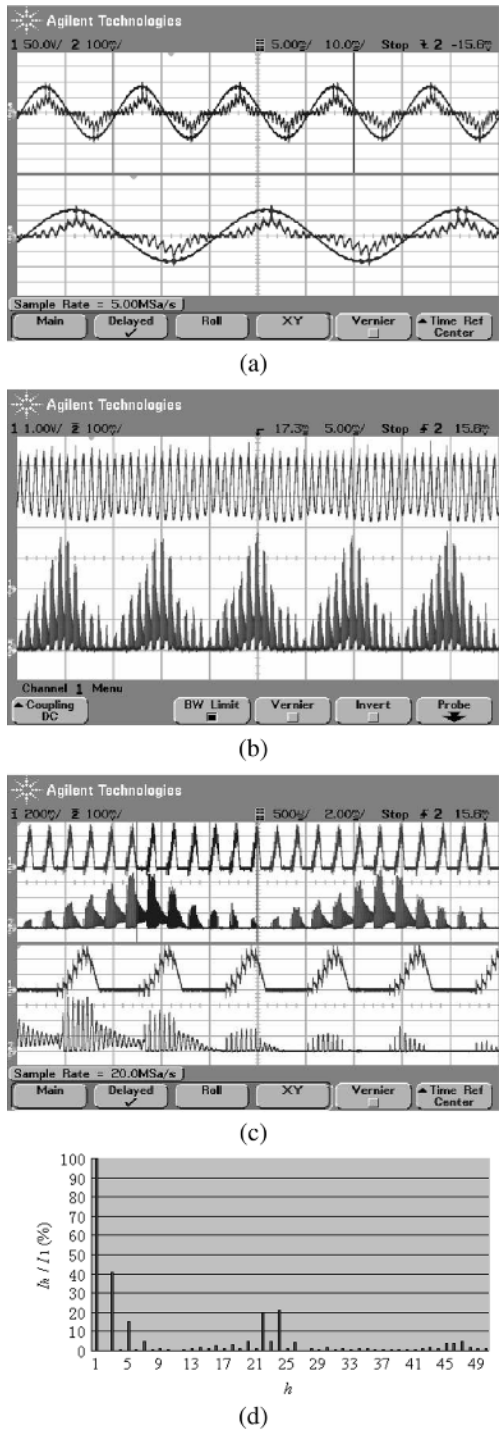

Fig. 14. Measured waveforms for $R = 13.9\ \Omega$. (a) Line voltage (50 V/div) and current (100 mV/div), time scale: 10 ms/div. (b) control voltage (upper trace: 1 V/div) and current of L_1 (lower trace: 100 mV/div), time scale: 5 ms/div. (c) current of L_1 (lower trace: 100 mV/div) and current of L_2 (upper trace: 200 mV/div), time scale: 2 ms/div. (d) harmonic spectrum of line current. The lower part of (a) and (c) also shows the enlargement of the selected waveforms.

Fig. 12 shows the measured waveforms for $R = 20.2\ \Omega$, where slow-scale instability just occurs. Fig. 12(a) shows the line voltage and current waveforms, from which we observe very small distortion in the line current. Fig. 12(b) shows the control voltage and the current of L_1. Here, the slight oscillation of the control voltage and the current in L_1 is clearly evident. Fig. 12(c) shows the currents in both L_1 and L_2. We observe that some part of the current in L_2 enters CCM, implying that the system operates in DCM–MCM operation mode. Fig. 12(d) shows the spectrum of the line current, from which we observe small spectral components around the 31st harmonics.

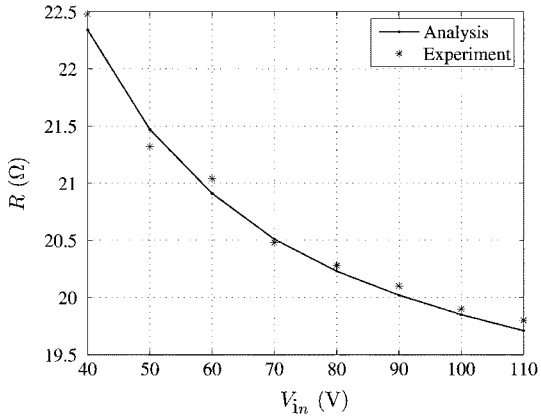

Fig. 15. Measured stability boundary in the parameter space of input voltage $V_{\rm in}$ (rms of $v_{\rm in}$) versus load resistance R.

Fig. 13 shows the measured waveforms for $R = 18.6\ \Omega$, where slow-scale instability appears with a larger oscillation amplitude. Fig. 13(a) gives the line voltage and current waveforms, which show large distortion in the line current. Fig. 13(b) shows the control voltage and the current in L_1, the oscillating amplitudes of which are obviously larger than those for $R = 20.2\ \Omega$. Fig. 13(c) shows the currents in both L_1 and L_2. We can readily observe that the current in L_2 operates in MCM and the system works in DCM–MCM operation mode. Fig. 13(d) shows the spectrum of the line current. We can see that there are some spectral components around the 31st harmonics, with a larger magnitude than those for $R = 20.2\ \Omega$ shown earlier in Fig. 12(d).

Fig. 14 presents the measured waveforms for $R = 13.9\ \Omega$, where slow-scale instability seriously develops. Fig. 14(a) gives the line voltage and current waveforms, showing significant distortion in the line current compared to that for $R = 18.6\ \Omega$ shown earlier in Fig. 13(a).Fig. 14(b) shows the control voltage and the current of L_1, which have a more severe oscillation. Fig. 14(c) shows the currents in both L_1 and L_2, from which CCM operation of the current in L_1 can be observed in some time intervals. Thus, the system works in MCM–MCM operation mode. Fig. 14(d) shows the spectrum of the line current. We observe spectral components around the 23rd harmonics having larger amplitudes than those for $R = 18.6\ \Omega$ around the 31st harmonics.

Comparing the results from simulations and experiments, we can conclude that they agree very well with each other qualitatively. The discrepancies can be attributed to the presence of parasitics in the experimental setup, measurement errors in K and τ_F, and the removal of harmonics of i_1 by filtering in the experimental circuits.

Finally, the boundaries of slow-scale instability at different input voltages are found. For convenience in making comparison, we use (12) and (13) to obtain the operation boundary within which slow-scale instability does not occur. Fig. 15 shows such a stability boundary in the parameter space of input voltage versus load resistance. As shown in Fig. 15, the experimental results agree very well with the analytical results. This verifies the validity of (12) and (13) in locating the normal operating region.

VII. Conclusion

PFC has become a primary concern for switching power supplies. For low power applications, the SSIPP is a cost effective solution which is widely used in practical applications. Although the steady-state design and control of the SSIPP have been thoroughly studied for many years, the detailed dynamics of this system, so far, has not been completely explored or clearly understood. In this paper, the slow-scale instability of an SSIPP operating in DCM–DCM has been reported. We have reported the results from "exact" cycle-by-cycle circuit simulations, and have discussed the effects of the slow-scale instability on power factor as the load resistance decreases. Moreover, it has been found that such instability is essentially caused by the so-called border collision. It is further shown that the border collision observed here is effectively a nonsmooth Neimark–Sacker bifurcation. By considering the transition between operation modes, the analytical expressions that define the normal operation boundary have been derived. Finally, an experimental circuit prototype has been built to verify the observations made from simulations. Since the slow-scale instability can greatly affect power factor and harmonic distortion, the results obtained here will be useful to the design of single-stage PFC power supplies.

Appendix
Derivation of Equation for Calculating V_c

In the steady state, the voltage V_C across the storage capacitor can be determined by equating the energy absorbed from the ac line during a half line cycle with the energy delivered to the load during the same half line cycle. Thus, the energy equality can be written as

$$\int_0^{T_{\rm L}/2} v_{\rm in} i_{\rm in} dt = \frac{1}{2} V_o I_o T_{\rm L} \tag{14}$$

where $i_{\rm in}$ is the input current from the ac line and I_o is the output current upon the load at steady state. Since $i_{\rm in} = i_1$, the above equation can be re-written as

$$\int_0^{T_{\rm L}/2} v_{\rm in} i_1 dt = \frac{1}{2} V_o I_o T_{\rm L}. \tag{15}$$

For brevity, we denote the on time of switch S, diode D_1 and D_2' by D_1T, D_2T and D_3T, respectively. By inspection of the waveforms shown in Fig. 3, D_2 and D_3 can be represented by D_1 as follows:

$$D_2 = \frac{v_{\rm in}}{V_C - v_{\rm in}} D_1 \tag{16}$$

$$D_3 = \frac{V_C - V_o}{V_o} D_1. \tag{17}$$

Furthermore, the averaged i_1 over the switching cycle is given by

$$\overline{i_1} = \frac{T}{2L_1} D_1 (D_1 + D_2) v_{\rm in} \tag{18}$$

$$= \frac{T D_1^2}{2L_1} \frac{v_{\rm in} V_C}{V_C - v_{\rm in}}. \tag{19}$$

Since $T \ll T_{\rm L}$ for most practical applications, we have

$$\int_0^{T_{\rm L}/2} v_{\rm in} i_1 dt \approx \int_0^{T_{\rm L}/2} v_{\rm in} \overline{i_1} dt \tag{20}$$

$$= \frac{V_C T D_1^2}{2L_1} \int_0^{T_{\rm L}/2} \frac{v_{\rm in}^2}{V_C - v_{\rm in}} dt. \tag{21}$$

Now, consider the charge balance on the forward output regulator, i.e.,

$$\frac{D_1+D_3}{2}T\frac{V_C-V_o}{L_2}D_1T=I_oT. \tag{22}$$

Substituting (17) into the above equation, I_o can be obtained as

$$I_o=\frac{TV_CD_1^2}{2L_2V_o}(V_C-V_o). \tag{23}$$

Hence, substituting both (21) and (22) into (15) yields

$$\int_0^{T_L/2}\frac{v_{\rm in}^2}{V_C-v_{\rm in}}dt=\frac{L_1T_L}{2L_2}(V_C-V_o) \tag{24}$$

from which V_C can be numerically obtained.

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