IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received February 14, 2022, accepted March 10, 2022, date of publication March 14, 2022, date of current version March 22, 2022.

Digital Object Identifier 10.1109/ACCESS.2022.3159476

Faster Convergence Controller With Distorted Grid Conditions for Photovoltaic Grid Following Inverter System

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This work was supported in part by the Visvesvaraya Ph.D. Scheme, Ministry of Electronics and Information Technology (MeitY), Government of India, under Award MEITY-PHD-2533; in part by Khalifa University under Award KKJRC-2019-Trans2; and in part by the Advanced Technology Research Council ASPIRE Virtual Research Institute (VRI) Program, Abu Dhabi, United Arab Emirates, under Award VRI20-07.

ABSTRACT The hysteresis current controller (HCC) for grid following inverter (GFI) system with *LCL*-filter is a well-known controller for its robustness, fast reference tracking, better dynamics, and easier implementation compared to other controllers. However, HCC behaves differently while integrating such a system with solar photovoltaics (PV). The PV-based GFI system requires fast convergence while transferring maximum power from PV to the grid at minimum converter losses through GFI. This paper therefore proposes a modified double-band HCC (MDBHCC) with proportional resonant (PR) controller for single-phase PV integrated GFI system with LCL-filter. The proposed algorithm implements a unipolar symmetrical PWM strategy for reducing inverter switching losses through a sequential logic with an adaptive clock. It improves the variation in switching frequency and limits the maximum switching frequency of HCC while enhancing the total harmonic distortion (THD) of the injected current into the grid at the point of common coupling. To alleviate the power quality problem and achieve zero steady state error, the proposed MDBHCC with PR control operates at lesser % THD. Simulation and experimental results are presented, with a significant decrease in switching frequency and an improvement in grid current harmonics at both steady-state and dynamic conditions.

INDEX TERMS GFI, hysteresis current control, LCL filter, power quality improvement, total harmonic distortion.

I. INTRODUCTION

Improvement in power electronic technology creates the way for the renewable energy source (RES) to raise its contribution in distributed power generation (DPG). The power transmitted towards the power grid needs a quality current demand from the photovoltaic (PV) based DPG unit [1], [2]. However, due to the random and stochastic character of PV based DPG structure, the regulation of the grid following inverter (GFI) becomes an enacting task in terms of the grid power injection [3]. Thus, a fast and effective control algorithm is desirable for stable operation of PV-based GFI with grid regulation.

The associate editor coordinating the review of this manuscript and approving it for publication was Gab-Su Seo.

1) LITERATURE REVIEW

The PV-based GFI power conditioning stage consists of two-stage converters. However, it introduces losses and reduces the system efficiency [4]. A single-stage PV-based GFI systems are becoming more popular to reduce costs and improve system efficiency. The single-stage system, on the other hand, faces difficulties in designing a control algorithm capable of achieving high power quality while transferring maximum

power into the grid [5]. The control algorithm in a single-stage PV-based GFI must take the following factors into account; 1) Operate at the maximum PowerPoint (MPP) with a sudden change in solar irradiance. 2) Maintain stable DC-link voltage regulation while transferring maximum power and minimizing the effect of double line frequency to reduce current harmonics. 3) Ensure better power quality and system protection during voltage sag and load changes [6]. 4) Integrate filtering and damping techniques to achieve high-quality power and mitigate resonance. Due to the high frequency GFI operation, the power pumped into the grid has more harmonic elements, causing voltage oscillations, transmission line losses, and grid instability. To enhance the quality of power injected to the grid, GFI with LCL-filters are primarily utilized [7], [8]. The steady-state errors caused by resonance at the lower grid harmonics are the deciding factor for designing an LCL-filter. An active damping approach instead of passive damping is widely used in the industrial sector to dampen the lower grid resonance, which increases the productivity of GFI. An active damping method that implements virtual resistance in the control algorithm are mentioned in [9], [10]. Numerous convoluted linear and nonlinear controllers for GFI, such as hysteresis current control (HCC), sliding mode control (SMC), and model predictive control (MPC), have been studied recently in the literature [11]–[14]. However, a major concern is the increased inverter switching frequency and the generation of variable switching frequency (VSF) leading to the productivity loss of the above-mentioned controllers on GFI [11], [12]. Additionally, SMC and MPC are computationally more complex in comparison to HCC [12]–[14]. Concerning HCC, the low current total harmonic distortion (THD) was derived through regulating the inverter current within the predetermined hysteresis band (HB) [15], [16]. HCC enables fast dynamic performance, easy implementation, and intrinsic overcurrent protection that does not require system parameter information [17]–[19].

Out of several HCC schemes, single-band HCC (SBHCC) and double-band HCC (DBHCC) are mostly popular [20], [21]. SBHCC operated three-phase GFI with LCL-filter is presented in [20], which utilizes a bipolar pulse width modulation (PWM) scheme. It results in the maximum switching frequency during the zero crossing of the reference current in case of the small hysteresis band [21]. Moreover, this creates sampling problems because of the larger fluctuation in the switching frequency [22]. For minimizing the switching frequency, a DBHCC (double band HCC) was recommended towards the GFI system [23], [24]. Out of very few literature, [25], [26] demonstrates the effectiveness of DBHCC for the single-phase GFI system with LCL-filter. Another hybrid DBHCC was discussed in the literature [27] for minimizing the harmonics existing in the single-phase GFI system accompanied by LCL-filter. The DBHCC scheme is also proposed in the literature to reduce the chattering phenomenon in the SMC with respect to single-phase GFI system [28]. A three-level HCC mentioned in the literature [22] minimizes the switching frequency sampling problem in the GFI systems with LCL-filter. A sizable increment in the current THD is noticed during zero-crossing with three-level HCC. A flexible HCC mentioned in [29] was proposed for the three-phase SiC-based GFI system accompanied by LCL-filter to reduce the range of switching frequency variation. However, the operating switching frequency in such cases remains higher. In [30], [31], HCC is applied for two-stage PV integrated system for transferring power. However, DC-link balancing and improving power quality are a major concern addressed for multilevel inverters. A power flow control approach with fast convergence controller is discussed in [32] under changing atmospheric conditions. However, the effect of high switching frequency on the inverter performance and efficiency is not addressed. In PV-based GFI system, to extract the maximum power from PV while maintaining a stable DC-link, an optimum proportional integral (PI) control with harmonics filter is essential [33]. Moreover, for a stable operation with changes in atmospheric conditions and grid disturbances, a robust and resilient current controller is forbidden [34].

2) MOTIVATION AND OBJECTIVES

Despite the fact that HCC is the simplest method available in the literature, the recent study lacks implementation and analysis. As a result, the following objectives are investigated in this paper.

- VSF leads to improper design of LCL-filter with resonance elimination capability [15]. Thus, limiting the switching frequency band within the variable switching frequency regulation is crucial. This can be achieved through designing an LCL-filter with active damping and proportional resonance (PR) control.
- VSF within a specified hysteresis band is a major concern for HCC operated PV-based GFI systems, as it leads to increased switching power loss in GFI when the current quality improves. Hence, a DBHCC scheme with VSF minimization needs to be investigated instead of other HCC methods available in literature.
- Effective utilization of PV power is possible at maximum power extraction while having a stable DC-link during changes in atmospheric conditions and grid disturbance. Moreover, an optimum DC-link reduces the converter power loss.
- A robust and fast convergence controller is needed for single-stage PV-based GFI systems, as increasing the efficiency of the overall system is essential while maintaining grid regulation.
- During PV integration through GFI, a modified DBHCC method must be investigated to meet the harsh demand of the low current THD and better power quality at reduced VSF, which minimize the converter power loss.

3) CONTRIBUTIONS AND PAPER ORGANIZATION

This paper involves the modified DBHCC (MDBHCC) method that comes up with relatively small fluctuations in

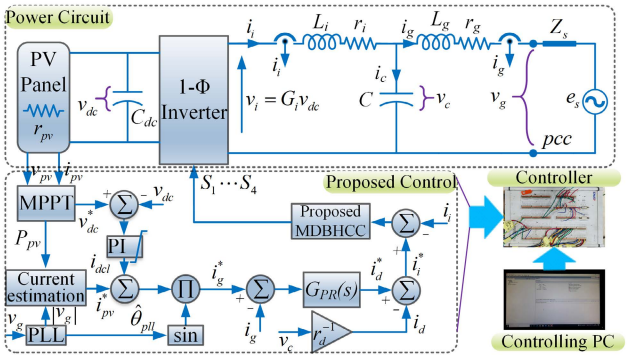


FIGURE 1. Single-phase GFI with LCL-filter control with active damping.

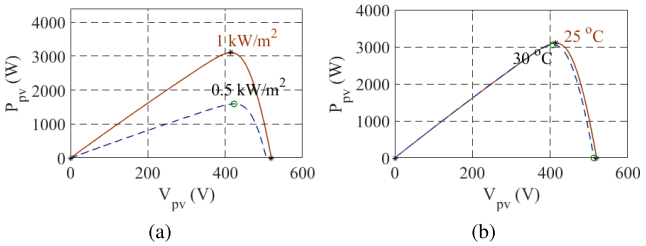


FIGURE 2. PV characteristic curve with (a) varied irradiance at 25° *C* (b) varied temperature at 1000 W/m^2.

the switching frequency, meanwhile offering superior output current quality at the cost of minimized switching frequency. The key contributions of this paper are listed as follows.

- Modelling of GFI with PV accompanied by the LCL-filter is discussed in terms of time constants. A design methodology for LCL-filter through the determination of resonance frequency is investigated, considering the impact of VSF.
- An effective PI-based power control method to extract the maximum power from PV array and provides fast convergence that helps to obtain the optimum DC-link and reduces the converter power loss.
- The suggested modified DBHCC uses an adaptive clock-based sequential logic algorithm that enhances the switching frequency without making any adjustment to the HB. The MDBHCC enhances the injected current harmonics through minimizing the switching frequency oscillations at reduced switching frequency.
- The effectiveness of the PV-based GFI performance based on % THD, and the average switching frequency (ASF) at a wide range of hysteresis bands is studied.
- The performance assessment along with the comparison of the suggested method accompanied by the DBHCC scheme is verified with the help of the experiment.

Section II describes the modelling of GFI with LCL-filter design through proper switching frequency selection. A detailed DBHCC control methodology is available in Section III. The experimental prototype description along with results and discussions are provided in Section IV. Finally, Section V concludes the proposed findings.

II. GFI SYSTEM MODELLING AND DESIGN CONSIDERATIONS

A. PV-GFI SYSTEM DESCRIPTION

A PV panel with single-phase GFI system through an LCL-filter followed by a source impedance Z_s ($= 0.01 + j0.047$) is interconnected to the single-phase grid, as presented in Fig. 1. Let p_{pv}, v_{pv} and i_{pv} are the PV power, voltage, and current, respectively. Fig. 2 shows the characteristic curve of the PV module for different solar irradiance and temperatures, representing v_{pv} to i_{pv} ratio. The DC-link capacitor (C_{dc}) is selected as per the rating of the GFI. The GFI is made of four insulated gate bipolar transistor (IGBT) switches, where S_q is considered as the switching pulse for the q^{th} IGBT. Here, $q = 1, 2, 3, 4$ is the switching pulse index. The LCL-filter consists of an inverter side inductor (L_i), a grid side inductor (L_g), and a capacitor (C) with internal resistance r_i, r_g and r_d, respectively. Here, r_d is considered as the damping resistance and utilized for active damping methods as described later in this section. Instead of the constant DC bus voltage v_{dc}, a variable one is chosen as per the v_{pv} with different irradiance to investigate the controller.

B. GFI MODELING

The state-space relation of PV-GFI system with LCL-filter can be written as (1).

$$\frac{d}{dt}\begin{bmatrix} i_i \\ i_g \\ v_c \\ v_{dc} \end{bmatrix} = \begin{bmatrix} -\tau_g^{-1} & 0 & L_g^{-1} & 0 \\ 0 & -\tau_i^{-1} & -L_i^{-1} & G_i L_i^{-1} \\ -C^{-1} & C^{-1} & 0 & 0 \\ 0 & -G_i C_{dc}^{-1} & 0 & 0 \end{bmatrix} \begin{bmatrix} i_i \\ i_g \\ v_c \\ v_{dc} \end{bmatrix} + \begin{bmatrix} -L_g^{-1} v_g \\ 0 \\ 0 \\ r_{pv}^{-1} C_{dc}^{-1} v_{pv} \end{bmatrix} \quad (1)$$

where τ_i ($= L_i/r_i$) represents the inverter side inductor time constant and τ_g ($= L_g/r_g$) represents the grid-side inductor time constant. G_i represents the switching function of the GFI and can be represented as (2) [35].

$$G_i = -\frac{j4}{\pi} \sum_{h=-\infty}^{\infty} \sum_{q=1}^{4} \frac{1}{h} \sin\left(h\tau_q\right) \sin\left(\frac{h}{2}\delta_q\right) e^{jh\omega t} \quad (2)$$

where δ_q and τ_q pulse width and switching instant of the q^{th} IGBT. ωt is the phase of the GFI pulses and h indicates the harmonic number. In (1), the grid side voltage (v_g) at the point of common coupling (PCC), and v_{pv} are considered as the control input for the overall system. The overall transfer function ($T(s)$) is calculated using (3), which is subdivided into $T_g(s)$ and $T_{GFI}(s)$ to design the LCL-filter for the VSF (variable switching frequency).

$$T(s) = \frac{i_g(s)}{v_{dc}(s)} = T_g(s) \cdot T_{GFI}(s) \quad (3)$$

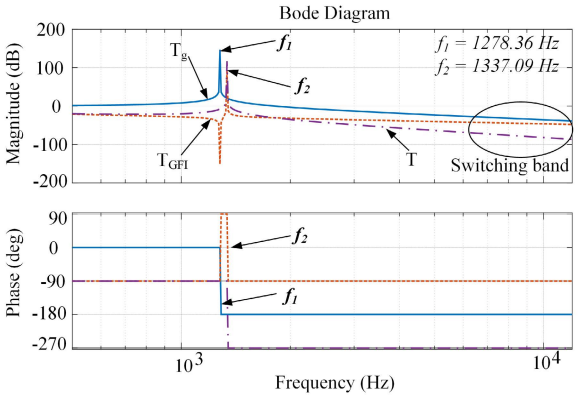


FIGURE 3. Bode plot of transfer functions $T_g(s)$, $T_{GFI}(s)$ and $T(s)$.

The transfer function $T_g(s)$ acts as a second-order low-pass filter by utilizing the grid-side inductor and capacitor. Because of the resonance, this causes unwanted variations in the grid current (i_g). The active damping technique, combined with the appropriate selection of resonance frequency, has become critical for eliminating such unwanted variations. The transfer function $T_{GFI}(s)$ ensures the GFI stability, which can be achieved through precise inner loop current control. As a result, accurate L_i modeling has become critical concerning the VSF operation. The transfer functions $T_g(s)$ and $T_{GFI}(s)$ obtained from Fig. 1 are expressed using (4)-(5), respectively.

$$T_g(s) = \frac{i_g(s)}{i_i(s)} = \frac{\omega_{n1}^2}{s^2 + \tau_g^{-1}s + \omega_{n1}^2} \tag{4}$$

$$T_{GFI}(s) = \frac{i_i(s)}{v_{dc}(s)} = \frac{\left(s^2+\tau_g^{-1}s+\omega_{n1}^2\right)G_i(s)}{s^3+\left(\tau_i^{-1}+\tau_g^{-}\right)s^2+\left(\tau_i^{-1}\tau_g^{-1}+\omega_{n2}^2\right)s + \left(\tau_i^{-1}-\tau_g^{-1}\right)\omega_{n1}^2+\tau_g^{-1}\omega_{n2}^2} \tag{5}$$

where $G_i(s)$ is the Laplace transform of G_i. $\omega_{n1} = 2\pi f_1$ and $\omega_{n2} = 2\pi f_2$ represent the angular frequency in respect to the resonance frequencies f_1 and f_2. Fig. 3 shows how frequency-domain analysis is used to determine the resonance frequencies f_1 and f_2.

C. AC SIDE FILTER DESIGN

By utilizing the frequency domain analysis, a filter design method based on the criterion provided in [7], [36] is applied in this section. The desired switching frequency band for the inverter, as shown in Fig. 3, must be greater than the resonance frequency to achieve accurate filtering of the switching harmonics. It also demonstrates that the phase delay of the system is within the control bandwidth, and that the inverter side current is used as feedback during the resonance frequency f_2, necessitating no active damping. However, when the grid current is used as feedback in the case of resonance frequency f_1, the GFI system becomes unstable and requires active damping. Because of the VSF, the harmonic range of the inverter side current has been expanded for hysteresis current control. It transfers the resonance frequency f_1 of the inverter side current to the grid side current, causing distortion within the grid current. As a result, the modeling of the grid side inductor and capacitor filter is intemperately reliant on determining the resonance frequency f_1 as well as the grid side current ripple. In contrast, the value of the inverter side inductor can be calculated using (6) [36], which is based on the maximum permissible current ripple of the inverter side current as well as the ASF chosen in the case of the switching cycle.

$$f_1 = \frac{1}{2\pi}\sqrt{\frac{1}{L_g C}} \quad \text{and} \quad f_2 = \frac{1}{2\pi}\sqrt{\frac{1}{L_g C}+\frac{1}{L_i C}} \tag{6}$$

where $10f_g < f_1 < 0.5f_{sw,avg}$ is chosen for better harmonic attenuation performance of the grid side current and can be utilized to design the appropriate value of L_i. In Fig. 3, it can be noticed that f_1 and f_2 are selected at 1278.36 Hz and 1337.09 Hz, respectively. On the other hand, a rise in the resonance frequency is observed with a decrease in the value of the grid side inductor, which causes harmonics in i_g and causes the hysteresis controlled converter to trip.

D. ACTIVE DAMPING AND RESONANCE CONTROL

In actual passive damping, the damping resistance r_d need to be introduced in the transfer function $T_g(s)$. However, it leads to a more complex analysis of the system with several disadvantages. Hence, for the active damping method, r_d is considered as the virtual resistance and only implemented in the control algorithm mentioned in Fig. 1. The active damping current (i_d, i.e., $i_d = v_c/r_d$) corresponding to r_d adjust the reference current (i_i^*, i.e., $i_i^* = i_d^* - i_d$) of GFI. Here, v_c being the measured voltage across LCL-filter capacitance and i_d^* is the reference current generated from the proportional resonant (PR) controller $G_{PR}(s)$ of (7). The grid current error (i.e., $i_g^* - i_g$) is considered as input to $G_{PR}(s)$.

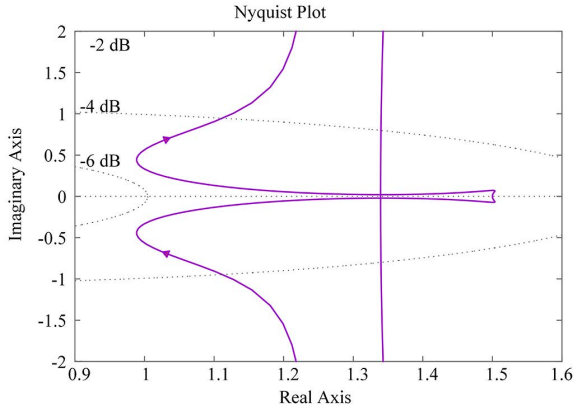
$$G_{PR}(s) = k_p + \frac{2k_r\omega_c s}{s^2 + 2\omega_c s + \omega_g^2} \tag{7}$$

where k_p, k_r and ω_c denote the proportional gain, the resonant gain, and the angular cutoff frequency of the PR controller. To analyze the stability as well as steady-state performance, it is desired to develop the transfer function $H_g(s)$ corresponding to reference grid current i_g^* and i_g which can be mentioned in (8).

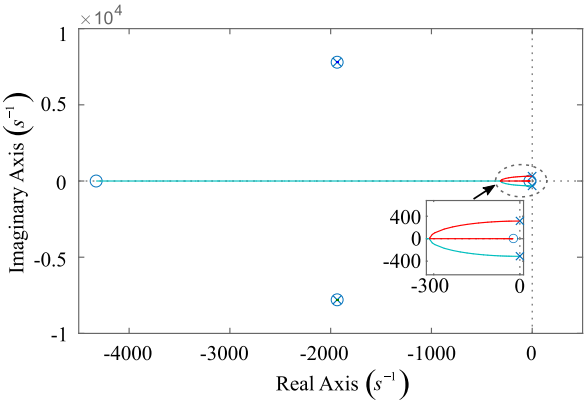
$$H_g(s) = \frac{i_g(s)}{i_g^*(s)} = \frac{s^2 + \tau_g^{-1}s + \omega_{n1}^2}{s^2 + \left(\tau_g^{-1} + \tau_d^{-1}\right)s + \tau_g^{-1}\tau_d^{-1} + \omega_{n1}^2} \tag{8}$$

where $\tau_d (= r_d C)$ represents the time constant with respect to the capacitor by taking the damping resistance into account. However, after removing the influence of resonance, it is discovered that the zero steady-state error is obtained at $|H(s)| = 1$ with $r_d \to \infty$. Now, the overall loop gain of the controller ($G(s)$) can be denoted as (9).

$$G(s) = G_{PR}(s)\, H_g(s) \tag{9}$$



(a) Nyquist plot



(b) Root locus with pole zero plot

FIGURE 4. Performance analysis for the transfer function $G(s)$.

The stability analysis of $G(s)$ can be obtained through analyzing Nyquist plot and root locus with pole zero plot, as mentioned in Fig. 4. It can be observed that all poles and zeros lie on the left half of the S-plane. Moreover, the root locus is indicating that the system is stable under the chosen K_p, K_i and ω_c values. The zero does not have the effect on the stability of the system; however, it improves the response of the system. Hence, the root locus and Nyquist plot both define the stability of the system as expected. It has been observed that the effect of resonance in the presence and absence of damping factors for the proposed controller is negligible and provides a stable performance, which is being validated through experimental verification in Section IV. Furthermore, an increase in r_d results in an increase in the time constant τ_d, which slows down the dynamic response of the GFI system. Smaller r_d values, on the other hand, cause oscillations in the grid current.

E. INCREMENTAL CONDUCTANCE MPPT ALGORITHM AND DC-LINK VOLTAGE CONTROL

To operate a solar array at MPP, an MPP tracking (MPPT) algorithm can be utilized for detecting the maximum PV voltage V_m and maximum PV current I_m. Single-stage system with MPPT control includes DC/AC converter control as well as power feedforward control logic, as mentioned in Fig. 1. A constant DC-link voltage (v_{dc}^*) can be maintained through the MPPT control while feeding the maximum PV power into the grid. In the proposed control in Fig. 1, an incremental conductance MPPT technique is used to achieve precise and fast PV power control with a low computational burden.

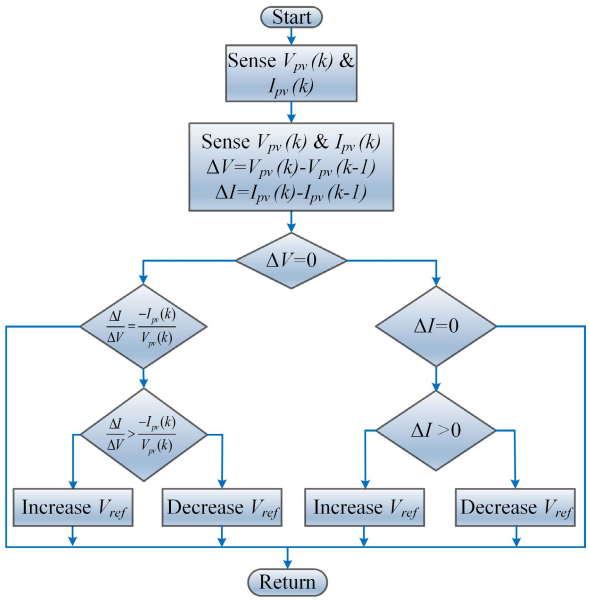


FIGURE 5. Flow chart of incremental conductance MPPT algorithm.

The incremental conductance method for MPP tracking utilizes the inequality relationship corresponding to p_{pv} as in (10), i.e., $dp_{pv}/dv_{pv} = 0$. The MPPT algorithm employs a computation of the sign of dp_{pv}/dv_{pv} using incremental conductance of di_{pv}/dv_{pv}. Concerning Fig. 2, the slope on the left side of the curve is considered as positive (i.e., $dp_{pv}/dv_{pv} > 0$), while the slope on the right side of the curve is taken as negative (i.e., $dp_{pv}/dv_{pv} < 0$). At MPP, the slope is considered as $dp_{pv}/dv_{pv} = 0$.

$$\frac{dp_{pv}}{dv_{pv}} = \frac{d(i_{pv}v_{pv})}{dv_{pv}} = i_{pv} + v_{pv}\frac{di_{pv}}{dv_{pv}} \approx I_m + V_m\frac{\Delta I_m}{\Delta V_m} \quad (10)$$

When there is a change in irradiation or temperature, the current ΔI_m changes, corresponding to ΔV_m as of (10). The flow chart of the incremental conductance MPPT algorithm is shown in Fig. 5. In the prescribed algorithm, the PV voltage and current are measured initially through voltage and current sensors, respectively. Each step requires the difference in voltage and current found in the previous and current states of the measurement. If the change in voltage is true, it is first compared to zero, and then it compares the instantaneous value and incremental conductance, which changes the reference voltage further. If the change in voltage is zero, a change in current is observed, which causes the reference current to change. The algorithm monitors the voltage change until MPP is reached to set the reference DC-link voltage v_{dc}^*. The rate of change in v_{dc}^* is decided by a gain factor α of MPP algorithm.

An appropriate DC-link voltage for different irradiance levels is important to achieve low power loss and minimum current THD. Once v_{dc}^* reference is decided through the MPPT algorithm, the DC-link voltage (v_{dc}) across the DC-link capacitor needs to be monitored by using a simple PI regulator. The PI regulator tracks v_{dc} with respect to v_{dc}^* followed by a limiter and produces the current component (i_{dcl}) indicating the power loss for maintaining the DC-link voltage. The limiting value of the limiter is decided by the GFI power rating and the maximum grid voltage fed to GFI. Considering p_{pv} as total power transferred to the grid as of Fig. 1, the reference grid current (i_{pv}^*) required to inject at PCC can be obtained by current estimation algorithm followed by a unit template signal generated by using the estimated grid phase angle ($\hat{\theta}_{pll}$) obtained from a state-of-the-art SOGI based phase locked loop (PLL) [37]. By stabilizing the DC-link at the required level, the reference current is adjusted to transfer power from inverter DC side to grid, using a fast grid current controller.

III. HCC FOR GFI SYSTEM WITH *LCL*-FILTER

The hysteresis current control unit for inner loop control is shown in Fig. 1. The current error (i.e., $i_i^* - i_i$) as the input provides the switching pulses as output by using the proposed MDBHCC. The proposed MDBHCC makes an attempt to reduce the impact of overmodulation during the switching of GFI through proper switching sequence selection. During switching sequence selection, the inverter-side inductance impact significantly. As a result, to obtain a 2-level output voltage, the upper and lower switches of each leg of the inverter act in a complementary manner. When the error exceeds the current hysteresis band (HB), the controller obtains the switching pulses. The selection procedure of HB is provided in the following.

A. HYSTERESIS BAND SELECTION

The determination of HB leads to VSF within the frequency band for hysteresis current control. The frequency band is chosen in such a way that the minimum switching frequency ($f_{sw,min}$) has no effect on the resonant frequency (f_{res}), and the maximum switching frequency ($f_{sw,max}$) does not exceed the hardware and sampling frequency limits [15]. As a result, by defining the switching frequency band as (11), the GFI and filter design can be easily accomplished.

$$10f_g < f_{res} < f_{sw,min} < f_{sw,avg} < f_{sw,max} \tag{11}$$

With a single-phase GFI, the maximum switching frequency of the grid-side filter inductance, DC-link voltage, and grid voltage at the point of common coupling greatly determines the choice of current hysteresis band. This does not have to be extremely small or exceedingly large. As a result, a trade-off is made between the allowable current THD and the average switching frequency ($f_{sw,avg}$), which also improves the GFI system tracking capability. An inverter side current ripple of between 5% and 10% is considered as an acceptable limit of fixed-band hysteresis current regulation.

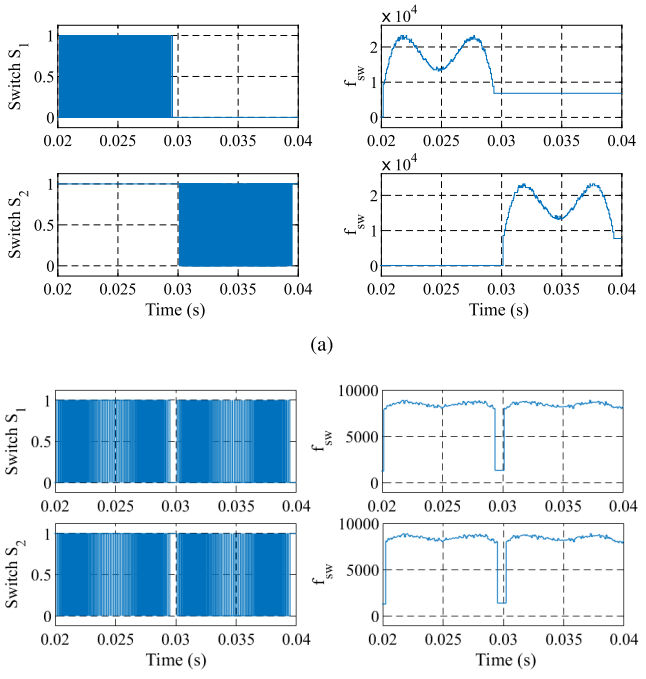


FIGURE 6. Switching pulses of switch S_1 and S_2 and corresponding instantaneous f_{sw} for (a) conventional DBHCC and (b) proposed MDBHCC.

B. MINIMIZATION OF SWITCHING FREQUENCY VARIATION

The proposed MDBHCC method takes advantage of both the benefits of unipolar symmetrical pulse-width modulation (SPWM) and the conventional DBHCC method mentioned in [23]. SPWM has a switching sequence of 01, 11, 10, 11, 01, 11, 10, 11 . . . and 10, 00, 01, 00, 10, 00, 01, 00 . . . for positive half cycle (PHC) and negative half cycle (NHC), respectively, for switching states S_1S_2. Whereas conventional DBHCC has PHC and NHC of 01, 11, 01, 11, 01 . . . and 10, 00, 10, 00, 10 . . . , respectively. Considering the combined switching patterns of SPWM and DBHCC, the proposed MDBHCC method has comparatively fewer oscillations and reduced ASF, as shown in Fig. 6. The switching pattern for the proposed MDBHCC can be represented as Fig. 7, which can be derived from the following procedure.

1) The initial phase of operation attempts to reduce the maximum switching frequency relating to the desired switching states, namely, S_1' and S_2', which are the modifications of the original switching states S_1 and S_2 as of Fig. 8. The output switching states S_1' and S_2' function as the trigger input to the discrete integrator, followed by a comparator. The comparator compares the integrator output and obtains a trigger signal '1' if the switching frequency of S_1' and S_2' equals/exceeds $f_{sw,max}$. Further, this trigger signal from comparators are used to trigger S_1 and S_2, respectively. To ensure safe operation, the corresponding procedure ensures that the GFI switching frequency never exceeds $f_{sw,max}$.

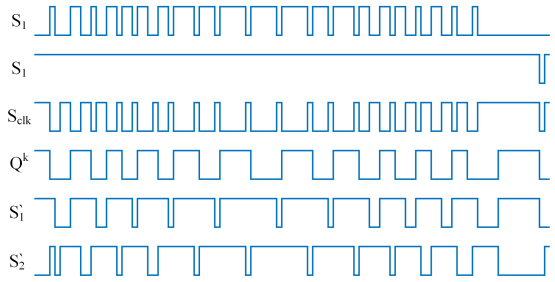


FIGURE 7. Switching pulse logic of proposed MDBHCC.

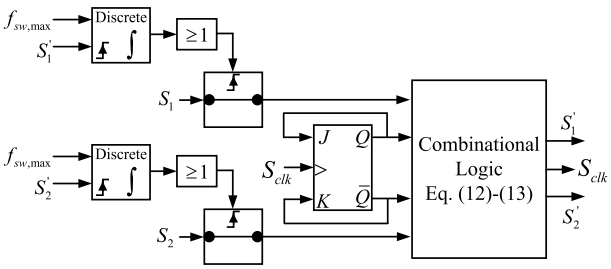


FIGURE 8. Proposed MDBHCC logic using sequential and combinational logic.

2) The later phase controls the switching frequency oscillation without affecting % THD of i_i. In this stage, the JK flip-flop is clocked using an adaptive clock signal (S_{clk}) to execute the zero state alternatively in each half cycle of the MDBHCC. S_{clk} is derived from the 'exclusive-or' operation of the switching states, as represented by (12).

$$S_{clk} = S_1 \otimes S_2 \tag{12}$$

The proposed JK flip-flop generates the subsequent state denoted as Q as well as its complementary state $\overline{Q}$ with the help of the S_{clk} with $\{J = \overline{Q}^{k-1},\ K = Q^{k-1}\}$ as function inputs. The term k refers to the current state, while $k-1$ concerns to the previous state. Q varies as the S_{clk} changes from low to high and high to low and derives the expression for S_1' and S_2', as given in (13).

$$\begin{aligned} S_1' &= (S_1 \cdot S_2) + (Q^k \cdot S_{clk}) \\ S_2' &= (S_1 \cdot S_2) + (\overline{Q}^k \cdot S_{clk}) \end{aligned} \tag{13}$$

With active states (11 & 00) in the double band comparator, S_1' and S_2' retain the same desired switching states S1 & S2, regardless of the switching states of S_{clk} or Q. To reduce the switching state oscillations and maintain ASF, two distinct zero states are used during $Q = 0$. The proposed MDBHCC is discussed in detail below, along with a switching frequency analysis.

C. PROPOSED MDBHCC

The switching logic of the MDBHCC is designed from (13) to generate the desired switching signals S_1' and S_2'. With the addition of two states in each symmetry, the ON T_{on} and OFF period T_{off} of the proposed MDBHCC method can be decided as (14), which are twice the ON and OFF period of the traditional DBHCC. With such addition of states, MDBHCC replicates the characteristics of the unipolar pulse with modulation.

$$T_{on} = \frac{2b_iL_i}{v_i - v_g}, \quad \text{and} \quad T_{off} = \frac{2b_iL_i}{v_g} \tag{14}$$

where b_i denotes the current HB. It can be observed from (14) that T_{on} and T_{off} have doubled while b_i has not changed. Now, the switching frequency of the proposed MDBHCC can be denoted as (15) and found to be a function of the inverter side inductance.

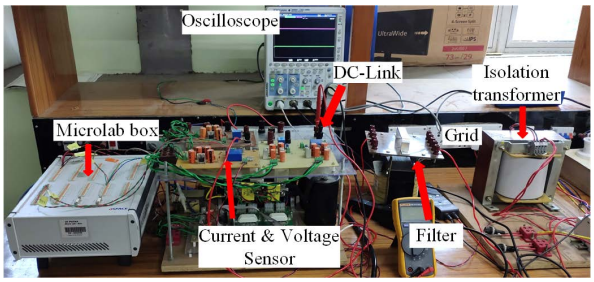
$$f_{sw} = \frac{(v_i - v_g)v_g}{2v_ib_iL_i} \tag{15}$$

The variation in the switching frequency, on the other hand, is narrowed down with the help of the suggested adaptive clock controlled logic gate algorithm, and it does not take into account any variation in b_i limit determined by the HB selection criterion. The %THD, on the other hand, has remained unchanged with the suggested method. The inverter side switches are optimally utilized, as shown in Fig. 6(b), and the oscillation in the switching frequency is also minimized in the case of the proposed MDBHCC when compared to the traditional DBHCC, as shown in Fig. 6(a). Figs. 6 and 7 show the switching pulses of the switches S1 and S2, as well as their respective real-time switching frequency plots with respect to the DBHCC. It can be seen from the diagram that the inverter switches operate in both a discontinuous and irregular manner and are addressed in the single-phase GFI using the suggested hysteresis current control schemes.

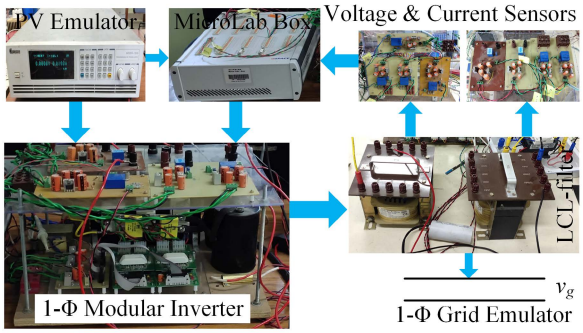
IV. RESULTS AND DISCUSSION

The performance of the proposed hysteresis current control method with respect to the PV-based single-phase GFI system accompanied by LCL-filter is validated by experiment and simulation, and the parameters are provided in table 2. A PV panel of 3.1 kW as shown in table 1 is utilized to feed power into the grid at PCC. To make an accurate performance evaluation, the proposed HCC method is tested using ASF and %THD for a single-phase GFI system with hysteresis band adjustment. The GFI system is made up of SKM100GB063D IGBT modules, HX 25-P current sensor, LV 25-P voltage sensor, and PV Emulator, as shown in Fig. 9. The GFI is controlled using a dSPACE MicroLabBox based digital controller that utilizes a sampling frequency of 25 μs. To investigate the effectiveness of the proposed MDBHCC with PR control, the following test scenarios are validated through the experimentation.

- Scenario 1: Operation at 1000 W/m^2 irradiance and 25°C in steady-state conditions.
- Scenario 2: Under dynamic change in irradiance from 1000 W/m^2 to 500 W/m^2 and 500 W/m^2 to 1000 W/m^2 at 25°C.
- Scenario 3: Robustness under grid voltage sag.
- Scenario 4: Under dynamic change in load condition.



(a)



(b)

FIGURE 9. Experimental prototype for single-phase PV-GFI system (a) complete setup (b) block representation of hardware connection.

- Scenario 5: Under dynamic change in temperature from 25°C to 30°C at 1000 W/m^2.

In the case of the GFI system accompanied by the LCL-filter, current HB of 1 A is considered for the experimental scenarios. Using the MDBHCC with PR controller, steady-state grid voltage performance at unity power factor is illustrated for all scenarios in Figs. 10–14.

1) SCENARIO 1

In this scenario, PV irradiance is kept at steady-state value of 1000 W/m^2 while temperature in PV emulator is maintained at $\approx 25°C$. The performance of the suggested MDBHCC with PR controller is evaluated through Fig. 10(a), which indicates that the grid current i_g remains in phase with v_g at PCC, while feeding maximum power of 3 kW into the grid. It can be seen that the proposed MDBHCC method generates less current ripple than the existing DBHCC method, as well as less ripple in the injected grid power. The grid current i_g is 13.1 A with THD of 1.93% at unity power factor. The proposed control with PR control exhibits zero steady state error. The active damping employed eliminates the effect of resonance in the grid current. The grid current is evaluated through the tracking of the reference current accompanied by the zero steady state error is shown in Fig. 10(b). In this plot, v_{dc} represents low double-frequency oscillations of 10 V with the proposed control. The lowered oscillation in v_{dc} is also due to the influence of the incremental conductance MPPT algorithm that minimizes the oscillations in PV current i_{pv} and further the PI controller keeps the DC-link voltage stable.

TABLE 1. PV array parameters.

Parameter	Value
Maximum power output at MPP (P_{pv})	3.1 kW
Open circuit voltage (v_{oc})	37.1 V
Maximum voltage (v_{pv})	29.6 V
Short circuit current (i_{sc})	8.26 A
Maximum current (i_{pv})	7.6 A
Maximum power (p_{pv})	224.96 W
Number of series (N_{se}) and parallel panels (N_p)	14 and 1

TABLE 2. Hardware prototype parameters.

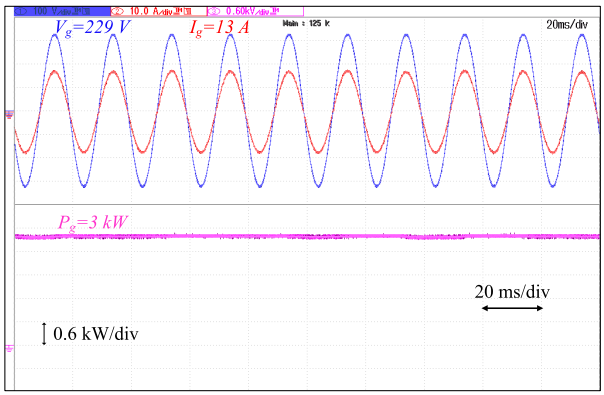
Parameter	Value
Grid voltage at PCC and frequency (V_g, f_g)	230 V, 50 Hz
DC-link Capacitor (C_{dc})	2200 μF
Grid and inverter side inductor (L_g, L_i)	0.31 mH, 3.3 mH
Filter Capacitor (C)	50 μF
Internal resistance (r_i, r_g)	0.6 Ω, 1.2 Ω
Damping resistance (r_d)	10 Ω
Grid impedance (Z_g)	0.01 Ω, 0.15 mH
PR controller parameters (k_p and k_r)	1.5, 1000
PI controller parameters (K_p and K_p/K_i)	1600, 0.8

2) SCENARIO 2

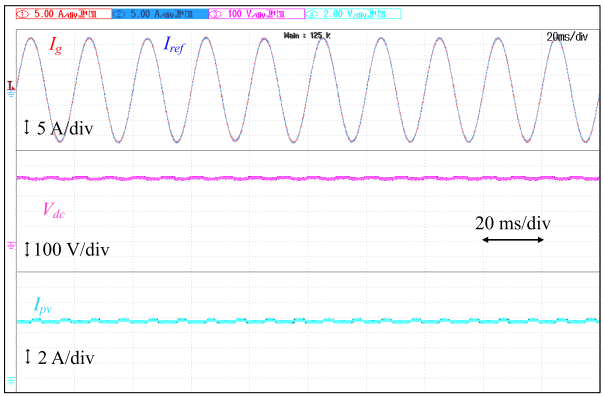
A dynamic change in irradiance from 1000W/m^2 to 500W/m^2 and 500W/m^2 to 1000 W/m^2 is illustrated in Fig. 11(a) (top). During this irradiance change, $\approx 25\,°C$ temperature is considered for the PV emulator. With the proposed control, it is observed that v_{dc} yields faster dynamic performance with ±3.5% fluctuations from its reference value v^*_{dc}, which is originally obtained from the incremental conductance MPPT algorithm. During this operation, the grid voltage v_g and current i_g at PCC behave sinusoidal nature with unit power factor. Fig. 11(a) (bottom) represents a zoomed portion of the aforementioned results during the transient period of irradiance change. Due to a sudden change in irradiance, the RMS value of i_g falls from 13 A to 6.6 A having a current THD of 4.19%. The reduction in grid current is observed to keep the DC-link voltage stable at MPP with the change in irradiance. The settling time of grid current i_g is about less than 1.5 cycles for dynamic change in irradiance. Along with the above performances, PV power p_{pv}, grid power p_g, and PV current i_{pv} are also investigated in Fig. 11(b) during solar irradiance change. The power feeding into the grid is 3 kW and 1.5 kW for 1000W/m^2 and 500W/m^2 irradiance, respectively. The concerned results exhibit lower ripple values as expected, except the significant impact on grid power step change in irradiance.

3) SCENARIO 3

Fig. 12 illustrates the experimental outcomes during the grid voltage sag condition. Grid voltage with 20% voltage sag is illustrated in Fig. 12(a), whereas, Fig. 12(b) indicates the performance evaluation with 30% sag in grid voltage. For both voltage sag conditions, the proposed control provides enhanced outcomes in terms of low ripple in i_g and v_g with unit power factor operation. The voltage sag of 20% and 30%

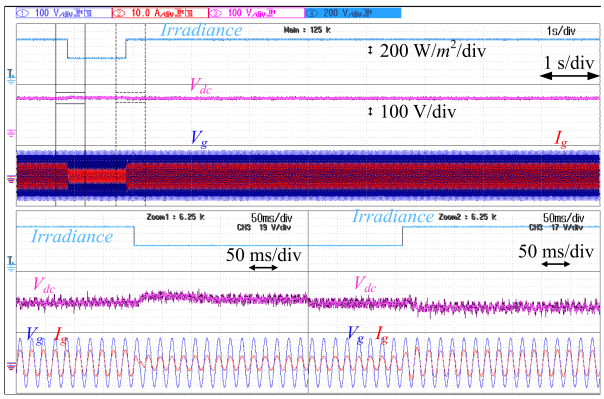


(a) v_g, i_g and P_g waveforms.

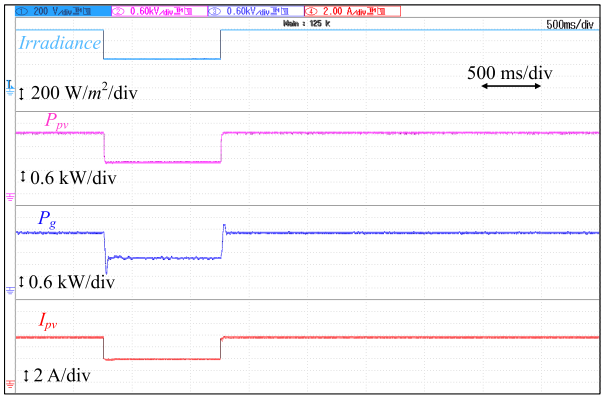


(b) i_g, i_{ref}, v_{dc} and i_{pv} waveforms.

FIGURE 10. Experimental results corresponding to test scenario-1.

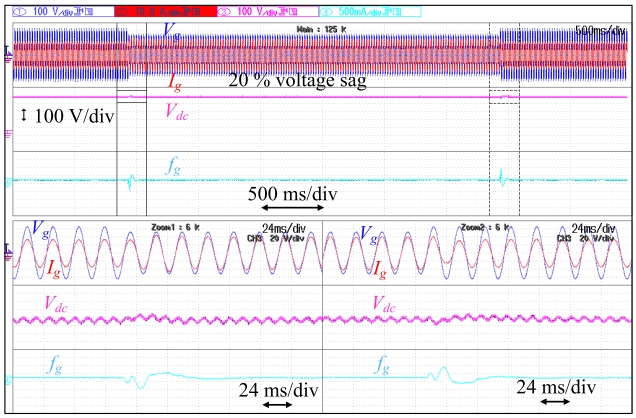


(a) Irradiance, v_{dc}, v_g, and i_g waveforms.

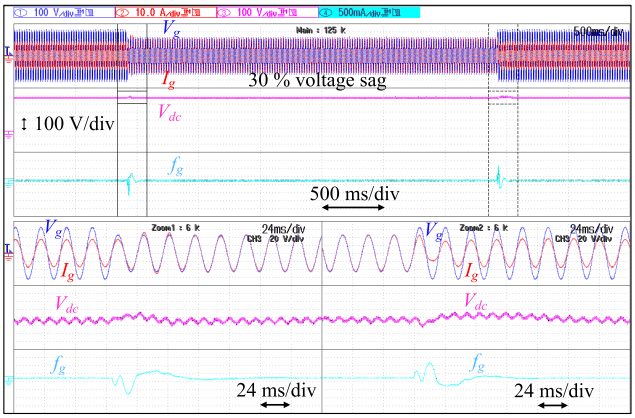


(b) Irradiance, P_{pv}, P_g and I_{pv} waveforms.

FIGURE 11. Experimental results corresponding to test scenario-2.



(a) v_g, i_g, v_{dc} , and f_g waveforms at 20% voltage sag.



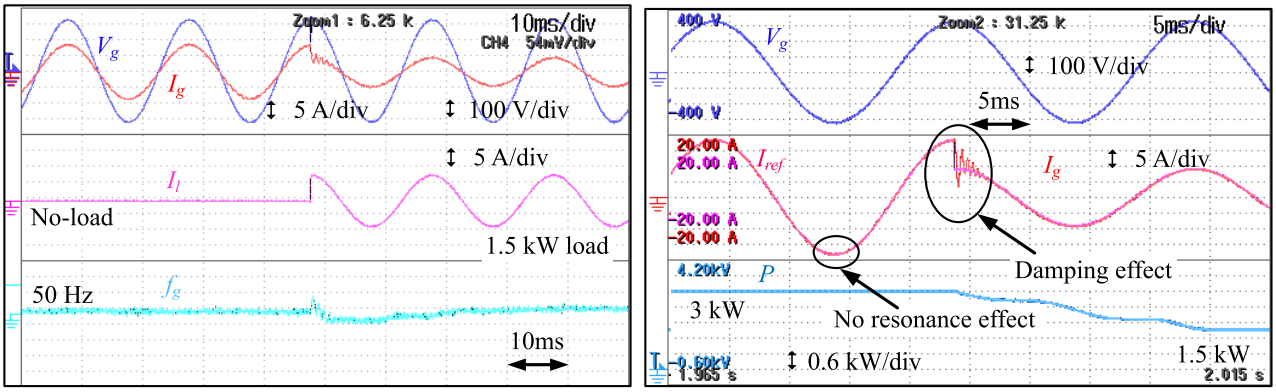
(b) v_g, i_g, v_{dc}, and f_g waveforms at 30% voltage sag.

FIGURE 12. Experimental results corresponding to test scenario-3.

is introduced in the grid voltage v_g, increases the grid current i_g injected into the grid to keep the power feeding into the grid P_g constant. During this voltage sag, the % THD of the grid currents are observed with 1.68% and 1.42%, respectively. At MPP, the DC-link voltage V_{dc} has achieved a stable operation. The maximum voltage fluctuation in DC-link at 20% voltage sag is 6 V, which is settled in 0.06 sec. However, 10 V of DC-link fluctuation appears under voltage sag of 30%, which is settled in 0.1 sec. As shown in the zoomed portion of the aforementioned outcomes in Fig. 12, the GFI with the proposed control and SOGI-PLL maintains a stable grid frequency (f_g) during the voltage sag after the restoration of grid voltage to the rated condition.

4) SCENARIO 4

Fig. 13 shows the test scenario corresponding to the dynamic load change and the effect of resonance on GFI system operation. A step change in load current i_l (from no-load to 6.6 A)



(a) v_g, i_g, i_l, and f_g waveforms.

(b) v_g, i_g, i_{ref}, and P_g waveforms.

FIGURE 13. Experimental results corresponding to test scenario-4.

TABLE 3. Comparison of proposed and existing methods.

Comparison Category	Proposed Method with PR	Single-phase [32]	Single-phase [6]	Three-phase [38]	Single-phase [26]	Single-phase [5]	Single-phase [33]
Number of converter stage	Single-stage	Single-stage	Single-stage	Two-stage	fixed DC supply	Single-stage	Single-stage
Computational burden	low	medium	medium	high	low	medium	high
Switching frequency f_{sw}	8.5 kHz	10 kHz	10 kHz	10 kHz	15 kHz	4 kHz	20 kHz
DC-link ripple (V)	10	20	Not Reported (NR)	5	fixed DC supply	NR	4
% THD$_i$ of i_g	1.93%	2.49%	1.67%	1.8%	2.62%	2.73%	2.06%
Overshoot of DC-bus voltage	3.5%	7.5%	5%	2.4%	fixed DC supply	NR	3%
PWM technique	PI+PR+HCC	pq+HCC	PR+RC	ADRC	PR+HCC	PR+PR	PR+SMC
Settling time of i_g	1.5 cycles	5 cycles	NR	1.5 cycles	0.5 cycles	2.5 cycles	2 cycles
Filter type	LCL	LC	LC	LC	LCL	LC	L
Peak efficiency	96.77%	96.42%	89.2%	NR	97.21%	95%	97.47%

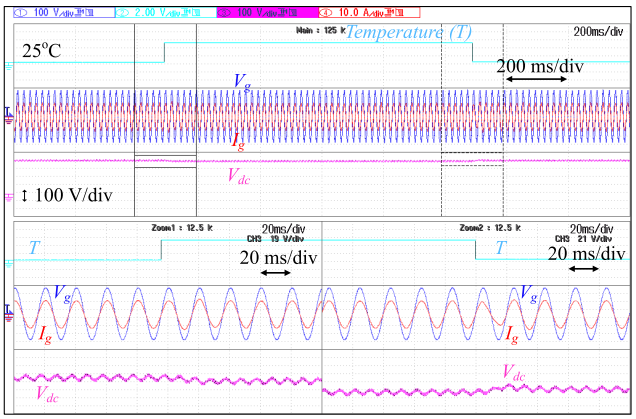


FIGURE 14. Experimental results corresponding to test scenario-5.

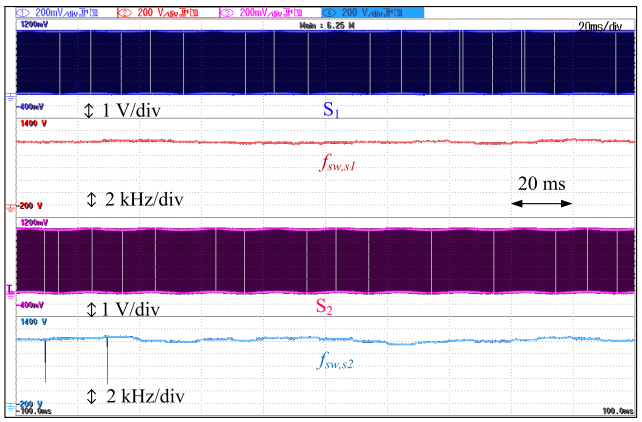


FIGURE 15. Experimental results showing switching pulse (S_1 and S_2) and corresponding switching frequency for proposed MDBHCC at HB of 1 A.

causes a steep change in the amount of grid current. However, the grid current i_g tracks its reference value of current along with better steady-state as well as the dynamic response. Moreover, during the load change, the active power feeding into the grid changed from $3\,kW$ to $1.5\,kW$. v_g and i_g are observed with nearly unit power factor operation. The influence of both the resonance and damping factor is analyzed with the help of experiments on the grid current, whereas the dynamic change in terms of the injected power within the grid is illustrated in Fig. 13(b). The THD of 3.34% is observed in the grid current with $1.5\,kW$ load power. Moreover, PLL with the proposed controller tracks the operating frequency of the grid at PCC, which keeps the PV-based GFI system stable. The proposed MDBHCC with PR control has better dynamic performance in case of step changes in load power.

5) SCENARIO 5

A dynamic change in temperature from 25 °C to 30 °C is considered at irradiance of 1000 W/m^2, shown in Fig. 14. With the change in temperature, the MPP of single-stage PV converter is shifted with the variation in the DC-link voltage. The grid voltage v_g and current i_g are operated at unity power factor while feeding active power into the grid. The grid

current THD is observed with 1.93% at 25 °C and 2.1% at 30 °C.

Fig. 15 represents the switching pattern for the switching state S_1 and S_2. It is illustrated that both the switching pulses are utilized fully during GFI operation. However, in the case of DBHCC, all switches are not utilized to its maximum capacity. The proposed MDBHCC outperforms DBHCC in this regard and maintains a constant switching frequency as expected in Fig. 15.

6) COMPARATIVE PERFORMANCE

In Table 3, a comparative performance of the proposed MDBHCC with PR controller with existing state-of-the-art literature [5], [6], [26], [32], [33], [38] is presented. The proposed controller has better output power quality with a peak efficiency of 96.77%. Compared with the existing PV integrated system, the proposed method has fast convergence time for current i_g feeding into the grid. Furthermore, the minimum DC-bus overshoot of 3.5% is observed for the proposed method. The overall performance of the proposed method is effective and highly suitable for single-stage PV integrated system while the maximum power of PV to grid with low computational burden and least switching frequency.

V. CONCLUSION

The single-phase PV-based GFI system accompanied by LCL-filter with dynamic modelling is employed in this paper and tested on a 3.1 kW prototype hardware test rig. The modelling of the overall system is studied with stability analysis of the system in case of variable switching frequency control. Thereafter, an efficient damping technique is deployed for damping out the impact of resonance prevailing within the grid current. Larger oscillations in the switching frequency along with the maximum switching frequency issues are eliminated with the help of the suggested MDBHCC algorithm. The current THD is lowest in case of the suggested MDBHCC, considering a hysteresis band of 1 A. Moreover, a PR controller is employed to achieve nearly zero steady state error. The suggested MDBHCC algorithm generates the least switching losses and provides better productivity when compared with the conventional DBHCC method. The dynamic response as well as the steady-state performance is experimentally validated in case of a step change in solar irradiance and temperature, voltage sag, and the injected power into the grid. Furthermore, the proposed PR with MDBHCC algorithm can facilitate the resonance and damping problem efficiently and provide fast convergence. Hence, it is highly suitable for PV-GFI systems.

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