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FAULT-CURRENT LIMITER USING A SUPERCONDUCTING COIL*

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Abstract

A novel circuit, consisting of solid-state diodes and a biased superconducting coil, for limiting the fault currents in three-phase ac systems is presented. A modification of the basic circuit results in a solid-state ac breaker with current-limiting features. The operating characteristics of the fault-current limiter and the ac breaker are analyzed. An optimization procedure for sizing the superconducting coil is derived.

Introduction

Continued growth of electrical power generation and transmission systems has resulted in higher levels of available fault currents and correspondingly greater demands on system protective components. The problem associated with increased fault currents may be attacked in the following ways: (1) develop higher interruption rating circuit breakers and retrofit existing substations with higher rating breakers; (2) restructure the power system to reduce available fault currents; or (3) insert current limiting devices in the systems that limit fault currents to levels compatible with existing installed protective devices. Because the first approach has been recognized as being very costly and the second approach eliminates the desirable advantages associated with tightly interconnected generation and transmission networks, emphasis has been placed on searching for a current limiting device that is economically competitive with the alternative of circuit breaker replacement and is compatible with present power system design philosophy and operating practice. During the last few years, a number of programs have been sponsored to investigate various techniques and devices applicable to limit fault currents in power systems.[1]

The different proposed schemes for a fault current limiter (FCL) can be classified as switched and non-switched devices.[2] The major effort in FCL development has concentrated on switched devices, in which the current is commutated very rapidly by a switching device from a low impedance main path to a high impedance parallel path. The advantage of a switched FCL is its low system loss during normal operation. A major disadvantage of a switched FCL is the control complexity of synchronized operation of sequential switching devices. In addition, the switching process requires a finite amount of time during which the fault current is only limited by the system impedance.

Recently a unique FCL method was proposed.[3] This method takes advantage of high power superconducting and solid state technology and offers considerable advantages in simplicity over the previously proposed methods. In this paper only the electrical operating characteristics of the novel FCL circuit and of one modification of the basic circuit, resulting in a solid-state ac switch, are described. In a companion paper an economic evaluation of all components of the FCL are presented in form of a parameter study that includes the superconducting coil design.[4]

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Solid-State Fault Current Limiter

The solid-state fault current limiter uses, as shown in Fig. 1, a diode bridge D1 to D4, and a biased superconducting coil, L, as a switched impedance in each phase of a three phase system. A circuit breaker, CB, is installed in series with the FCL and interrupts the reduced fault current. The bias voltage supply, V_b, that can be implemented as a full wave controlled Graetz bridge, provides the coil bias current, i_L. The amplitude of the bias voltage is just high enough to overcome the voltage drop of a pair of diode strings, D1 and D4 or D2 and D3. The coil bias current, i_L, is adjusted to a value I_o during normal, non-faulted operation of the transmission line. The value I_o is chosen to be higher than the peak amplitude of the line current, I_{max}, to allow overloading of the line. As long as the line current at any time is smaller than the bias current, I_o, the diode bridge is always conducting and, other than for the small forward voltage drop impedance of the diode strings D1 to D4, does not present any impedance to the current flow of the line current. Figure 2 depicts the current-time relationship over one 60 Hz cycle for the coil and line current and for the different diode currents. For both positive and negative half periods of the line current, the diode currents are positive and therefore the diodes are conducting as long as the bias current, I_o, is larger than the peak amplitude of the line current, I_{max}.

In the case of a line fault, as indicated by a dashed arrow in Fig. 1, the line current increases in amplitude until it reaches the value I_o. At that instant one pair of diode strings, D1 and D2 or D3 and D4, becomes reversed biased and ceases to conduct. When one pair of diode strings goes into the blocking state, the inductance, L, is automatically switched into the ac circuit and limits the rate of increase of the fault current. By making the inductance, L, much greater than the ac system source impedance, a very slow increase of fault current can be obtained. The

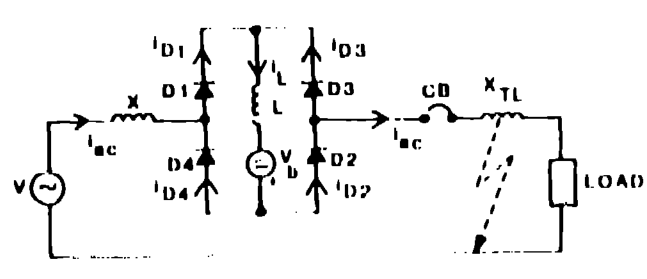

Fig. 1. Single phase, solid-state, superconducting fault current limiter.

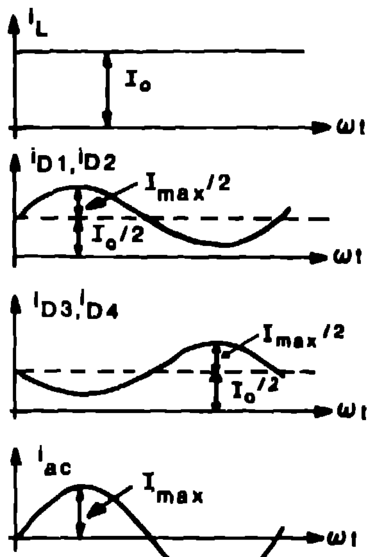

Fig. 2. Steady state currents of solid-state, superconducting fault current limiter.

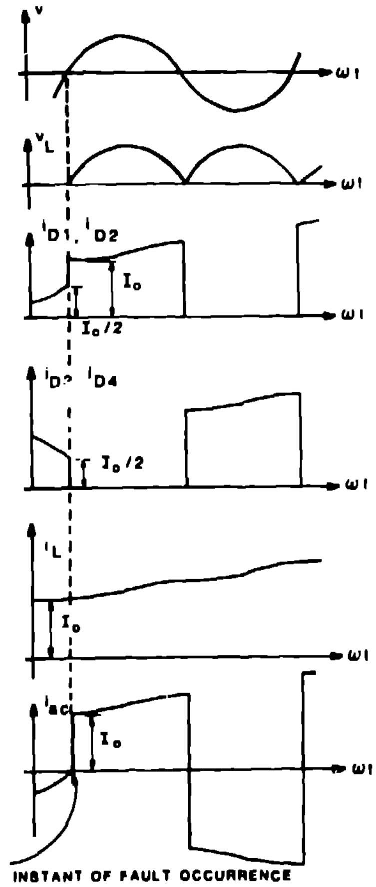

Fig. 3. Currents and voltages in superconducting current limiter during fault conditions.

superconducting coil cannot limit the current indefinitely. Therefore, the circuit breaker must be opened to limit the current within a reasonable time, in the order of one or two cycles, depending upon the mechanics of the breaker design. Operation of the FCL is entirely automatic without the need for sensing and control. In addition, the fault current is limited in the first half cycle. A superconducting coil is selected over a normal coil to minimize the system losses. Figure 3 shows the current-time dependency for various circuit currents for a fault condition. For simplicity, the assumption is made that the fault occurs at the zero crossing of the load current. The driving voltage, v_L, for the coil current is a rectified sine wave voltage. Therefore, the coil current increases from the initial I_o value according to the equation

$$I_L = I_{on} + \frac{V_{max}}{\omega L}(1 - \cos \omega t), \quad (1)$$

with I_{on} the initial value after the nth half period and V_{max} the peak amplitude of the phase voltage.

Solid-State AC Switch

A modification of the basic solid-state FCL was suggested, that results in a solid-state ac breaker with current limiting features.[5] By replacing the diodes of the FCL circuit by controlled devices, such as thyristors or silicon controlled rectifiers (SCRs), a device is created that can reduce the line current to zero after a line fault. Compared with the diode circuit, the SCR circuit requires control logic for gating of the SCRs and a fault current detection circuit.

The thyristor circuit behaves identically to the diode circuit during the non fault time of operation. Initially all the thyristors of the four strings have to be gated simultaneously to establish a current. After the initial gate pulse, no other gate pulses are required, because the SCRs are conducting. After the occurrence of the fault, when one pair of thyristors strings ceases to conduct the current, the SCR circuit has the additional feature of allowing phase delay action. By delaying the gate pulses of always two sets of SCR strings, a negative voltage can be applied across the coil, thus reducing the coil and line current to zero. In the worst case, the fault current decreases from its maximum value after one half cycle (8.33 ms). That time is the maximum necessary with proper control to delay the phase angle of the thyristors. Because the solid-state switch acts like a half cycle breaker, a smaller superconducting coil and a lower overcurrent rating of the solid-state power devices are required compared with the diode circuit.

The circuit behavior of the solid-state switch is shown in Fig. 4. The assumption is again made that the fault occurs at the zero crossing of the line voltage. During the first half cycle after the fault, the positive half cycle of the line voltage is impressed on the superconducting coil and the coil and line currents increase in the same way as in the diode circuit. One half cycle after the fault occurrence, the gate firing pulses are delayed to the inversion end stop of about 160°. The negative half cycle of the line voltage appears across the coil, thus forcing the coil current to decrease. By firing the thyristors at the safe commutation level of about 160°, the line current can be reduced to zero in less than two cycles. As with the diode circuit, the ac switch limits the fault current from the moment the fault current becomes larger than the coil bias current by inserting a large impedance, L, into the circuit. Because the ac switch reduces the current to zero, an inexpensive disconnect, that opens when the current is zero, can be used in place of an expensive circuit breaker.

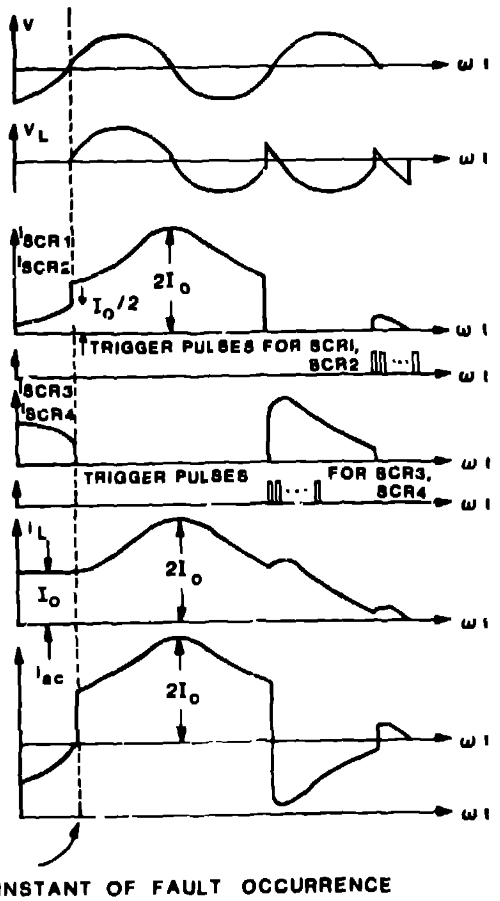

Fig. 4. Currents and voltages in superconducting current limiter and ac switch during fault conditions.

Coil Size Optimization

An optimal coil size must be determined to design an economical superconducting FCL. The price of a superconducting coil is, to a first approximation, proportional to the peak stored magnetic energy. If a very small inductance is chosen for the FCL circuit, the coil current would increase to a very high value during a fault until the breaker opens. This would lead to a high value of magnetic energy and to an expensive coil. A very large inductance would limit the fault current to a relatively low value; however, the magnetic energy is still large. Between these two extremes a coil inductance can be chosen that results in the smallest stored energy. To minimize the coil price, the maximum magnetic energy of the coil, W_{max},

$$W_{max} = \frac{1}{2} L I_{Lmax}^2, \tag{2}$$

has to minimized. The current, I_{Lmax}, is the maximum current in the coil that occurs at breaker opening time for the FCL or, in the worst case, at one half cycle after fault occurrence for the ac switch. The current I_{Lmax} consists of two components, the bias current, I_o, and the current increase, $n\Delta I$, caused by the line voltage, $v = V_{max} \sin \omega t$, impressed for n half cycles on the coil;

$$I_{Lmax} = I_o + n\Delta I \tag{3}$$

During one half cycle the coil current increases by the amount,

$$\Delta I = \frac{V_{avg}}{L} \frac{T}{2}, \tag{4}$$

with the sinusoidal voltage averaged over one half cycle as

$$V_{avg} = \frac{2V_{max}}{\pi} \tag{5}$$

and the period, T, of the sine wave. Inserting equation (4) into (3) and equation (3) in turn into (2) results in

$$W_m = \frac{1}{2} L I_o^2 + I_o n \frac{V_{avg} T}{2} + n^2 \frac{V_{avg}^2 T^2}{8L}. \tag{6}$$

The value I_o is determined by the current value to be limited and is not a parameter. The magnetic energy is a function of the inductance, L. Differentiating W_m with respect to L results in

$$\frac{dW_m}{dL} = \frac{1}{2} I_o^2 - \frac{n^2 V_{avg}^2 T^2}{8L^2}. \tag{7}$$

The magnetic energy has its minimum for the coil inductance

$$L = \frac{n V_{avg} T}{2 I_o}. \tag{8}$$

Note that the inductance for a coil with the smallest stored energy is only proportional to the number of half cycles of breaker opening time. By choosing an inductance according to Eq. (8), the breaker current at opening time, which is identical to the maximum coil current, is always $2I_o$. This represents very effective current limiting. The fault current is only about 1/30th of the maximum fault current that could occur without the limiter in the circuit. The above derivation shows that the optimal coil for an ac switch (n = 1) is one half or one fourth the size of the coil for the diode FCL circuit, depending on the respective use of a one cycle (n = 2) or two cycle (n = 4) breaker. Plotting of the magnetic energy as a function of optimum inductance with n as the parameter gives a set of curves for sets of V_{avg} and I_o values with shallow minima. Deviation of ± 20% from the theoretical optimum results in only a small increase of stored magnetic energy and coil cost.

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