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Fault-Tolerant Operation Strategy for Reliability Improvement of a Switched-Capacitor Multi-Level Inverter

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***Abstract*— the necessity of using several components in multilevel inverters jeopardizes the reliability of their operation. Hence, the aim of this research is to propose a novel single-phase fault-tolerant topology based on switched-capacitor concept to ensure robustness of the converter in the occurrence of a fault. The proposed single source converter steps up the input voltage seven times with a simple control strategy. Fault Tolerance of the converter is achieved by considering multiple fault cases and providing several redundant switching schemes concerning the type and location of failure. Each switching scheme is designed in a way to ensure the tolerability to both single and multiple open/short circuit failure. Also, self-voltage balancing of the capacitors, as well as the same amount of voltage levels and amplitude in the output is guaranteed. Experimental analysis is carried out, and the results confirm the viability of the proposed inverter under normal and post-fault operating modes**.

***Index Terms*—Multi-Level Inverters, Fault Tolerant, Single source, Switched-Capacitor, Reliability assessment.**

I. INTRODUCTION

Nowadays, renewable energy sources are gaining higher attention from industries for their clean nature and supportive government regulations. The integration of such low voltage DC sources to the existing AC power grids has necessitated the application of Multilevel Inverters (MLIs) [1]. Moreover, MLIs have become popular in many applications such as photovoltaic systems [2], uninterrupted power supply [3], solid state transformers [4], and electric vehicles [5]. These structures benefit from better output quality, improved performance, lower voltage stress on their switches, and less Total Harmonic Distortion (THD)[6], [7]. However, MLIs have a higher number of devices and a more complex control system compared to two-level conventional ones [8]. This may lead to a greater failure rate, which can hinder them from appropriate operation. Hence, it is important to investigate the reliability and fault tolerance constraints of MLIs. To meet the reliability restrictions, continuous operation despite the failure is essential.

Fault-Tolerant (FT) operation of an MLI is a combination of procedures executed to preserve its performance close to the normal one. Generally, FT operation consists of detection, location, and isolation of the inoperative section and thereupon, performing an appropriate corrective action (post-fault strategy) [9]. Various FT strategies are studied and introduced in the literature, as categorized in Fig 1. Accordingly, most researchers have introduced a post-fault strategy either by adding auxiliary hardware to the inverter or by changing the software of the conventional structure. Auxiliary hardware addition is achieved by reconfiguring or modifying the circuit topology to help the operation of the MLI in faulty conditions. This strategy suffers from the complexity, cost, and size increment of the MLI that may not be realizable in every situation. Thus, several viable approaches are proposed by just modifying the control strategy of the circuit through either modulation or operation control of the inverter. These strategies make it possible to continue the proper operation after failure. Consequently, the reliability of the converter would improve. The authors in [10], [11] introduced fault-tolerant MLIs with redundant operation states in the form of different switching strategies to reduce the downtime and also improve the robustness of the inverter. Although [10] has the same output voltage levels in post-fault, capacitors' voltages balancing is lost in some fault situations. [11] proposed a topology with the ability to tolerate open and short circuit faults of its switches; however, only some of the switches are fault-tolerant. Therefore, the converter is partially fault-tolerant. The authors in [12] introduced a modified flying-capacitor structure to perform properly in case of a fault. [13]–[15] added a parallel redundant leg to the main module, ensuring a post-fault operation under single and multiple switch faults. Similarly, in [16] an H-bridge is used as a redundant leg in case of fault occurrence. While the number of the generated voltage levels is constant for [14]–[16] after the failure, some voltage levels are lost in single or multiple switch failures in [13]. [17] introduced a bypass mechanism to isolate the faulty part and then restores the voltage amplitude by sharing the voltage deficit among other healthy modules.

Fig. 1.Different fault-tolerance methods proposed for MLIs

In some studies, an additional module is inserted for each leg to achieve an appropriate performance during fault occurrence. [18], [19] added an extra redundant module to the conventional modular multilevel converter. A fault analysis of the MLI structure presented in [20], is provided in [21]. This inverter uses an end-side H-bridge module to generate a bipolar output voltage as well as [22] that suffers from this issue. The problem with an end-side H-bridge is that its switches have to withstand the maximum output voltage, which limits their use in low/medium voltage applications. However, the occurrence of

a fault on a single switch of the H-bridge would render the inverter useless.

This work aims to investigate the fault tolerance of a novel switched-capacitor MLI. The performance of the proposed inverter is evaluated under normal operation and various failures. To reach these goals, this study is organized as follows: In section II, the principle of the proposed topology, its normal switching states, and design considerations such as capacitance calculation and power loss analysis are studied. Then, a comprehensive discussion over the converter performance under various short and open circuit faults is provided, and several fault cases are analyzed in section III. Afterward, the reliability and comparative analyses of the proposed inverter are investigated in section IV. Additionally, the effectiveness of proposed FT strategy through experimental examinations are carried out in section V. Lastly, the paper is concluded in section VI.

II. Topology Description

The overall configuration of the proposed inverter is depicted in Fig 2. This structure consists of two smaller sub-converters paralleled to a single DC source (V_{dc}), which can directly charge multiple capacitors at each stage. The proposed converter uses several capacitors to make a near-sinusoidal staircase voltage by a combination of series connection of capacitors, which does not need any inductors or transformers. Thus, it has lower weight and smaller size and consequently, lower cost. The converter is capable of boosting the input, producing 15-levels of voltage ($\pm7V_{dc}$, $\pm6V_{dc}$, …, $\pm1V_{dc}$, and 0) with eight capacitors, 36 switches, and 30 driver circuits. One of the main advantages of the presented converter is that it can produce a bipolar output without using an H-bridge. This means that no switch has to endure the peak output voltage. So, the converter has a low Peak Blocking Voltage (PBV) and therefore, a low Total Blocking Voltage (TBV). By switches bearing a lower voltage stress, the failure probability decreases and accordingly, the employment of the converter in high voltage/power application with low input voltage increases.

A. Principle of Normal Operation

The charging pattern of the capacitors can be seen in Fig. 2. Each of the capacitors is charged up to V_{dc} (unary charging) by being connected parallel to the source at different output levels. In this way, the capacitors are getting fully charged and balanced automatically without any external controllers and voltage sensors. In order to create different voltage levels, the input source and the capacitors should be connected in series and discharged to the load. Different modes of operation and the switch states for the desired output levels are illustrated in Fig 2. Among many available paths, optimal ones are selected to achieve the best voltage balancing of the capacitors. Nearest Level Modulation (NLM) is adopted to control the operation of the proposed converter (Fig. 3). By applying this technique, the desired output voltage waveform is formed by tracking the nearest voltage level (V_{nl}) to the reference voltage (V_{ref}). Then, the time intervals of each level are estimated and corresponding switching states are selected [23]. Using this method simplifies the control process in achieving high number of output levels.

B. Capacitance Calculations

Calculation of the capacitances is essential to ensure that capacitors' voltages do not fluctuate more than a certain

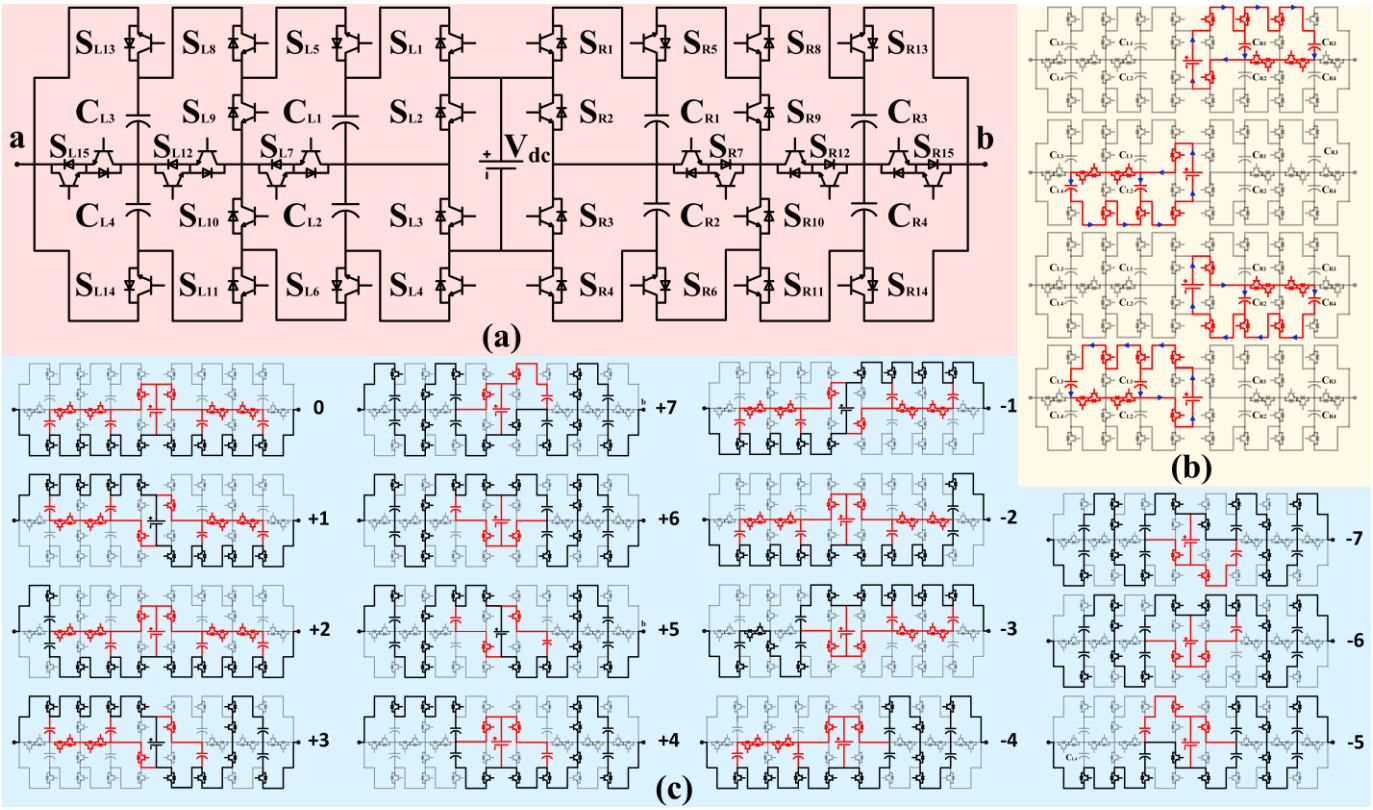

Fig. 2. (a) Overall structure of the proposed FT-MLI, (b) capacitors' charging paths, and (c) current paths of each output voltage level in normal operation mode

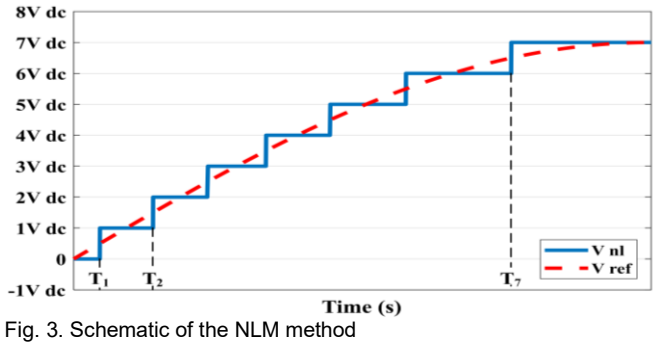

Fig. 3. Schematic of the NLM method

amount. As these voltages contribute to synthesizing the output voltage, the capacitors' voltage ripple is confined to a selected range. This voltage drop depends on the magnitude of the output current, output frequency, and the charging and discharging time of the capacitors [24]. Thus, the amount of charge pumped to the output by the capacitors can be calculated and used to determine the capacitances for a permissible voltage ripple. Considering the amplitude of the output current (I_{out}) with the output frequency (f_{out}), the maximum discharging of each capacitor (ΔQ_{Ci}) is obtained by (1).

$$\Delta Q_{Ci} = \int_{t_{1i}}^{t_{2i}} I_{out}\sin(2\pi f_{out}t - \varphi)dt \quad (1)$$

Where, the longest discharging period happens in [t_{1i}, t_{2i}]. Since all the capacitors are fed by the input dc source, all their voltages are equal to the amplitude of the input source. Therefore, the capacitances of all capacitors would be the same. Then, assuming maximum voltage ripple of k and a resistive load of R, the capacitances (C_{Li}, C_{Ri} for i=1, 2, 3, 4) of the proposed structure can be calculated by:

$$C_{Li} = C_{Ri} \geq \frac{\Delta Q_{Ci}}{kV_{dc}} = \frac{7}{k.R}\int_{t_{1i}}^{t_{2i}} \sin(2\pi f_{out}t)dt \quad (2)$$

Accordingly, the variation of the circuit capacitances versus load changes and the ripple curtailment is illustrated in Fig. 4.

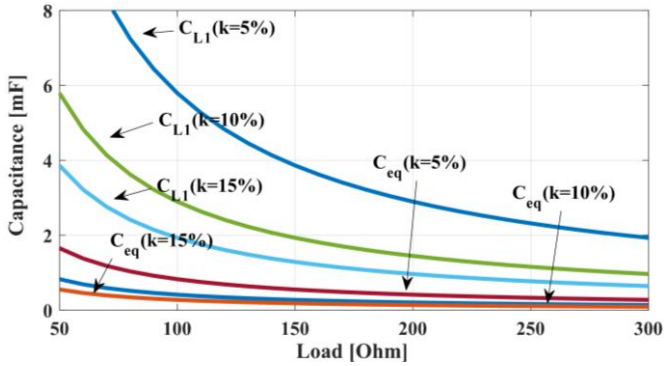

Fig. 4. Circuit capacitances versus load changes

C. Power loss analysis

Generally, power loss in switched-capacitor converters is classified into three groups: switching loss, conduction loss, and the loss caused by capacitor voltage ripple [7].

1) Switching losses

Switching loss is caused by a delay in the switch's turning on and off, which can be calculated by (3), (4).

$$P_{s,on} = \frac{1}{6}f_s V_{off-state} I_{on-state}.t_{on} \quad (3)$$

$$P_{s,off} = \frac{1}{6}f_s V_{off-state} I_{on-state}.t_{off} \quad (4)$$

Where, $V_{off\text{-}state}$ and $I_{on\text{-}state}$ are off-state voltage and switch current when the switch becomes fully turned on, respectively [25]. Thus, the total switching loss of the circuit (P_{sw}), which is the sum of turn-on and turn-off losses, is calculated by (5):

$$P_{sw} = \sum_{j=1}^{N_{switch}} \left(P_{sj,on} + P_{sj,off}\right) \quad (5)$$

2) Conduction losses

Conduction loss for power switches and power diodes in each level (L) is calculated as follows [24]:

$$P_{con-L} = (k_1 V_{on}^{sw} + k_2 V_{on}^{D}) i_{av-L} + (k_1 R_{on}^{sw} + k_2 R_{on}^{D}) i_{rms-L}^2 \quad (6)$$

Where, V_{on}^{sw}, V_{on}^{D} are the on-state voltage of the switches and diodes, respectively. Also, R_{on}^{sw} is the on-state resistance of switches and R_{on}^{D} is on-state resistance of diodes. The number of circuit elements involved in forming each level is listed in Table I. Moreover, $i_{rms\text{-}L}$ and $i_{avg\text{-}L}$ are the RMS and average current of semiconductors in each level (for [t_a, t_b]) for a quarter of a cycle, obtained from (7).

$$i_{av-L} = \frac{4}{T}\int_{t_a}^{t_b} I_m \sin\omega t dt\,, \quad i_{rms-L} = \sqrt{\frac{4}{T}\int_{t_a}^{t_b} (I_m \sin\omega t)^2 dt} \quad (7)$$

TABLE I
EQUIVALENT PARASITIC RESISTANCE FOR EACH LEVEL

Output voltage Level (×V_{dc})	0	±1	±2	±3	±4	±5	±6	±7
No. of Switches (K_1)	4	4	5	7	8	10	10	13
No. of Diodes (K_2)	4	4	2	3	2	2	2	1

Finally, the total conduction losses for the proposed inverter can be calculated by:

$$P_{con}^{total} = \sum_{L=1}^{7} P_{con-L} \quad (8)$$

3) Losses due to the capacitors voltage ripple

The difference between the DC input voltage (V_{dc}) and each capacitor's voltage is the origin of the capacitor ripple loss [7]. The voltage ripple of a capacitor is acquired from:

$$\Delta V_{ripple,C} = \frac{1}{C}\int_{t_c}^{t_d} i_c(t)dt \quad (9)$$

It is worth mentioning that, i_c is the capacitor's current, and [t_c, t_d] is its discharge time. So, the capacitor's ripple losses can be calculated by (10).

$$P_{Rip} = \frac{f_{out}}{2}\left(C_i \Delta V_{ripple,C}^2\right) \quad (10)$$

Finally, sum of the losses and efficiency are calculated by (11), where P_{loss} and P_{out} are the converter's loss and output powers, respectively. Figure 5, provides an overview of the circuit's efficiency curves for various loads and input voltages.

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}} = \frac{P_{out}}{P_{out} + P_{sw} + P_{Con} + P_{Rip}} \quad (11)$$

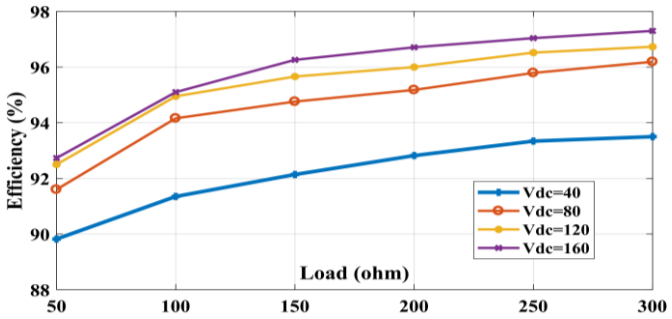

Fig. 5. Efficiency curves for various loads at different input voltages

III. Fault-Tolerant Operation Strategy

Since the proposed converter consists of two parallel identical sub-converters (left side and right side), the impact of faults on one sub-converter is analyzed considering that the other side is intact. The first step to analyze the effects of faults is to categorize them. Hence, various types of open circuit (OC) and short circuit (SC) faults on switches and capacitors are investigated, and then different strategies are also adopted. Accordingly, if fault occurrence leads to the loss of a capacitor in its path, to mitigate the effects of the lost capacitors on the output levels, a new capacitor charging strategy is used. For this reason, the second-tier capacitors ($C_{L3,4}$ or $C_{R3,4}$) are charged twice the input voltage ($2V_{dc}$) which is possible by series connection of the first-tier capacitors (binary charging) (Fig. 6). The first-tier capacitors ($C_{L1,2}$ and $C_{R1,2}$) are charged to the input voltage as before. In this way, same output levels and amplitude will be maintained. It is worth noting that by adopting this charging strategy in normal operation mode, the proposed converter is capable of producing a 23-level output voltage.

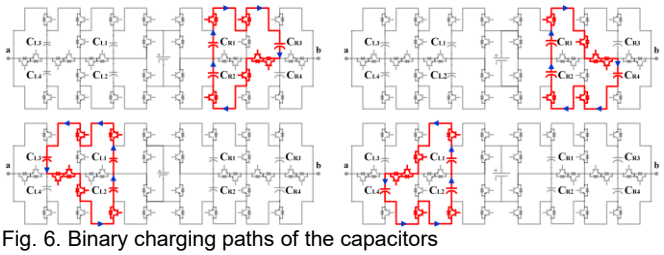
Fig. 6. Binary charging paths of the capacitors

The proposed inverter is capable of operating under various types of faults. For this reason, four redundant switching schemes for various fault cases, including single or multiple faults are defined and presented in Table II. Furthermore, all fault zones corresponding to each case are visualized in this table. After a fault is detected, the appropriate switching scheme is applied, and the inverter continues to operate with the same output voltage (15 levels). The overview of the proposed FT control algorithm is illustrated in Fig 7.

1) *Case A*

If OC fault occurs in one or more of the switches, including (S_{R2}, S_{R4}, S_{R6}, S_{R10}, S_{R11}, S_{R14}) or the capacitors (C_{R2}, C_{R4}), the relevant switching scheme will be implemented. Hence, the fault location will be isolated by turning the faulty parts off. Similarly, this switching scheme could be employed, if SC fault occurred in one of the switches (S_{R6}, S_{R10}, S_{R11}) and in one or both of the (S_{R1}, S_{R3}) switches or the capacitors (C_{R2}, C_{R4}). Also, the corresponding current paths are represented in Fig. 8.

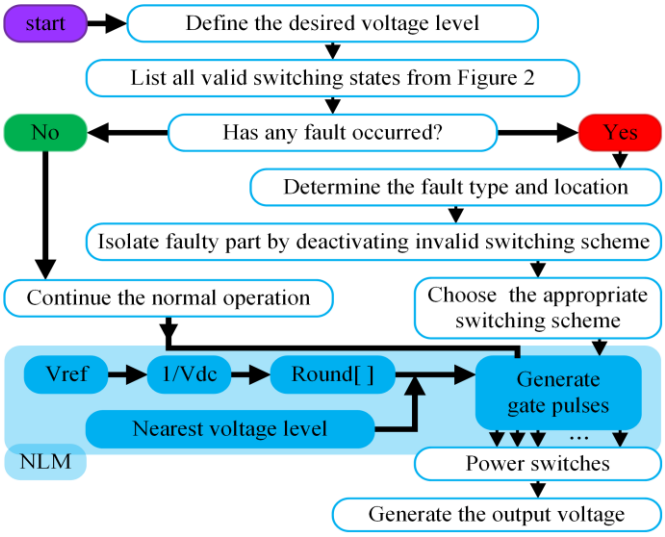

Fig. 7. Flowchart of FT control strategy

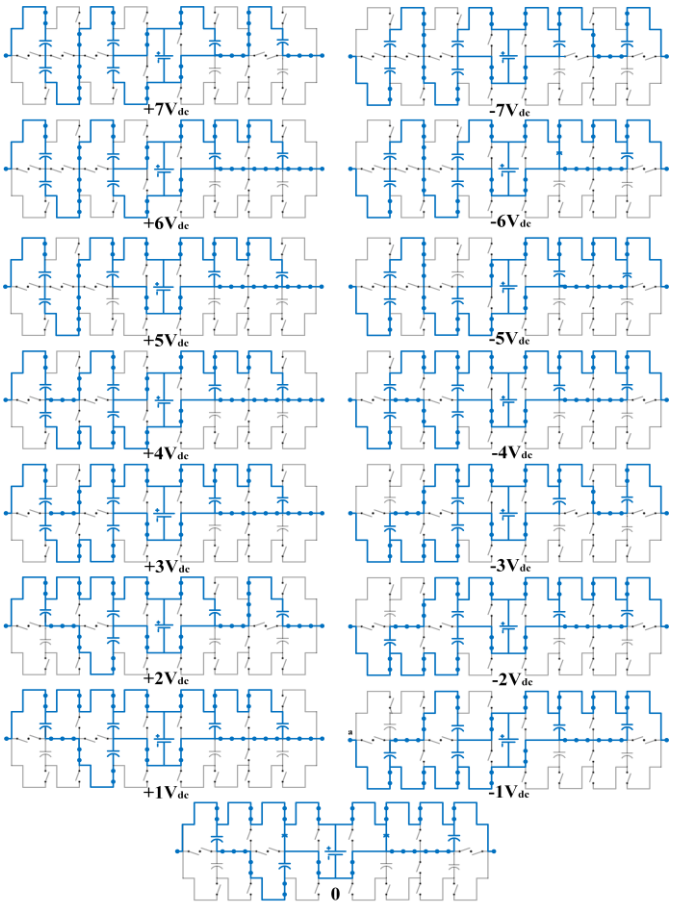

Fig. 8. Current paths for case A

2) *Case B*

The same approach can be applied to a second group of switches. If any of the following cases of fault happen, the switching scheme shown in Table II-B is implemented:

- OC fault occurs in one or more of switches (S_{R1}, S_{R3}, S_{R5}, S_{R8}, S_{R9}, and S_{R13}) or the corresponding capacitors (C_{R1}, C_{R3})
- Or SC fault occurs in one of (S_{R5}, S_{R8}, S_{R9}) and for one or both of (S_{R2}, S_{R4}) switches or the capacitors (C_{R1}, C_{R3}).

TABLE II
ON Switches in Post-Fault Scheme for Fault Cases A to D

L	Case A		Case B		Case C		Case D	
	Left Side	Right Side	Left Side	Right Side	Left Side	Right Side	Left Side	Right Side
0	13,12,10,8,6,5,3,1	1,3,5,7,8,12,13	14,12,11,9,6,5,4,2	2,4,6,7,11,12,14	2,4,6,11,14	14,12,11,9,6,5,4,2	14,12,12,9,6,5,4,2	2,4,6,11,13,14,15
1	13,12,10,8,6,5,3,1	1,3,5,7,8,12,15	13,12,10,8,6,5,3,1	2,4,6,7,11,12,14	2,4,6,11,14	13,12,10,8,6,5,3,1	13,12,10,8,6,5,3,1	2,4,6,11,13,14,15
2	13,12,10,8,6,5,3,1	1,3,7,8,9,15	15,12,11,9,6,5,4,2	2,4,6,7,11,12,14	1,3,6,11,14	13,12,10,8,6,5,3,1	15,12,11,S9,6,5,4,2	2,4,6,11,13,14,15
3	13,12,11,9,6,5,3,1	1,3,5,7,8,12,15	13,12,11,9,6,5,3,1	2,4,6,7,11,12,14	1,3,6,11,14	13,12,10,8,6,5,4,2	13,12,1,9,6,5,3,1	2,4,6,11,13,14,15
4	13,12,11,9,6,5,4,2	1,3,5,7,8,12,15	13,12,11,9,6,5,4,2	2,4,6,7,11,12,14	2,4,6,11,14	13,12,11,9,6,5,4,2	13,12,11,9,6,5,4,2	2,4,6,11,13,14,15
5	13,11,10,9,5,3,1	1,3,5,7,8,12,15	13,11,10,9,5,3,1	2,4,6,7,11,12,14	1,3,6,11,14	15,11,10,9,5,4,2	13,11,10,9,5,3,1	2,4,6,11,13,14,15
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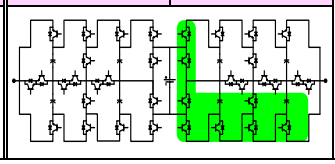
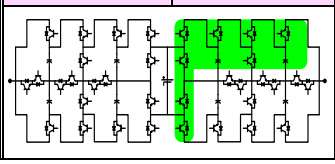
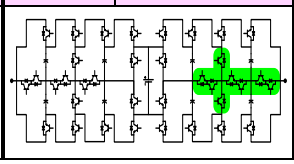
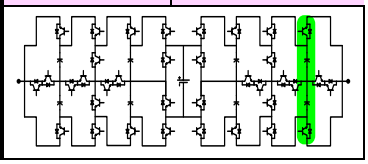
Fault Zones								

3) *Case C*

Case C is devoted to fault on bidirectional switches and its switching strategy (Table II-C) will be applied, when:

- OC fault has occurred in one or more of (S_{R7}, S_{R12}, S_{R15})
- Or SC fault occurred in one of (S_{R7}, S_{R12}, S_{R15}) or for one or both of (S_{R9}, S_{R10}) switches.

4) *Case D*

If an SC fault happens on one or both of S_{R13} and S_{R14}, capacitors C_{R3} and C_{R4} will be short-circuited and their voltages compromised. Thus, for the post-fault operation, S_{R13}, S_{R14} and S_{R15} are considered ON and C_{R3} and C_{R4} are not used anymore. The corresponding switching pattern under such fault is described in Table II-D.

IV. Topology Evaluation

A. Reliability Investigation

The chance of proper operation of an equipment in a specified time is introduced as reliability analysis [21]. For this reason, the failure ratio of each device component during this time is considered per 10^9 hours denoted by λ [26]. Thus, reliability function (R) is introduced as follows:

$$R(t) = e^{-\int_0^t \lambda(t)dt} \quad (12)$$

Reliability analysis of a converter ($R_{converter}$) is obtained by calculating the reliability functions of all the circuit components, including switches (R_{sw}) and capacitors (R_c) as follows:

$$R_{converter}(t) = R_{sw}(t) + R_c(t) \quad (13)$$

For a converter that can operate properly with (k) number of components, including n switches and m capacitors in the circuit, $R_{converter}$ can be calculated by:

$$R_{converter}(t) = \prod_{i=1}^{n} e^{-\lambda_{swi}t} \prod_{i=1}^{m} e^{-\lambda_{c_i}t} \quad (14)$$

According to 'i out of k' redundant structure method, for investigating FT converters working with (i) number of circuit components out of overall (k) number, $R_{converter,}$ can be mathematically modeled for both healthy and faulty conditions [26], [27]. For the proposed converter, because of topology symmetry, 18 switches and four capacitors are considered in this investigation. Besides, since, each circuit component is vulnerable to separated factors, reliability calculation for each device is a bit different, which should be considered. Switches are exposed to the operating voltage, manufacturing technology, quality, and environmental factors. Thus, the failure ratio of each switch (λ_{sw}) can be calculated by:

$$\lambda_{sw}=\lambda_{b,sw}\,\pi_{t,sw}\,\pi_{s,sw}\times10^{-9}/h \quad (15)$$

In this equation, $\lambda_{b,sw}$ represents the base failure rate of each switch at $100^{\circ C}$ junction temperature (T_j) which is mainly related to the technology of that semiconductor device. Besides, the effect of temperature on switches is defined as temperature ratio ($\pi_{t,sw}$) determined by:

$$\pi_{t.sw} = e^{4640\left(\frac{1}{373}-\frac{1}{T_j+273}\right)} \quad (16)$$

Another crucial factor for obtaining useful lifetime of switches is related to their voltage stress. Considering operating standing voltage (V_{CE}) and nominal standing voltage ($V_{CE-rated}$) for each switch in the circuit, the stress factor of each switch ($\pi_{s,sw}$) is defined as:

$$\pi_{s.sw} = 0.22e^{1.7\left(\frac{V_{CE}}{V_{CE-rated}}\right)} \quad (17)$$

Similarly, considering ambient temperature (T_a) and capacitor's applied voltage ratio (s), base failure rate ($\lambda_{b,c}$) of an electrolytic capacitor can be achieved by (18). Besides, concerning capacitance coefficient (π_{cv}) as described in (19), the failure rate of the electrolytic capacitor (λ_c) can be mathematically modeled as represented in (20) [28], [29].

$$\lambda_c=\lambda_{b,c}\,\pi_{cv}\times10^{-9}/h \quad (18)$$

$$\pi_{CV}=0.34\times(C)^{0.18} \quad (19)$$

$$\lambda_{b.c}=3.175[s^3+8]e^{\left[5\cdot09\times\left(\frac{T_a+273}{378}\right)^5\right]}\times10^{-4} \quad (20)$$

Accordingly, failure rates of each switch and capacitor without any failure are calculated, and the results are brought in Table III. Consequently, the reliability of the healthy converter can be calculated by (14). On the other hand, for calculating $R_{converter}$ in faulty conditions, the failure rates of all switches and capacitors in the post-fault operating mode should be recalculated [21]. For example, if S_{R1} fails at the moment of t_1 and all other parts continue their operation to the moment of t, the reliability of the converter will obtain through (21). Similarly, this task should be performed for all the circuit components as well.

TABLE III
FAILURE RATES OF CIRCUIT COMPONENTS IN HEALTHY OPERATION

component	failure rate
$\lambda_{sw,R1}=\lambda_{sw,R2}=\lambda_{sw,R3}=\lambda_{sw,R4}=\lambda_{sw,R7}=\lambda_{sw,R9}=\lambda_{sw,R12}=\lambda_{sw,R15}$	0.6355×10^{-5} /h
$\lambda_{sw,R5}=\lambda_{sw,R6}=\lambda_{sw,R8}=\lambda_{sw,R11}=\lambda_{sw,R13}=\lambda_{sw,R14}$	0.7118×10^{-5} /h
$\lambda_{c,R1}=\lambda_{c,R2}$	1.128×10^{-5} /h
$\lambda_{c,R3}=\lambda_{c,R4}$	1.069×10^{-5} /h

Then, regarding 21/22 redundant structure method, $R_{converter}$ can be achieved through (22).

$$R_{f.R1}(t)=\int_0^t \lambda_{sw.R1}e^{-\lambda_{sw.R1}t_1}\left[\prod_{i=2}^{36}e^{-\lambda_{sw.i}t_1}\right]\left[\prod_{i=2}^{36}e^{-\lambda_{sw.i}'(t-t_1)}\right]\left[\prod_{i=1}^{8}e^{-\lambda_{c_i}t_1}\right]\left[\prod_{i=1}^{8}e^{-\lambda_{c_i}'(t-t_1)}\right]dt \quad (21)$$

$$R(t)=R_{normal}+2\times(R_{f,R1}+\ldots+R_{f,R18})+2\times(R_{f,C1}+\ldots+R_{f,C4}) \quad (22)$$

B. Comparative study

A detailed comparison of the proposed FT-MLI with recent FT topologies is investigated in this section, and the results are brought in Table IV. This assessment includes the number of required components for generating the desired voltage levels, and their operational factors such as boosting ratio, PBV, and TBV. Also, the FT performance of these topologies under different types of single/multiple, OC and SC faults is investigated. Obviously, the ability of the converter to maintain its voltage levels under different probable faults is a key factor. Accordingly, the proposed inverter generates a 15 level voltage (with a boosting ratio of 7) by using a single DC source and low voltage stresses on all the components (PBV=$2V_{dc}$ or $0.28V_{out\_max}$). Moreover, the structure is capable of operating under various types of single and multiple failures on switches and/or capacitors while maintaining the same amplitude and number of voltage levels in its post-fault operation.

Similarly, [11], [13] benefit from the same FT capabilities, but this comes at the cost of using more semiconductors per level. Also, [13] requires two input sources to generate the intended levels. Although [15] introduced a highly resilient structure, it does not boost the input voltage. In other words, its boost ratio is limited to the sum of the two input sources. On the other hand, [21], [22], and [30] introduced FT topologies with a fewer number of circuit components per level, but they lose voltage levels in several probable failure cases. In addition, the use of an end-side H-bridge in [21] makes it more vulnerable to any type of faults and considerably reduces its reliability. Notably, the FT ability of [22], [31] is achieved by using 4 and 10 relays to bypass the faulty parts, respectively. Furthermore, the structures introduced in [31], [32], and [16] lose voltage levels after multiple switch faults (more than one).

TABLE IV
COMPARISON OF THE PROPOSED FT-MLI TOPOLOGY WITH SIMILAR ONES

Ref.	A	B	C	B/A	D	E	F	G	H	I	J	K	L	M	N
[30]	7	12	12	1.7	-	3	1	12	1	×	√	√	×	×	-
[32]	7	16	16	2.3	1	3	2	18	1	√	√	√	×	×	-
[31]	7	12	12	1.7	-	3	1	12	1	√	√	√	×	×	-
[16]	5	14	12	2.8	1	1	2	8	2	×	√	√	√	×	×
[22]	15	16	16	1.1	-	3	7	56	1	×	√	√	√	√	√
[21]	49	42	35	0.9	9	1	24	92	24	×	√	√	√	√	√
[13]	5	18	14	3.6	-	2	2	36	1	√	√	√	√	√	-
[11]	5	16	11	3.2	1	1	2	22	2	√	√	√	√	√	√
[15]	9	16	16	1.8	2	2	1	16	1	√	√	√	√	√	√
Prop.	15	36	30	2.4	8	1	2	46	7	√	√	√	√	√	√

***A: Number of output levels**
***B: Total number of semiconductor devices**
***C: Number of driver circuits**
***D: Number of capacitors**
***E: Number of sources**
***F: PBV (×Vdc)**
***G: TBV (×Vdc)**
***H: Boost ratio (Vout / Vdc)**
***I: Maintaining the same voltage levels after failure**
***J: Tolerant to single switch OC**
***K: Tolerant to single switch SC**
***L: Tolerant to multiple switch OC**
***M: Tolerant to multiple switch SC**
***N: Tolerant to capacitor failure**

Finally, to make a fair reliability comparison, the structures with similar fault-tolerance abilities were narrowed down to [21], [22], [30], and [31]. Accordingly, their reliability indexes were assessed and the relevant equations were calculated. Similarly, the reliability indexes for conventional MLIs including Neutral Point Clamped (NPC), flying Capacitor (FC), and cascaded H-Bridge (CHB) were calculated. Then, in order to better clarify their differences, the reliability of all the topologies versus operating hours is graphically compared in Fig. 9 With regard to this figure, the proposed structure shows a more promising behavior compared to the other counterparts.

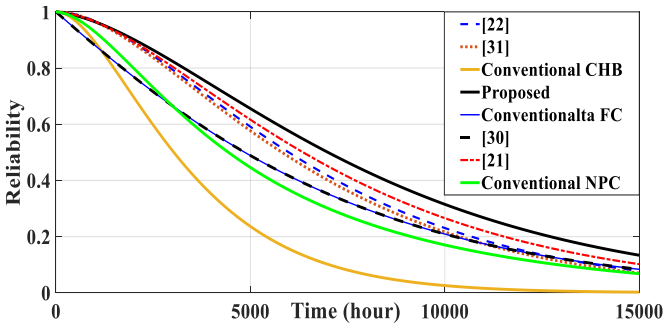


Fig. 9. Comparative Reliability analysis versus Lifetime of the proposed FT-MLI against other counterparts

V. EXPERIMENTAL RESULTS

To investigate the proposed topology and evaluate its performance, a laboratory prototype (Fig. 10.a) is implemented and examined under various loads and fault conditions, based on the specifications of Table V. Notably, the design procedure of the proposed inverter, like other switched-capacitor circuits, mostly involves determining the appropriate capacitances and semiconductors regarding the intended test criteria. Hence,

according to (2), Fig.4, and considering a $5 \le k \le 10$ percent voltage ripple for the desired operating point, 2200 µF is chosen for all the capacitors. Similarly, the switches are selected based on their PBV in the circuit and the rating of the test conditions. Moreover, to apply the NLM technique and generate the gate signals for the switches, a DSP microcontroller is used. Then, to protect the control circuit, these signals are isolated and amplified before being applied to each switch (Fig. 10.b).

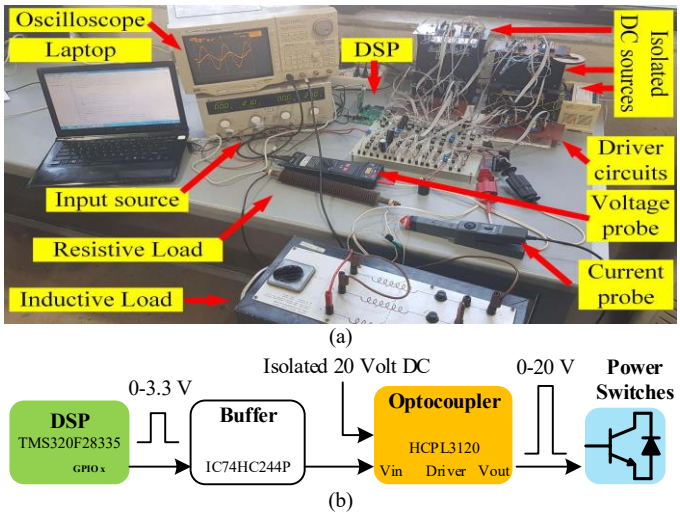


Fig. 10. (a) Experimental setup of the laboratory prototype, and (b) control diagram of the circuit switches

TABLE V
SPECIFICATIONS OF THE LAB PROTOTYPE

Parameter/ Component	Value
Input Voltage	40V-DC
Maximum output voltage	280V-peak AC
Output Frequency	50Hz
IGBT / Diode	12N60 / MUR860
Capacitors	2200µF
Load	Z_1=250 Ω
	Z_2=250 Ω +330 mH
	Z_3=130 Ω +76 mH

Fig. 11 depicts the experimental output voltage and current of the proposed topology under normal operating conditions, supplying resistive and resistive-inductive loads. A 15-level staircase voltage waveform with an amplitude of seven times the input voltage, is generated in the output using unary charging mode (Fig. 11. a and b). Also, Fig. 11.c shows the capability of the circuit to boost the input voltage up to eleven times and produce a 23-level voltage with binary charging mode. The experimental efficiency of the circuit versus load impedance variation under normal operating conditions and unary charging mode, is provided in Fig.12. Moreover, the performance of the circuit is assessed under sudden load change from Z_1 to Z_3 and the result is presented in Fig. 13. This shows that despite a sudden change in the load current, the circuit is well capable of maintaining its output voltage levels and amplitude.

To obtain a FT operation, four post-fault switching schemes are introduced in section III, where each one of them is associated with a certain zone of the circuit. The proposed algorithm works in such a way that the faulty zone is bypassed in an event of fault to maintain the output voltage levels.

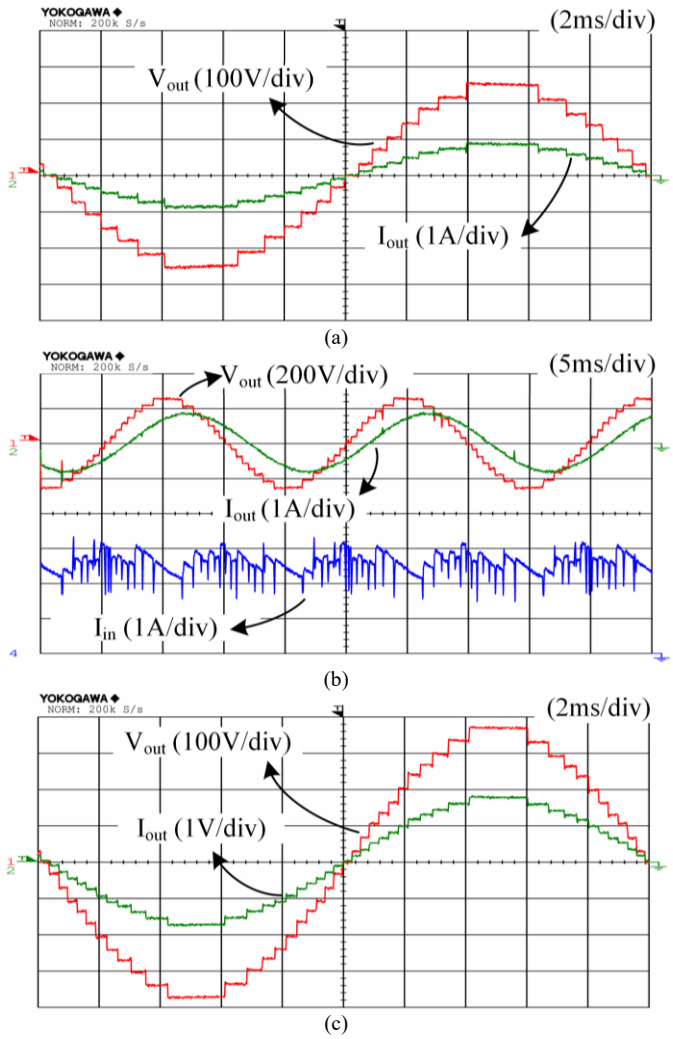


Fig. 11. Experimental results under normal operation for a (a) 15-level resistive load, (b) resistive-inductive load, (c) 23-level resistive load.

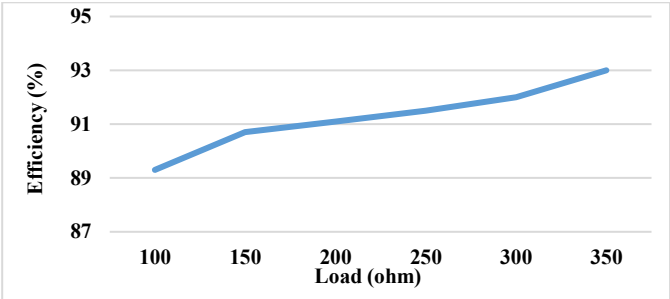


Fig. 12. Experimental efficiency versus load impedance variation

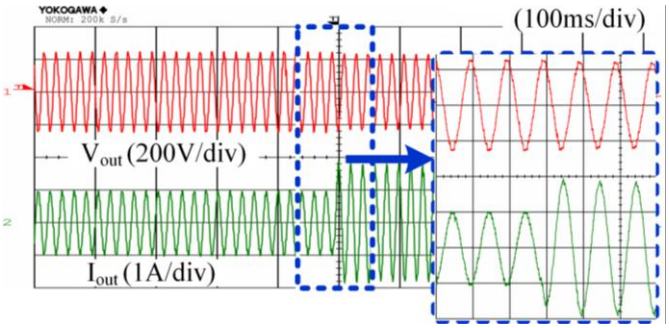


Fig. 13. Output waveforms under sudden load change from Z_1 to Z_3.

To validate the FT performance of the proposed inverter and schemes, and whether it maintains its output voltage despite any probable component failure, different faults corresponding to each case (introduced in Table II) are examined. Diverse fault types associated to each case are investigated in the following, which are extendable to all the other possible faults in that case. Each test includes three successive stages of the circuit during normal, mid-fault, and post-fault operation modes. Initially, the inverter performs normally. After the fault happens, the adequate switching scheme is applied regarding the proposed FT algorithm by adopting redundant current paths, which isolates the faulty part. The experimental results under an OC fault on S_{R5}, are illustrated in Fig. 14. After the fault happens, the switching scheme for fault case B is chosen to isolate the faulty part regarding the proposed FT algorithm. According to Fig. 14.a, the output voltage of the converter deteriorates under the fault and some levels of the negative half cycle are lost. Afterward, at the post-fault stage, the output is restored to the pre-fault conditions by adopting the new switching scheme. Fig. 14.b demonstrates that voltages of the first-tier capacitors on the healthy side (left-side) experience a mild drop and then recover slowly as the second-tier capacitors' voltages are doubled (due to binary charging strategy). Also, it indicates that by selecting capacitances properly, their voltage ripple will remain in the desired boundaries. It should be noted that the effect of OC fault on S_{R5} is similar to OC on other circuit components in that particular fault zone, which is the removal of C_{R1} and C_{R3} form the output voltage (discussed in case B on section III). Thus, the experiment is not repeated for them.

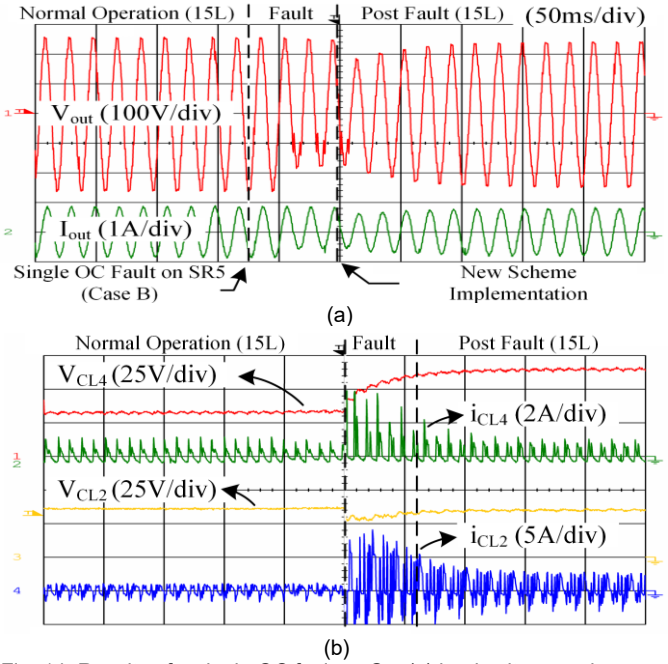


Fig. 14. Results of a single OC fault on S_{R5} (a) load voltage and current, (b) waveforms of C_{L4} and C_{L2}.

In addition, the harmonic contents of the experimental output voltage are obtained under normal and post-fault operation modes and the results are shown in Fig. 15. According to results, the inverter satisfies the IEEE-Std. 519-2014 requirements for harmonic content, in both conditions.

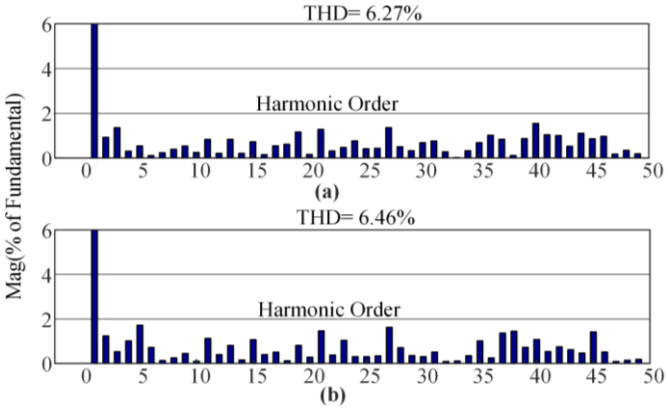


Fig. 15. Experimental harmonic spectrum of the output voltage (without any filters) under (a) normal and (b) post fault operation modes.

The effect of S_{R6} OC fault on the output waveforms of the converter is illustrated in Fig. 16.a. In this condition, some of the output voltage levels in the positive half-cycle are lost; because, the charging path of C_{R4} is cut off in the mid-fault stage leading to its voltage to drop and both C_{R2} and C_{R4} are not used anymore (Fig. 16.b). This issue is solved by implementing the appropriate switching strategy (case A) in which C_{R2} and C_{R4} are bypassed and are not further used for the post-fault stage of the operation. Notably, OC fault on S_{R2}, S_{R4}, S_{R10}, S_{R11} and S_{R14} has similar impact to the circuit like S_{R6} (case A on section III). Therefore, the test is not repeated for them.

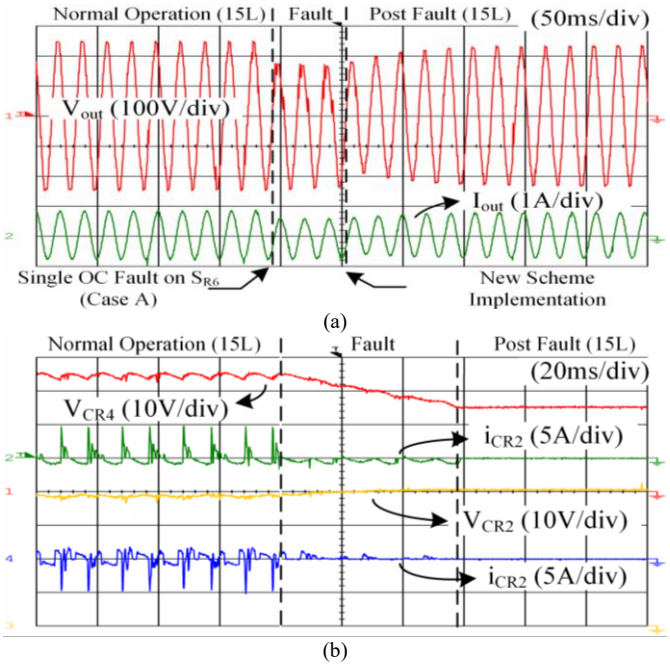


Fig. 16. Results of a single OC fault on S_{R6} (a) load voltage and current, (b) waveforms of C_{R4} and C_{R2}.

A multi OC fault scenario was created for S_{R2}, S_{R6}, S_{R10} and S_{R14}, in which all of them are facing OC fault, at the same time. As shown in Fig. 17, during the fault mode, the output voltage is severely deformed and its amplitude drops. In addition, C_{R2} and C_{R4} are disconnected due to the open-circuited parts. Thus, they are not incorporated for the post-fault operation of the circuit. Therefore, by implementing the new scheme (case A), the output voltage waveform recovers its initial value.

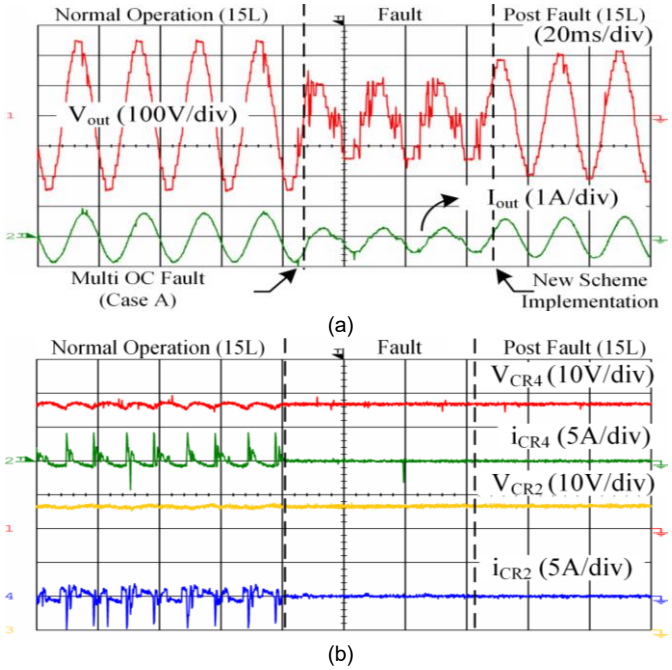


Fig. 17. Results of multi OC fault on S_{R6}, S_{R10}, and S_{R11} (a) load voltage and current, (b) waveforms of C_{R4} and C_{R2}

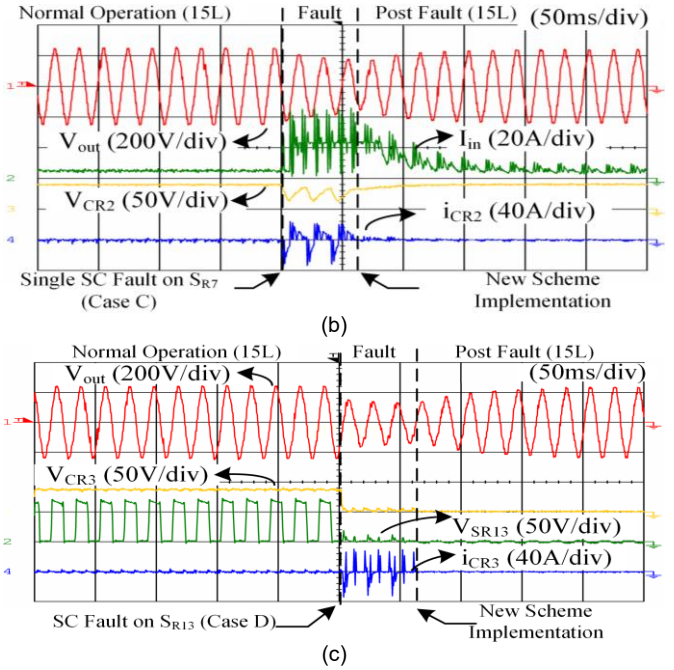
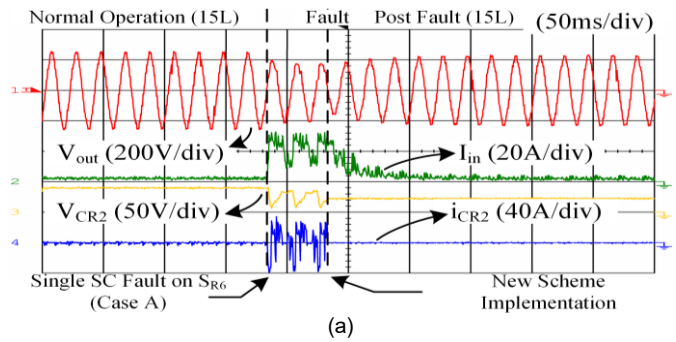


Fig. 18. Results of a single SC Fault on (a) S_{R6}, (b) S_{R7} and (c) S_{R13}

As the switches may face a short circuit failure, the effect of SC on S_{R6} are demonstrated in Fig. 18.a. In this situation, C_{R2} and the input source are short-circuited in some levels. As a result, their current significantly increases and voltage of C_{R2} drops. Persistence of this condition can harm the circuit as well as the input source; however, by applying the appropriate switching scheme (case A), the output voltage and current waveforms restore their normal values despite the problem. Also, C_{R2} is isolated from the output current path and its post-fault voltage remains the same. In another case of switch failure, the effect of SC on S_{R7} is presented in Fig.18.b. In this condition, C_{R1} and C_{R2} are short-circuited in some instances and as a result, during the charging period, the input source is short-circuited as well. Afterward, proper switching scheme (case C) is implemented leading to the load voltage recovering to its former normal state. Notably, unlike C_{R3} and C_{R4}, during the post-fault operation, C_{R1} and C_{R2} are still in use. Finally, the effect of SC on S_{R13} is depicted in Fig. 18.c, in which C_{R3} is also short-circuited; ergo, its current rises drastically and the load voltage is deformed. To fix this defect, the switching scheme for fault case D is adopted for the post-fault operation mode. The same result is achieved by applying the fault case D for the multiple SC fault on the S_{R13} and S_{R14}. Thus, the same experiment is not repeated.



VI. Conclusion

In this paper, a novel fault-tolerant multilevel inverter is proposed. The single-source topology can generate a 15-level output voltage despite short or open circuit failure on its circuit parts. Additionally, it can boost the input voltage seven times based on the switched-capacitor concept, with the inherent self-voltage balancing of the capacitors. FT operation is achieved by introducing additional switching schemes besides the main one to ensure the flawless post-fault performance of the circuit for any probable fault cases. In post-fault switching schemes, part of the healthy capacitors are binary charged while the faulty zone is bypassed. The presented FT strategy is applicable in both single and multiple failures and maintains both levels and amplitude of the output voltage without the necessity of any auxiliary component. Besides, the reliability of the presented structure is evaluated by the i out of k redundant method. Then, its superiority is proved in comparison to recent FT-MLIs and conventional ones. Eventually, experimental results of the proposed converter in normal operation mode and open/short circuit fault conditions are investigated, validating the favorable performance of the proposed FT strategy.

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