

Fault Tolerant QCA Logic Design With Coupled Majority-Minority Gate

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ABSTRACT:

Synthesis of efficient DFT (Design for Testability) logic is of prime importance in robustly testable design of QCA based logic circuits. An ingenious universal QCA gate structure, Coupled Majority-Minority (CMVMIN) gate, realizes majority and minority functions simultaneously in its 2-outputs. This device enables area saving implementation of complex QCA logic. In the current work, we investigate cost effective DFT for QCA designs realized with CMVMIN. The fault effects at the gate outputs due to cell deposition and cell misplacement defects are characterized for concurrent testable circuit design. The effective use of unutilized outputs of CMVMIN gates, realizing a circuit, leads to the proposed fault tolerant design that may not be possible with the conventional gate structures.

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