Fault Tolerant Three-Phase AC Motor Drive Topologies: A Comparison of Features, Cost, and Limitations

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***Abstract*—This paper compares the many fault tolerant three-phase ac motor drive topologies that have been proposed to provide output capacity for the inverter faults of switch short or open-circuits, phase-leg short-circuits, and single-phase open-circuits. Also included is a review of the respective control methods for fault tolerant inverters including two-phase and unipolar control methods. The output voltage and current space in terms of *dq* components is identified for each topology and fault. These quantities are then used to normalize the power capacity of each system during a fault to a standard inverter during normal operation. A silicon overrating cost factor is adopted as a metric to compare the relative switching device costs of the topologies compared to a standard three-phase inverter.**

***Index Terms*—Inverter faults, phase-leg short-circuits, silicon overrating cost factor (SOCF), single-phase open-circuits, three-phase inverter, three-phase ac motor drive topologies.**

I. Introduction

THE RELIABILITY of adjustable speed ac motor drives is an area of great interest for all members of the drives community and marketplace. This is particularly the case for the military, aerospace and automotive industries that are increasingly adopting variable speed drives in order to improve overall system efficiency and performance. There are certain safety critical applications such as steering, fuel pumps, and brake-by-wire systems, where operation of the drive is of paramount importance and continuous operation of the system must be insured. As a result, parallel redundancy is often employed for these systems, although at a high system cost.

The need for these fault tolerant systems has inspired much research in the area. Analysis, modeling, and simulation of various inverter and machine faults have been presented in many papers, and overviews of these results are given in [1] and [2].

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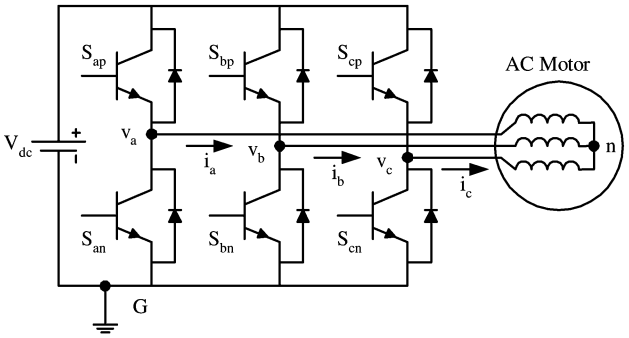

Fig. 1. Standard three-phase ac drive structure.

Modular parallel redundant systems have been proposed as a means of providing fault tolerance, as in [3]. Machine design modifications have also been proposed for improving the drive system fault tolerance, [4]. Systems with phase numbers higher than three have also received considerable attention as an approach to providing drive system redundancy [5], [6].

A great deal of research has been done on intelligent control methods for standard three-phase induction, permanent magnet, or synchronous reluctance motors to achieve some degree of fault tolerance. These control techniques have been combined with modified versions of the standard inverter bridge configuration (see Fig. 1) to create systems that are tolerant to one or more types of faults. Papers that report fault tolerant systems include [6], [12]–[15], and [18]–[21]. These papers all rightfully claim to provide fault-tolerant capabilities under the conditions specified. It is the goal of this paper to analyze each of the topologies and the control methods presented in these papers in order to compare the features, implementation costs, and performance limitations of each of the methods. New contributions in this paper include a comparison of silicon device ratings for each topology to that of a standard three-phase inverter and identification and normalization of the equivalent three-phase output capacity of each system in terms of the space vector voltage and current limits for each given fault.

II. Fault Tolerant Systems

A. Definitions and Comparison Metrics

The concept of a fault tolerant drive system is that it will continue to operate in a satisfactory manner after sustaining a fault. The term "satisfactory" implies a minimum level of performance after the fault, and will therefore be heavily influ-

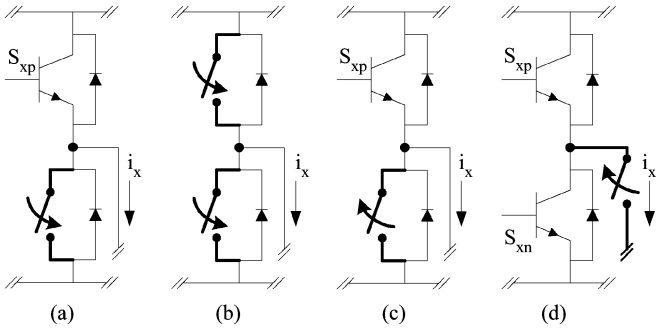

Fig. 2. Inverter faults considered: (a) single switch short-circuit, (b) phase-leg short-circuit, (c) single switch open-circuit, and (d) single-phase open-circuit.

enced by system requirements. While faults contained within the motor and dc link capacitors are serious events, this paper will limit itself to comparing fault tolerant topologies where the faults remain within the power inverter stage.

The faults under consideration (see Fig. 2) are

1) single inverter switch short-circuit;
2) phase-leg short-circuit;
3) single inverter switch open-circuit;
4) single-phase open-circuit (internal or external to inverter).

In an effort to quantify the cost associated with each of the topologies studied, and proposed, it will be useful to compare the rating requirements and output capacity of the topologies when compared to that of a standard three-phase inverter topology (Fig. 1). To quantify the output capacity of each of the systems in the presence of a fault, a fault power rating factor (FPRF) is proposed. This is defined as

$$\text{FPRF} = \frac{\text{maximum kVA output during fault}}{\text{max. kVA output of std. unfaulted inverter}}. \quad (1)$$

This FPRF rating is a normalization of the amount of power (kVA) that can be produced during the fault to the amount of power (kVA) that the standard inverter can produce during normal, unfaulted operation. Since the faulted output power rating is generally less than the unfaulted output power rating, the inverse of the FPRF can be used to determine a necessary additional overrating factor for all of the inverter components if the full rated output power is needed for the specified fault tolerant topology.

To compare the cost associated with the extra silicon devices in the fault tolerant topologies, a silicon overrating cost factor (SOCF) is proposed and defined as

$$\text{SOCF} = \frac{\text{weighted kVA rating of all switches}}{\text{kVA rating of standard inverter switches}}. \quad (2)$$

By this definition, the standard inverter would have a SOCF of 1.0, meaning that it does not have any additional switches present. For this calculation, it is assumed that each switch in the standard inverter has to block the dc bus voltage of 1 per unit (pu) and carry a peak phase current of 1 pu. Throughout the paper, the additional device ratings and output voltage and current capacities will be presented in terms of these base quantities.

The switch of choice in a modern drive is the IGBT (or MOSFET). Many of the topologies being compared add extra devices with the functional form of SCRs and TRIACs, which will likely be implemented as a pair of SCRs, connected back-to-back. Since these are lower-performance and lower-cost switches, this needs to be considered when calculating the SOCF. For this comparison, it will be assumed that

$$1 \text{ SCR} = 0.5 \text{ IGBT} \quad (3)$$

$$1 \text{ TRIAC} = 1 \text{ IGBT}. \quad (4)$$

For topology comparison purposes, the required anti-parallel diode for the IGBT is considered to be packaged inside the power switch module.

The relationships in (3) and (4) will be used to adjust the kVA rating of the extra components. These relationships reflect engineering approximations to the actual cost of the required components that also include the estimated cost impact of additional bus structures, control logic, and/or sensors. Looking forward, it is worth noting that the major conclusions of this paper do not depend on the precise values of these factors, and interested readers are invited to explore the impact of other values.

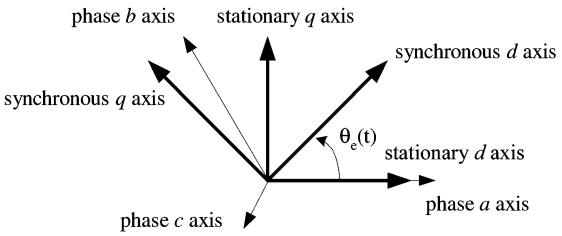

Fig. 3. Reference frame definitions.

For purposes of modeling and control, it is convenient to use the familiar direct and quadrature axis representation of the output capacity of the inverters. The reference frame definitions used in this paper are shown in Fig. 3. The transformations between the abc and dq coordinates are then given as

$$\begin{bmatrix} f_q^s \\ f_d^s \\ f_0^s \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ 1 & -\frac{1}{2} & -\frac{1}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} f_a^s \\ f_b^s \\ f_c^s \end{bmatrix} \quad (5)$$

$$\begin{bmatrix} f_q^e \\ f_d^e \\ f_0^e \end{bmatrix} = \begin{bmatrix} \cos\theta_e & -\sin\theta_e & 0 \\ \sin\theta_e & \cos\theta_e & 0 \\ 0 & 0 & 1 \end{bmatrix} \quad (6)$$

where f represents any voltage, current, or flux. The superscript s represents the stationary frame, and the superscript e represents the synchronous frame.

Using these definitions, the limits of the fundamental torque producing d and q axis voltage and current for the standard inverter are shown in Fig. 4. In the figure, the switching states of the inverter are also shown with "p" representing an upper switch turned on while "n" represents a lower switch turned on. Therefore, the state "pnn" has switches $S_{\text{ap}}, S_{\text{bn}}$, and S_{cn} turned on as labeled in Fig. 1. The standard inverter under unfaulted operation is capable of producing a fundamental peak phase voltage of 0.577 pu with space vector PWM without overmodulation. It is further capable of controlling a peak phase current of 1 pu as shown in the figure.

B. System Issues

The ability of a three-phase induction motor to operate with a single-phase excitation has been studied in many papers for well

TABLE I
CHARACTERISTIC RATINGS OF FAULT TOLERANT INVERTER TOPOLOGIES

Topology	Fuses	Split dc bus?	Auxiliary Switches	I rating of Auxiliary Switches (per unit)	Fault Power Rating Factor (*FPRF*)	Silicon Overrating Cost Factor (*SOCF*)	Fault Tolerant to			
							1 switch short	Phase.-leg short	1 switch open	1 phase open
Standard (Fig.1)	0	N	None	N/A	0	1	Not fault tolerant			
Switch-redt. top. (Fig.5) for open-phase faults	0	Y	1 (TRIAC)	1.73	0.50	1.29				X
Switch-redt. top. (Fig.5) for shorted switch faults	3	Y	3 (TRIAC)	1.00	0.50	1.50	X		X	
Switch-redundant topology (Fig.5)	3	Y	3 (TRIAC) 1 (TRIAC)	1.00 1.73	0.50	1.79	X		X	X
Double switch-redundant topology with a four terminal motor (Fig. 9)	8	N	8 (SCR) 2 (IGBT)	1.00 (SCR) 1.73 (IGBT)	0.58	2.24	X	X	X	X
Phase-redundant topology with a three terminal motor (Fig. 10)	6	N	6 (SCR) 3 (TRIAC) 2 (IGBT)	1.00 (SCR) 1.00 (TRIAC) 1.00 (IGBT)	1.0	2.33	X	X	X	X
Cascaded inverter topology (Fig. 11)	0	N	None	N/A	0.58	1.15				X
Cascaded inverter topology w/ TRIACs (Fig. 11)	0	N	3 (TRIAC)	1.00	0.58	1.44	X		X	X
Four-leg inv. top. w/ 2-phase control (Fig. 12)	0	N	2 (IGBT)	1.73	0.58	1.58				X
Four-leg inv. top. w/ unipolar control (Fig. 12)	0	N	2 (IGBT)	1.73	0.58	1.58			X	

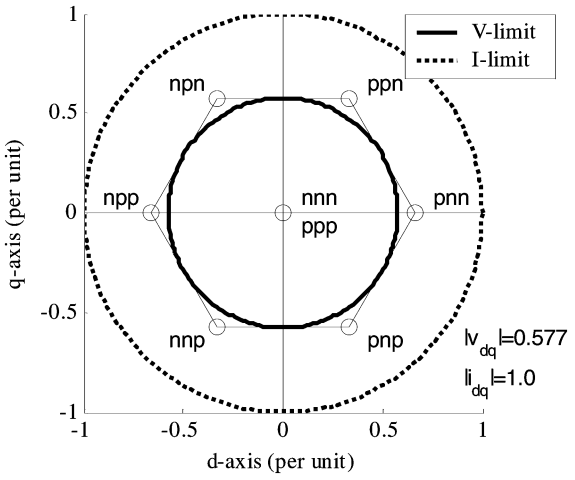

Fig. 4. Phase fundamental voltage and current limits of the standard inverter during normal unfaulted operation.

over 50 years. However, when operating with single-phase excitation, the torque produced is pulsating in nature. Furthermore, the motor has no starting capacity in this configuration. As a result of these limitations, it will be assumed that the standard three-phase inverter has no output capacity for a three-phase motor in the presence of a single-phase open-circuit fault or any of the other three inverter faults under consideration. In contrast, all of the other topologies and control methods presented in this paper are capable of self-starting and smooth torque production since they are capable of producing circular stator current trajectories in the dq plane.

It should also be noted that system efficiency will typically be reduced during faulted operation. Since faulted operation represents an emergency operating condition, system efficiency is assumed to be a secondary concern as long as the system is thermally able to accommodate increased losses. These incremental losses during post-fault operation are typically modest and dependent on the selected topology. Any topological changes that affect efficiency during normal operation are noted in Section III.

Any fault tolerant inverter drive topology is just one key part of a larger machine drive system. A fault tolerant system needs to incorporate an appropriate control architecture that includes a monitoring system, fault detection strategy, and controller reconfiguration for fault handling and subsequent post-fault operation. Several methods are available to detect open-circuit type faults [7], [8]. Short-circuit type faults can be detected by incorporating logic in conjunction with desaturation hardware protection [9], [10]. Controller reconfiguration has also been addressed, [11]. While necessary and important for a complete fault tolerant machine drive system, these control system considerations are beyond the scope of this paper and will not be discussed further here.

III. FAULT TOLERANT DRIVE TOPOLOGIES

Table I summarizes the capacities and requirements of the various fault tolerant topologies that have been proposed in the literature. Also included, for comparison, is the standard three-phase inverter. For this comparison, the capacity of the system under fault is given in terms of the unfaulted system capacity using the adopted fault power rating factor.

It should be noted that the dq voltage and current limits which characterize the output capacity of the various topologies are presented in terms of the fundamental frequency components. Several of the control methods use a zero sequence current component to maintain a circular flux trajectory after the fault. This detracts from the available fundamental current component due to the inverter switch current limits and is accounted for. However, the zero sequence voltage required to drive the zero sequence current is neglected. In typical ac machines, the zero sequence circuit consists of a very small impedance. Furthermore, there is no speed voltage term associated with the zero sequence circuit as there is with the fundamental frequency circuit. As a result, any zero sequence currents can be induced with, at most, a few percent of the total output voltage capacity of the inverter.

A. Switch-Redundant Topology

An early attempt to add fault tolerant capacity to a standard three-phase inverter topology for induction motors was pre-

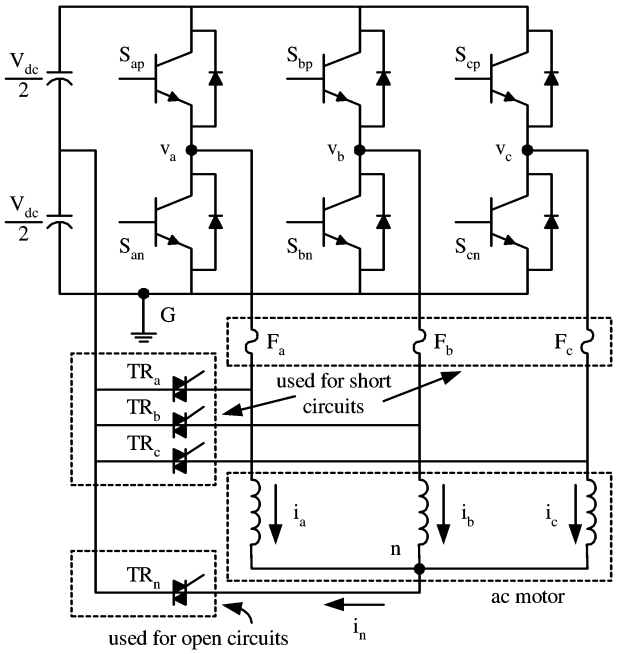

Fig. 5. Switch-redundant topology.

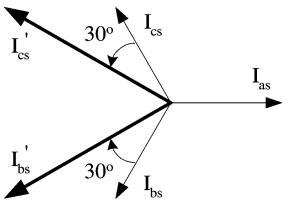

Fig. 6. Current phasor relationships before (I_{as}, I_{bs}, I_{cs}) and after (I'_{bs}, I'_{cs}) an open phase fault on phase a.

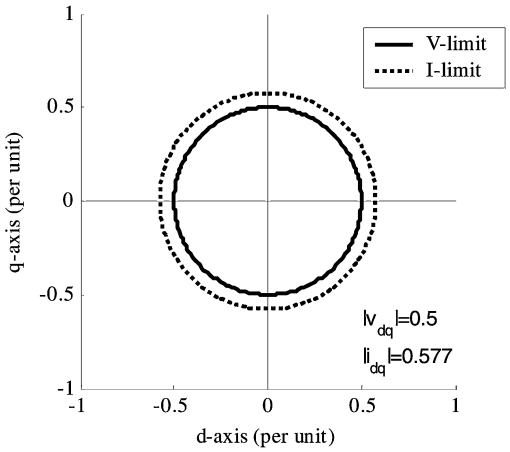

Fig. 7. Phase fundamental voltage and current limits of the switch-redundant inverter after a single-phase open-circuit fault.

sented in [13] and [14]. This topology will be referred to as the switch-redundant topology and is shown in Fig. 5. This topology incorporates four TRIACs or back-to-back connected SCRs and three fast acting fuses. The fuses are connected in series with the load phases. Since this topology is a combination of topologies and control methods to accommodate an opened phase [13], and a shorted switch [14], they will be considered separately.

In the case of an opened phase fault [Fig. 2(d)], only TRIAC TR_n needs to be present in the topology of Fig. 5, and the presence of the three series fuses is not required. When the system detects an opened phase fault, TRIAC TR_n is fired in order to connect the neutral of the motor to the midpoint of the dc bus.

In order to maintain a constant flux trajectory and insure disturbance free operation of the system, the phase currents of the unfaulted phases need to be increased in magnitude by a factor of $\sqrt{3}$ and phase shifted 30° away from the axis of the faulted phase. The phasor diagram of this for an open-circuit fault on phase a is shown in Fig. 6. This increase in phase current is in the form of a nontorque producing zero sequence current and is necessary to achieve a circular flux trajectory. As a result, the available torque producing current is reduced by a factor of $\sqrt{3}$, assuming a post-fault phase current of one pu. Since the motor neutral is connected to the midpoint of the dc link in the post-fault condition, the system still has the capacity to apply $\pm 1/2$ of the dc link voltage across each of the remaining phases. This implies that, in terms of the original three-phase system, the space vector voltage capacity of the system has decreased from 0.577 pu to 0.5 pu.

The voltage and current operating space of the switch redundant topology for an open-phase fault is shown in Fig. 7. Due to the zero sequence current, the TRIAC TR_n needs to be rated for $\sqrt{3}$ pu current as indicated in Table I. Overall, the system has a FPRF of 0.5 and SOCF of 1.29.

In the case of a short-circuit switching device failure in switch S_{an} [Fig. 2(a)], the circuit of Fig. 5 operates as follows. It is assumed that some type of hardware based short-circuit protection in the inverter will automatically open the complementary transistor, S_{ap}, in order to avoid a shoot-through failure by short-circuiting the dc bus. Using this signal and additional control logic, the controller turns on TRIAC, TR_a. This causes a short-circuit through the lower half of the dc bus, the failed-shorted switch, the TRIAC, and the fast blow fuse. As a result, the fuse will open and clear the shorted switch out of circuit. The TRIAC TR_a, is subsequently controlled to be continuously on during this post-fault condition. The equivalent circuit is now topologically identical to the four-switch three-phase inverter, or B4 topology [22]. In this post-fault operating condition, the inverter is capable of impressing one-half the phase voltage of the standard unfaulted inverter and the full rated current of the inverter as shown in Fig. 8. In terms of motor capacity, this topology will allow for the full rated motor torque production, but the system will enter the field weakening mode at approximately one-half speed compared to when the system has full voltage capacity. Hence, the faulted system is capable of producing up to one-half of the rated system power.

In order to protect against a shorted switch, only the three TRIACs, TR_a, TR_b, and TR_c are required to be present. It should also be noted that this topology has a drawback in that it requires access to the center point of the dc bus.

While not considered in [14] where the switch-redundant topology was proposed, it is possible for the topology to work for the case of a single-phase open-circuit fault and a single switch open fault. In both of these cases, the post-fault

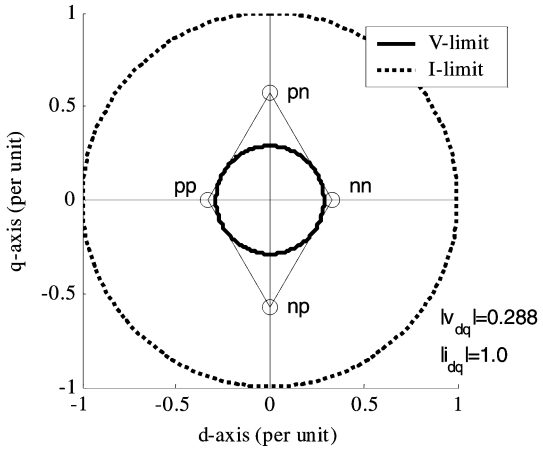

Fig. 8. Phase fundamental voltage and current limits of the switch-redundant inverter after a single-switch short-circuit fault.

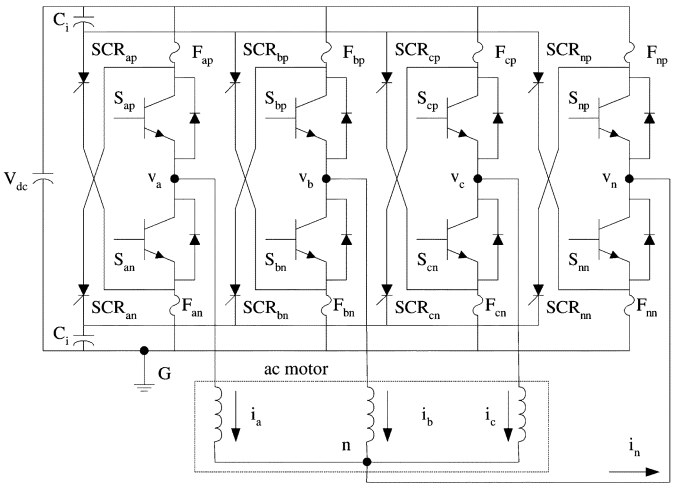

Fig. 9. Double switch-redundant topology.

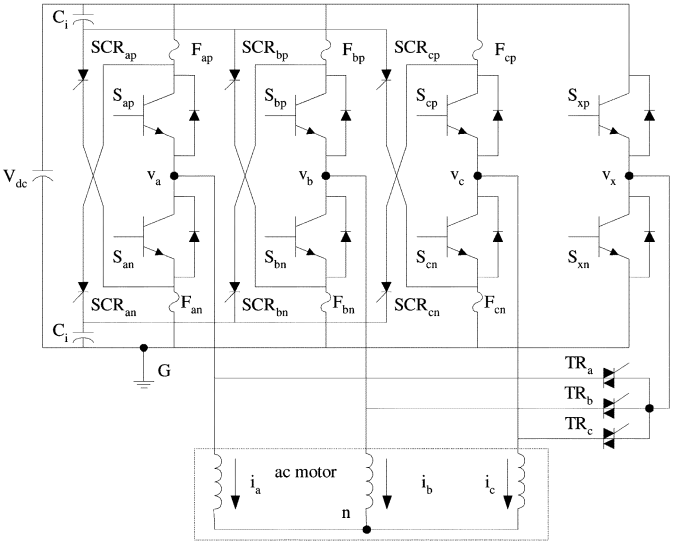

Fig. 10. Phase-redundant topology.

performance capacity will be the same as proposed in the paper for the single switch short-circuit fault. Due to topology constraints, the circuit can only accommodate an opened phase fault if the open phase occurs in the circuit between the leg terminal and the TRIAC terminal. Essentially, this would imply that the fuse has blown open accidentally or has been physically disconnected. In the case of an opened switch fault, the inverter could simply command the TRIAC in the faulted phase to close and command the IGBTs in the faulted phase to turn off.

It is further possible to combine the topologies proposed in these two papers, [13], [14], along with the method highlighted here for the opened switch fault to produce a to topology that is fault tolerant to a single shorted switch, a single opened switch, and an opened phase fault. This resultant topology would be as drawn in Fig. 5 and is included in Table I.

B. Double Switch-Redundant Topology

A fault redundant topology for permanent magnet motors was presented in [15]. This topology will be referred to as the double switch-redundant topology and is shown in Fig. 9. The topology consists of a four-leg inverter with additional components for fault tolerance driving a four terminal motor. The additional components needed for fault tolerance include two fuses and two SCRs per phase leg. Also, one pair of capacitors, C_i, is needed in order to clear the fuses and isolate a short-circuit path. This circuit is unique in that it is capable of providing fault tolerance to a phase-leg short-circuit [Fig. 2(b)]. In fact, this circuit is capable of providing fault tolerance to any of the four fault conditions being considered.

After detecting a fault, (phase a for example), the control sends signals to SCR_{ap} and SCR_{an} to turn on. For each IGBT in the phase leg, this causes a transient short-circuit through the main dc link, the auxiliary capacitor C_i, the SCR, and fuse. Using the charge transferred to the auxiliary capacitor, the fuse clears and the faulted phase-leg is removed from the circuit. The auxiliary capacitors need to be sized large enough that a sufficient amplitude and duration of current to clear the fuse is induced. The two capacitors are necessary so that a dc bus shoot-through short-circuit is not induced through the SCRs and IGBTs in the phase. Essentially, the capacitors create a means for the current in the SCRs to decay so that they can turn off. While the SCRs themselves are not in the circuit conducting current in the post-fault control, they have to have a sufficient current rating so they can clear the fuses. As a result, each SCR current rating will be on the order of the rated phase current of the inverter.

The post-fault control strategy in terms of commanded currents of the double switch-redundant inverter is identical to that of the switch-redundant inverter to an opened phase fault. One difference however is the fact that the motor neutral is connected to a fourth inverter leg as opposed to a direct connection to the center point of the dc link. This serves two significant purposes. First, the system is free of the dc midpoint balancing problems and minimum capacitance sizing issues that were addressed in [13]. Second, the control method of shifting the voltage at the neutral point of the machine that has been developed for single-phase induction motors [16], [17] can be applied to the three-phase system with an opened phase fault. Since the three-phase motor windings are displaced by 120° as opposed to 90° for the single-phase motor, the benefits

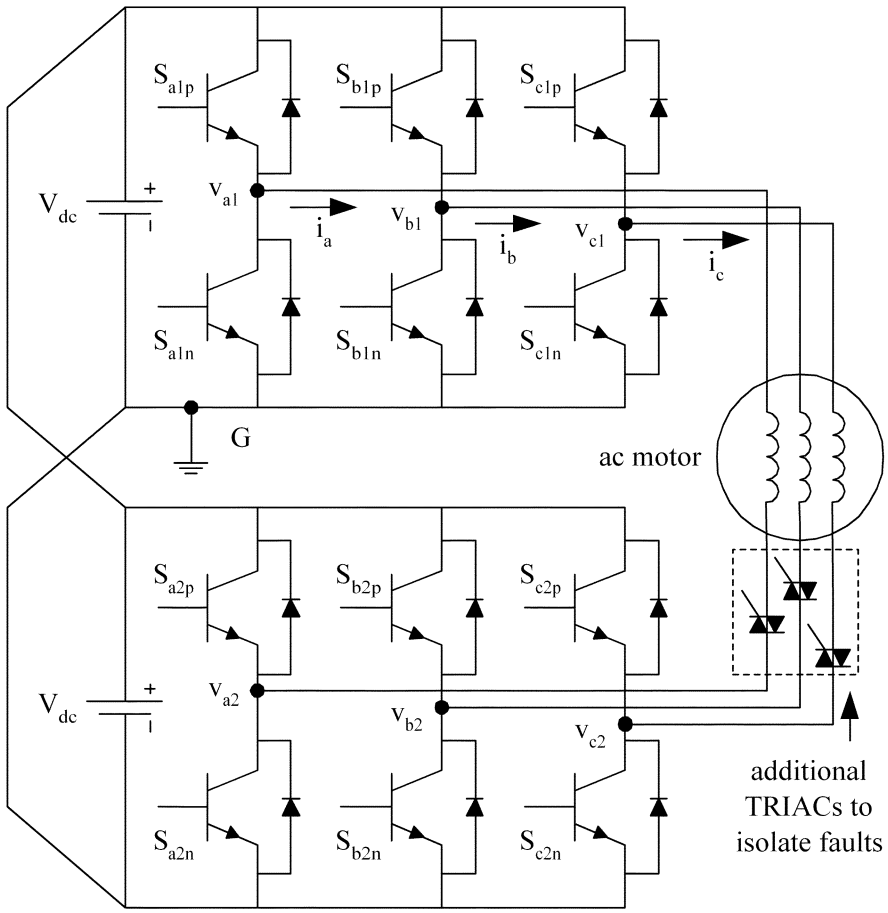

Fig. 11. Cascaded inverter topology.

are not as dramatic. Nevertheless, the space vector voltage in terms of the equivalent three-phase system can be increased to 0.577 from 0.5 using this technique. As a result, the double switch-redundant topology has a FPRF of 0.58 and SOCF of 2.24. It is important to note that it is possible for a fault to occur in the neutral leg, which does not carry any current during normal operation but is being modulated by the control. If this occurs, the SCRs in that leg will isolate the neutral leg of the system and the remaining system will operate as the standard three-phase inverter capable of producing 1-pu output power without any fault tolerant capacity.

C. Phase-Redundant Topology

The ability to isolate a faulty phase-leg opens the possibility of introducing a spare inverter leg for improved fault tolerance as shown in Fig. 10. The configuration [15] will be referred to as the phase-redundant topology. This circuit topology incorporates the fault isolating SCRs and fuses in only the three active legs of the inverter. A spare fourth leg of the inverter is connected in place of the faulty phase-leg after the fault isolating devices have removed that leg from the system. During normal operation, this spare phase-leg is inactive and not switching. As a result, the three TRIACs shown in the topology act as static transfer switches to connect this output to the faulted phase only when needed. This topology, which was not tested in the paper, has the unique ability to maintain rated output power in the post-fault operating mode which is a substantial improvement over the 0.58-pu output capacity when a two-phase control approach is adopted. The phase-redundant topology has a SOCF of 2.33 and is fault tolerant to each of the four faults being considered. It is also the only topology being considered that does not require additional stator leads to be brought out of the motor. This topology, without any of the fuses or SCRs, was experimentally demonstrated in [18] for the case of an opened phase and opened switch fault on an induction motor.

It is important to note that the presence of the fuses in these two topologies will have the effect of increasing the dc bus inductance. Since great care is normally taken when physically laying out the bus structure in order to minimize the parasitic bus inductance, the addition of inductance due to the fuses and fuse holders must be considered during the system design. Also, careful selection of the fuse is required to avoid nuisance faults due to fuse failure while simultaneously guaranteeing the expected post-fault operating capacity.

D. Cascaded Inverter Topology

The concept of parallel redundancy was one of the first means for providing fault tolerance in an induction motor drive system [6]. In this paper, a general n-phase motor was proposed for use with each phase being driven by an individual single-phase drive unit. The use of an individual single-phase inverter for each phase of the motor was also employed in [19], while dual

three-phase inverters in a modular system were employed in [3]. A novel variation on this idea was proposed in [25], and [26]. While these papers did not deal with the issue of fault redundancy, they addressed performance improvements that can arise from the use of individual phase drive units. As an example, [26] showed that the voltage space of the cascaded inverter is the same as a three-level inverter. The proposed cascaded inverter topology is simply a repartitioning of the phase legs found in a standard single-phase or three-phase inverter, and is shown in Fig. 11.

The cascaded inverter allows for the full bus voltage to be applied to each of the motor phases. As a result, it is necessary to adjust the number of turns in the motor to keep the kVA rating of system constant when compared to the standard topology [23]. When done properly, the cascaded inverter will have the same voltage and current space as the standard inverter as illustrated in Fig. 4, after the turns ratio adjustment is considered. Even though the number of devices is doubled, the required kVA of the topology is increased only 15% compared to a standard inverter since this topology has a SOCF of 1.15 as given in Table I. It should be noted that the SOCF of this converter is not equal to 1 as a direct result of the lower switch utilization ratio of the single-phase converter [24]. The turns ratio adjusts the output current and voltage for constant kVA between the converters. However, the switches still need to be rated to block the full dc voltage even though the phase voltage has only been increased by $\sqrt{3}$, and thus, the lower switch utilization ratio and increased SOCF.

The fault tolerance capacities of the cascaded inverter shown in Fig. 11 are somewhat limited. The inverter provides fault tolerance for an opened phase fault as indicated in Table I. In this case, the two-phase control method previously applied to the switch-redundant topology, double switch-redundant topology and phase-redundant topology would be used. However, protection for a short-circuited switch fault cannot be provided by turning off the remaining switches in the phase because a current circulating path remains consisting of the winding, the shorted switch, and a diode in the unfaulted inverter. Mutual coupling between the phases induces current to flow in the faulted winding, producing undesirable pulsating torque in the machine. This was considered a major factor in the machine design presented in [4]. For an open-switch fault, a path through the anti-parallel diodes is also present, but it includes the dc link. Any voltage induced in the faulted phase would have to be larger than the dc link voltage before current would be induced in the winding. As a result, fault tolerant operation for a single switch open-circuit fault will be limited to speeds which place the motors peak line-to-line back-emf less than the dc link voltage.

It is recognized that the use of multiple single-phase or cascaded inverters provides the potential for fault tolerance due to single switch open and single switch short-circuit faults. However, additional components are needed to isolate the faulted unit or phase from the system, as were employed in [6]. A potential isolating device would be a TRIAC inserted in series with each output phase as highlighted in Fig. 11. With a TRIAC available to isolate the faulted phase from the system, this configuration of the cascaded converter is capable of being fault tolerant to single switch short-circuits, single switch open-circuits, and phase-leg open-circuits. In all of these cases, the resultant control method used after the fault is cleared would be the two-phase control method outlined earlier. As a result, this system would have a fault power rating factor of 0.58. The SOCF for this system is 1.44 as listed in Table I. It should further be noted that this configuration would result in increased inverter losses during normal operation due to the series switch.

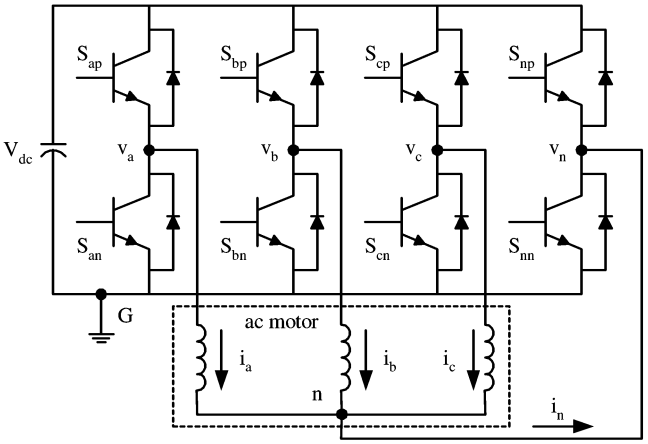

Fig. 12. Four-leg inverter topology.

E. Four-Leg Inverter Topology

The use of a four-leg inverter as shown in Fig. 12, to improve the fault tolerance of induction motor drives was demonstrated in [20] and [21]. In [20], the same two-phase control method for a single-phase open-circuit fault was utilized as discussed previously for the phase-redundant topologies. It has a post fault power rating of 0.58 pu and a SOCF of 1.58. An advantage of using this topology over the switch-redundant topology for a single-phase open-circuit fault is that the four-leg topology does not require access to the midpoint of the dc bus.

A different approach to fault tolerance using a four-leg inverter was taken in [21]. The fault considered in this paper was for an opened switch fault, which could occur as a result of a gate drive unit failure. The method presented could accommodate an opened switch fault on all three phases so long as all of the faults occurred in the upper or lower switches, but not a combination of upper and lower switches. Note that a fault in the neutral leg could not be accommodated. The post-fault control action consisted of commanding a three-phase set of unipolar currents, with two of three phases always conducting a nonzero current. This control method had previously been exploited to produce a three-phase motor drive with only three switches [27]. The unipolar currents control method does not change the available voltage space of the converter, but does negatively impact the current space. Due to the presence of a zero sequence current, the torque producing dq currents are reduced to 0.58 pu as shown in Fig. 13. It should be noted that the currents have been calculated assuming a pre- and post-fault phase current peak value of 1 pu and this distinction is necessary since the post-fault currents are not sinusoidal in shape. The neutral leg in this fault tolerant control scheme will then carry 1.73-pu current.

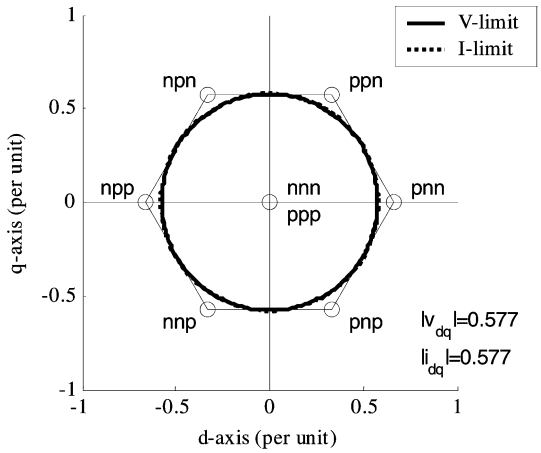

Fig. 13. Phase fundamental voltage and current limits of the four-leg inverter after a single switch open fault.

IV. Conclusion

This paper has reviewed the fault tolerant three-phase ac motor drive topologies that have been presented in the literature. An approach based on the fundamental inverter output space in terms of dq axis limits has been adopted as a basis to identify the potential performance limits of each of the topologies. From these limits, a fault power rating factor (FPRF) has been defined which normalizes the faulted system capacity to a standard three-phase inverter during normal unfaulted operation. To compare the relative cost of adding the fault tolerant capacity in each of the topologies, this paper has defined a SOCF which relates each circuit's weighted switch capacity to that of a standard three-phase inverter.

This review of the alternative topologies and control methods makes it clear that there is significant cost associated with providing fault tolerant operation. All of the topologies require additional components in the form of silicon switches and/or fuses to provide this capacity in the presence of a fault that would otherwise not be present in a standard three-phase inverter drive. Among the topologies and faults considered, key results include the following.

1) The switch-redundant topology provides the full post-fault current rating for both a single-switch short or single switch open fault at a modest cost increase (approximately 50%) and is a good candidate provided the midpoint of the dc link is available for use. Furthermore, this topology can be adapted to accommodate open phase faults with an additional TRIAC.
2) The double switch-redundant topology with a four terminal motor is fault tolerant to all four inverter faults considered: Single switch short-circuit, phase-leg short-circuit, single switch open-circuit, and single-phase open-circuit. It has a post-fault kVA delivery factor (FPRF) of 0.58.
3) The phase-redundant topology with a three terminal motor is fault tolerant to all four of the considered faults and has a FPRF value of 1.0. This superior solution also has the highest component cost of any fault tolerant topology at 233% of that of a standard inverter.
4) The use of single-phase units or cascaded inverters has the smallest cost penalty factor (SOCF) at 115% of the cost of a standard inverter but only provides fault tolerance to open phase faults. With the addition of TRIAC in each phase, this system is fault tolerant to single switch open, and short faults, and single-phase open-circuits. This increases the SOCF cost factor to 144% for a FPRF value of 0.58.
5) Four-leg inverters provide fault tolerance only to open phase or open switch faults at a relatively high cost.

In conclusion, a careful assessment of the likelihood of each type of fault and the required post-fault capacity is necessary to determine which topology is best suited for each application.

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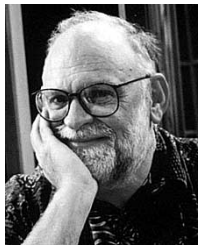

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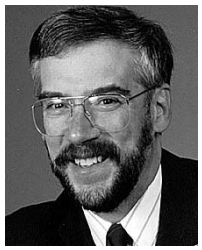

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