FDSOI SRAM Cells for Low Power Design at 22nm Technology Node

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***Abstract*—The silicon-on-insulator (SOI) MOSFET is considered as an alternative to the bulk (silicon-based MOSFET in CMOS circuits for applications requiring low-voltage and low-power operation. Fully depleted SOI (FDSOI) benefits from a high current driven ability; so, this technology preserves advantageous features, such as steep sub threshold characteristics and small short channel effects. This paper presents a comprehensive assessment of different SRAM (Static Random Access Memory) cells utilizing different numbers of transistors (i.e. 8 and 9). These cells are evaluated by HSPICE for different performance metrics (such as write/read delay, stability, critical charge, power consumption and tolerance to voltage threshold variation) at the 22nm technology node.**

***Index Terms*—Low Static Power, FDSOI, SRAM Cell, SNM**

I. INTRODUCTION

Process advances in semiconductor technology have made possible the design and manufacturing of digital chips with billions of transistors; these chips are used in diverse applications in which power consumption is a stringent requirement. As reported in the ITRS Roadmap [1], at least 70% of a microprocessor chip consists of memories; this percentage is expected to rise in the future. Moreover, as technology scaling continues, the high density in memories has caused an increase in power dissipation, thus significantly affecting leakage. Therefore, new technologies and designs of memories are required. Also, leakage reduction in the standby mode is critical for processors, because handheld and mobile consumer electronics (such as phones) have long idle times.

At 22nm and lower feature sizes, the traditional CMOS technology using bulk (silicon-based) MOSFETs is not fully capable to meet the demands of smart mobile devices [2] due to its fundamental physical limits. Limitations due to carrier mobility (decreasing due to impurity scattering), gate tunneling current (increasing due to the thinner gate insulator) and p-n junction leakage (increasing due to the shallow junction) are growing concerns when scaling is further reduced.

New device structures have been proposed to improve the electrostatic integrity with respect to the performance of a bulk MOSFET. Among these novel devices, silicon-on-insulator (SOI) based transistors have grown in popularity which were introduced by IBM in 1998. SOI based devices can be categorized into two types: Fully-depleted (FD) and Partially-depleted (PD) SOI transistors.

This paper focuses on the capabilities of FDSOI for low power memory design at the 22nm node. Two different designs beyond a conventional 6T SRAM cell design are proposed to show the FDSOI potential for memory design. This technology preserves advantageous features, such as steep sub threshold characteristics and small short channel effects, so it is particularly suitable for the design of memory cells. A comprehensive assessment of different SRAM (Static Random Access Memory) cells utilizing different numbers of transistors (i.e. 8 and 9) is pursued. These cells are evaluated by HSPICE for different performance metrics (such as write/read delay, stability, critical charge, power consumption and tolerance to voltage threshold variation) at the 22nm technology node.

This paper is organized as follows. Section II presents a brief review of FDSOI. Section III details the proposed SRAM cell designs. Section IV presents the simulation results and comparison between FDSOI and bulk based designs with respect to different figures of merit. Section VI concludes the manuscript.

II. REVIEW

An undoped ultra-thin fully-depleted (FD) SOI MOSFET with high-κ dielectric and metal gate is an attractive solution for nanoscale implementation. The inner picture of Figure 1 shows the schematic cross sections of FDSOI MOSFET; the most significant feature of a FDSOI MOSFET is that the depletion region fully reaches the bottom of the Si film. Therefore, the body region is fully depleted which affect the electrical characteristics (such as the threshold voltage) of a MOSFET. For continued scaling, FDSOI not only addresses the issues of physical limitations of bulk devices, but it also makes low power design possible. The so-called BOX layer gives SOI MOSFETs many advantages over bulk MOSFETs such as very small P-N junction leakage and drain-to-substrate capacitance, no body effects which can be used to make fast stacked gates [3], more better subthreshold characteristics and lower RDF due to its intrinsic undopped thin channel region.

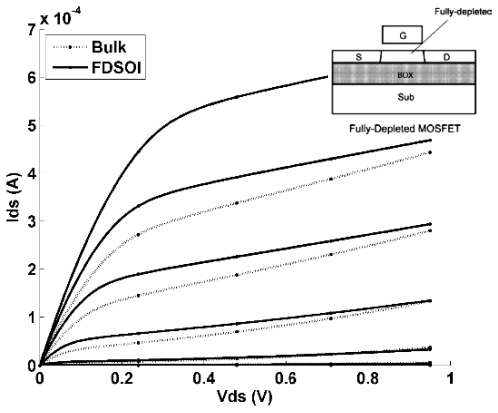


Figure 1 Schematic cross section of FDSOI MOSFET Devices and VTC

Predictive compact models are extensively used for circuit level design; the development of these models allows a fair comparison between bulk and FDSOI based designs for the same process and device features. In [4], a pre-silicon modeling methodology is introduced; it unifies bulk and FDSOI based on BSIM4/BSIM4SOI and same process/device features. Using this methodology, 22-nm technology node model cards are generated and aligned with the ITRS targets. MOSFET performance is also aligned with experimental results. Figure 1 shows that the I_{on} of a FDSOI MOSFET is higher (nearly twice) than a bulk MOSFET under the same biasing conditions; moreover, the channel length modulation and short channel effects are not as significant as for a bulk MOSFET.

Next, consider the circuit techniques for reducing power consumption in a SRAM. Leakage in a SRAM can occur either inside the cell itself, or on the access transistor paths [5][6]. The transistor which is actually leaking in a cell depends on the stored value, the logic level of the wordline (WL) and the type of operation (i.e., the value of the bitline BL). A low power design of a SRAM cell can be achieved by reducing the dynamic power when in operating mode or the leakage current when in standby mode. The techniques commonly used for reducing leakage power in bulk CMOS circuits are forced stacking, sleep transistor, MTCMOS/SOI technology [3] and low vdd voltage/power (Subthreshold operation). Specifically, some of these techniques can also be used in FDSOI based designs of a low leakage SRAM.

III. PROPOSED FDSOI SRAM DESIGNS

In this section, two low-power designs are introduced, namely (I) 8T stack forced SRAM cell; (II) a subthreshold 9T SRAM cell with low power supply.

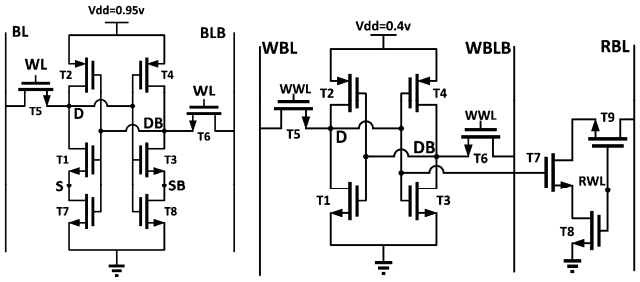
A. Force Stacked 8T SRAM Cell

A force stacked 8T SRAM Cell is proposed to decrease the standby leakage power. In this scheme [8], additional NMOS transistors are connected in series (i.e. the stack). The total gate area of all NMOS transistors of the stack is the same as the non-stacked NMOS transistors. The following condition applies to a two-transistor stack

$$w_u \le \frac{w_{pd}}{2}, w_l \le \frac{w_{pd}}{2}$$
$$w_u + w_l = w_{pd}$$

where w_{pd} is the width of the NMOS transistor prior to stacking, w_u is the width of the upper transistors (T1 and T3) of the stack and w_l is the width of the bottom transistors (T7 and T8) of the stack. The leakage current flowing through the stack is dependent on the number of "off'' transistors in the stack; it has been shown that this technique is effective in reducing the subthreshold leakage current for nanometer CMOS [9].

Figure 2 (a) shows the proposed FDSOI MOSFET based SRAM cell using a force staking technique. As commonly applicable to a 6T SRAM cell, all transistors have minimum gate length (i.e. 22nm); the cell ratios are given by $w_{pd}/w_a = 4/3, w_{pu}/w_a = 2/3$ (w_a is the width of the access transistor). The stack transistor width is given by $w_u/w_l = 5/3$.



(a) (b)

Figure 2 (a) Circuit of proposed force stack 8T FDSOI SRAM cell (b) Circuit of proposed subthreshold low-voltage 9T SRAM cell

B. Subthreshold Low-Voltage 9T SRAM Cell

The proposed subthreshold low-voltage SRAM cell is shown in Figure 2 (b). A FDSOI based SRAM cell can benefit from lowering the supply voltage to 0.4 volts, thus reducing both static and dynamic power consumptions. The subthreshold cell is made of a conventional 6T SRAM cell and a readout buffer. The buffer is enabled by the control signal RWL turning T9 and T8 on when performing the read operation. When reading a '0', T7 is turned on and the precharged RBL line is discharged; when reading a '1', T7 is off and RBL stays to the precharged high state. The cell operates in the subthreshold region and the supply voltage value is decreased, as in a 6T SRAM, the read stability and write ability become weaker. The read out buffer is introduced to compensate for the weaker read stability. As the read operation is isolated from the storage node, the read SNM is nearly equal to the standby SNM. Sizing of the transistors must also be considered; the ratio of the pull-down transistor T1 to the access transistor can be smaller than in the 6T SRAM to further decrease the leakage power of the cross-coupled inverters. To enhance the weaker write ability, the ratio of the pull-up transistor T2 to the access transistor is made smaller by having a wider access transistor. Moreover, tradeoff between read speed and static leakage must be assessed for sizing the read buffer.

IV. SIMULATION AND COMPARISON

In this section, the proposed memory cells are simulated and compared to the bulk CMOS counterpart. The PTM model is used for the bulk MOSFETs and the 22nm model generated for the FDSOI MOSFETs as described previously. Sizing of the SRAM cell is the same for both bulk and FDSOI based designs and are optimized for the write operation and to avoid a destructive read [7]. The simulation results show that the subthreshold 9T design cannot be fully functional using bulk MOSFETs; however this design operates correctly when FDSOI is utilized. Moreover, FDSOI performs better in the subthreshold region than the bulk MOSFET due to the reduced short-channel effect [10].

A. Power

Power consumptions under different operations mode are simulated. The results of Figure 3 show that the FDSOI cells have significantly lower static power consumption in the standby mode, i.e. for FDSOI, the inner oxide layer under the channel region isolates the current path from drain to source. The active power is shown in Figure 4; due to the high current

driving capability, all FDSOI-based memory cells have higher dynamic power consumption than their bulk-based counterparts. As shown in Figure 5, the standby power of all SRAM cells is reduced when the power supply Vdd is decreased.

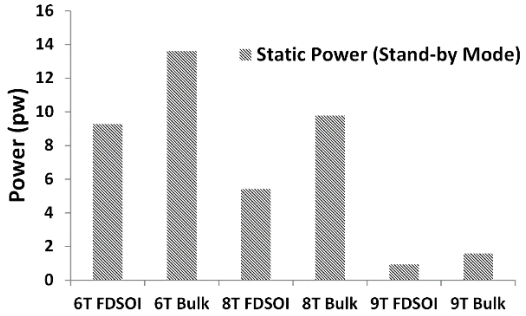


Figure 3 Static power of memory cells

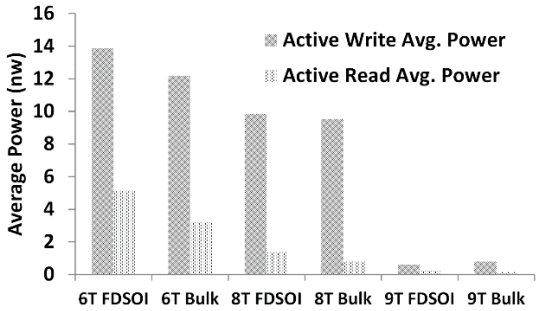


Figure 4 Active power of memory cells

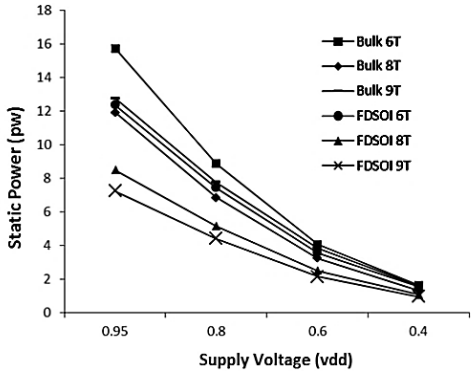


Figure 5 Static Power at different supply voltage values

B. Delay

Table I shows the results for the read and write delays for all SRAM cells considered in this paper at different values of power supply; in all cases the FDSOI based SRAM cells are faster than the bulk based counterparts due to the smaller drain-to-substrate capacitance and higher current driving capability. It is also observed that when vdd decreases down to 0.4v, the 6T and 8T cell begins to fail for write operation; it means 0.4v Vdd is functional limits for 6T and 8T design. Actually, under 0.4v Vdd, the SRAM enter subthreshold region, 9T design is still functioning in this region.

C. Static Noise Margin

The static noise margins (SNM) of the read and write operations must guarantee the correct functional stability of a SRAM cell [11]. The values of the read, standby and write SNMs of the FDSOI and bulk cells are summarized in Table II. Compared to bulk based SRAMs, the FDSOI based SRAMs have a slightly larger SNM in all cases; for the different structures, the 6T SRAM cell has similar SNMs as the 8T SRAM cell. While retaining a similar write SNM, the 9T SRAM cell has a better read SNM than the 6T and 8T cells due to the read buffer (so separate from the storage node).

TABLE I READ AND WRITE DELAY OF VARIOUS SRAM CELLS (PS)

Vdd	0.95v		0.8v		0.6v		0.4v	
	Write	**Read**	**Write**	**Read**	**Write**	**Read**	**Write**	**Read**
FDSOI (6T)	16.7	5.1	53.1	10.9	88.7	30.0	4712.3	1735.2
FDSOI (8T)	21.2	14.8	62.3	36.2	80.3	36.1	4113.8	2005.9
FDSOI (9T)	18.2	8.5	56.2	16.5	86.4	27.3	4546.6	1518.5
BULK (6T)	40.2	10.3	90.6	30.6	779.7	132.7	Fail	7757.0
BULK (8T)	35.9	25.6	84.1	60.1	680.0	272.4	Fail	15298.0
BULK (9T)	47.3	15.7	97.2	34.5	899.7	242.4	Fail	10259.8

TABLE II SNMS

	FDSOI (6T) SNM (mv)			Bulk (6T) SNM (mv)		
Vdd	**Read**	**Standby**	**Write**	**Read**	**Standby**	**Write**
0.95v	178.80	388.35	391.45	175.29	369.38	382.75
0.8v	148.73	329.02	341.93	141.64	307.77	333.25
0.6v	104.49	240.51	198.03	96.77	222.31	156.68
0.4v	61.43	149.08	86.72	52.13	134.69	Fail
	FDSOI (8T) SNM (mv)			**Bulk (8T) SNM (mv)**		
Vdd	**Read**	**Standby**	**Write**	**Read**	**Standby**	**Write**
0.95v	226.68	402.08	427.38	180.45	390.21	423.12
0.8v	174.28	339.43	372.99	139.65	326.60	370.49
0.6v	94.61	248.64	234.66	93.66	237.56	183.84
0.4v	53.59	155.73	145.91	46.10	106.02	Fail
	FDSOI (9T) SNM (mv)			**Bulk (9T) SNM (mv)**		
Vdd	**Read**	**Standby**	**Write**	**Read**	**Standby**	**Write**
0.95v	388.01	388.10	461.01	346.61	347.38	430.26
0.8v	328.73	328.78	392.94	290.24	290.72	372.10
0.6v	240.21	240.23	301.86	212.02	212.30	290.95
0.4v	148.69	148.69	136.38	129.62	129.64	Fail

D. Impact of Process Variation

TABLE III VTH VARIATION FOR FDSOI AND BULK [12]

	Bulk MOSFET	**FDSOI MOSFET**
σ(Vth)| RDF	45mV	21mV
σ(Vth)| LER	25mV	10mV
σ(Vth)| TOTAL	51mV	23mV

For a SRAM cell design, the Vth variation of a transistor plays a critical role in its operation; the local component of this variation is referred to as the intra-die Vth variation, and is mainly due to random dopant fluctuation (RDF) in the channel and line edge roughness (LER). The dopant distribution increases with process scaling for controlling the short channel effect; the extent of the variation is usually measured by the standard deviation. The experimental results are reported in Table III (it is assumed that the LER and RDF are independent random variables); a FDSOI MOSFET accomplishes a significant reduction in the random dopant fluctuation due to the intrinsic undopped thin channel region. The FDSOI MOSFET also shows a smaller LER-induced variation due to the reduced short-channel effects.

The impact of process variation on the SNMs of the SRAM cells is evaluated next; in the simulation for the Vth variation, a Gaussian distribution and independent random components are assumed for the variation. Monte Carlo simulation of the SNM is performed; the value of the mean, sigma and variance are shown in Table IV. These results yield the following conclusions: (1) For superthreshold 6T and 8T design, the 8T cell has a better SNM than the 6T cell in all cases; (2) For subthreshold 9T design, although Vdd is very low (i.e. 0.4V), the read SNM is comparable to the 6T cell; (3) For all designs, the FDSOI MOSFET has a better tolerance in terms of SNM to threshold voltage variation than a bulk MOSFET.

TABLE IV MONTE CARLO SIMULATION OF IMPACT OF VTH RANDOM VARIATIONS ON THE SNM OF SRAM CELLS*

SNM Monte Carlo (Mean)						
	6T FDSOI	6T Bulk	8T FDSOI	8T Bulk	9T FDSOI	9T Bulk
Standby	377.49	344.90	393.34	367.21	138.22	109.73
Read	166.95	152.40	258.21	184.47	137.97	111.09
Write	392.46	383.93	430.13	428.38	138.00	162.06
SNM Monte Carlo (Sigma)						
	6T FDSOI	6T Bulk	8T FDSOI	8T Bulk	9T FDSOI	9T Bulk
Standby	8.39	19.51	7.07	15.48	8.35	17.28
Read	10.75	20.36	11.97	14.47	8.13	16.85
Write	13.80	34.39	13.34	29.85	31.46	53.81
SNM Monte Carlo (variance)						
	6T FDSOI	6T Bulk	8T FDSOI	8T Bulk	9T FDSOI	9T Bulk
Standby	0.07	0.38	0.05	0.24	0.07	0.30
Read	0.12	0.41	0.14	0.21	0.07	0.28
Write	0.19	1.18	0.18	0.89	0.99	2.90

*Note: For 6T and 8T design, the vdd is nonimal 0.95v. For 9T design the vdd is 0.4v.

E. Critical Charge

A further measurement considered in this manuscript for SRAM cell comparison is the resilience to soft error. This is usually related to the so-called critical charge which is defined as the smallest injected charge at certain circuit node that could flip the memory cell. The larger critical charge is, the better soft error resilience it has. The critical charge is usually depend on the node parasitic capacitance, circuit structure and other device physics. Table V shows the simulated critical charge due to the parasitic capacitance at node D and DB. The 6T and 9T cells have larger critical charge than the 8T SRAM cell and due to less parasitic capacitance of FDSOI, all FDSOI based cell is less resilience to soft error than its bulk MOSFETs counterpart. However, it is believed that the SOI technology has an intrinsically well 5X to 10X lower soft error rate than bulk due to the oxide layer acting as a block for the track of electron-holes pairs to drift to the p-n junctions [2]. Due to limitation of the device model, the soft error reduction benefit from the oxide layer cannot be observed at the circuit level simulation here.

TABLE V CRITICAL CHARGE DUE TO PARASITIC CAPACITANCE (FC)

Node	**6T FDSOI**	**6T Bulk**	**8T FDSOI**	**8T Bulk**	**9T FDSOI**	**9T BULK**
DB	0.295	0.365	0.265	0.305	0.270	0.335
D	0.9	0.81	0.41	0.39	0.84	0.79
S	NA	NA	1.15	1.20	NA	NA
SB	NA	NA	1.50	1.65	NA	NA

V. CONCLUSION

In this paper, the 22nm FDSOI MOSFET has been used for SRAM cell design; two memory cells using different number of transistors have been investigated. An extensive evaluation based on HSPICE simulation has been presented for comparative assessment versus bulk (MOSFET) designs. The rankings of these cells are presented in Table VI. Compared with the corresponding MOSFET-based cell structure, the static power of a FDSOI based design is nearly 47.5% less, while retaining a similar SNM and circuit complexity. However, the read and write delays are improved by 58% and 40.9% respectively due to high driving capabilities of FDSOI devices. Additionally, due to the low Vth variation, FDSOI cells shows low sensitivity in terms of SNM.

TABLE VI RANKING OF SRAM CELL DESIGNS

	Power	Delay		Avg. SNM	Vth Var.	Crit. Charge	Transistor
		Read	Write				
FDSOI 6T	4	***1***	***1***	5	3	4	***1***
FDSOI 8T	2	2	2	3	***1***	6	2
FDSOI 9T	***1***	5	3	***1***	2	5	3
Bulk 6T	6	3	4	6	6	***1***	***1***
Bulk 8T	3	4	5	4	4	3	2
Bulk 9T	5	6	6	2	5	2	3

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