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Feedback write scheme for memristive switching devices

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Abstract In nanoscale memristive switching devices, the statistical distribution of resistance values and other relevant parameters for device operation often exhibits a lognormal distribution, causing large fluctuations of memristive analog state variables after each switching event, which may be problematic for digital nonvolatile memory applications. The state variable w in such devices has been proposed to be the length of an undoped semiconductor region along the thickness of the thin film that acts as a tunnel barrier for electronic transport across it. The dynamical behavior of w is governed by the drift diffusion of ionized dopants such as oxygen vacancies. Making an analogy to scanning tunneling microscopes (STM), a closed-loop write scheme using current feedback is proposed to switch the memristive devices in a controlled manner. An integrated closed-loop current driver circuit for switching a bipolar memristive device is designed and simulated. The estimated upper limit of the feedback loop bandwidth is in the order of 100 MHz. We applied a SPICE model built upon the TiO_2 memristive switching dynamics to simulate the single-device write operation and found the closed-loop write scheme caused a narrowing of the statistical distribution of the state variable w.

1 Introduction

Nonvolatile memory technology (NVM) based on charge storage (e.g., Flash) is rapidly approaching its fundamental miniaturization limit. This has motivated the quest for a CMOS compatible alternative to established NVM techniques. Memory based on electrically switchable device resistance, generally termed resistive random access memory (RRAM), has attracted much attention thanks to smaller sizes, lower cost, enhanced write endurance, and faster write speed [1]. RRAM covers a large variety of working mechanisms and material systems, including phase-change memory (PCM) in chalcogenides [2], electrochemical metallization cells in solid electrolytes [3], and oxygen vacancy mediated switching in binary or more complex transition-metal oxide (TMO) compounds [4, 5]. Most of these RRAM devices exhibit pinched hysteresis loops in their I–V characteristics and they are generally described as memristor [6] and memristive systems [7]. The concept of a memristive system has been built upon a solid mathematical foundation to model various aberrant electrical phenomena in amorphous dielectric films [8], and even biological neurons [7]. Memristive devices are both scientifically and technically interesting and hold promise for NVM, defect-tolerant circuitry [9], and neuromorphic computing [10].

For NVM applications, the compatibility with mature CMOS technologies is considered a prerequisite, which requires memristive devices to work in binary or other digital modes. However, bearing similarities with biological neurons, memristive devices are intrinsically analog devices, in which the characteristic internal state(s) depends on the history of the device, and continuously evolves as an electrical stimuli (voltage or current) is applied. The analog behavior may pose a fundamental challenge to use memristors as building blocks for Boolean logic systems. In fact, in RRAM devices, it is frequently observed that applying an unbounded voltage write pulse can produce large fluctuations in device resistances. The statistical distributions of resistance values, and other relevant parameters for device operation, e.g., switching delay time, exhibit a lognor-

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mal law, where the measured values are distributed over a much wider range than a more plausible normal distribution [11–13]. Such lognormal distributions of device parameters are a potential obstacle for the reliability and longevity of RRAM.

In this article, we attempt to mitigate the issue of lognormal distributions in memristive switching devices by adopting a regulated write operation to a selected memristive memory cell to avoid overwriting and producing unreliable targeted memristive states. An integrated feedback (FB) current driver circuit has been proposed and designed to switch memristive devices to predetermined resistive states. A device SPICE model based on a dynamics study of TiO_2 switching devices was used to simulate the ON/OFF (aka. SET/RESET) switching operations of a memristor device using a closed-loop FB write driver. The efficacy of the FB write circuit was demonstrated by a set of Monte Carlo SPICE simulations designed to compare open-loop and closed-loop write operations. It was observed the open-loop write circuit produced a broad lognormal distribution of the analog state variable, while the closed-loop write circuit produced a much narrower distribution. Preliminary experimental results from using FB in a close-loop write circuit to write TiO_2 based memristive devices are encouraging.

The widespread lognormal distribution is postulated to be rooted upon a multiplicative cascade of individual conditional events, rather than the usual summation of individual probabilities that would cause a normal distribution. Lognormal distributions are found in the permeability of disordered porous media [14] and hopping conduction in amorphous materials [15]. It was hypothesized that for such uncorrelated random systems, a percolation description is appropriate. In a randomly disordered medium, the preferential selection of high conductivity paths, often associated with propagating dangling bonds, occurs predominantly over a critical path connecting local clusters of sufficiently high conductance in a cascade manner [16].

In PCM, the distribution of the switching delay time was found to be generally lognormal with a median that decreases with increasing SET current, i.e., the differential probability distribution function $\propto \exp[-(\ln t - t_0)^2/\tau]$, where t_0 and τ are fitting parameters [11]. Distributions of other relevant physical parameters, such as the saturation nucleate size in PCM, were also found to be lognormal. Compared with PCM devices, where the lognormal distribution is well characterized, the statistical study of oxide-based resistive switches is less understood, although lognormal distributions are known to occur in stress-induced leakage current (SILC) in ultra-thin gate oxides [17]. In TiO_2 based memristive switching devices, lognormal distributions of switching parameters have been observed and analyzed [18]. Figure 1(a) shows an example of endurance measurements of a TiO_2 memristive switch. The on-state resistance R_{ON} is observed to follow approximately a lognormal distribution (Fig. 1(b)), which turns into a normal distribution if plotted as a function of $\log(R_{ON})$ (Fig. 1(b) inset).

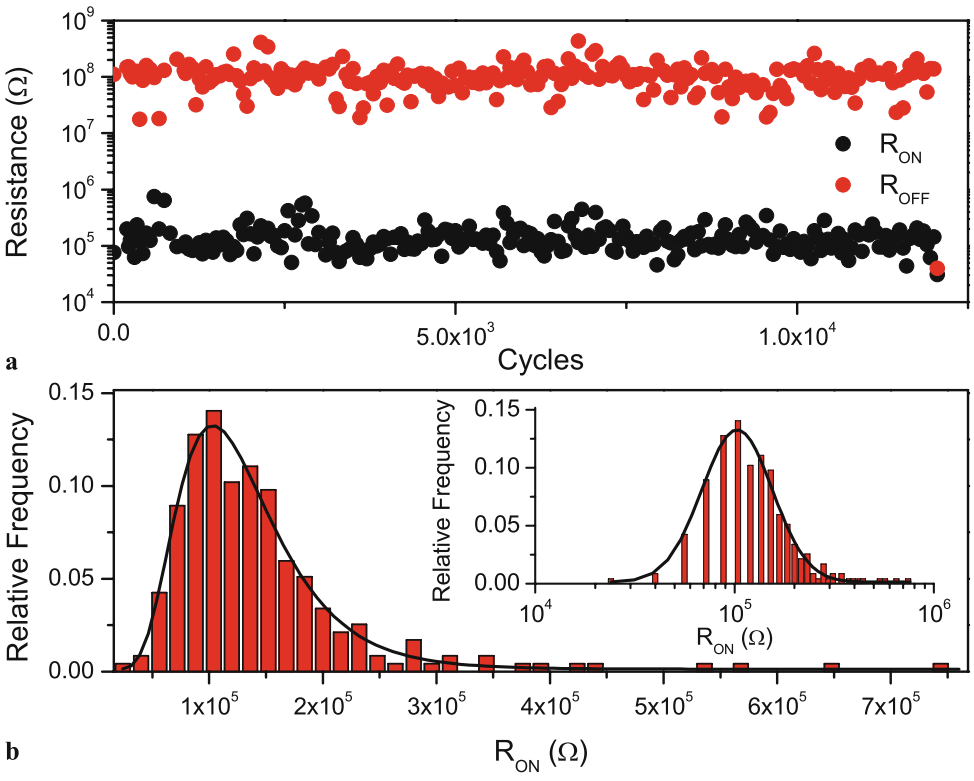

Fig. 1 (**a**) Experimental endurance test data of a TiO_2 memristive switching device. R_{ON} and R_{OFF} represent the resistance values in the low-resistive ON and high-resistive OFF states, respectively. (**b**) Statistical histogram and lognormal fit for the relative frequency of R_{ON} values. *Inset* shows the same histogram in log–linear fashion

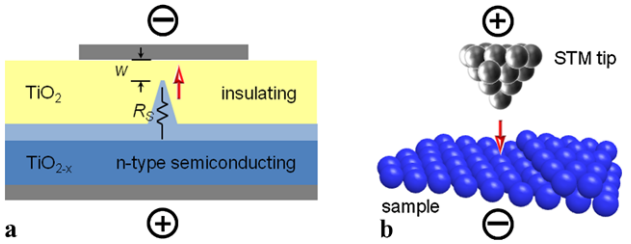

Fig. 2 Comparison between memristor tunnel gap and STM. (**a**) Schematic crossection of a metal-oxide-metal memristive switching device. In the device, schematic w and R_S represent the tunneling barrier width and the electroformed channel resistance, respectively. (**b**) Schematic tunnel junction formed between a STM tip and a conductive substrate

For TMO-based memristive switching devices, electronic and structural characterizations are converging to support a picture of defect-mediated resistive switching. Typically, the thin-film TMO material, mostly in an amorphous form, can be modeled as a defective wide-bandgap semiconductor sandwiched by two metal electrodes to form a metal-insulator-metal (MIM) structure. Typically, an Ohmic-type bottom interface is formed, e.g., by partially reducing the TMO layer. The top interface is typically made by a noble metal electrode, e.g., Pt that does not react with the TMO layer and generates a Schottky-type depletion region. An electroforming step is often required to obtain hysteretic switching in the as-deposited TMO layer. After electroforming, conductive filaments with a high concentration of oxygen vacancies acting as active dopants are produced by the high electric field (E field) [19]. Figure 2(a) shows the schematic cross-section of such a MIM switching device using TiO_2/TiO_{2-x} as an example material system.

In nonlinear circuit theory, the memristor concept was introduced by Chua [6] to represent the fourth unique passive circuit element connecting charge q and flux φ (time integration of voltage). It was soon expanded to a broader class of nonlinear dynamical memristive systems [7]. A canonical memristive system can be described by two coupled equations. The instantaneous I–V relation (1) takes the form of a normal resistive device, in which the generalized resistance is a function of a state variable or a set of state variables w. The dynamics equation of the state variable (2), however, is written in a differential form, where only the time derivative of the state variable is explicitly determined, implying that w depends on the device history rather than instantaneous electrical stimuli.

$$V = R(w, i) \cdot i \tag{1}$$

and

$$\mathrm{d}w/\mathrm{d}t = f(w, i) \tag{2}$$

where $f(w, i)$ is an arbitrary function for a memristive system. For a memristor, $f(w, i) = i$.

In their original mathematical forms, both the memristor and memristive systems are current-controlled, while voltage-controlled systems are equivalently possible. However, the implication of device current as explicit control variable has not been fully exploited, and current control deserves further examination.

It was only until recently that the memristor concept was linked to MIM resistive switching devices [20]. Specifically, the state variable w in many such MIM devices can be ascribed as the length of an undoped semiconductor region along the thickness of the thin film that acts as a tunnel barrier for electronic transport across it. The switching dynamics of TiO_2 memristive device was studied by a state-evolution procedure based on the framework of memristive system [21]. It was shown that the I–V characteristic for each state of the TiO_2 memristive device can be reduced to a single state variable by fitting to the equivalent circuit model of Fig. 2(a): an Ohmic resistor R_S in series with an electron tunnel barrier w. A rectangular tunnel barrier with image forces fits the experimental data well with physically reasonable parameters.

Since a dynamic tunnel junction works well in the phenomenological model of TiO_2 switching devices, it would be instructive to make an analogy between the ON switching of a memristive device, and an STM tip approaching a conductive surface. Although these two physical systems are drastically different, some insight may be gained by comparing their characteristics, as in both cases a tunneling gap gets established by the motion of conductive regions.

In STM, a metallic tip with nanoscale dimensions is driven by stepping a piezoelectric transducer, the "walker," toward a conductive substrate until a tunneling gap is formed at a distance less than $\sim$1 nm, so that electron tunneling across the gap is established if a tip bias is applied across the gap. Such a tip-approaching procedure is regulated by an analog or digital FB circuit that constantly monitors the current level between the tip and substrate with a fixed tip bias. When the tip is approached to a close-enough distance to the substrate, so that a tunnel current emerges and reaches a current set point, the FB circuit responds and stops the stepping walker in a timely manner so the tip would not crash into the substrate. After a tip approach is finished, a fine-tuned piezoelectric scanner is driven to maintain the tunnel gap and the corresponding tunnel current near the set point. The highly nonlinear exponential dependence of the tunnel current on the tunnel gap is utilized as an extremely sensitive distance probe, so that atomic corrugations on the substrate can be recorded when the tip is raster scanned over the substrate with a fixed tunnel current level maintained by the FB circuit.

In the case of a memristive device, if the current flowing through the device is dominated by electron tunneling, then the current level during switching should be an extremely sensitive probe of the tunnel gap w. It is shown

that for both ON and OFF switching of TiO_2 devices, the time derivative of w, or the switching speed, is proportional to $\sinh[i/i_0]\exp[-w/w_c]$, where w_c is a scaling parameter [21]. Such a highly nonlinear switching dynamics may be the consequence of E field and junction self-heating, both of which can explain the observed exceptionally large storage to switch time ratio [22].

Therefore, a fast analog FB loop may serve dual purposes: Firstly, it could greatly narrow down the stochastic distribution of state variable w and make the switching parameters more uniform for binary operations. Secondly, it becomes possible to set w continuously to realize multilevel-cell (MLC) memory. A noteworthy difference between the case of STM and memristor switching is that, in STM the tunnel current is maintained to be constant after reaching the set point; while in memristor ON switching, the current should be removed immediately to store the analog state variable (tunnel gap).

In developing the concept of the closed-loop write scheme, we have referred to a phenomenological memristive device model in which the state variable w is a length parameter, i.e., the tunnel gap formed between a dopant-rich conductive filament and a Schottky-type electrode. However, the application of such a FB write method should not be limited by the microscopic device model or a specific state variable. Even if the state variable is not a length parameter (e.g., tunnel gap), the FB write scheme is still applicable.

Retrospectively, several methods have been used to gain some control on the resistance state in writing a RRAM cell or memristive device. The common mechanism of these methods is to limit the current or voltage level during switching event to steer the resulted analog state. Their advantages and disadvantages are briefly discussed in the following.

1.1 Current compliance

In both electroforming and switching of MIM memristive devices, it is a common practice to limit the SET/RESET currents by applying a current compliance (Icomp) in the voltage source or source measure unit (SMU). Applying Icomp was found to provide at least two benefits, protecting the device from being overwritten (e.g. too conductive or shorted), and the possibility of setting the device resistance state continuously for MLC operations. As an example, Fig. 3 shows a set of bipolar switching I–V curves measured in a four-terminal configuration on a $TiPt/TiO_2/Pt$ nanoscale crossbar sample with the device junction size of 50×50 nm^2. The TiPt bottom electrode (BE) forms an Ohmic-like contact with a partially reduced TiO_{2-x} layer, while the pure Pt top electrode (TE) forms a Schottky-like contact with a highly resistive TiO_2 depletion region. Details of device fabrication and characterization have been reported previously [19]. The switching I–V traces were acquired by sweeping the external bias with a preset Icomp level at the SMU (Agilent 4155A). The switching polarity is such that a negative bias applied to TE switches the device from a high resistance state (HRS) to a low resistance state (LRS) (ON switching); while a positive bias switches the device from LRS to HRS (OFF switching). Hence, a bipolar round-trip voltage sweep of $0 \rightarrow -V \rightarrow 0 \rightarrow +V \rightarrow 0$ forms a complete switching cycle that presumably should return the device to its original state. In Fig. 3, four sequential switching cycles were executed with different Icomp settings. In the first two switching cycles, Icomp was set at $-75/200$ μA for ON/OFF switching, respectively; while in the last two switching cycles, Icomp for ON switching was changed to -175 μA. For ON switching, it is clear that the final resistance state is determined by the level of Icomp. Higher Icomp will switch the device to a more conductive state. The first two and the last two I–V traces are overlapped, indicating that repetitive switching cycles at the same Icomp level do not alter the device characteristics. Therefore, the observed tuning effect of Icomp is not just a coincidence, but rather a systematic behavior reflecting the intrinsic switching dynamics of a memristive system.

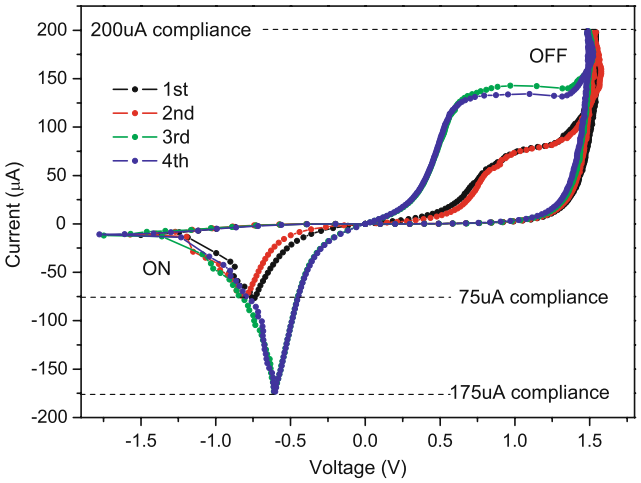

Fig. 3 Switching I–V curves of a nanoscale $TiPt/TiO_2/Pt$ crossbar device showing the effect of current compliance on memristive state. The device junction size is 50×50 nm^2

While it is convenient to use Icomp to improve the device characteristics or obtain a MLC operation in a single cell test, it is not universally applicable. For example, it is nontrivial to apply Icomp for short voltage pulses applied for endurance tests. In such cases, a large resistor placed in series with the device was often used to limit the write current, which effectively turns the voltage source into a current source. The efficacy of such series resistor is not guaranteed due to the RC discharge caused by the cable and stray capacitance.

1.2 1T1R structure

While the passive crossbar matrix architecture holds the promise for the highest possible storage density thanks to stackability and a smaller footprint per storage node, the active-matrix "1T1R" structure, i.e., one transistor per resistive switch node, is being actively pursued for near-term RRAM implementations. The concept of a 1T1R structure is directly inherited from CMOS memory technology. At each storage node, a MOSFET select transistor is placed in series with the switching device to decouple unselected memory cells from the array. The benefit of introducing the select transistor is a significant reduction of crosstalk and read/write disturbs in the memory matrix, while the disadvantage is the scaling limitation due to the transistor footprint and additional contact. Stacking multiple layers would also be problematic without access to reliable thin-film transistors. In fact, the select transistor may provide dual roles as both a blocking switch and an analog electron "flow valve" to limit the SET/RESET currents during write. Since a MOSFET operated in the saturation mode can be used as a current source, the SET/RESET current limits can be tuned by adjusting the gate voltage. Substantial improvement in write endurance has been reported in switching HfO_x RRAM cells if a 1T1R circuit was used instead of a 1R circuit [23]. Moreover, MLC operation has been demonstrated by adjusting the SET current in ON switching [24, 25].

1.3 Active feedback circuit

For a passive crossbar array, the option of using a 1T1R circuit no longer applies. To obtain a similar effect as Icomp or 1T1R, an alternative method is to use external circuitry to provide similar functionality. An active FB loop is found useful in such a case. A closed-loop program/erase circuit can constantly monitor the device resistance during the program/erase operation, and immediately terminate the programming voltage or current when a predetermined resistance state is sensed. Compared to aforementioned methods, an additional advantage of a FB circuit is the write time is limited as well as the write current/voltage. In the case of 1T1R circuit, the set current is limited by the select transistor, while the set duration (e.g., pulse width) is predetermined, which may be longer than needed. With a fixed write pulse width, there are no means that could be practically implemented that can monitor the state of the memory cell during the write period and terminate the write pulse when the desired state was achieved. Since the state of a memristive device is affected by the time integral of the electrical stimuli (i.e., flux or charge) rather than their instantaneous values, controlling the programming signal pulse width is necessary to control the device resistance. MLC operations can be realized by such a FB mechanism.

Using a FB driver circuit that controls current instead of voltage has several expected advantages. On the cell performance perspective, an extra knob to control the write operation is made possible. The memristive device can be written to a targeted analog state with optimized current waveforms. Both the magnitude of the current (pulse height) and time duration (pulse width) can be engineered. For example, a ramp current with an increasing current magnitude is preferred than a square-wave pulse for cleaner frequency domain components. The current ramp rate may be engineered as a linear or nonlinear function of time, e.g., logarithmic, to minimize the overshoot of the state variable w. A more complex circuit can be designed to adjust the current ramp rate in real time by applying the concept of a proportional-integral-derivative controller (PID controller) to reach the optimal damping condition of the system. However, PID FB or its variants (PI, PD, etc.) are not compatible with memristive memory applications due to complexity and footprint considerations.

On the practical side, to be integrated into a high-density memory chip, a closed-loop FB write circuit should be implemented with CMOS circuitry with a minimal footprint and low power consumption. For example, a single FB driver circuit can be used to write memory cells sequentially when coupled to multiplexer/demultiplexer circuitry, albeit at the expense of a slower write speed if compared with parallel write schemes. In general a high bandwidth, low power FB circuit is desired for high-speed write operations.

This paper will only discuss the write operation of a single memristive device. Writing to a memristive memory cell embedded in a crossbar array is beyond the scope of this work and will be covered separately. An important aspect for writing memristive memory cells embedded in a transistor-less, passive, crossbar memory array is to minimize issues of crosstalk, e.g., interference from sneak-path currents through neighboring cells in the LRS; and interference from half-select currents through half-selected devices connected to the selected row or column. It is assumed that the issues of interference from parasitic sneak-path or half-select currents can be addressed by engineering the memory cell device by such means as using a composite memory cell made of a complementary pair of memristive elements that always have the same high resistance independent of the stored binary information [26].

2 Circuit design and simulation

Let us now discuss the details of a prototype FB circuit designed for writing a memristive switch to a predetermined state. Figure 4 illustrates an analog FB circuit designed for ON (SET) switching, in which the device switches from a HRS to a LRS. The FB controlled SET operation is performed in three consecutive steps: First, identical current

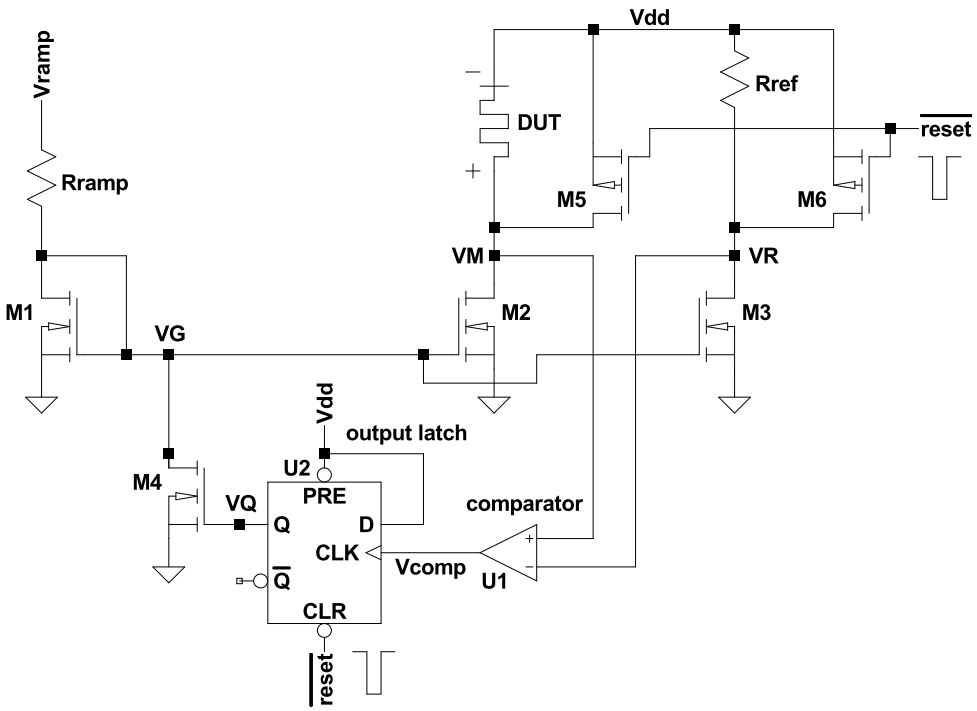

Fig. 4 Schematic circuit diagram of a closed-loop current driver to switch a memristive device (DUT) connected in floating configuration from HRS to LRS. With a slight modification, similar driver circuit can be used to switch the DUT in grounding configuration (not shown)

ramps are simultaneously applied to the memristive device under test (DUT) and a linear reference resistor R_{ref}. The current ramp is created by a ramp voltage applied to an input circuit containing a current limiting resistor and the master transistor (M1) of a dual-output current mirror. One output of the dual-output current mirror applies the current ramp to the DUT (IM) through the slave transistor M2, and the second output applies the same current ramp to R_{ref} (IR) through the second slave transistor M3. The level of current ramp is controlled by the current limiting resistor R_{ramp}. The voltage drops caused by the dual ramp currents are monitored by sensing the corresponding voltages on the DUT (VM) and on R_{ref} (VR) using a high-speed differential comparator (U1). The value of R_{ref} is selected to set the target resistance state of the DUT to be approximately equal to R_{ref}. Since the memristive DUT has nonlinear I–V characteristics and is more resistive at low bias voltages, VM at low currents is initially less than VR and changes in a highly nonlinear manner as a linear current ramp is applied. When a HRS to LRS switching event occurs in the DUT, the resistance suddenly drops and the voltage drop across the DUT suddenly decreases, causing the sense voltage VM to increase and surpass the reference voltage VR. As a result of the switching event, the differential input to the comparator, VM–VR, changes sign, and the output (V_{comp}) switches from logic low to logic high. The comparator output is connected to the clock input of a D flip-flop (U2) and the Q output of the latch is connected to the gate of a shunt transistor (M4). The latch output (VQ) is initially reset to logic low to set the shunt transistor (M4) in the high impedance state. When the output of the comparator (U1) switches from logic low to logic high, the latch (U2) will toggle and cause VQ to switch to and maintain a logic high state to switch M4 to a low resistance state. When M4 is in a low resistance state, M4 will bypass the ramp current flowing through M1 and clamp the mirror gate control voltage (VG) to near ground. Consequently, the mirror output transistors (M2 and M3) are switched off and the current ramps through the DUT and R_{ref} are terminated, even though V_{ramp} could still be rising. The LRS resistance value of the DUT will be set to be approximately equal to R_{ref}, and the corresponding state variable w, will be fixed and not be written beyond the designed state threshold.

The FB write circuit in Fig. 4 was simulated using the Cadence Virtuoso Spectre Circuit Simulator. The MOSFETs in the FB circuit were modeled using the TSMC 350 nm (channel length) CMOS technology node. In the simulations, we applied a SPICE model developed for the TiO_2 memristive device [27] in which the switching device is modeled as a tunnel junction with barrier width w in series with a channel resistor [21]. The tunnel barrier width w can be modulated by changing the magnitude and polarity of the voltage/current signals applied to the memristor SPICE model. The memristor SPICE model implements the modeling equations of a TiO_2 memristive device as described in Ref. [21]. Wide channel widths (20 μm) were used for the mirror transistors to accommodate relatively large write currents (∼1 to 10 mA) required to switch the TiO_2 memristive device. For high-density integration, the device write current will need to be reduced to the order of 10 μA or less.

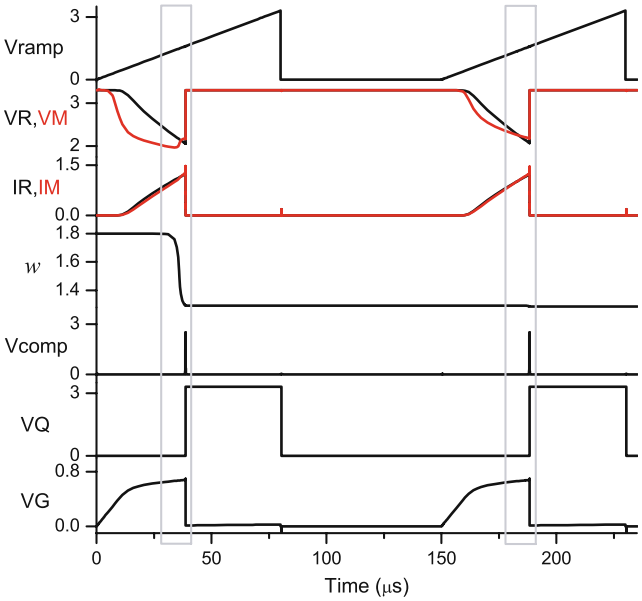

Fig. 5 Simulated waveforms of two sequential FB ON switching operations of a model TiO_2 memristive device using the SPICE model from Ref. [27]. The voltage and current units are volt and mA and the unit for w is nm. The switching events are highlighted by the *gray boxes*

Figure 5 summarizes the simulated waveforms of the SET operation using the closed-loop write circuit shown in Fig. 4. The supply voltage V_{dd} was set at 3.3 V. A sequence of two linear current ramps was simulated, while results from other types of ramp waveforms are qualitatively similar. The simulation shows that the memristor state variable w remains at the initial value of 1.8 nm (OFF state) until VM approaches near the switching threshold, where w quickly drops to 1.3 nm within a switching period of ~8 μs. Further decrease of w is prevented by the response of the FB loop that terminates the current flowing through the DUT. The efficacy of the FB circuit is demonstrated by the fact that a second write cycle applying an identical current ramp does not further decrease w, while in the case of an open-loop write, w continues to decrease (data not shown).

To design a physical FB circuit, special considerations are needed to minimize the overall FB loop response time, i.e., the time delay between the instant the DUT switches to an ON state and the instant that the current ramp is terminated. A high-bandwidth comparator with the shortest possible propagation delay at an allowable power consumption budget is desired. The FB circuit is designed to bypass the current ramp rather than turn off the externally sourced voltage ramp to minimize the time delays in terminating the DUT current. To this end, the shunt transistor (M4) as well as the output transistors in the current mirror (M2 and M3) are selected to be fast switching MOSFETs with minimal node capacitance. N-channel MOSFETs (NMOS) are therefore preferred than their p-channel counterparts (PMOS) for higher mobility and smaller node capacitance. A latched comparator output stage is necessary to maintain the comparator output level after the DUT has been switched to prevent oscillations in the FB circuit. This is due to the fact that once the current ramp is terminated, the voltage drop across the DUT and R_{ref} will change, and the relationship of the inputs to the differential comparator may flip and cause the shunt transistor to prematurely turn off and re-establish a high current through the DUT before the external voltage ramp can be removed. Designs of similar regenerative two-input latched comparator circuits are abundant in the literature [28]. After the DUT is written, the FB circuit including the comparator may be reinitialized for the next write operation. A reset signal is applied to reset the comparator latch to a logic low while two reset transistors (M5 and M6) are pulsed to initialize the differential latched comparator.

It is noteworthy that the basic design of this FB circuit is not exclusive and is not limited to the presented example. For example, the simple current mirror is far from an ideal current source. To increase the output impedance or extend the voltage range, more complex current mirror variants can be applied, such as cascode, wide-swing cascode, or gain-boosted current mirrors incorporating operational amplifiers. The cost of more complex current mirrors is a larger footprint and higher power consumption. To further reduce the power consumption, another NMOS transistor can be placed in between R_{ramp} and the mirror master transistor M1. The gate of this transistor is controlled by the $\bar{Q}$ output of the latch U2, so that when the memristor is switched to the ON state, the current ramp through M1 is physically turned off rather than be shunted through M4 to ground. The circuit footprint is also reduced because the channel width of M4 does not need to be larger than M1.

For bipolar switching memristive devices, a bi-directional current flow through the DUT will need to be realized. A relatively simple method to implement bi-directional current flow is to utilize an "H-bridge" design, in which the DUT bridges two or more current mirrors serving as the FB driver for the SET/RESET operation. A set of CMOS inverter switches is used to apply either a positive or negative current to the DUT and to switch in the corresponding reference and FB control circuits. With mirrors composed of either NMOS or PMOS transistors, the DUT can be placed in either floating or grounded configurations. Circuit block diagrams of two examples of bipolar FB current write drivers are shown in Fig. 6.

The stochastic distribution of memristive switching can be emulated in SPICE simulations by adding a Gaussian variance to the scaling parameter w_c in the model equation of motion for w that fits experimental result from TiO_2 devices [21]. Assuming a 3% variance of w_c ($w_c = 1.07 \times 10^{-1}$ nm, $\sigma = 3.21 \times 10^{-3}$ nm), Monte Carlo simulations were performed for both open-loop and closed-loop ON switching. In both cases, the same current ramp was supplied to the DUT and reference device. The pulse width in

the open-loop case was adjusted to be identical to the nominal pulse width in the closed-loop (FB) case. 100 Monte Carlo cases were simulated with the fixed pulse width in the open-loop model, whereas the pulse width in the FB model varied as a function of the statistical variable w_c. The initial OFF state is set at $w = 1.8$ nm. Figure 7 shows the histograms of the distribution of w for 100 Monte Carlo write operations. The results for the open-loop write simulations show a distribution for w with a range of 1.29 to 1.71 nm and a mean value of 1.40 nm, and for closed-loop write the variance of w is reduced by a factor of ∼7 to the range of 1.29 to 1.35 nm with a mean value of 1.32 nm. Moreover, in the open-loop case, the w distribution is skewed to larger values, suggesting a lognormal distribution. By intentionally inserting a propagation delay τ in the FB loop, the resulted mean value of w shows a systematic downshift, indicating that the device is overwritten to more conductive state if the FB response is delayed. The lower limit of $\tau = 1$ µs in our simulation is very conservative. It is expected that further narrowing of w distribution could be reached by a much faster FB loop. A bandwidth in the order of 100 MHz is feasible with the current CMOS technology.

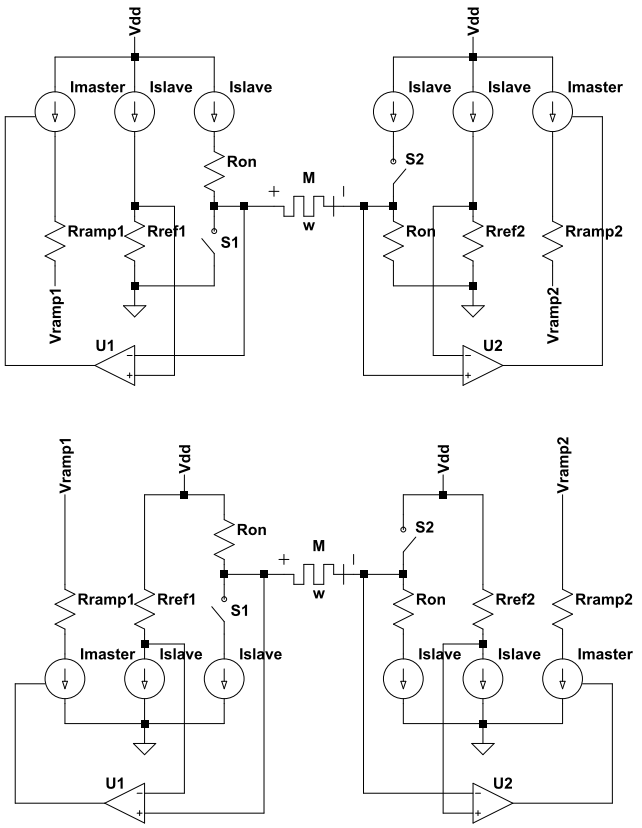

Fig. 6 Functional circuit block diagrams of the closed-loop write circuit for set and reset a bipolar switching memristor device with the floating DUT configuration (*top*), and grounding DUT configuration (*bottom*). Instances of R_{on} represent the on-resistance values of NMOS/PMOS switches

3 Experimental test

A prototype breadboard test circuit was constructed using discrete MOSFET transistors and comparator chips. In the initial tests, nonlinear negative-differential–resistance (NDR) devices, such as thyristors and lambda diodes, were used to emulate the ON and OFF switching I–V characteristics of memristive devices. Although these off-the-shelf devices do not have the nonvolatile memory effect, they do exhibit a relative fast (∼1 µs) switching-like I–V that can be used to mimic the memristive switching. Other benefits of

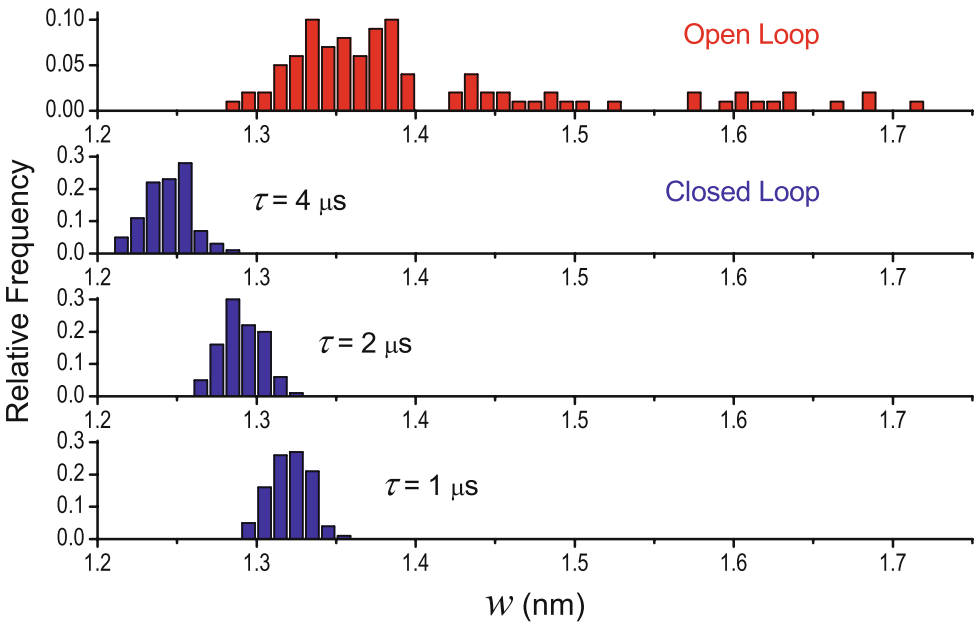

Fig. 7 Distributions of the analog state variable w for ON switching in the open-loop (*topmost panel*) and closed-loop (*lower panels*) write operations obtained by Monte Carlo simulations assuming a 3% Gaussian noise in the scaling parameter w_c. The mean value of w shows a systematic downshift as the FB delay time τ increases from 1 µs to 4 µs

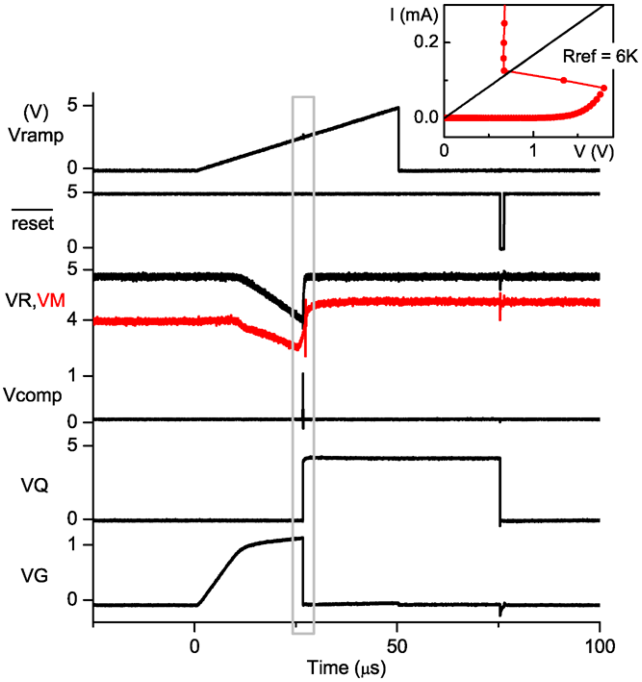

Fig. 8 Measured waveforms of FB ON switching operation of a thyristor device. The switching event is highlighted by the *gray box*. *Inset* shows the measured thyristor I–V characteristics together with the slope of $R_{\text{ref}} = 6\ \text{k}\Omega$

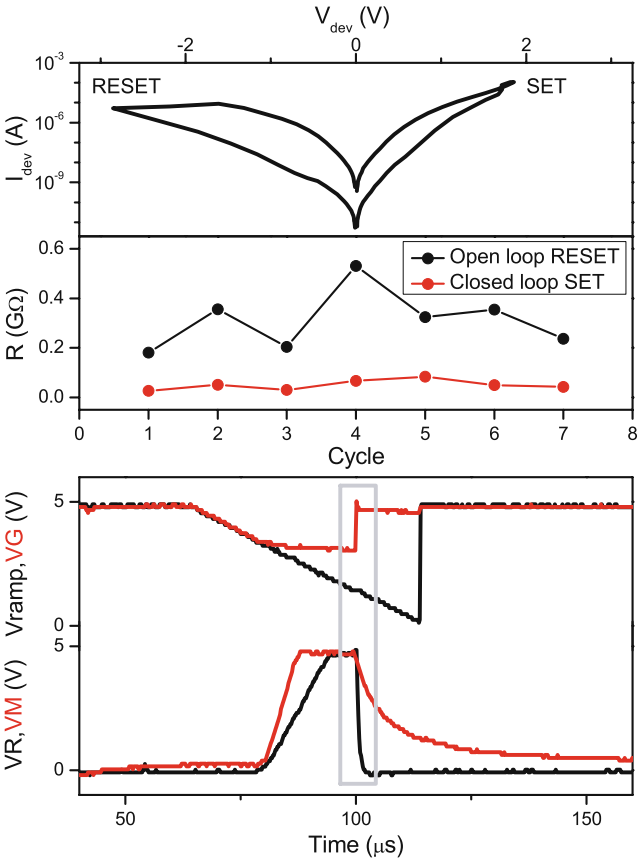

Fig. 9 *Top* to *bottom*: I–V characteristics, zero-bias resistance values, and switching waveforms of closed-loop/open-loop ON/OFF switching operations of a nanoscale TiPt/TiO_2/Pt crossbar device. Note that the waveforms are flipped vertically because the FB circuit was built with PMOS mirrors with the DUT in grounding configuration. V_{dd} was set at 5 V

using the conventional NDR devices to demonstrate the FB write circuit include voltage/current robustness and flexibility in I–V characteristics tunable by additional passive resistors or diodes. As shown in Fig. 8, the waveforms produced by a thyristor device (thyristor: BS08D and a Zener diode) in FB ON switching are similar to the simulated results in Fig. 5. While tests on TiO_2 memristive devices are still ongoing, preliminary results already confirmed that the device can be SET or RESET using the FB circuit (see Fig. 9). However, the performance of the FB driver is hindered by the fairly large stray capacitances on the breadboard and the large lead resistance of the nanoscale crossbar device. For example, a large bypass capacitor at the drain node of the M2 transistor discharges after the gate of M2 is switched off, which will overwrite the memristor device by providing extra flux. Printed circuit board and surface mount packages are beneficial to mitigate this issue, with a final goal of fabricating an integrated FB write circuit to drive passive memristor crossbar arrays.

4 Summary

As a summary, we have defined a closed-loop current-feedback process to limit the writing of a memristor device to a predetermined state threshold value. Overwriting of the memristive analog state is prevented by removing the write current after the predetermined resistance threshold is exceeded. A CMOS feedback write driver circuit is designed and simulated using a device SPICE model based on the switching dynamics of TiO_2 memristive devices. Monte Carlo simulation results show that an active feedback effectively narrows the statistical distribution of the state variable w, the tunneling barrier width, which affects the resistance in an exponential fashion. Both an integrated and a discrete version of the feedback driver circuitry have been designed and constructed, and experimental tests on TMO based memristive devices are currently being undertaken.

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References

1. R. Waser, R. Dittmann, G. Staikov, K. Szot, Adv. Mater. **21**, 2632 (2009)
2. W. Welnic, M. Wuttig, Mater. Today **11**, 20 (2008)
3. R. Waser, M. Aono, Nat. Mater. **6**, 833 (2007)
4. H. Pagnia, N. Sotnik, Phys. Status Solidi A **108**, 11 (1988)
5. A. Sawa, Mater. Today **11**, 28 (2008)
6. L.O. Chua, IEEE Trans. Circuit Theory **18**, 507 (1971)
7. L.O. Chua, S.M. Kang, Proc. IEEE **64**, 209 (1976)
8. G. Dearnaley, A.M. Stoneham, D.V. Morgan, Rep. Prog. Phys. **33**, 1129 (1970)
9. G.S. Snider, Nanotechnology **18**, 365202 (2007)
10. K.K. Likharev, J. Nanoelectron. Optoelectron. **3**, 203 (2008)
11. A.G. Steventon, J. Phys. D, Appl. Phys. **8**, 1869 (1975)
12. I.V. Karpov, M. Mitra, D. Kau, G. Spadini, Y.A. Kryukov, V.G. Karpov, Appl. Phys. Lett. **92**, 173501 (2008)
13. A. Chimenton, IEEE Electron Device Lett. **31**, 198 (2010)
14. A.J. Katz, A.H. Thompson, Phys. Rev. B **34**, 8179 (1986)
15. V. Ambegaokar, B.I. Halperin, J.S. Langer, Phys. Rev. B **4**, 2612 (1971)
16. C.B. Shah, Y.C. Yortsos, Phys. Fluids **8**, 280 (1996)
17. W. Lai, J. Sune, E. Wu, E. Nowak, in *Proceedings of the 42nd Annual IEEE Reliability Physics Symposium* (2004), p. 102
18. G. Medeiros-Ribeiro, F. Perner, R. Carter, H. Abdalla, M.D. Pickett, R.S. Williams, Nanotechnology **22**, 095702 (2011)
19. J.J. Yang, M.D. Pickett, X. Li, D.A.A. Ohlberg, D.R. Stewart, R.S. Williams, Nat. Nanotechnol. **3**, 429 (2008)
20. D.B. Strukov, G.S. Snider, D.R. Stewart, R.S. Williams, Nature **453**, 80 (2008)
21. M.D. Pickett, D.B. Strukov, J.L. Borghetti, J.J. Yang, G.S. Snider, D.R. Stewart, R.S. Williams, J. Appl. Phys. **106**, 074508 (2009)
22. D.B. Strukov, R.S. Williams, Appl. Phys. A **94**, 515 (2009)
23. M.-J. Tsai, in *Advances in Nonvolatile Memory Materials and Devices, Engineering Conferences International*, Suzhou Industrial Park, China (2010)
24. H.Y. Lee, P.S. Chen, T.Y. Wu, Y.S. Chen, C.C. Wang, P.J. Tzeng, C.H. Lin, F. Chen, C.H. Lien, M.-J. Tsai, in *IEEE Electron Dev. Meeting (IEDM)* (2008), p. 297
25. U. Russo, D. Kamalanathan, D. Ielmini, A.L. Lacaita, M.N. Kozicki, IEEE Trans. Electron Devices **56**, 1040 (2009)
26. E. Linn, R. Rosezin, C. Kugeler, R. Waser, Nat. Mater. **9**, 403 (2010)
27. H. Abdalla, M.D. Pickett, in *IEEE International Symposium on Circuits and Systems* (*ISCAS 2011*) (2011) (accepted)
28. I.E. Opris, Electron. Lett. **33**, 1273 (1997)