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Review Article

Ferroelectric Devices for Intelligent Computing

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Recently, transistor scaling is approaching its physical limit, hindering the further development of the computing capability. In the post-Moore era, emerging logic and storage devices have been the fundamental hardware for expanding the capability of intelligent computing. In this article, the recent progress of ferroelectric devices for intelligent computing is reviewed. The material properties and electrical characteristics of ferroelectric devices are elucidated, followed by a discussion of novel ferroelectric materials and devices that can be used for intelligent computing. Ferroelectric capacitors, transistors, and tunneling junction devices used for low-power logic, high-performance memory, and neuromorphic applications are comprehensively reviewed and compared. In addition, to provide useful guidance for developing high-performance ferroelectric-based intelligent computing systems, the key challenges for realizing ultrascaled ferroelectric devices for high-efficiency computing are discussed.

1. Introduction

In the past few decades, the advancements in information technology have improved the global economy while changing people's lifestyle. This revolution relies on two aspects, the establishment of information-processing theories and development of electronic hardware. These established theories and the software based on them enable computers to process highly complicated tasks. Simultaneously, with the rapid evolution of computing hardware, the computing capability (CC) of devices has considerably expanded as it is mainly driven by transistor scaling. However, in the past decade, transistor scaling is approaching its physical limit, hindering the further development of the CC. In addition, as shown in Figure 1(a), computing systems need to overcome several challenges for processing increasing amounts of data in the present era. The issue of "heat wall" [1], which hinders the enhancement of the main frequency of the processer owing to the rising power density and heating effect, needs to be addressed. Furthermore, the issue of "memory wall" [2], which is caused by large performance or area gap between the logic device and memory cell, and the von Neumann bottleneck [3], which refers to the delay and power issues caused by the inefficient data transfer between the memory module and logic processor, need to be overcome. As the demand for computing power increases, new materials and novel transistors should be explored to support the development of CC-based emerging technologies.

Intelligent computing is a new research area whose development highly relies on the improvement of CC [4, 5]. However, owing to the aforementioned computing bottlenecks, new storage and logic devices with higher speed and lower power consumption, such as memristors and phase-change memory devices, need to be introduced [6–9].

Among all the available technological alternatives, ferroelectric devices can overcome the "heat wall," "memory wall," and von Neumann bottleneck, as shown in Figure 1(b). As identified more than a century ago, the polarization of ferroelectric materials can be retained even after the removal of the external electric field. Ferroelectric materials have been

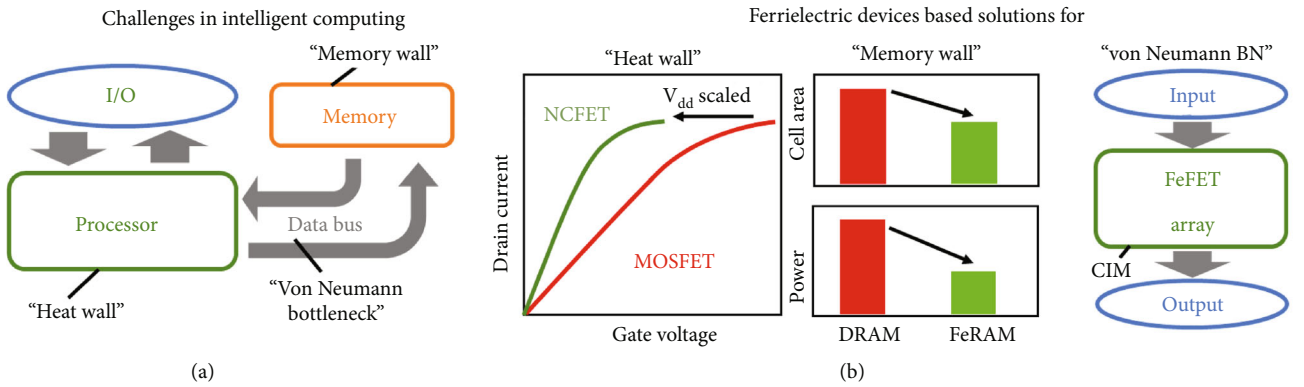

Figure 1: Schematics of (a) challenges faced by modern computers using von Neumann architecture and (b) solutions for "heat wall," "memory wall," and von Neumann bottleneck based on ferroelectric devices.

widely used as special-purpose memories in devices such as aerospace storage devices [10, 11]. In traditional ferroelectric materials, such as zirconium titanate (PZT) or barium titanate (BTO), the domain size is critical for retaining the polarization [12, 13]. The thickness scale of these materials is greater than 10 nm; thus, they are not adaptive to the nanoscale IC fabrication process. New ferroelectric materials and devices with high scalability potential can solve these issues. For example, a negative capacitor field-effect transistor (NCFET) with hafnium-based ferroelectric gate oxides can enhance the subthreshold swing (SS) to reduce the driving voltage of the integrated circuits (ICs), thus effectively suppressing the power consumption and heating effect [14]. Ferroelectric capacitor-based random access memory (FeRAM) and ferroelectric field-effect transistor- (FeFET-) based memory show excellent performance in dynamic random access memory (DRAM) replacement and embedded applications [15, 16]. In addition, FeFETs can be used as artificial neurons and synaptic devices in the neuromorphic system to overcome the von Neumann bottleneck [17, 18].

In this article, we focus on emerging ferroelectric devices applicable for highly efficient and intelligent computing. High-κ and other novel ferroelectric materials are reviewed in Section 2. This is followed by a comprehensive summary of the authors' study on low-power ferroelectric logic devices (Section 3), high-performance memory arrays (Section 4), and neuromorphic computing demonstrations (Section 5). Section 6 concludes this article with future prospects for emerging ferroelectric devices and their application in intelligent computing.

2. Emerging Ferroelectric Materials

Ferroelectricity has been observed in many types of materials. However, when the film thickness is reduced to less than 10 nm, most of the conventional ferroelectric materials lose their polarization characteristics at 25°C [19], rendering the ferroelectric devices incompatible with the nanoscale very-large-scale-integration-circuit processing technologies. The discovery of the polarization effect in high-κ materials, which are the commonly used gate-oxide materials for nanoscale MOSFETs, is a breakthrough for the mass production of ferroelectric transistors. In this section, we focus on the polycrystalline Hf-based and amorphous oxide-based ferroelectric materials and devices that have been shown to be compatible with the CMOS fabrication process. In addition, some recently reported novel ferroelectric materials and devices are also briefly described.

2.1. Doped-HfO_2 Ferroelectric Materials. Since the discovery of ferroelectricity in doped-HfO_2 films in 2011 [20], ferroelectric field-effect transistors (FeFETs) and ferroelectric random access memory (FeRAM) have received significant attention [21–25]. Polycrystalline doped-HfO_2 films are considered as promising gate-oxide materials owing to their excellent ferroelectric properties as well as high compatibility with the ultrascale CMOS process. Compared with traditional perovskite ferroelectric materials, doped-HfO_2 ferroelectric films exhibit a higher coercive field (E_c~1–2 MV/cm) and lower permittivity (~30), which are desirable for low-power nonvolatile memory devices with excellent retention characteristics.

Doped-HfO_2 materials have three types of crystal structures, namely, monoclinic, tetragonal, and cubic structures. The phase transition can be achieved through several approaches, for example, application of mechanical stress, postdeposition annealing, and application of higher deposition pressure [26, 27]. In 2011, Böscke et al. discovered that the use of Si as a dopant could facilitate the formation of asymmetric orthorhombic-phased HfO_2 and hence the generation of ferroelectricity in the film [20]. Subsequently, various elements were introduced as dopants for the formation of ferroelectric doped-HfO_2 materials, such as $HfZrO_x$ (HZO), $HfAlO_x$ (HAO), $HfLaO_x$ (HLO), and $HfGeO_x$[28, 29]. Among these doped-HfO_2 ferroelectric materials, HZO was studied most intensively owing to its remarkable ferroelectric characteristics, particularly at a Zr composition between 0.3 and 0.7. From the perspective of fabrication, it is easier to achieve stable and uniform HZO ferroelectric films by atomic layer deposition and annealing. Moreover, the annealing temperature required for forming the ferroelectric HZO thin films can be as low as 400°C [30], while that for HfO_2 films doped with other elements is usually greater than 650°C [31–34].

Recently, material properties, such as oxygen vacancy, doping concentration, film stress, and surface/interfacial energy, have been reported to influence the ferroelectric properties of doped-HfO_2 ferroelectric films. Peng et al. [35] measured the polarization-voltage (P-V) curves of the HZO films with different Zr compositions. Figure 2 shows the P-V curves for TaN/HZO/TaN samples. For the postannealing temperature within the range of 500–550°C, the P-V curves of the HZO metal-insulator-metal (MIM) structures tend to saturate in a subloop state. As the Zr composition increases, the remnant polarization (P_r) of the film becomes stronger, and the hysteresis loop becomes narrower at a zero voltage bias; these can be considered to be the superimposed antiferroelectric-like characteristics [33, 36]. Pesic et al. [37, 38] reported the use of electrodes with different work functions to introduce a built-in electric field into the antiferroelectric layer to achieve a stable ferroelectric phase. Reyes-Lillo et al. [39] reported that the conversion of ZrO_2 from the antiferroelectric to the ferroelectric state could be realized by introducing compressive strain into the ZrO_2 film. In addition, Materlik et al. [40] suggested that the stability of the metastable ferroelectric phase was related to the surface energy effect and proposed a model based on the surface energy.

2.2. Amorphous Oxide-Based Ferroelectric Materials. Excessive research has focused on promoting the fabrication and application of polycrystalline doped-HfO_2 FeFETs [41, 42]. However, when the devices are scaled down to the nanometer level, the domain- and grain-boundary-induced variations in the polycrystalline doped-HfO_2 ferroelectric films degrade their performance and reliability [43, 44]. Thus, an amorphous or single crystalline ferroelectric material is desirable for achieving high-performance and reliable ferroelectric devices [45].

Recently, ferroelectric-like phenomena have been observed in amorphous oxides. These phenomena are related to the mobile oxygen vacancies in the amorphous materials. Because amorphous materials lack domains or boundaries, the amorphous ferroelectric oxides mentioned above can be used for achieving nanoscale transistors exhibiting low device variation and nonvolatile storage function [46, 47]. Amorphous materials that exhibit polarization switching include ZrO_2 [48], Al_2O_3 [49, 50], HfO_2 [51], La_2O_3 [52], and TiO_2 [53], which are compatible with the conventional CMOS process and have been employed as high-κ gate dielectrics for logic transistors.

Liu et al. [48] reported the P-V loop characteristics of a TaN/α-ZrO_2/Ge device, demonstrating a ferroelectric-like device behavior with a nonzero P_r less than 2 $\mu C/cm^2$. In contrast to doped-HfO_2 ferroelectric devices, no wake-up or imprint phenomena were observed for the ferroelectric α-ZrO_2 capacitors. Peng et al. [49, 50] reported the integration of amorphous Al_2O_3 films in MIM and MOS capacitors to achieve polarization-switching characteristics, as shown in Figures 3(a) and 3(b). Piezoresponse force microscopy (PFM) tests of the Al_2O_3 film on TaN/Si samples were conducted, demonstrating the opposite natures of ferroelectric dipoles on the surface of Al_2O_3 on TaN. X-ray photoelectron

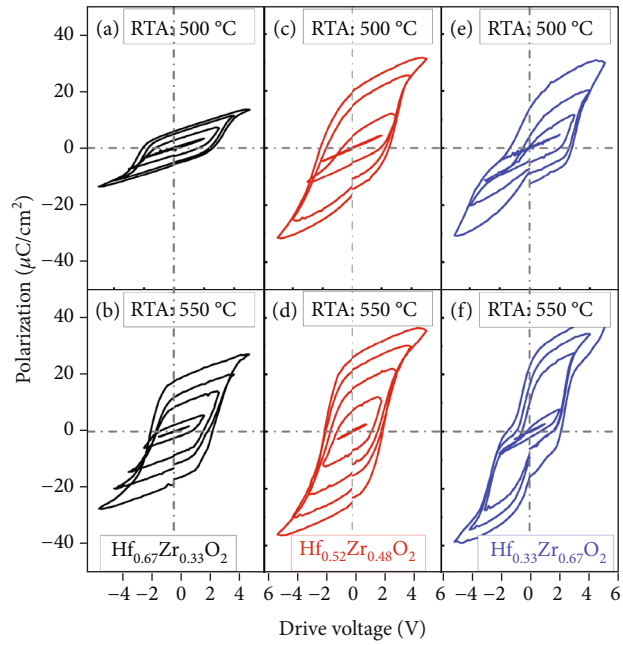

Figure 2: Measured P-V curves of HZO films with different Zr compositions annealed at 500 and 550°C. (a) and (b) show the $Hf_{0.67}Zr_{0.33}O_2$ film annealed at 500 and 550°C, respectively. (c) and (d) show the $Hf_{0.52}Zr_{0.48}O_2$ film annealed at 500 and 550°C, respectively. (e) and (f) show the $Hf_{0.33}Zr_{0.67}O_2$ film annealed at 500 and 550°C, respectively. With the postannealing temperature increasing from 500 to 550°C, the P-V curves of the HZO tend to saturate in a subloop state. An evolution of the film from ferroelectric to antiferroelectric-like behavior is observed as the Zr composition increases [35].

spectrum (XPS) measurement showed that a TaO_x interface layer was formed between TaN and Al_2O_3. This layer provided oxygen vacancies in the form of Al suboxides due to the scavenging effect, as shown in Figures 3(c) and 3(d). Feng et al. [54] strategically modulated the deposition conditions of Al_2O_3 in TaN/Al_2O_3/Si capacitors to change the film property from paraelectric to ferroelectric-like. The oxygen-deficient Al_2O_3 layer with the migration barrier is the key for achieving ferroelectric-like properties. It can be hypothesized that as more oxygen vacancies (Vo^+) are generated in the Al_2O_3 film, the migration barrier for Vo^+ and O^{2-} becomes weaker. The in situ ARXPS results clearly show the scavenging effect at the interface, which occurs upon TaN film deposition, leading to the formation of the TaON interfacial layer. The TaON interfacial layer was proposed to act as an oxygen reservoir. The transport of the Vo^+ and O^{2-} pair was introduced to explain the dynamic process of polarization switching, as shown in Figures 3(e) and 3(j), with the consideration of the gate leakage current. With an applied gate bias, the ions pass through the migration barrier of the oxide layer to the interface. The barrier will "lock" these separated charging ions even after the applied voltage is removed. This assists in generating interface-induced long-range polarization.

2.3. Other Emerging Ferroelectric Materials. The development of ferroelectric transistors is a significant breakthrough

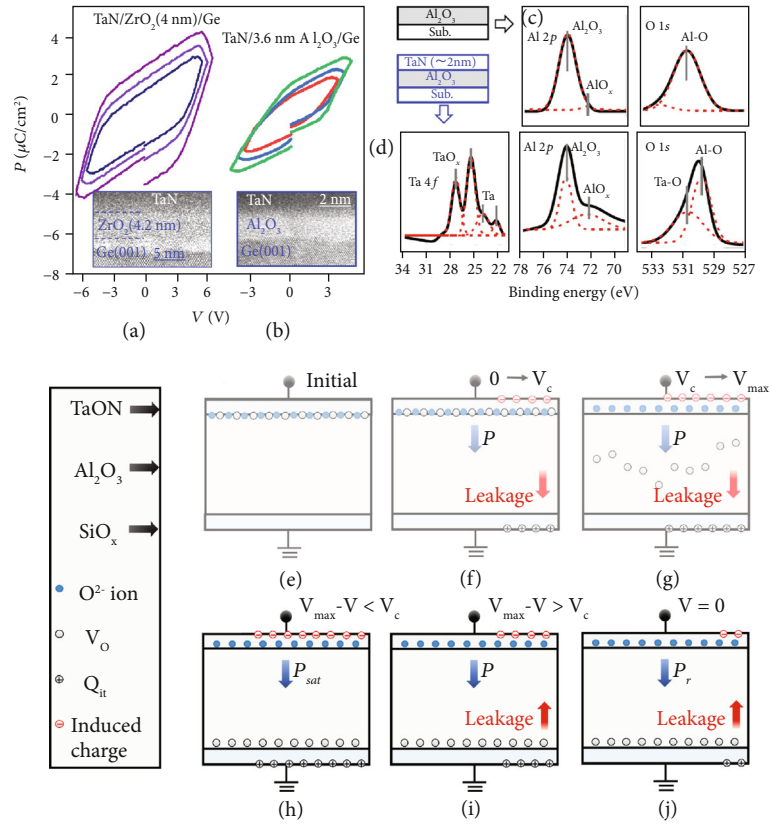

FIGURE 3: Measured *P-V* curves and corresponding HRTEM images of (a) $TaN/ZrO_2/Ge$ [48] and (b) $TaN/Al_2O_3/Ge$ ferroelectric capacitors [50], showing the amorphous oxide. Core-level XPS spectra of (c) Al_2O_3 and (d) TaN/Al_2O_3 samples [49]. The solid and dashed lines show the measured and deconvolution results, respectively. (e–i) Proposed mechanism of ferroelectric-like behavior in $TaN/Al_2O_3/Si$ stack through migration of Vo^+ and O^{2-} (half cycle of polarization switching) [54].

in a wide range of intelligent computing applications such as nonvolatile memories, logic devices, and synaptic transistors. Such devices generally have planar MOSFET structure, in which the ferroelectric/semiconductor heterostructure is the fundamental building block [55]. Therefore, the realization of high-quality ferroelectric/semiconductor heterostructures is the core of this device integration technology. In traditional direct deposition techniques such as atomic layer deposition (ALD) and pulsed laser deposition (PLD), the integration of ferroelectric oxide thin films on conventional semiconductors is often hindered by critical issues in the growth process, including oxidation of the semiconductor surface, high thermal budget for ferroelectric growth, and lattice mismatch [56]. Atomically thin two-dimensional (2D) semiconductors that can form heterostructures using the van der Waals (vdW) force may be promising candidates to overcome this limitation and broaden the material set for high-quality ferroelectric/semiconductor heterostructures [57]. A typical fabrication process of the ferroelectric/2D semiconductor heterostructure is shown in Figure 4(a). With this transfer-based integration, precrystallized ferroelectric and semiconductor layers can be bonded at low processing temperatures. Such a physical assembly method is based on the vdW interaction between the layers and does not involve a direct chemical process, which is required in the aforementioned direct deposition approaches. Thus, versatile ferroelectric/2D semiconductor heterostructures with a clean interface can be easily realized through vdW integration without any strict requirements for direct chemical vapor deposition, such as lattice matching and high-temperature postfabrication crystallization. Moreover, compared to conventional bulk semiconductors, 2D semiconductors can enhance the modulation of the gate electric field owing to the reduced dielectric screening and therefore suppress the leakage current in the FETs owing to the confined charge carriers; they can also realize novel functions that are not possible using bulk semiconductor devices [58–60]. Therefore, 2D semiconductors provide an untapped material platform for achieving unprecedented advancements in the device performance and functionality of ferroelectric transistors [61].

In this section, we present a timely review of the recent advancements in intelligent computing applications based on the ferroelectric transistors prepared using 2D semiconductors (Figure 4). Nonvolatile memories are among the first applications of 2D ferroelectric-gate transistors [62, 63]. A typical 2D FeFET structure consisting of a ferroelectric gate (PZT thin film) and an approximately 2 nm thick 2D WSe_2 channel is shown in Figure 4(b) [63]. Excellent nonvolatile memory properties including a high switching ratio of 10^4, robust retention up to 1000 s, and excellent fatigue properties have been obtained in such a 2D FeFET (Figure 4(b))

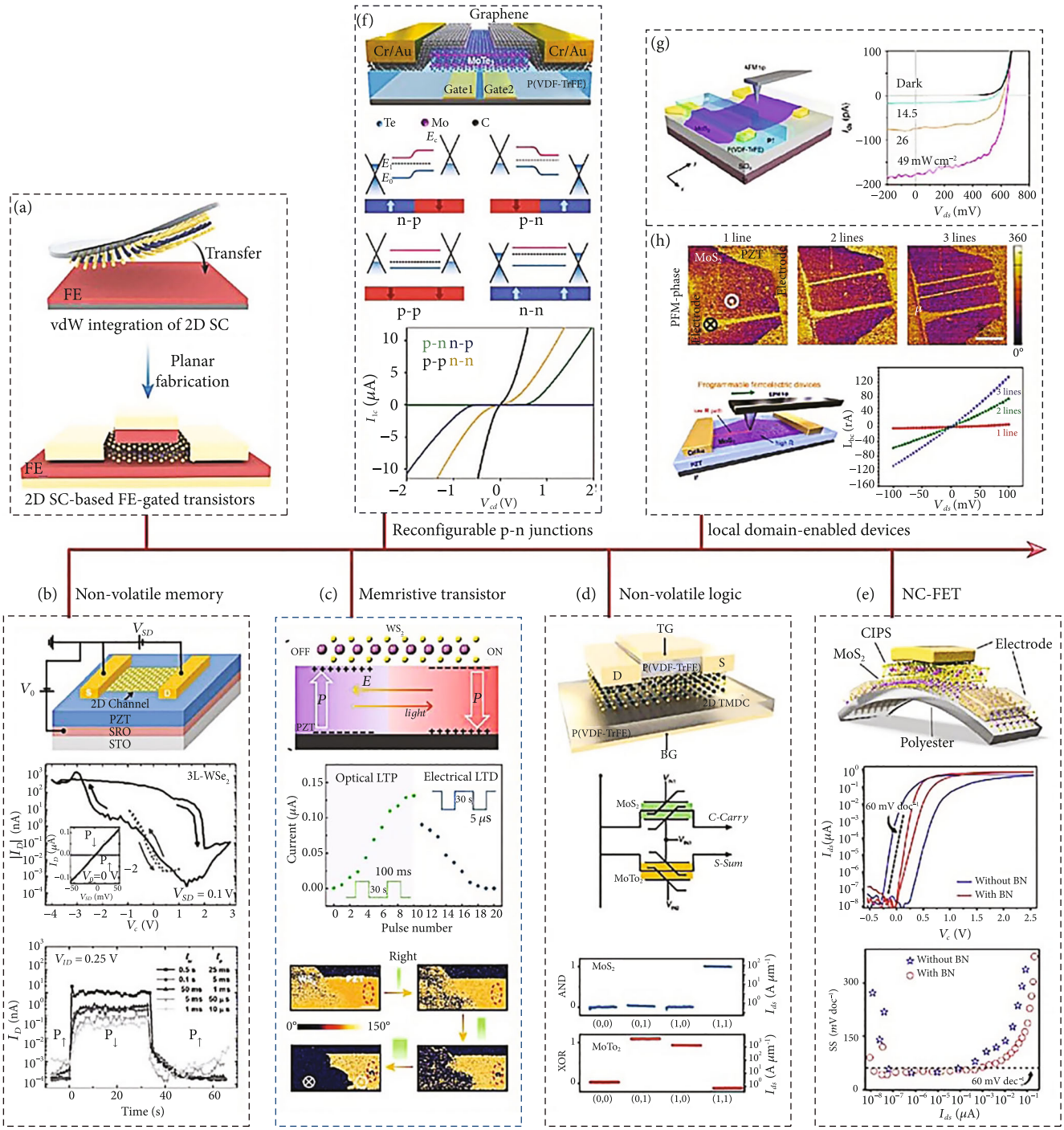

FIGURE 4: Intelligent computing applications of 2D semiconductor- (SC-) based ferroelectric- (FE-) gate transistors. (a) vdW integration of 2D semiconductor/ferroelectric heterostructures. Freestanding 2D semiconductor layers can be transferred onto the ferroelectric thin film. (b) Nonvolatile memories based on WSe_2/PZT FeFETs and their electronic properties [63]. (c) Optoelectronic memristive 2D FeFETs with synaptic functions [66]. (d) Nonvolatile logic gates and half adder based on dual-ferroelectric-gate 2D transistors [67]. (e) A full vdW CIPS/MoS_2 heterostructure-enabled flexible NC-FET and sub-60 mV/dec subthreshold swing is shown at the bottom panel [69]. (f) Reconfigurable homojunction based on split-ferroelectric-gate 2D transistors [70]. (g, h) p-n diode for photodetection and nanodomain-based conducting path engineering for local programmable memories, respectively, fabricated by the local nanoscopic scanning probe technique [71].

[63]. Here, during the 2D FeFET fabrication process, 2D semiconductor flakes are mechanically exfoliated onto PZT thin films without any high-temperature annealing. Benefiting from such a vdW integration process, the ferroelectric film/2D semiconductor structure is expected to retain a virginal interface with a genuine vdW gap; thus, it is expected

to solve the interface problems observed in conventional semiconductor-based FeFETs and exhibit a smaller depolarization field as well as a superior retention performance [64]. Beyond the binary memory effect induced by full polarization switching in 2D FeFETs, fractional polarization variation subjected to mixed ferroelectric domain configurations can be exploited as an approach to tune the electrical properties of 2D channels. Memristive behaviors featuring multilevel resistance states have been achieved in such devices by carefully modulating the switching history of 2D FeFETs. These devices can be used as 2D memristive ferroelectric transistors and synaptic devices [65]. Recently, light-controlled 2D memristive ferroelectric transistors have been proposed based on the efficient optoelectronic properties of 2D semiconductors. As shown in Figure 4(c), Luo et al. demonstrated the optoelectronic tunability of the memristive effect in WS_2/PZT FeFETs, wherein optically controlled long-term potentiation (LTP) and electrically modulated long-term depression (LTD) were achieved [66]. The optically mediated resistance switching behavior is based on light-triggered ferroelectric domain switching (PFM-recorded domain evolution images are shown in Figure 4(c)), which is due to the interplay between the photoinduced charge dissociation process in the 2D channels and the ferroelectric depolarization effect in the PZT thin films. This heterostructure-enabled new functionality suggests that the versatile coupling effects between the ferroelectrics and 2D semiconductors might lead to the development of more intriguing function devices. In addition to memristive-enabled analog computing devices, the ferroelectric-induced nonvolatile memory effect has been further explored for constructing nonvolatile logic devices. For example, dual-ferroelectric-gated 2D transistors, in which the double gate terminals could serve as two logic input variables for the one-transistor- (1T-) structured Boolean logic gate, have been proposed, as shown in Figure 4(d) [67]. Unipolar MoS_2 and ambipolar $MoTe_2$ semiconductor channels can be used to operate 2D dual-gate FeFETs as AND and XOR logic gates, respectively. A heterogenous 2T-cell-based nonvolatile half adder was also developed by accurately connecting these two devices. Because dual-ferroelectric-gated transistors cannot be easily achieved using conventional materials and fabrication techniques, the use of 2D materials and vdW integration lead to a new pathway for device structure and function innovations of FeFETs. In addition, 2D NCFETs can be operated with subthermal switching slopes and integrated with silicon-based substrates [68]. By exploiting the intrinsic mechanical flexibility of 2D materials, a full vdW $MoS_2/CuInP_2S_6$-(CIPS-) based flexible NCFET has been realized [69]. This device can further extend the application spectrum of 2D electronic devices (Figure 4(e)).

In addition to the aforementioned devices based on the homogeneous ferroelectric-gating effect, local ferroelectric-polarization-mediated 2D homojunctions can be used to enhance the CC in intelligent computing applications. Because of the ambipolar electronic properties and ultrathin nature of 2D semiconductors, electrostatic doping has been used as an efficient approach for selectively achieving p- and n-type 2D FETs [72–74]. The high doping capacity and local domain engineering ability of ferroelectrics compared to those of conventional dielectrics render them a promising gate material for nonvolatile and reconfigurable 2D homojunctions [75]. For example, Wu et al. showed that reconfigurable p-n, n-p, p-p, and n-n homojunctions could be realized in a single transistor using the local ferroelectric gating in split-ferroelectric-gated $MoTe_2$ transistors (Figure 4(f)) [70]. Furthermore, using the scanning probe technique with nanometer-level precision, arbitrary and rewritable nanopatterns with distinct electronic properties could be created on-demand in 2D semiconductors atop a ferroelectric gate. This technique was used to locally create p-n homojunctions in 2D MoS_2/P(VDF-TrFE) transistors, as shown in Figure 4(g) [71]. With such a device, excellent photodetection characteristics including a responsivity of approximately 12 A/W and detectivity over 10^{13} Jones in tip writing were achieved. Lipatov et al. further demonstrated the facile generation and erasing of conducting channels in unipolar MoS_2 channels atop the PZT ferroelectric film (Figure 4(h)), indicating an innovative nanoscopic engineering methodology for ferroelectric memory devices [76]. In general, beyond conventional ferroelectric-gate devices, 2D semiconductor-based ferroelectric-gated transistors have shown potential for more sophisticated device functions and high CMOS compatibility for device fabrication, paving the way for the development of intelligent computing devices.

3. Ferroelectric-Based Efficient Logic Device: NCFET

Reducing the driving voltage of the chips is a potential method to break the "heat wall," and its feasibility is highly dependent on the SS of the transistor. Ferroelectric NCFETs, together with the voltage amplification effect, can overcome Boltzmann's tyranny and achieve an SS of sub-60 mV/dec. Thus, they are regarded to have one of the most promising device architectures for ultralow-power applications and can reenable the rapid development of the IC industry [77–79]. Comprehensive investigations of NCFETs in terms of understanding the mechanisms involved, analysis of characteristics, determining design rules, and improvement in reliability have been performed in both the industry and academia [80–90]. This section focuses on the evolution of the NCFET technology and advancements in this field.

In 2008, Salahuddin and Datta proposed the concept of NCFET [91]. As shown in Figure 5(a), an NCFET is realized by replacing the conventional dielectric in a planar MOSFET with a ferroelectric material. The device utilizes negative differential capacitance ($dP/dE < 0$) to achieve surface potential amplification and an SS of sub-60 mV/dec. Prior to 2015, there was a lack of systematical characterization of its basic electrical performance, which hindered the practical application of its highly efficient logic device concept. To bridge this gap, Han et al. performed a series of studies on this topic [49, 92–94]. In 2016, Zhou et al. reported the first ferroelectric Ge and GeSn NCFETs (Figures 5(a)–5(c)) [95]. Incorporated with CMOS-compatible ferroelectric HZO, the Ge and GeSn NCFETs demonstrated an SS of less than 60 mV/dec, enhanced on-

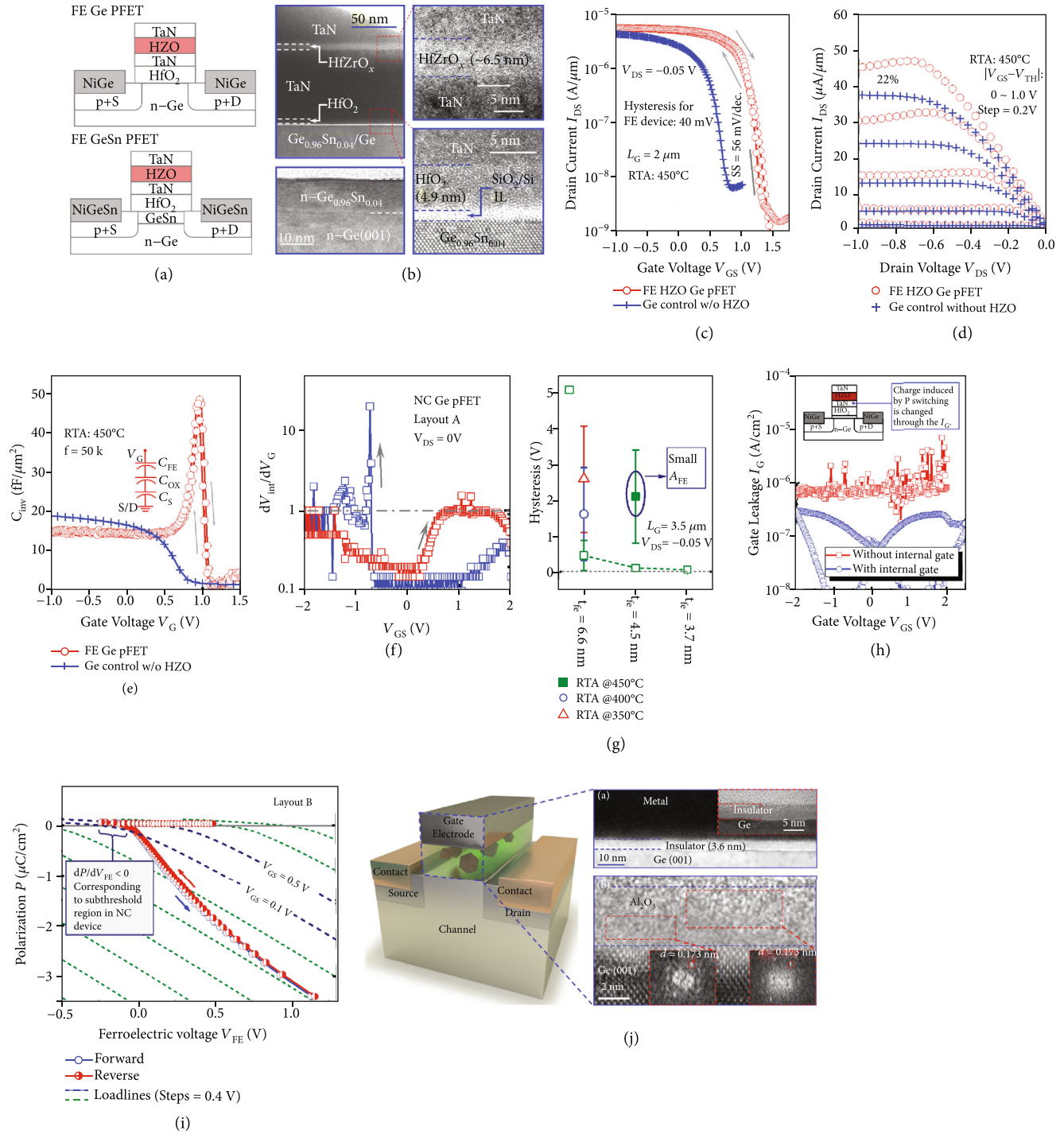

FIGURE 5: Investigation of NCFETs: (a, b) schematics and HRTEM images of the gate stack [95]; (c–f) basic electrical characteristics of I_{DS}-V_{GS} curves, NDR effects, capacitance peaks, and voltage amplification effects [81, 95, 96]; (g, h) performance optimization of hysteretic behavior and frequency characteristics [101–104]; (i) nature of NC effect [107]; (j) amorphous NCFETs [109].

state current, suppressed off-state current, and improved transconductance. Additionally, the other important characteristics of NCFETs were systematically reported, particularly the unique output and inversion capacitance characteristics, demonstrating the typical phenomenon of negative differential resistance (NDR) and inversion capacitance peaks (Figures 5(d) and 5(e)) [81]. As shown in Figure 5(d), the NDR effect causes a decrease in current with increasing drain voltage, which not only shows the potential for short channel effect (SCE) suppression but also opens a new pathway to improve the intrinsic gain or output resistance for analog applications. Figure 5(e) shows the capacitance characteristics of an NCFET and its reference device. Several times of enhancement in inversion capacitance are gained in NCFET, and the mechanisms of accelerated switching and enhanced gate control were revealed. The

voltage gain characteristics of a specially designed NCFET with an exposed internal metal gate were also investigated to monitor the response of the internal gate voltage (V_{int}) with V_{GS}. Figure 5(f) shows the $dV_{int}/dV_{GS} - V_{GS}$ curves of the NCFETs, where the voltage amplification ($dV_{int}/dV_{GS} > 1$) was achieved for both forward and reverse sweeping of V_{GS}, corresponding to the abrupt switching in $I_{DS} - V_{GS}$ curves at the same location of V_{GS}. This confirms that the voltage gain was induced by negative capacitance (NC) effects and the subsequently low SS (sub-60 mV/dec) [96, 97]. Thus far, the electrical characteristics of NCFETs have been systematically characterized and used for various NCFET-based applications.

After a careful investigation of the basic electrical characteristics of NCFETs, a thorough examination of the appropriate design rules for the transistors should be performed to optimize their hysteretic behaviors and frequency characteristics. According to Salahuddin and Datta, the inventors of NCFET, a ferroelectric capacitor (C_{FE}) usually demonstrates an intrinsic phenomenon of polarization hysteresis loops, leading to the instability and invalidity of the NC effect as well as the hysteretic behavior of NCFET [91]. Nonetheless, the NCFET can be stabilized using a series-placed conventional dielectric capacitances (C_{DE}). That is, the electrical performance of NCFETs depends on the capacitance matching degree. Hence, several research groups have focused on the elimination of hysteretic characteristics of the NCFETs [14, 81, 96, 98–104]. Since 2017, Zhou et al. systematically investigated the design rules for capacitance matching in NCFETs from various aspects, including the ferroelectric properties [100], thickness of the ferroelectric films (t_{FE}), and area ratio of C_{FE} to C_{DE} (C_{FE}/C_{DE}). As illustrated in Figure 5(g), the increased rapid thermal annealing temperature, decreased t_{FE}, and increased C_{FE}/C_{DE} can effectively modulate the magnitude of hysteresis, validating the design rule for capacitance matching and its effectiveness in optimizing the electrical performance of NCFETs. The frequency characteristics are the next key bottleneck for the practical application of NCFETs, owing to the requirement of high-speed switching for ICs. In 2015, Khan investigated the frequency characteristics of a PZT using the R-C delay system. The switching delay of the PZT capacitor was shown to have a decreasing tendency with a decrease in resistance connected in series. It was predicted that the intrinsic delay of the ferroelectric material could be as low as 19.9 ns. However, research on the frequency characteristics of NCFETs is still lacking. In 2017, Xidian University and GlobalFoundries [87] investigated the frequency characteristics of NCFETs and proposed a high-frequency compatible metal-ferroelectric-insulator-semiconductor (MFIS) architecture to realize an SS of sub-60 mV/dec in NCFETs operated up to the gigahertz scale. The MFIS structure could achieve faster polarization switching owing to its large leakage channel (Figure 5(h)) [101].

For the validation of the NC concept and the theoretical and experimental evaluations of the design rules, more attention was focused on understanding the NC effect. In 2016, Zubko et al. theoretically predicted the existence of the NC effect as a result of the field-drivable ferroelectric dipoles, which has piqued considerable interest in this field [105]. In 2018, Samsung [106] reported that the NC effect was caused by the ferroelectric polarization delay and could only be obtained during the transient response. In 2019, Yadav et al. [88] and Hoffmann et al. [89] separately demonstrated that the NC effect could be observed at both the micro- and macrolevels. However, the origin of the NC effect and its impact on the characteristics of NCFETs remained unknown. In 2019, Han et al. reported two important studies [107, 108] (Figure 5(i)), which experimentally clarified that the NC effect originated from the depolarization field and that incomplete polarization switching was sufficient to produce the NC effect for hysteresis-free NCFETs to achieve enhanced electrical performance. These studies are of great importance for the optimization of NCFET in terms of basic performance and reliability characteristics.

Owing to the discovery of the CMOS-compatible doped-HfO_2 ferroelectric materials, both ferroelectric memory and ferroelectric-based efficient logic devices have gained increasing attention. However, because of the intrinsic properties of doped-HfO_2 ferroelectric materials, the related ferroelectric devices always suffer from various reliability issues, such as the threshold voltage shift induced by the imprinting effect, performance variation induced by the wake-up effect, and insufficient endurance characteristics. In 2019, Peng et al. reported a new type of ferroelectric-like materials, known as the nanocrystal-embedded insulator (NEI), consisting of a main dielectric body and an embedded nanocrystal-ZrO_x [109]. The mechanism of such materials is quite different from the mainstream mechanism of doped-HfO_2 ferroelectric materials. The ferroelectricity of the former is not based on the nonasymmetric ferroelectric domains and can thus circumvent the performance shift appearing in the latter. Figure 5(j) shows the schematic of the NEI NCFETs and HRTEM images of the gate stack. Such novel NCFETs fabricated by nanocrystal ZrO_2 grains can also achieve a sub-60 mV/dec SS, an enhanced on-state current, a suppressed off-state current, and the NDR effect. In addition, the utilization of such types of ferroelectric materials can expand the range of gate insulators for use in future electronic devices to achieve improved electrical performance, high device reliability, and good process compatibility.

In this section, we comprehensively reviewed the revolution of NCFETs. Over the past decade, the concept of NCFETs was established theoretically and demonstrated experimentally from various perspectives, such as the basic electrical characteristics, typical phenomena, performance optimization, frequency characteristics, mechanism analysis, and structure innovations. Additional applications based on the excellent electrical properties of NCFETs have been proposed, particularly ultralow power applications, small short-channel effect (SCE) applications, and analog applications. In the future, the understanding of the NC mechanisms at the atomic level, better circuit design, and process compatibility should be focused upon, which can facilitate the practical application of NCFETs in the post-Moore era.

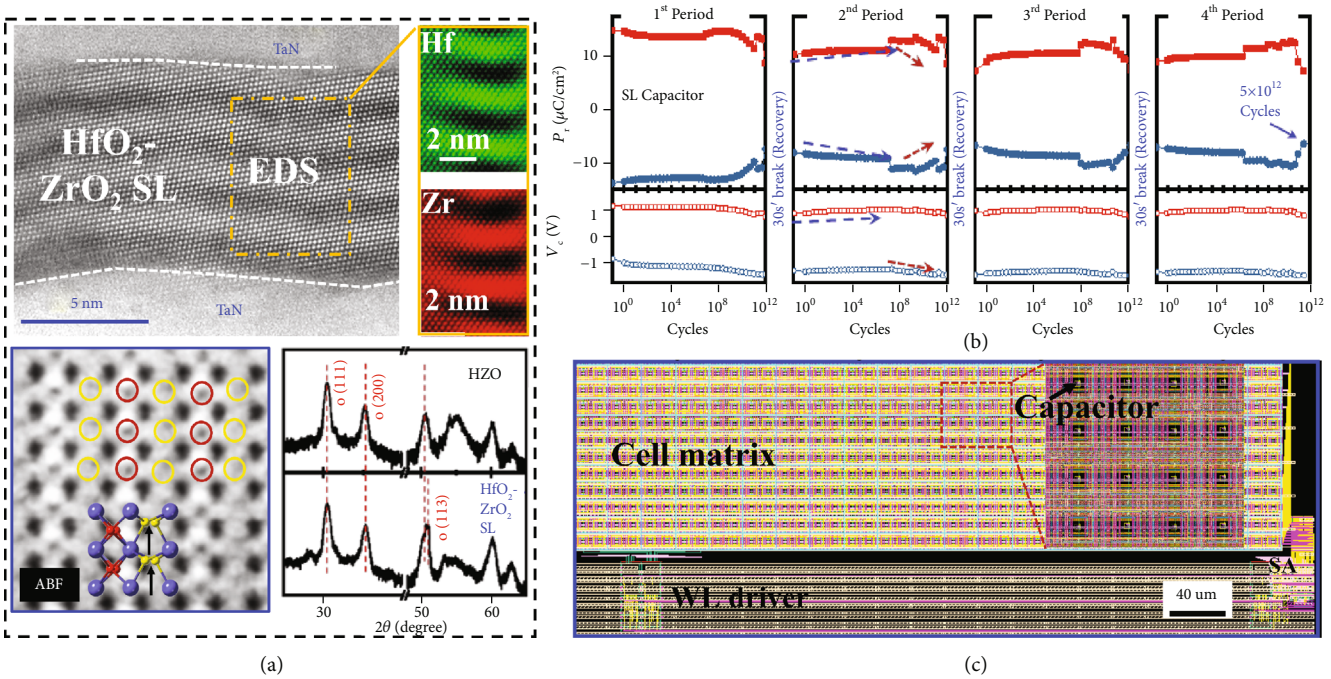

FIGURE 6: (a) HRTEM image, STEM ABF image, and GIXRD curves of MFM stacks with HfO_2-ZrO_2 SL [92]. (b) The endurance performance of SL MFM capacitors [92]. (c) Local layout view of the FeRAM test chip with different blocks, including the WL driver, SA, and cell matrix [118].

4. Ferroelectric-Based High-Performance Memories

The conventional dynamic RAM (DRAM) uses a capacitor to store data. Cell leakage current and wire parasitic capacitance in the ICs pose significant challenges for further scaling down the cell size. Nevertheless, the ferroelectric capacitor can store information through the P_r charge, which is nonvolatile, and possesses a much higher charge density per area. Therefore, replacing the dielectric material of a flash device with doped-HfO_2 ferroelectrics or amorphous oxide ferroelectrics to realize an FeFET is an alternative method to further reduce the power or delay of these memories, which will help bridge the gap between the performances of these devices and logic devices.

Gong et al. recently demonstrated doped-HfO_2 one transistor on capacitor (1T-1C) FeRAM for high-speed embedded nonvolatile memory (eNVM) and DRAM replacement applications [110]. This device exhibited a low operation voltage of 2.5 V and a high operation speed of 14 ns. Many relevant studies [111–114] reported that the engineering of material and device structure could improve the performance of the FeRAM. It was observed that the oxygen content or oxygen vacancy affected the o-phase content in the HZO film [111]. Therefore, P_r could be optimized through oxygen content engineering, such as by tuning the oxygen deposition time in the ALD film deposition process, changing the electrode materials, and depositing an additional interfacial layer/seed layer [115–117]. Although the feasibility of doped-HfO_2 FeRAM has been proven, some of its key parameters, such as endurance, cannot meet the requirement for practical applications.

To address this issue, Peng et al. [92] reported an HfO_2-ZrO_2 superlattice (SL) FE film as the gate dielectric for FeFETs. A compressive strain was introduced into the HfO_2 layer owing to the lattice mismatch between HfO_2 and ZrO_2, which was conducive to form the nonpolar phase of the ferroelectric (FE) film. The deviation of the alternate oxygen rows from the centers of the four nearest Hf/Zr atoms induced a dipole moment and resulted in a ferroelectric behavior. The SL MIM capacitors exhibited significantly improved endurance performance and fatigue recovery capability compared to the HZO MIM capacitors, as shown in Figures 6(a) and 6(b). Xiao et al. [118] designed and realized a 16-kbit 1T-1C FeRAM array with BEOL-integrated HZO-based ferroelectric capacitors. The ferroelectric characteristics of the test key (1C) and single cell (1T-1C) were discussed. Endurance up to 10^9 cycles at the array level was achieved for the first time. Figure 6(c) showed the local layout view of the 1T-1C FeRAM test chip with different blocks in terms of the WL driver, sense amplifier, and cell matrix. Cell matrices with a size of 64×32, 128×32, and 256×32 were used to investigate the effect of bitline length on the memory window (MW).

Flash memories are also widely used for embedded and storage applications. An FeFET can be considered a floating gate device, in which the gate dielectric is replaced by ferroelectric oxides. This device exhibits the following characteristics: (1) enhanced CMOS process compatibility owing to lower operation voltage and simpler structure, (2) low power owing to the electric-field-driven polarization switching mechanism, (3) low write latency enabled by fast polarization switching, and (4) nondestructive read-out owing to the three-terminal device structure. Thus, an FeFET array-

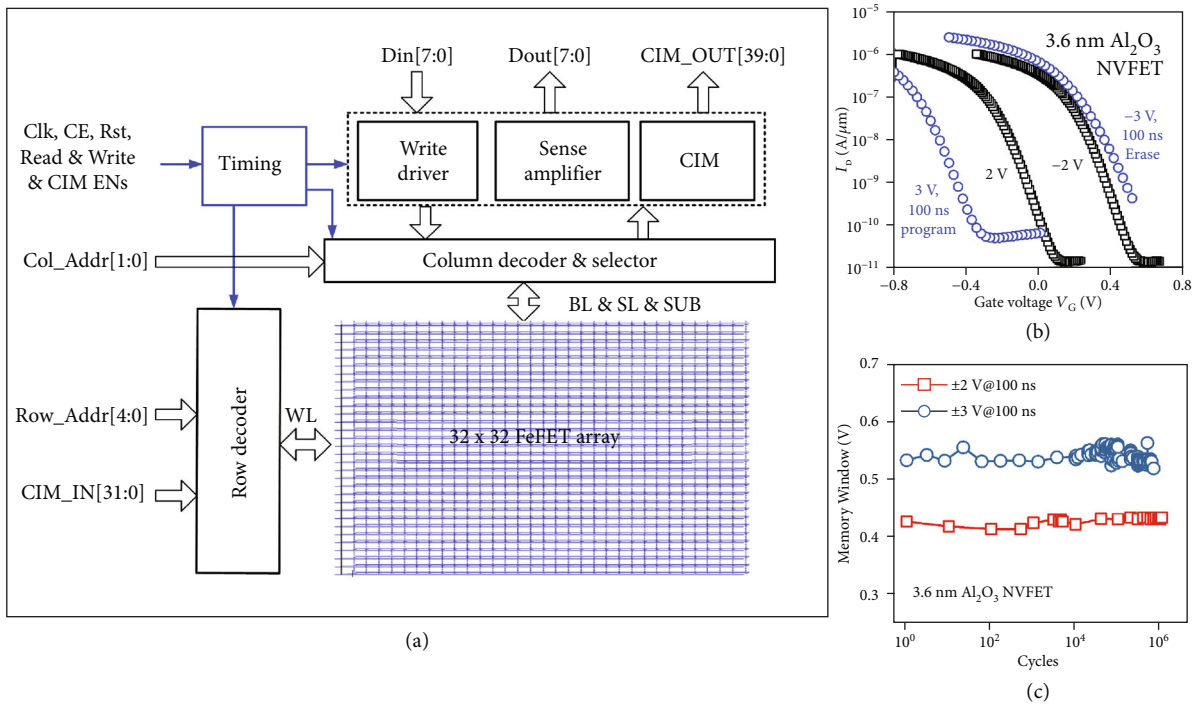

FIGURE 7: (a) Schematic of the circuits of the FeFET-based memory. (b) Read $I_D - V_G$ after the write operation [51]. (c) Endurance of amorphous Al_2O_3 FeFET [51].

based memory based on flash memory could be realized without redesigning the architecture and circuits. A typical FeFET memory array and its peripheral circuitry are shown in Figure 7(a). The architecture includes a coder/decoder, I/Os, sensitive amplifiers, write buffers, controllers, and a data bus; this architecture is similar to that of a NOR flash. At the circuit level, the only difference is that the write operation for an FeFET can be realized using an electric field; however, for the flash device, this operation is realized by hot carrier injection. Recently, GlobalFoundries has demonstrated FeFET-based memory with 28 nm bulk technology and 22 nm FDSOI CMOS technology [41, 119], indicating the possibility of FeFET-based circuit integration on advanced CMOS platforms.

Typically, the gate stack of FeFETs is in the form of MFIS structures. The threshold voltage (V_{th}) of FeFETs can be modulated by an external voltage pulse applied at the gate electrode using two stable polarization states and polarization switching of ferroelectric materials [120]. Thus, information can be stored as different V_{th} states in an FeFET. When a sufficiently large positive voltage pulse is applied, the polarization of the ferroelectric oxide is reversed (down state), and the FeFET switches to a low-V_{th} state. On the contrary, if a sufficiently large negative voltage is applied, the polarization reverses again (up state) and the FeFET switches to a high-V_{th} state. The voltage difference between the V_{th} of these two different states is defined as the MW. The MW of FeFETs with a sufficiently large P_r can be approximately evaluated by the following equation [120]:

$$\mathrm{MW} = 2\,a\,E_c\,t_{\mathrm{FE}}, \tag{1}$$

where α is a coefficient that represents the MW degradation caused by nonideal effects such as charge trapping, E_c is the electric field, and t_{FE} is the ferroelectric film thickness.

An amorphous ZrO_2-based ferroelectric FET has been demonstrated to improve the performance and compatibility of the FeFET [49, 121]. For embedded NVM applications, a 0.78 V MW can be achieved using a program voltage of 2.7 V and an erase voltage of −2.8 V with a pulse width of 5 μs. For embedded DRAM applications, program and erase speeds of approximately 10 ns can be achieved using a program voltage of 7.4 V and an erase voltage of −8.6 V, with an MW larger than 0.2 V [49]. An amorphous Al_2O_3 nonvolatile FET can achieve a MW above 0.85 V under ±3 V at a pulse width of 100 ns under the program/erase (P/E) condition (Figure 7(b)) [51]. The P/E voltage can be further reduced to ±1.6 V, thus exhibiting the potential of the device for applications at a lower operation voltage compared to that of doped-HfO_2 FeFETs. Amorphous oxide-based FeFETs show good endurance characteristics but a severe degradation in the retention performance. Nonvolatile FETs with α-Al_2O_3 show a stable MW without any degradation over 10^6 P/E cycles at ±3 V and 100 ns (Figure 7(c)) [51]. The trapping/detrapping effect is also a key factor that influences the MW of these devices.

5. Ferroelectric Devices for Neuromorphic Computing

Since the inception of the computing system, data storage and processing have been separate functions owing to the large difference between the two in terms of the working speeds, operation modes, and fabrication technology. The

von Neumann architecture has addressed these compatibility problems, leading to developments in the field of computing. However, the performance and efficiency of data-centricity are restricted by circuit delay and power issues owing to the large time and power consumption required for the transport and exchange of data between the memory and processing modules, which is referred to as the von Neumann bottleneck. Thus, novel computing devices and architecture have attracted considerable interest to resolve this issue.

One of the possible solutions is neuromorphic computing. The information storage and processing in the brain are hybrid functions in nature. Imitation of the neuron system for information processing is referred to as neuromorphic computing. The most important components in such a system are artificial neurons and synapses. According to reported studies [94, 122–135], FeFETs can implement both artificial neurons and synapses. For applications in neurons, FeFETs functioning as pulsed neural networks have been commonly used in previous studies. Because FeFETs have hysteretic $I_d - V_g$ characteristics, they can possess both on and off states and can be used as a switch to charge or discharge a capacitor. In a study by Wang et al. [125], a unique device model was used in the form of a one-transistor-one-FeFET structure. This model could control the gate voltage of the FeFET to produce an arbitrary output of the neuron and an inhibitory input. Furthermore, Yan et al. conducted a study based on Ref. [125] to investigate the effect of voltage bias on the output voltage of a neuron [122]; they explained the mechanism associating the inhibitory input with the computational biological neuron model. In addition, Chen et al. fabricated a novel leaky-FeFET (L-FeFET) to mimic biological neurons [126]. Luo et al. [127] improved the L-FeFET model and experimentally demonstrated that the hardware cost could be considerably reduced using an architecture comprising one resistor and two transistors. They added an inhibitory port to realize spiking neural networks, providing a promising direction for the integration of neuromorphic computing systems in the future.

Moreover, FeFETs can simultaneously perform storage and processing functions; therefore, they can be used for artificial synapse applications involving spike neural networks (SNNs) [128] and convolutional neural network (CNNs) [51]. Many studies have investigated the writing methods of FeFETs as synapses in neural networks to achieve better performance. For a single FeFET device, Jerry et al. demonstrated three write pulse schemes: identical pulses, pulses with incremental voltages, and pulses with incremental pulse widths affecting the update of the switch polarization [129]. From the results [129], it was concluded that the use of write pulses with suitable incremental voltage could help achieve excellent linearity and superior accuracy in neural network simulation. Furthermore, Nguyen et al. implemented a writing method involving fixing the gate pulse while gradually increasing the drain pulse, and compared the differences to impose incremental gate pulses [130]. The effects of different ferroelectric structures [131] and working temperature [132] were also examined in the application of deep neural networks. The charge trapping and release dynamics of HZO-based FeFET were explored, and a gate-stack design for enlarging the MW was determined [133]. For FeFET-based memory arrays with NOR and NAND architectures, the write disturbance effect for unselected memory cells was extensively tested [134]. Charge trapping and polarization switching were found to be the two mechanisms that affect the write disturbance. In contrast, Choe et al. proposed a three-dimensional AND-type architecture for matrix-vector multiplication and demonstrated its performance on deep neural networks [135].

In addition to polycrystalline doped-HfO_2 FeFETs, metal/amorphous dielectric/semiconductor gate stacks exhibit the switchable ferroelectric-like P, which can be used to implement analog synapses and SNNs. Recently, an analog synapse device based on a nonvolatile field-effect transistor (NVFET) with the amorphous ZrO_2 dielectric has been fabricated and demonstrated. This ZrO_2-based device exhibited superior synaptic characteristics, including good symmetry and linearity for both potentiation and depression, with small cycle-to-cycle variations. The ratio of the maximum to minimum conductance (G_{max}/G_{min}) of the device was 130, and the middle states was over 30. The spike-timing-dependent plasticity (STDP) was reproduced in the device. Based on emulated STDP functions, an SNN-based architecture has been constructed, and it has been shown that the offline and online training recognition accuracies reach 94 and 87%, respectively [128]. Moreover, various synaptic behaviors including long-term potentiation (LTP), long-term depression (LTD), and STDP have been reproduced in ferroelectric-like FETs integrated with 3 and 6 nm thick Al_2O_3 dielectrics when different types of electrical stimuli were applied to the gate, as shown in Figure 8(a) [94]. The dynamic response of the LTP and LTD is illustrated in Figure 8(b) [94]. An SNN architecture based on the properties of analog synapses was also built. Online training was conducted based on the synaptic characteristics of the device, and a decent accuracy (>80%) was achieved for fixed amplitude potentiation/depression pulses (±3 V/100 ns, Figure 8(c)). All of these results indicate that the amorphous Al_2O_3 synaptic device has high application potential in neuromorphic computing [94].

Novel amorphous-dielectric-based ferroelectric-like devices can also be used for realizing CNNs owing to their advantages in terms of linearity and asymmetry, which help increase the accuracy of these devices. In Ref. [51], the NEI layer (3.6 nm thickness) comprised ferroelectric nanocrystals embedded in amorphous Al_2O_3. Thus, the operating voltages and depolarization effects were lower compared to those of the conventional doped-HfO_2 films, which can be used in a CNN architecture. With fixed-amplitude potentiation/depression pulses with a 100 ns pulse width, an NEI FeFET synapse achieved a weight update with small nonlinearity ($\alpha_p = 0.12$, $\alpha_d = -0.09$) and asymmetry factors. A CNN was designed and emulated for a Mixed National Institute of Standards and Technology (MNIST) dataset, and it achieved an online training accuracy of 92% [128]. Furthermore, FeFETs with the amorphous Al_2O_3 gate dielectric exhibit high endurance, decent memory window with low program/erase voltage, and analog synapse properties, achieving a high

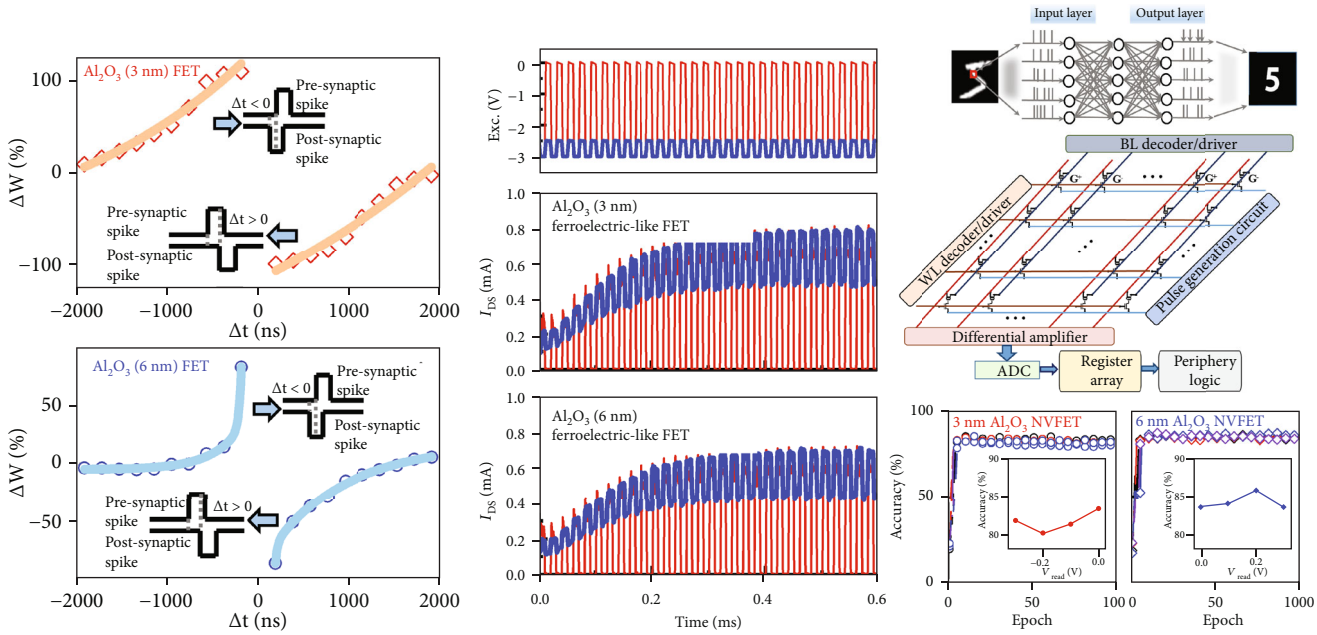

FIGURE 8: Analog synapse network based on ferroelectric devices. (a) Measured STDP curves of 3 and 6 nm thick amorphous Al_2O_3 synaptic transistors with a spike period of 190 ns. (b) Waveform of different excitatory input pulses. (c) The SNN architecture includes a three-layer fully connected structure and is based on the LIF model for recognizing handwritten digits. Circuit implementation simulation using SNN synapse arrays. Accuracy above 80% can be achieved using the SNN based on Al_2O_3 transistors under various values of V_{read} [94].

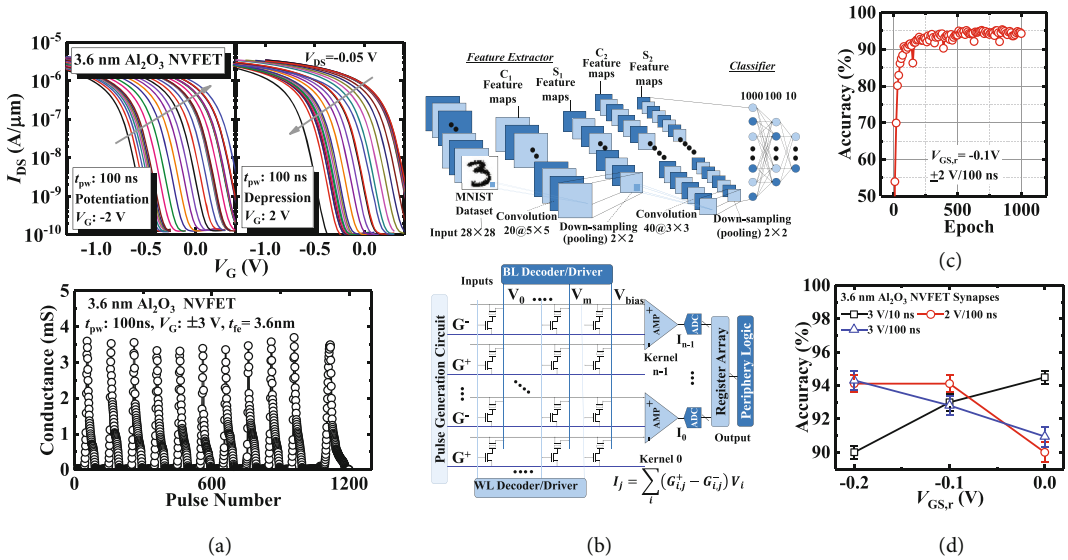

FIGURE 9: Convolutional neural network based on ferroelectric devices. (a) Analog synaptic behaviors of Al_2O_3 Ge FeFET and multiple cycles of consecutive alternating potentiation and depression. (b) Architecture of convolutional neural network, which consists of two convolution layers and one fully connected layer (MNIST dataset is used). (c) Learning accuracy evolution of convolutional neural network based on Al_2O_3 FeFET synapse. (d) Accuracy above 90% can be achieved in a convolutional neural network based on Al_2O_3 FeFET by varying the operation voltage and pulse width [51].

learning accuracy for the CNNs [51]. As shown in Figure 9(a), multiple cycles of consecutive alternating potentiation/depression pulses were applied to the FeFET, showing highly repeatable conductance profiles, which can be used in the CNN weight update. A CNN architecture utilizing a sign backpropagation (SBP) algorithm was designed based on the one-transistor-one-FeFET synapse cell to investigate the impact of the FeFET synapse performance on the online training, as shown in Figure 9(b). Online neural network training simulations parameterized by the FeFET synapses were conducted, and a high learning accuracy (>94%) was achieved for a fixed pulse amplitude of potentiation/

depression pulses (±2 V, 100 ns) with a read gate voltage of −0.1 V, as shown in Figure 9(c). Figure 9(d) shows the statistical plots of the learning accuracy of the neural network operated with different $V_{GS,r}$ and potentiation/depression conditions of the FeFET synapses. A high learning accuracy (>90%) was achieved owing to the improvement in the synaptic behavior.

In addition, ferroelectric tunnel junctions (FTJs) have attracted significant attention for synaptic device applications owing to their compact device structure, nondestructive readout scheme, and high write/read access speeds [136]. FTJ is a two-terminal resistive nonvolatile memory device consisting of a nanometer-thick ferroelectric film and conductive metal electrodes at both ends. The operation of the FTJ memory device relies on the modulation of the interface barrier height owing to the ferroelectric switching and quantum tunneling through an ultrathin barrier layer. The modulation of the tunneling current due to ferroelectric polarization reversal is called the tunneling electroresistance (TER) effect and is used to store/process information as an artificial synapse.

Thus far, three types of ferroelectric materials have been adopted in the current FTJ technology: ABO-type perovskites [137, 138], such as $BaTiO_3$ (BTO) and $PbZr_{0.2}Ti_{0.8}O_3$; 2D van der Waals materials [139, 140], such as $CuInP_2S_6$ (CIPS) and α-In2Se3; and binary oxides, such as HfO_2 and $Hf_{0.5}Zr_{0.5}O_2$ (HZO) [141, 142]. The first two types of FTJs can achieve a large TER ratio, but they are incompatible with the modern CMOS process. With the discovery of ferroelectricity in the polycrystalline $Hf_xZr_{1-x}O$, doped-HfO_2 FTJs have been extensively explored, and a TER ratio up to 100 can be achieved.

The development of FTJs is still in the preliminary stage. The suppression of the sneak current and distribution correlation of the high/low resistance in the array structure still requires further analysis. Fujii et al. [143] reported that doped-HfO_2-based self-compliant FTJs could achieve a low operating current of less than 100 nA, low operating voltage of 2 V, and switching ratio exceeding 10. Recently, Goh et al. [144] reported a self-rectifying FTJ with a TiN/HZO/TaN/W stack, a low operating current of less than 100 nA, high TER (~10^2), and 10^8 endurance cycles.

FTJs are also widely used in nonvolatile memories and neurosynaptic computing, particularly for artificial synaptic applications. FTJs have been demonstrated to be able to mimic various synaptic behaviors under different types of pulses, including STDP, LTP, and LTD. Ryu et al. [145] reported the continuously tunable conductivity of FTJs with a Ti/Au/Al_2O_3/HZO/Si structure and identified that the conductance increased with the number of potentiation pulses and decreased with the number of depression pulses; the results revealed that the synaptic weight was continuously tunable. In addition, the STDP function of biologic synapses in FTJs was demonstrated. Ryu et al. [145] reported the evaluation of synaptic properties, such as the LTD and LTP, of the HZO FTJs using three different pulse schemes. The conductance state gradually changed with the number of pulses, and more than 30 stable intermediate states were achieved. The pattern recognition rate based on the MNIST dataset was calculated using a neural network simulator with a multilayer perceptron, and an accuracy of approximately 90% was achieved. In addition, Xiao et al. [146] simulated FTJ devices and demonstrated that the best synapse characteristics could be obtained through the pulse amplitude modulation scheme; furthermore, they suggested that increasing the amplitudes between consecutive pulses would further improve the linearity, number of states, and conductance ratio.

6. Future Outlook

Over the past decade, remarkable progress of nanoscale ferroelectric devices based on emerging oxide materials has been achieved, from the conceptual stage to industrial demonstration. In this article, we attempted to categorize the state-of-the-art ferroelectric devices as low-power logic devices, high-performance memory cells, and neuromorphic devices for intelligent computing to meet the requirements of different applications. If the tradeoff between process compatibility and device performance can be achieved, NCFET, FeRAM, or FeFET memory and ferroelectric synapse devices can be integrated into the same chip to realize a multifunctional intelligent computing system. The architecture and computing algorithms for ferroelectric devices need to be further improved. Based on the progress achieved in the ferroelectric device-processing technology, the integration of low-power logic, high-performance memories, and neuromorphic systems on one chip seems to be feasible with continuous process improvement. This will help realize the development of high-performance and high-efficiency intelligent computing systems in the future.

Conflicts of Interest

The authors declare no conflicts of interest.

Acknowledgments

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