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Cite as: AIP Advances **4**, 107117 (2014); https://doi.org/10.1063/1.4898150
Submitted: 13 March 2014 • Accepted: 30 September 2014 • Published Online: 10 October 2014

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Ferroelectric gate tunnel field-effect transistors with low-power steep turn-on

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(Received 13 March 2014; accepted 30 September 2014; published online 10 October 2014)

Using a ferroelectric $PbZrTiO_3$ gate stack, the range of the steep subthreshold swing in tunnel field-effect transistors was extended by 3.5 orders of magnitude demonstrating an improvement in the swing (by approximately double the slope). The drain conductance (g_d) shows only 16% enhancement with large V_{DS} (~−1.5V) indicates internal voltage amplification with ferroelectric negative capacitance effect beneficial to small lateral drain-source bias voltages (−0.1 V). The concept of coupling the ferroelectric polarization is proposed. The power consumption is also discussed in low-power applications of steep subthreshold slope devices. [http://dx.doi.org/10.1063/1.4898150]

Tunnel field-effect transistors (TFETs) have attracted a great deal of attention for achieving a steep subthreshold swing with band-to-band tunneling (BTBT) operation in future sub-10-nm technology nodes. Because of its small bandgap energy relative to Si, Ge could enhance the tunneling probability of tunnel-based field-effect transistors with high current requirements.[1–3] Recently, epitaxially grown Ge (epi-Ge) p-TFETs on bulk (110) Si substrates[4] and planar p-TFETs on SOI (Si on insulator)[5] substrates have been reported. The hetero-tunnel field-effect transistor was proposed and modeled,[6] demonstrating steeper switching and higher currents than conventional TFETs.[7] However, one issue associated with the development of TFETs is the small range of the steep swing, caused by the saturation of the surface potential which bends with increasing gate voltage [Fig. 1(a)].

The steep swing range of a TFET is typically 1–3 orders of magnitude, which is less than that of a metal-oxide-semiconductor field-effect transistor (MOSFET) (4–6 orders of magnitude).[8] The subthreshold swing (*SS*) equation for a TFET is:

$$SS = \frac{\partial V_g}{\partial(\log_{10} I_d)} = \ln(10)\left[\frac{\partial V_d}{V_d \partial V_g} + \frac{E+b}{E^2}\frac{\partial E}{\partial V_g}\right]^{-1}, \quad (1)$$

where V_g and V_d are the gate and drain voltages, respectively, E is the electric field, and b is a constant. Equation (1) shows the dependence of *SS* on voltage and electric field. A higher applied voltage is beneficial for swing. However, the higher driving voltage required by the circuit is not feasible in device applications. A high electric field at the tunneling junction is expected to achieve a steep swing. The dopant segregation of a steep junction profile was reported to have a steep swing that had a range over ~4 orders of magnitude.[5]

In this work, device integration by ferroelectric (FE) polarization coupling is applied to TFETs. This was established experimentally in validating negative capacitance (NC). Incorporating NC into a gate stack is beneficial for energy band bending as it amplifies the internal voltage. It also assists in enhancing the BTBT probability, as shown in Fig. 1(a).

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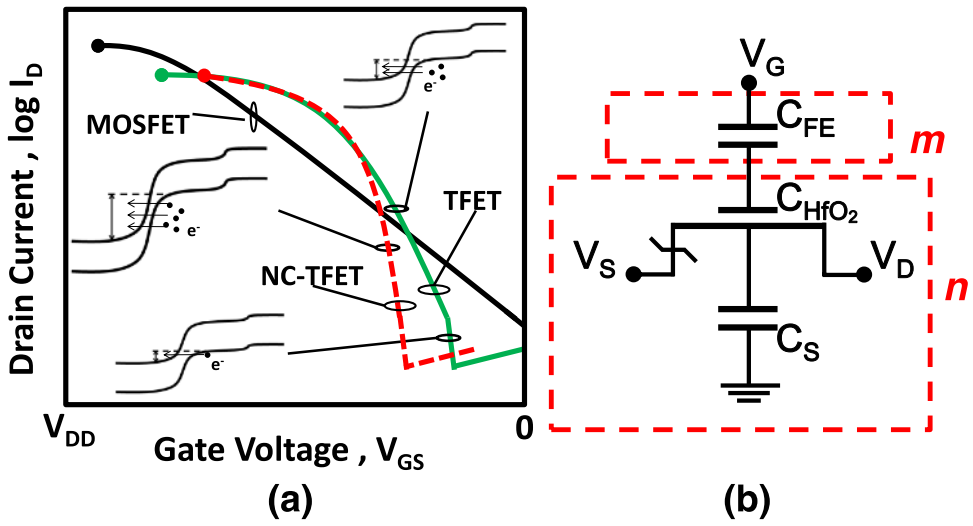

FIG. 1. (a) Schematic of the transfer characteristics of MOSFETs, TFETs, and NC-TFETs. The increased current in the TFET was slowed because of the bending saturation of the surface potential with the gate voltage sweep. Using an integrated ferroelectric material as a negative capacitance feature would extend the steep subthreshold swing range in a TFET. (b) The equivalent circuit of a NC-TFET, including the C_{FE}, C_{HfO2}, and C_s for the TFET. m and n can be found using Equation (2).

Standard 6-inch MOS (metal-oxide-semiconductor) base line and gate-last processes were employed in this study. Nominally pure Ge layers were directly grown on 150-mm p-type Si substrates at 525 °C by UHVCVD (ultra-high-vacuum chemical-vapor deposition) using GeH_4 as the precursor and H_2 as the carrier gas. A Si cap was grown on top of the epi-Ge to passivate and smooth the surface.[9–11] To fabricate the devices, p+ and n+ regions were defined and implanted into the epi-Ge with BF_2 (40 keV, 4×10^{15} cm^{-2}) and P (10 keV, 5×10^{15} cm^{-2}) for the drain and source electrodes, respectively. The dopants were activated by rapid thermal annealing (RTA) in ambient N_2 in two steps: 650 °C for 60 s in step 1 and 700 °C for the spike ramp in step 2. A 7.8-nm-thick HfO_2 gate dielectric was formed using atomic layer deposition and a 120-nm-thick TiN metal gate was deposited by sputtering. To improve the interface between HfO_2 and the semiconductor, the samples were annealed at 550 °C for 30 s before the metal gate was deposited. The TiN and HfO_2 layers were defined by dry etching to create the metal gate in the final process. After definition of the gate stack, a ~30-nm-thick SiO_x layer was deposited using plasma-enhanced chemical vapor deposition and spacer formation. A 10-nm-thick Ni layer was deposited using a sputtering system, followed by RTA in ambient N_2 at 250 °C for 30 s and 500 °C for 30 s to form a Ni silicide/germanide film. This was accompanied by a dopant-segregated process as a result of the specific implant conditions and the Ni thickness. Finally, the gate electrode was defined by lithographic patterning and Ag/$PbZrTiO_3$ (PZT) (10 nm/30 nm) was deposited using an electron-beam evaporator and a lift-off process. The characteristics of the TFET and NC-TFET devices (before and after FE (PZT) deposition, respectively) were the same device for easy comparison.

The general expression for *SS* for a FET is:

$$SS = \frac{\partial V_g}{\partial(\log_{10} I_d)} = \underbrace{\frac{\partial V_g}{\partial \psi_s}}_{m} \underbrace{\frac{\partial \psi_s}{\partial(\log_{10} I_d)}}_{n} = \left(1 + \frac{C_s}{C_{ins}}\right) \frac{\partial \psi_s}{\partial(\log_{10} I_d)}, \tag{2}$$

where ψ_s is the surface potential, and C_s and C_{ins} are the semiconductor and insulator capacitances, respectively. The FE polarization of NC-TFETs improved *SS* values in both the body factor (m) and the n-factor (i.e., according to the Boltzmann tyranny, $\ln(10)k_bT/q$ for a MOSFET at room temperature; here k_b, T and q are the Boltzmann constant, the absolute temperature and the electronic charge, respectively). The equivalent circuit for the TFET included C_{FE}, C_{HfO2} and C_s, which denote the capacitances of the ferroelectric material, HfO_2 and the semiconductor, respectively

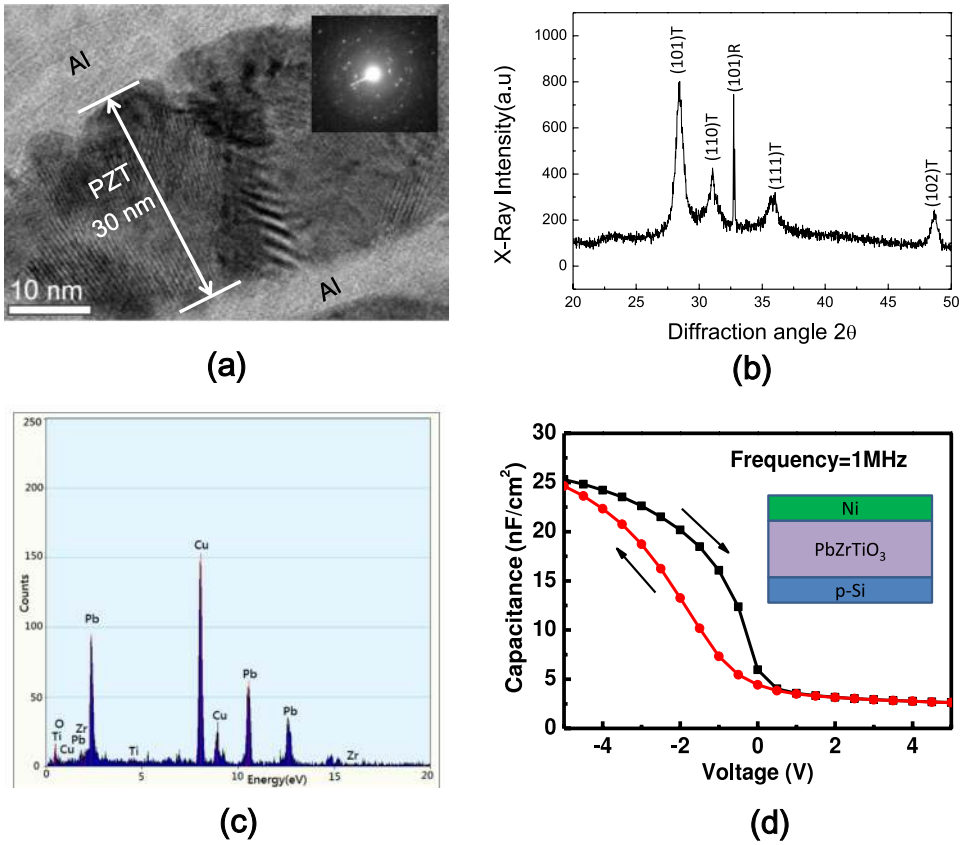

FIG. 2. (a) Cross-sectional TEM of a ~30-nm-thick PZT film on the metal. The inset shows the diffraction pattern of PZT, indicating that it is polycrystalline. (b) The XRD of PZT. The crystalline is identified as tetragonal and rhombohedral phase. (c) The EDX of PZT using an E-gun evaporator system; a low oxygen content was observed. (d) The capacitance-voltage (C-V) of MFS. It shows a clockwise hysteresis and indicates due to FE behavior not traps.

[Fig. 1(b)]. The NC approach is beneficial for body factors are less than unity, such as for polymer FE MOSFETs with $SS < 60$ mV/decade.[12,13] PZT was used and designed with simulations and experiments to obtain an enhancement in capacitance concomitant with NC in the crystalline ferroelectric–dielectric bilayer.[14–16] The possible lowering of the n-factor can be addressed by employing a new transport mechanism, such as TFETs with a BTBT mechanism.

To experimentally validate FE NC, a top gate metal and PZT layers were deposited on the metal and Si as MFM (metal/FE/metal) and MFS (metal/FE/semiconductor) structure [Fig. 2(a) and (d)]. PZT was deposited on all samples at the same time, including metal, Si and the TFET. Figure 2(a) displays a cross-sectional TEM (transmission electron micrograph) of the PZT after it was annealed at 400 °C, showing the resulting ~30-nm-thick polycrystalline layer with a 10- to 30-nm grain size. This was confirmed by the TEM diffraction pattern, shown in the inset in Fig. 2(a). Besides, the crystalline of PZT is identified as tetragonal and rhombohedral phase by XRD (X-ray Diffraction) (Fig. 2(b)). The low oxygen content of PZT, caused by E-gun evaporation growth, was observed by EDX (energy-dispersive X-ray spectroscopy) (Fig. 2(c)) and is beneficial for polarization in ferroelectric applications.[17] The Cu signal originates from the Cu ring holding the TEM samples. The hysteresis FE was validated on MFS with capacitance-voltage measurement. It shows a clockwise hysteresis in Fig. 2(d), i.e., negative shift in capacitance with reverse sweep (+5V to −5V). The MFS with reverse sweep attracts positive charges (holes) have to overcome coercive field of PZT, therefore, the more negative applied bias is necessary. Note that the positive shift in capacitance is attributed to electrons trapping and de-trapping process with localized states of dielectric, like flash memory operation concept. However, the capacitance with reverse sweep in Fig. 2(d) is stretched out since the electrons are released from the interface trap state, which is occupied by electrons with

sweep from +5V. This results the recombination with generated holes and capacitance increases gently as compare with that of forward sweep. The polarization was experimentally extracted from hysteretic internal voltage (V_{int}) versus V_g and obtained the amplification of the $V_g(dV_{int}/dV_g)$ and the ratio was greater than 1.[16] The voltage was amplified during the positive-to-negative sweeps and was applicable to the p-type operations of both the MOSFETs and TFETs.

Coupling the FE gate stack with the TFET displayed the features of gate voltage amplification along with surface potential amplification. The transfer characteristics of the NC-TFET significantly improve the *SS* value (Fig. 3), by about 3.5 orders of magnitude, which then enhanced the output current characteristics. The TFET and the NC-TFET was the same device before and after PZT deposition, respectively. They were the same TFET for comparison and to avoid TFET uniformity issues. The V_{int} was amplified by the non-linear behavior of the FE NC, leading to a surface potential (ψ_s) with the V_g sweep and a reduction in the m ($\partial V_g/\partial \psi_s$) below 1 [see inset in Fig. 3]. This indicated that the surface potential of the NC-TFET was amplified by the V_g sweep, in comparison with that of the TFET. However, with a large V_g, the amplification vanished and both surface potentials were similar.

Figure 4(a) shows that the drain conductance (g_d) only had a 16% increase with a large V_{DS} (~−2.5 V) [Fig. 4], when compared with the peak g_m (V_{DS} = −0.1 V).[16] This indicates internal voltage amplification with FE NC effect beneficial to small lateral drain-source bias voltages (−0.1 V). The FE NC showed an improvement in the subthreshold range, while the BTBT boost was slightly enhanced by the saturation current.

The power consumption is an important issue for the application of NC technologies. The dynamic power consumption is proportional to CV^2f, where C is the capacitance, V is the power supply voltage, and f is the frequency. The insets in Fig. 5 show the gate capacitances of a

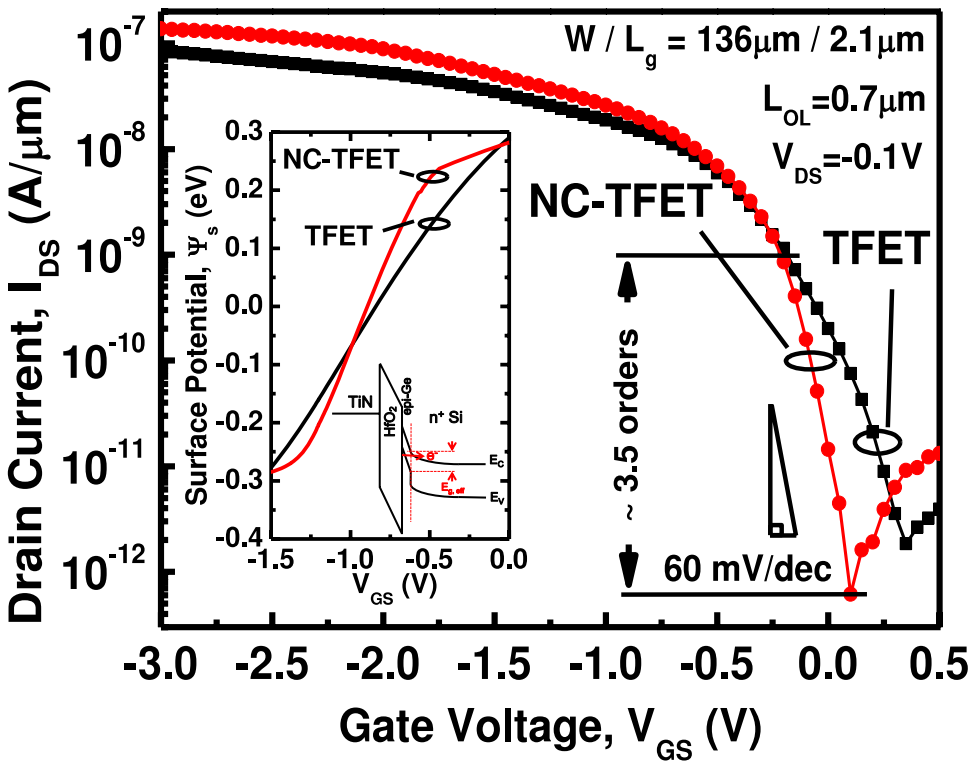

FIG. 3. Transfer characteristics (I_d-V_g) of the NC-TFET. The subthreshold swing was improved significantly with a FE NC. The current of the NC-TFET was enhanced with a large V_{GS}. Note that the TFET and NC-TFET used were the same TFET, before and after deposition of the PZT, respectively, for comparison and to avoid TFET uniformity issues. The inset shows the calculated surface potentials of the TFET and NC-TFET. The surface potential of the NC-TFET was amplified during the V_g sweep and enhanced the BTBT. The inset shows the BTBT mechanism in the TFET.

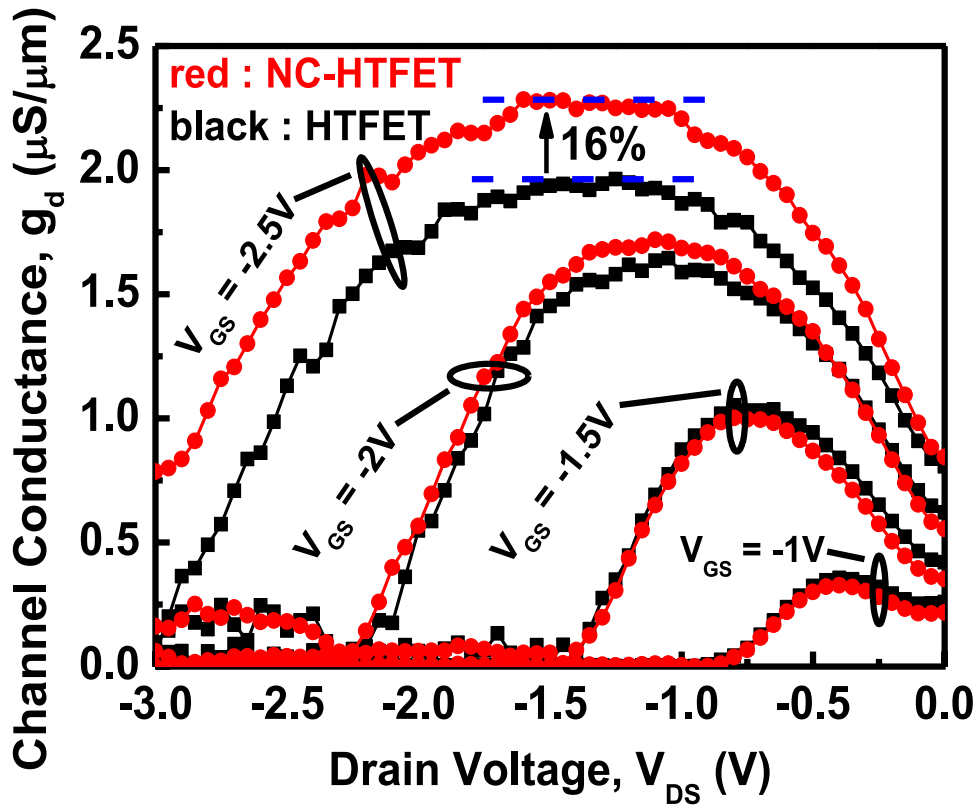

FIG. 4. Drain conductance (g_d) vs V_{DS}. The peak g_d increased by 16% with the integration of NC. The FE NC showed an improvement in the subthreshold range, while the BTBT boost was slightly enhanced by the saturation current.

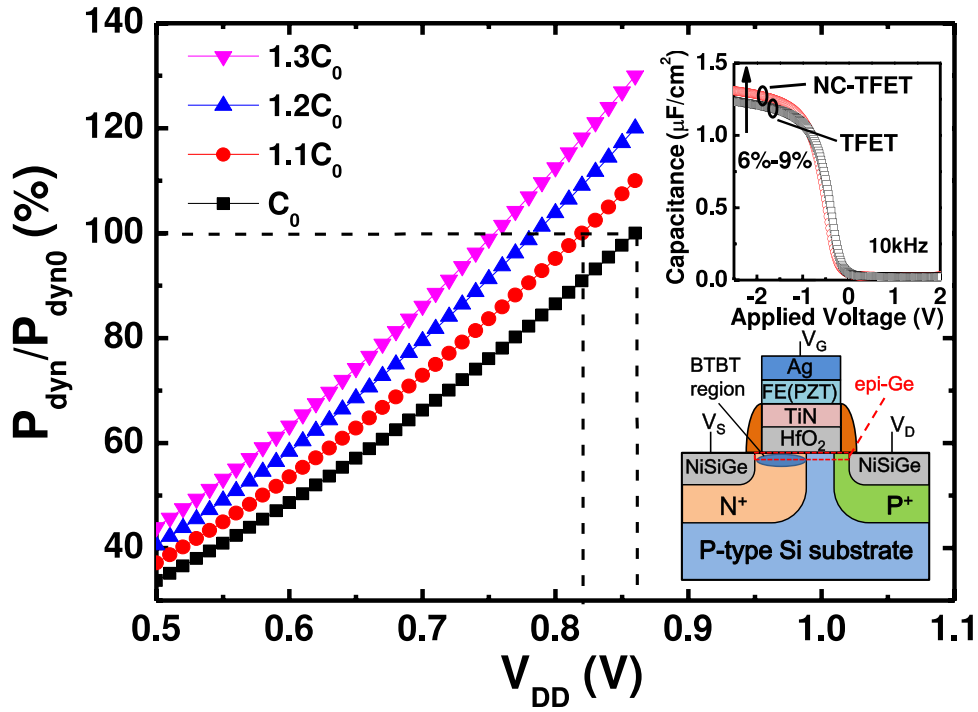

FIG. 5. The estimated dynamic power consumption with power supply voltage (V_{dd}) and capacitance (C). The insets show the gate capacitances of the NC-TFET with an enhancement of 6–9%, compared with that of a TFET. The bottom right is a schematic of the NC-TFET.

NC-TFET, which were enhanced by 6–9% compared with a TFET. Figure 5 also shows a schematic of the NC-TFET. The enhanced capacitance was attributed to NC effects, according to the series capacitance in the effective circuits. However, the purpose of a steep subthreshold slope FET, such as a TFET or the NC concept, is to lower the power supply voltage (V_{dd}). The V_{dd} is expected to go below 0.5 V in future generations. Note that V_{dd} = 0.86 V for 16/14 nm in the current technology node. Therefore, increasing the capacitance and decreasing the square of the voltage may lead to a lower consumption of the dynamic power for ferroelectric negative capacitance devices under fixed frequencies. The estimated dynamic power consumption is shown in Fig. 5. If capacitance is increased by 10% for an integrating FE NC, into the current technology node, the V_{dd} would decrease from 0.86 V to 0.83 V, while maintaining the same power consumption. Establishing a compact model for NC is beneficial in estimating the exact power consumption.

In conclusion, a significant improvement in the subthreshold swing (by approximately twice the slope) and an extended range of the steep swing by ~3.5 orders of magnitude were demonstrated with a FE NC gate stack integrated with a TFET. The internal voltage amplification with FE NC effect beneficial to the subthreshold range, while the BTBT boost was slightly enhanced by the saturation current. The validity of the FE NC characteristics was established experimentally, and the power consumption is also discussed in low-power applications of steep subthreshold slope devices. The performance of a steep subthreshold slope device with an integrated FE could be improved in future applications by optimizing the device structure and processing conditions.

ACKNOWLEDGMENTS

The authors gratefully acknowledge financial support from the National Science Council Taiwan under Grant Nos. 103-2221-E-003-023, 102-2221-E-003-030-MY3 and 102-2622-E-002-014. The processes were supported by National Nano Device Laboratories (NDL) and the UHV-CVD was supported by Prof. C. W. Liu, National Taiwan University (NTU), Taiwan.

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