Ferroelectric HfO$_2$ Tunnel Junction Memory With High TER and Multi-Level Operation Featuring Metal Replacement Process

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ABSTRACT We have investigated device design of HfO$_2$-based ferroelectric tunnel junction (FTJ) memory. Asymmetry of dielectric screening property in top and bottom electrodes is the key for high tunneling electroresistance (TER) ratio. Thus, metal and semiconductor electrodes are proposed. There exists a design space of ferroelectric material parameters to achieve high TER ratio under the constraint of depolarizing field. We have developed an FTJ fabrication process to realize the design. Large polarization charge and symmetric switching voltage are obtained by top metal replacement process. High TER ratio >30 and multi-level cell operation have been successfully demonstrated. Retention characteristics is promising, however, endurance characteristics should be improved for reliable operation.

INDEX TERMS Ferroelectric tunnel junction (FTJ), ferroelectric HfO$_2$, tunneling electroresistance.

I. INTRODUCTION

In highly information-oriented society, cyber physical system is an important platform where IoT edge devices sense and communicate data, and cloud servers collect and analyze big data. Under the constraint of power consumption, transistors and memories have to be energy-efficient. Non-volatile memory (NVM) will play a key role to enable energy-efficient computing. IoT edge devices need a low-cost and low-power non-volatile memory (NVM), and servers need a storage class memory to fill the gap in the memory hierarchy. Moreover, new artificial intelligence (AI) algorithms and applications need massive parallel computing. In-memory computing with NVM can overcome the von-Neumann bottleneck.

Among various NVMs, ferroelectric (FE) memory have revived thanks to the recent discovery of FE-HfO$_2$ [1]. FE-HfO$_2$ is expected to overcome several issues in conventional FE materials such as scalability, stability, reliability and environmental safety. If all these issues are solved by FE-HfO$_2$, FE memory can be a promising candidate of low power NVM due to its field driven operation principle.

Ferroelectric tunnel junction (FTJ) memory is an emerging memory. It is a two terminal resistive change memory, which can be a competitor for high-density cross-bar memory. FTJ typically consists of a thin FE layer and top and bottom electrodes as shown in Fig. 1. Tunneling current flows through the FE layer. By applying voltage and flipping polarization, tunneling barrier height can be modulated and resistance of the FTJ is changed. FTJ memory was originally proposed as "polar switch" by Esaki *et al.* back in 1971 [2]. Since then, there are reports on experiments and theories for FTJ using conventional FE materials [3]–[11]. Although there are several experimental reports on FTJ with FE-HfO$_2$ [12]–[19], however, design guideline and process issues [13] are not fully addressed yet.

In this work, first, we address the issues of FTJ design. Next we show a design guideline. Then we develop a fabrication process with FE-HfO$_2$. Finally, we realize high on/off resistance ratio and multi-level cell operation. Reliability issues are discussed.
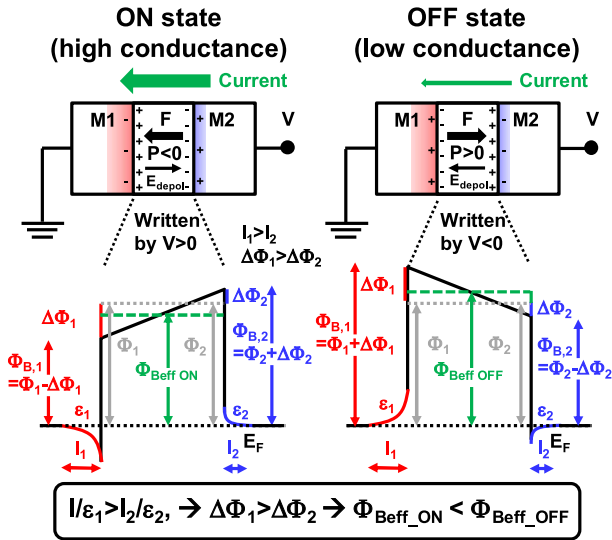
FIGURE 1. Schematic illustration of the operation principle of FTJ. Tunneling barrier height and thus TER can be modulated by applying voltage and switching polarization in the FE layer.

FIGURE 2. Simulation framework for FTJ based on direct tunneling model and dielectric screening length. This model can capture device characteristics in low read voltage region.

FIGURE 3. Simulated *I-V* curves of FTJ with different top and bottom electrodes based on the framework of direct tunneling and dielectric screening length.

on these results, asymmetric dielectric screening property is important to obtain high TER ratio. In this work, we propose to use a metal and a semiconductor for top and bottom electrodes, respectively.

With the asymmetric dielectric screening property of metal-ferroelectric-semiconductor (MFS) structure FTJ, we explore design space of material parameters such as remanent polarization (P_r) and ferroelectric thickness (t_F). Fig. 4 shows the contour plot of the simulated TER ratio as a function of P_r and t_F. In general, as P_r and t_F increase, TER ratio increases. However, there is a constraint; depolarizing field (E_{depol}) should not exceed coercive field (E_c) [12]. Otherwise FTJ does not have data retention. E_{depol} was also calculated and indicated by dotted lines in Fig. 4. Typical E_c of FE-HfO$_2$ is about 1 MV/cm, which is the boundary. Design space should be explored below this boundary in Fig. 4. P_r is 3~5 μC/cm^2 and t_F is 3~5 nm.

III. PROCESS DEVELOPMENT FOR FTJ

To realize the device design in Section II, we develop FE-HfO$_2$ FTJ processes. Fig. 5 shows the process flow. Starting from N$^+$-Si substrate which is doped by 1×10^{19}cm^{-3}, the substrate was cleaned by RCA wet clean. HfO$_2$ film was deposited by atomic layer deposition (ALD) system at 250°C with 50% Zr doping (HZO). Then there are four different types of process from A to D for top metal and anneal process. In process A, TiN is deposited and then post metallization anneal (PMA) is performed. In process B, post deposition anneal (PDA) is performed and then TiN is deposited. In process C, PDA is performed and then Al is deposited. In process D, TiN is deposited and PMA is performed. Then TiN is stripped and Al is deposited instead. TiN is deposited by radio-frequency (RF) reactive sputtering in N$_2$ ambient and the thickness is 50 nm. PDA and PMA are performed in RTA system at 500 °C for 10 sec.

II. FTJ DEVICE DESIGN

First, we study the impact of top and bottom electrodes by using a simple model. The FTJ model is based on direct tunneling current model with finite screening length and barrier height modulation [6] as shown in Fig. 2. The model is valid in that read voltage of FTJ is supposed to be low, where direct tunneling should be dominant. Note that the TER ratio is defined as (I_{on}-I_{off})/I_{off}. Fig. 3 shows *I-V* curves with different top and bottom electrodes. With identical metals such as TiN for top and bottom electrodes, TER ratio is almost zero. If top and bottom electrodes have different band offsets, TER ratio is still very small. Then, if top and bottom electrodes have different dielectric screening properties, TER ratio becomes large. More specifically, effective dielectric screening length (debye length / dielectric constant) should be different between top and bottom electrodes. Based
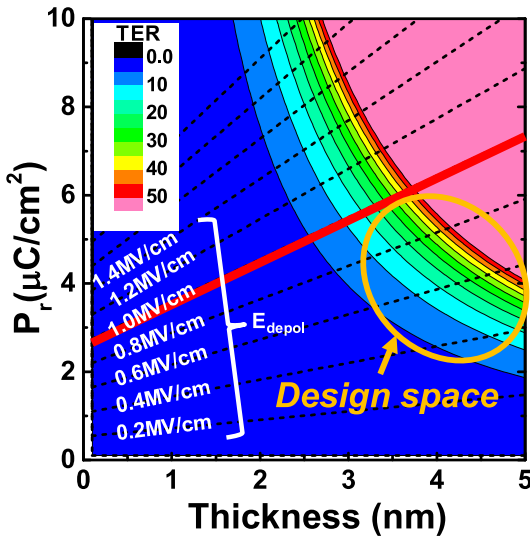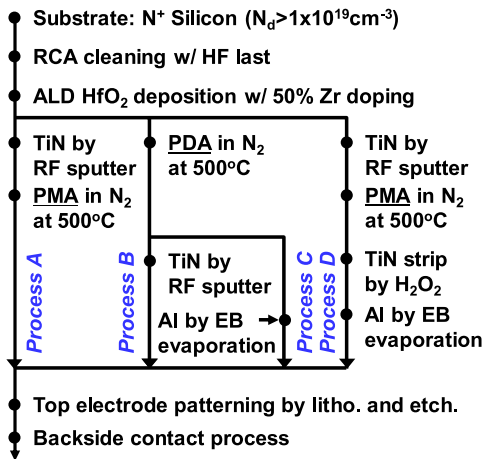
FIGURE 4. Contour plot of the simulated TER ratio of FE-HfO$_2$ FTJ as a function of P_r and t_F. E_{depol} is indicated by dotted lines. Red line shows the typical E_c = 1 MV/cm of FE-HfO$_2$.


FIGURE 5. Fabrication process flow of FE-HfO$_2$ FTJs. There are four different types of process from A to D for top metal and anneal process.

TiN is stripped by H$_2$O$_2$. Al is deposited by EB evaporation and the thickness is 100 nm. the samples are finished with patterning top electrode and back side contact process. X-ray photoelectron spectroscopy (XPS) is used for characterizing the surface of the HZO film. X-ray diffraction (XRD) and transmission electron microscope (TEM) are used for characterizing crystalline property of the HZO film. FTJs are tested by electrical measurement.

We fabricated and characterized ferroelectric property of 10 nm-thick FE-HfO$_2$ for process A to process D. Fig. 6 shows low frequency *I-V* measurement results with electrical cycling.

Process A is a default process. The polarization charge is large but the switching voltages are very asymmetric. This means that large voltage is needed for switching in the positive voltage side and voltage margin is very small in the
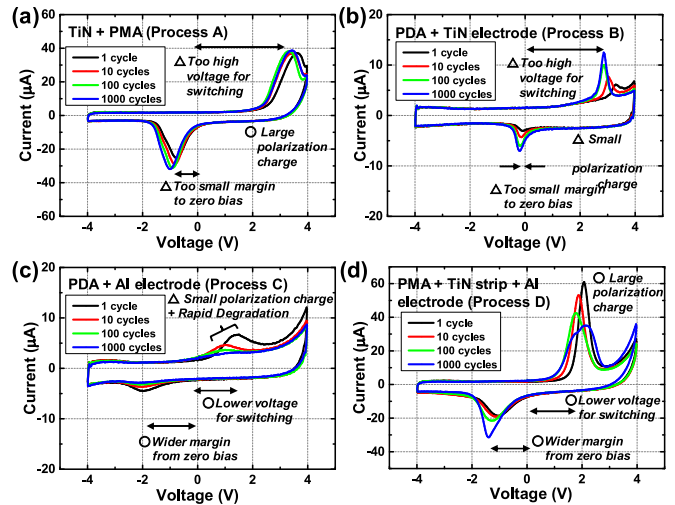

FIGURE 6. Measured low frequency *I-V* curves for (a) process A, (b) process B, (c) process C, and (d) process D, with electrical cycling.

negative voltage side. This can be attributed to the internal field caused by the workfunction difference between top and bottom electrodes. Top TiN electrode should be replaced by another metal such as Al. Since Al cannot endure PMA process, PDA was evaluated. In process B, the polarization charge becomes small because of less FE-phase formation than in process A. The switching voltages are still asymmetric. In process C with Al electrode, the switching voltages become symmetric thanks to the workfunction adjustment. However, the polarization charge is still small for PDA similarly to process B. Furthermore, after electrical cycling, ferroelectricity is severely degraded possibly because of the interaction between the Al electrode and the HZO film. In process D, the switching voltages become symmetric while large polarization charge is maintained. There are three reasons why process D works. First, with TiN capping on top, HZO film can be crystallized as FE-phase more effectively by PMA than by PDA without TiN capping. Second, during PMA, the surface of HZO film is nitrided so that the interaction between Al and HZO is suppressed. Third, workfunction of the top metal is properly adjusted by Al top electrode. The surface nitridation was confirmed by XPS spectra of samples with PMA + TiN strip, and PDA as shown in Fig. 7 (a). N1s spectrum signal and the chemical shift by nitrogen bonding in Hf4f spectra are clearly seen. FE-phase formation is confirmed by comparing XRD spectra of the samples with PMA, PDA and PMA + TiN strip. FE orthorhombic phase is maintained even after stripping TiN without monoclinic phase.

IV. FTJ CHARACTERIZATION RESULTS AND DISCUSSIONS

Based on the process D developed in Section III, we thinned the thickness of HZO down to 4 nm and fabricated FTJ. Fig. 8 shows the cross sectional TEM images of the fabricated FTJ. HZO is uniformly deposited and fully crystallized.
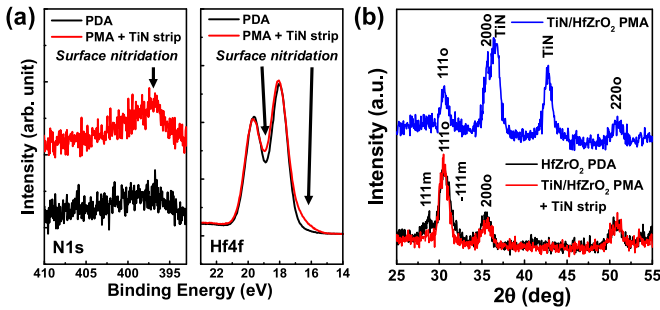
FIGURE 7. (a) Measured XPS spectra of N1s and Hf4f for the samples with PMA + TiN strip and PDA. (b) Measured XRD spectra for the samples with PMA, PDA and PMA + TiN strip.
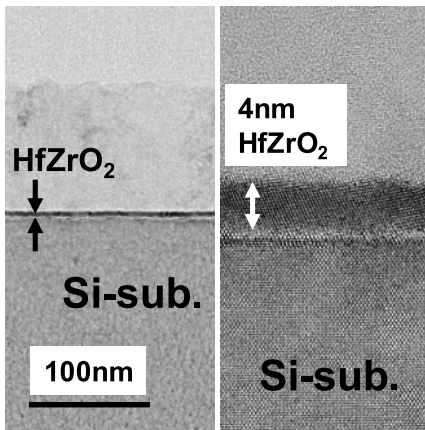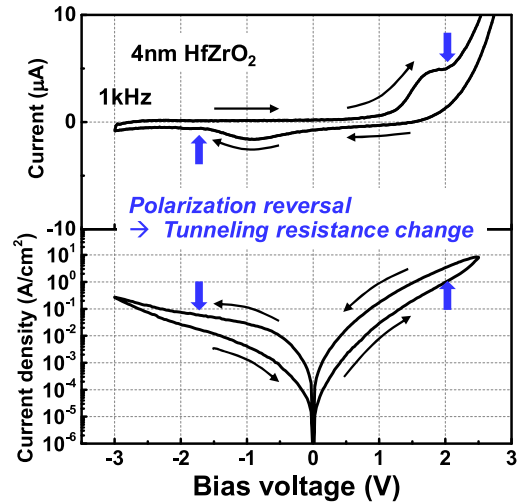

FIGURE 8. Cross sectional TEM images of the fabricated FTJ with 4 nm-thick HZO film. Top electrode is Al. HZO is uniformly deposited and fully crystallized.
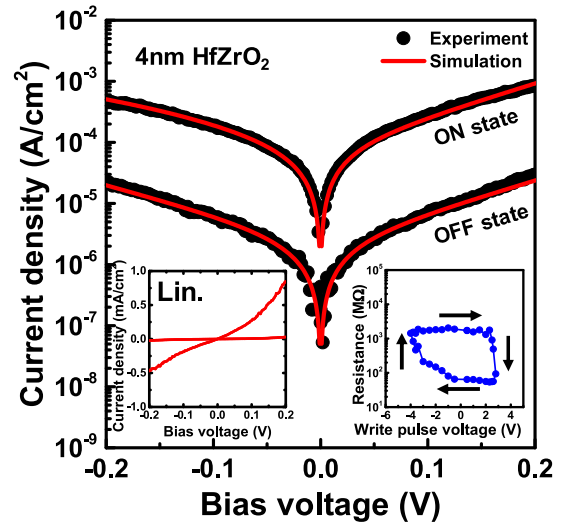

FIGURE 9. Measured (top) low frequency *I-V* curve at 1 kHz and (bottom) DC *I-V* curve of the fabricated FTJ. Polarization charge is estimated to be 5 μC/cm² at 4 nm thickness.

FIGURE 10. Measured read *I-V* current with +2.8 V/−4.0 V write/erase pulse voltage. The left inset shows the same *I-V* curve with the linear scale. The right inset shows the resistance versus write pulse voltage.

Then we measured low frequency and direct-current (DC) *I-V* curves of the FTJ as shown in Fig. 9. Hysteresis is seen in the DC *I-V* curve which corresponds to the polarization switching in the low frequency *I-V* curve at 1 kHz. Polarization charge is estimated to be 5 μC/cm² at 4 nm thickness from transient measurement, which is within the design space as described in Section II.

Then we measured read *I-V* current with write pulse voltage. Read voltage is limited to 0.2 V to avoid disturbance by read operation. As shown in Fig. 10, with +2.8 V/−4.0 V write/erase voltage, TER ratio as high as 30 is achieved. The simulation result fits very well to the measured *I-V* curve in the direct tunneling regime at low read voltage. The key fitting parameters are as follows. For FE-layer, $P = 5$ μC/cm², $d = 4$ nm, $\varepsilon_{stat} = 30$. For bottom semiconductor electrode, $l_1 = 0.9$ nm, $\varepsilon_1 = 12$, $\Delta\Phi_1 = 0.23$ eV. For top metal electrode, $l_2 = 0.05$ nm, $\varepsilon_2 = 2.0$, $\Delta\Phi_2 = 0.076$ eV.

Write pulse dependence on resistance of the FTJ is shown in the inset of Fig. 10. The curve is obtained by changing write pulse voltage gradually. In the positive write pulse region, the resistance changes abruptly from the high resistance state (HRS) to the low resistance state (LRS). This is because accumulation charge is formed in the
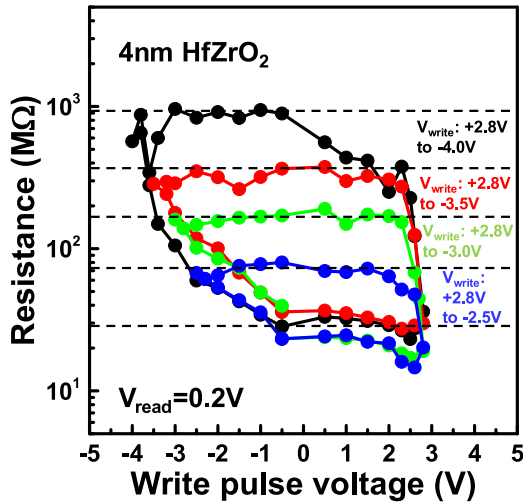
bottom N⁺-Si electrode and large voltage is induced on the FE layer. On the other hand, in the negative write pulse region, the resistance changes gradually from LRS to HRS. This is because depletion layer is formed in the bottom N⁺-Si electrode and large voltage drops on the depletion layer.

Since the depletion layer works like a voltage buffer in the negative write pulse voltage, the resistance in HRS can be changed by adjusting the maximum write pulse voltage with moderate write noise margin. Fig. 11 shows the resistance versus write pulse voltage with different maximum write pulse voltages. Multi-level cell operation is achieved by first setting to the lowest resistance state in positive write pulse voltage and then applying negative write pulse voltage for target resistance level. Each level has a flat level of the

FIGURE 11. Measured resistance of the FTJ versus write pulse voltage as a function of maximum write pulse voltages.
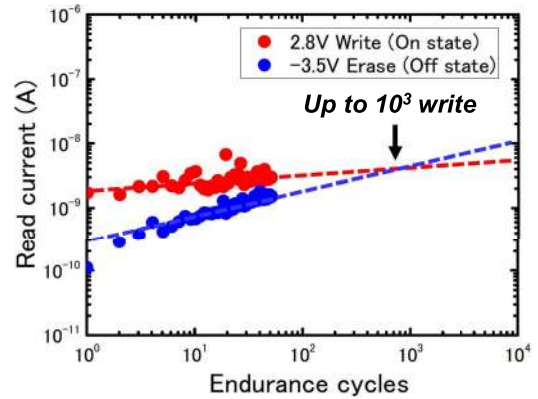

FIGURE 12. Measured retention characteristics of FTJ with 2.8 V/ −3.5 V write/erase pulse voltages.

FIGURE 13. Measured endurance characteristics of FTJ with 2.8 V/ −3.5 V write/erase pulse voltages.

V. SUMMARY

We investigated the device design for FE-HfO₂ FTJ. Asymmetric dielectric screening property in top and bottom electrodes is important. MFS structure FTJ was proposed. Design space in material parameters was explored for high TER ratio under the constraint of E_{depol}. We developed the metal replacement process to realize the design. With 4 nm-HZO film, TER as high as 30 was achieved with multi-level cell operation, which are promising results for storage memory and emerging AI applications. While retention characteristics of the FTJ is satisfying, however, endurance characteristics is only up to 10^3 cycles and needs to be significantly improved.

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resistance versus write pulse voltage, which means that each level is immune to disturb voltage.

Lastly, we examined reliability of the FTJ in terms of retention and endurance characteristics. Fig. 12 shows the retention characteristic of the FTJ, where 10-year retention is expected. Note that LRS is degraded toward HRS and the amount of degradation in LRS is larger than HRS. This could be due to the internal field at retention state. As shown in Fig. 6(d), there is slight asymmetry of switching voltages even with process D. Therefore, the negative internal field is applied to both LRS and HRS at retention state, and thus LRS is gradually erased and drifted to HRS.

Fig. 13 shows the endurance characteristics of the FTJ, where only up to 10^3 cycles are expected but breakdown occurs before the expected cycle times. Endurance degradation can be attributed to the stress induced leakage current by formation of defects and percolation paths during electrical cycling [20]. Further investigation on the degradation mechanism and improvement of endurance characteristics are important and our future work.

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