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We report on the fabrication and electrical characterization of field-effect transistors at the surface of tetracene single crystals. We find that the mobility of these transistors reaches the room-temperature value of 0.4 $cm^2/V\,s$. The nonmonotonous temperature dependence of the mobility, its weak gate voltage dependence, as well as the sharpness of the subthreshold slope, confirm the high quality of single-crystal devices. This is due to the fabrication process that does not substantially affect the crystal quality. © *2003 American Institute of Physics.*
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Common strategies for the fabrication of organic field-effect transistors (FETs) are based on thin-film technology.[1,2] This choice is motivated by the existing deposition techniques for organic thin films that facilitate device fabrication. At the same time, thin films usually contain a considerable amount of structural imperfections, which affect negatively the transistor performance.[3]

For small organic molecules, crystalline films can be used to reduce the amount of structural defects. It has been found, however, that also the performance of transistors based on these films are affected by structural imperfections, even when only one crystalline grain is present between the source and drain.[4] This is due to disorder present in the first few molecular layers, in contact with the substrate, which constitute the device active region.[5] For this reason, improving the quality of organic thin-film transistors (TFTs) requires highly ordered molecular films, in which the order extends up to the interface with the substrate.

An alternative route to the production of high-quality organic FETs is to fabricate devices on the surface of a free-standing single crystal of organic molecules. If a fabrication process that preserves the quality of the crystals[6,7] can be developed, the resulting single-crystal FETs should perform better than their TFT counterpart. Whereas considerable amount of work is currently aiming at improving the quality of organic TFTs,[2,4,5,8,9] the investigation of single-crystal organic FETs has received only limited attention.[10–14]

In this letter, we discuss the fabrication and electrical characterization of field-effect transistors at the surface of tetracene single crystals. The fabrication process is based on adhesion of pregrown, free-standing crystals to a thermally oxidized Si wafer on which source and drain electrodes are deposited in advance. As we will show, this process preserves the quality of the starting crystals. From the electrical evaluation of a large number of devices we find that the mobility of the charge carriers (holes) in our single-crystal FETs is reproducibly high, reaching 0.4 $cm^2/V\,s$ in the best device. In addition, the observed temperature and gate voltage dependence of the mobility as well as the subthreshold slope indicate that the performance of single-crystal devices compares well to the best existing organic thin film transistors.[3]

The FET fabrication involves two main steps: the growth of single crystals and the preparation of a substrate on which the crystal is subsequently placed.[15] Tetracene single crystals are grown by means of physical vapor deposition in a temperature gradient in the presence of a stream of argon gas. The setup used for the crystal growth is similar to that described in Ref. 16. The source material is 98% pure tetracene purchased from Sigma-Aldrich. Crystals grown from as-purchased tetracene are used as the source material for a subsequent regrowth process, which results in crystals of increased chemical purity. Tetracene crystals grown using physical vapor deposition are platelets. For the devices described in this letter we select thin (~1-μm-thick) single crystals obtained by stopping the second regrowth process at an early stage.

The substrates used for the FET fabrication are highly doped (n- or p-type) Si wafers, covered with a layer of 200 nm thermally grown SiO_2. The conducting Si wafer serves as the gate electrode, with the SiO_2 layer acting as the gate insulator. Gold contacts are deposited on top of the SiO_2 by means of e-beam evaporation through a shadow mask (see Fig. 1 for the precise geometry and dimensions). The dimensions of the Au contacts as well as the tetracene crystal size determine the transistor channel length L and channel width W. This allows us to study transistors with different W/L ratios. Prior to placing the tetracene single crystals on top of the substrate, the SiO_2 surface is cleaned by reactive ion etching (RIE) in an oxygen plasma. We found that this cleaning step is crucial for reproducible FET behavior.[17]

Freshly grown tetracene crystals placed on RIE-cleaned SiO_2 strongly adhere to the substrate. Adhesion only occurs for very thin crystals (~1 μm) that are sufficiently flexible and it is probably due to electrostatic forces. The crystals placed onto substrates are then inspected under an optical microscope using cross polarizers. This allows us to select single-crystalline samples without visible defects for in-depth electrical characterization.[18] The top view of a device fabricated following this procedure is shown in Fig. 1(c).

We have characterized more than ten single-crystal FETs exhibiting similar overall behavior. Electrical characterization is performed in the vacuum chamber of a flow cryostat

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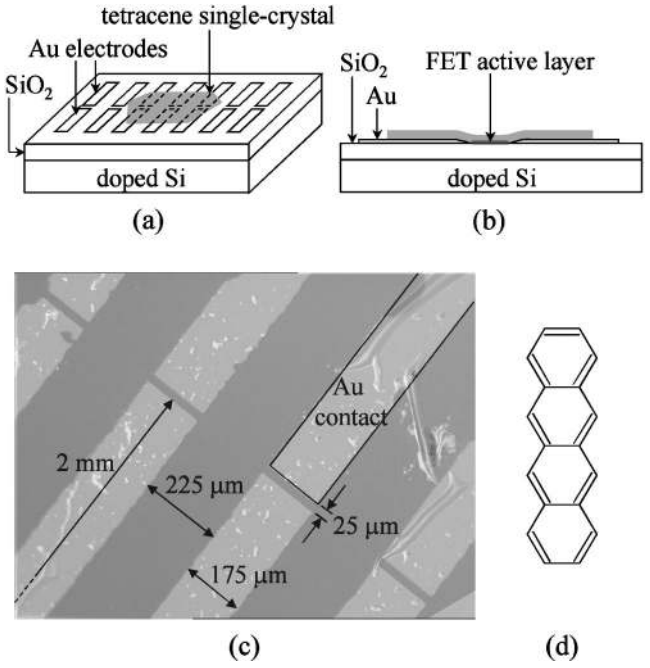

FIG. 1. Schematic representation (a) and side view (b) of a tetracene single-crystal FET. (c) Optical microscope image of a tetracene single-crystal FET. In this device, the semi-transparent tetracene single crystal extends over several pairs of electrodes, which are clearly visible under it. In most cases smaller crystals have been used which extend over only one or two pair of contacts. These different configurations allow us to study transistors with different W/L ratios on the same crystal. (d) Molecular structure of the tetracene molecule.

at a pressure of 10^{-7} mbar, using a HP4156A semiconductor parameter analyzer. The measurements shown in this letter have been performed in a two-terminal configuration.

Figure 2 shows the outcome of the measurements for one of the transistors with highest mobility. The current increases with increasing negative gate voltage. This indicates field-effect-induced hole conduction, which is the expected behavior for tetracene. The field-effect mobility is evaluated

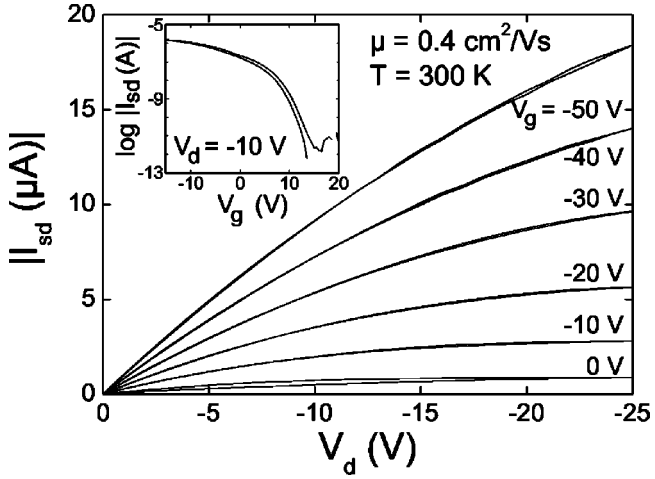

FIG. 2. Source-drain current I_{sd} versus drain voltage V_d measured at different values of V_g. The inset shows the dependence of $\log(I_{sd})$ on V_g at fixed V_d, for a different device, which has a mobility $\mu=0.05$ cm^2/V s and a threshold voltage $V_t \simeq 0.3$ V. From this plot we calculate the subthreshold slope to be 1.6 V/decade.

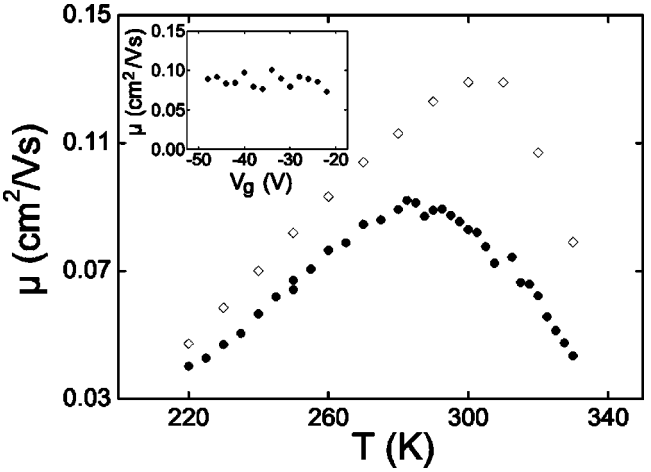

FIG. 3. Temperature dependence of the field-effect mobility for two different devices, measured at large negative gate voltage. The inset illustrates that at large negative gate voltage, -20 to -50 V, where the highest mobility is observed, μ is essentially independent of V_g.

in the linear regime of operation, where I_{sd} is proportional to V_d:

$$I_{sd}=\frac{W}{L}\mu C_d(V_g-V_t)V_d. \tag{1}$$

Here C_d is the capacitance per unit area of the SiO_2 layer and V_t is the threshold voltage. From Eq. (1) we obtain the mobility by calculating the derivative of I_{sd} with respect to both V_d and V_g and neglecting the dependence of μ on V_d and V_g.

For all the FETs investigated we found room-temperature values of the mobility larger than 0.01 cm^2/V s. In many cases $\mu>0.1$ cm^2/V s and the maximum mobility achieved so far is $\mu=0.4$ cm^2/V s (Fig. 2). This value is better than the highest mobility recently reported in tetracene TFTs and indicates the high quality of our single-crystal FETs.[19]

The threshold voltage [defined by Eq. (1)] is positive in all our devices. It ranges from 0 to 30 V and is typically $V_t \simeq 10$ V.[20] We do not normally observe a positive threshold voltage in FETs fabricated without the RIE cleaning, nor do we observe linear conduction through single crystals contacted with evaporated gold contacts. These observations suggest that the current flowing at zero gate voltage is not due to conduction through the crystal bulk (i.e., crystal doping) but rather to charge accumulated at the surface.[21] We believe that the charge accumulation is induced by the electrostatic adhesion of tetracene crystals to the RIE cleaned SiO_2 surface.

As an additional characterization of the single crystals FETs, the inset of Fig. 2 shows $\log(I_{sd})$ vs V_g at fixed drain voltage ($V_d=-10$ V). These data were measured on a FET with a relatively low mobility of $\mu=0.05$ cm^2/V s, i.e., they can be considered as typical. From this measurement we find the subthreshold slope to be 1.6 V/decade. Normalizing this value to the capacitance of the dielectric gives 28 V nF/decade cm^2. These values are comparable to what is found for the best pentacene TFTs [15–80 V nF/decade cm^2 (Refs. 11, 19, and 21)].

Further proof of the high quality of the tetracene single-crystal FET is provided by the temperature dependence of the mobility. Temperature-dependent measurements were performed in the range 220–330 K, since for $T>330$ K tetracene crystals rapidly sublime at the pressure present in the measurement chamber, and for $T<200$ K, a structural phase transition[22] often results in a lowered mobility and in damage to the devices. Figure 3 shows data from two different FETs. The mobility initially increases with lowering the temperature from 330 to 280–300 K, and then decreases when the temperature is lowered further. Such a nonmonotonous temperature dependence is not usually observed in organic TFTs, which typically exhibit a thermally activated decrease of μ with decreasing T, over the entire temperature range investigated.[19,23]

The observed temperature dependence of the mobility is qualitatively similar to the one expected for high-purity organic crystals in the presence of shallow traps, which is given by $\mu \propto T^{-n} \exp(-E_t/kT)$.[24,25] As long as E_t is not much larger than kT, this formula accounts for a nonmonotonous temperature dependence of μ in the temperature range investigated. The observation of a maximum mobility at room temperature indicates that $E_t \approx 50-100$ meV (i.e., a few times kT at room temperature). This is consistent with the weak gate voltage dependence of the mobility, see the inset of Fig. 3, which also points to weak trapping.[5]

To obtain more information about the quality of the tetracene crystals and about the FET fabrication process, we have performed time-of-flight (TOF) measurements on several thick (100–200 μm) tetracene crystals grown by the same technique.[26] For all crystals investigated, the room temperature mobility found in TOF experiments ranges from 0.5 to 0.8 $\mathrm{cm}^2/\mathrm{V\,s}$, comparable or slightly higher than that obtained from our best FETs. Also, the temperature dependence of the mobility is similar to that observed in FET measurements.[27] Finding comparable values for the bulk and the surface mobility[28] suggests that the FET fabrication process does not severely degrade the quality of the crystal surface. We conclude that, presently, the limiting factor for the mobility of the tetracene single-crystal FETs is the quality of the as-grown crystals.

In conclusion, we have shown that high-quality organic single-crystal FETs can be realized, whose performance is comparable to the best existing organic thin film transistors. As research on organic thin film FETs has now been going on for many years, whereas work on single crystals has just started, we consider this result to be particularly promising for future developments.

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