Check for updates

OPEN

Filamentary Resistive Switching and Capacitance-Voltage Characteristics of the a-IGZO/TiO$_2$ Memory

Kwan-Jun Heo[1,2], Han-Sang Kim[1], Jae-Yun Lee[1] & Sung-Jin Kim[1] ✉

In this study, molybdenum tungsten/amorphous InGaZnO (a-IGZO)/TiO$_2$/n-type Si-based resistive random access memory (ReRAM) is manufactured. After deposition of the a-IGZO, annealing was performed at 200, 300, 400, and 500 °C for approximately 1 h in order to analyze the effect of temperature change on the ReRAM after post annealing in a furnace. As a result of measuring the current-voltage curve, the a-IGZO/TiO$_2$-based ReRAM annealed at 400 °C reached compliance current in a low-resistance state, and showed the most complete hysteresis curve. In the a-IGZO layer annealed at 400 °C, the O_1/O_{total} value increased most significantly, to approximately 78.2%, and the O_3/O_{total} value decreased the most, to approximately 2.6%. As a result, the a-IGZO/TiO$_2$-based ReRAM annealed at 400 °C reduced conductivity and prevented an increase in leakage current caused by oxygen vacancies with sufficient recovery of the metal-oxygen bond. Scanning electron microscopy analysis revealed that the a-IGZO surface showed hillocks at a high post annealing temperature of 500 °C, which greatly increased the surface roughness and caused the surface area performance to deteriorate. Finally, as a result of measuring the capacitance-voltage curve in the a-IGZO/TiO$_2$-based ReRAM in the range of —2V to 4V, the accumulation capacitance value of the ReRAM annealed at 400 °C increased most in a nonvolatile behavior.

The unit cell size of the currently developed dynamic random access memory (DRAM) is gradually decreasing for high integration in the manufacturing process[1–3]. This DRAM miniaturization increases difficulty in the capacitor process, and makes it challenging to develop highly integrated cells[4,5]. NAND flash memory, which is nonvolatile memory, faces limitations in terms of control and yield in production because of the complex manufacturing method and the increased number of processes resulting from the structural change from 2D to 3D[6–8]. Consequently, resistive random access memory (ReRAM) is drawing attention as a next-generation memory that overcomes the disadvantages of previous types of memory and has the advantages of high density, nonvolatility, and speed[9–11]. In particular, ReRAM has an access time approximately 10^5 times faster than flash memory. It can accept a low voltage, similar to DRAM, and can be produced in a simple metal-insulator-metal (MIM) structure[12–15]. The resistance variation characteristic of ReRAM is caused by the dissolution and movement of metal ions based on electrochemical migration at the interface. As a major material for memory motion control, titanium dioxide (TiO$_2$), which has high conductivity, is mainly being researched[16–18]. Meanwhile, TiO$_2$ implements switching motions using oxygen vacancy, which plays the role of a carrier. However, it has the problem of aggravating the endurance characteristic of memory because of the generation/recombination between oxygen vacancies in the movement process, which causes carrier trapping, reduces the on/off ratio, and lowers electron mobility[14,19–21].

The electron movement of amorphous indium-gallium-zinc oxide (a-IGZO), which is an oxide semiconductor, is generated through ns-orbitals, in general, and a-IGZO is regarded as a very promising electronic material that can overcome the shortcomings of TiO$_{2-x}$. It can obtain fast electron mobility, even in an amorphous state, and can implement excellent resistance switching characteristics in memory[22–24]. However, a-IGZO thin films produced by low-temperature sputtering require post-heat treatment to lower contact resistance at the interface between the electrode and the oxide semiconductor layer[25,26]. The post-heat-treatment process can affect the

[1]College of Electrical and Computer Engineering, Chungbuk National University, Cheongju, 28644, Korea. [2]R&D center, SK hynix, 2091, Gyeongchung-daero, Bubal-eup, Icheon-si, Gyeonggi-do, 13558, Korea. ✉e-mail: ksj@cbnu.ac.kr
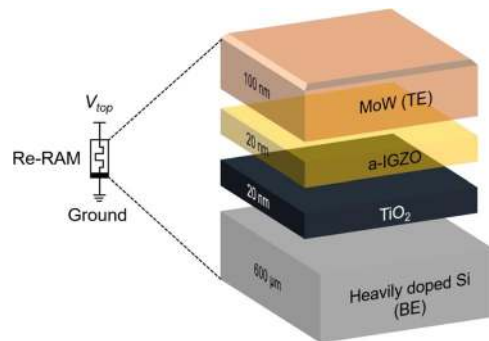
Figure 1. Structure of a-IGZO/TiO$_2$-based ReRAM manufactured with post annealing in a furnace at 200, 300, 400, and 500 °C.

reduction of the electron trap density and improve electrical performance (such as electron mobility) by removing defects at the semiconductor interface, and increasing the binding force between metals and oxides in the semiconductor[27–29].

In this study, therefore, memory with a heterojunction structure is manufactured using an a-IGZO oxide semiconductor as an active layer with excellent switching characteristics based on fast electron mobility and a high on/off ratio, compared with TiO$_{2-x}$. The electrical, surface, and component effects (based on temperature differences) were examined to determine the most suitable post-heat-treatment condition of the a-IGZO oxide semiconductor. Finally, the capacitance-voltage (C-V) characteristics were observed in order to investigate the characteristics of ReRAM in a metal-insulator-oxide-semiconductor (MIOS) structure based on the manufactured a-IGZO.

Experimental Section

Figure 1 shows the structure of the molybdenum tungsten (MoW)/a-IGZO/TiO$_2$/n-type silicon (Si)-based MIOS ReRAM manufactured in this study. The electric symbols indicate that the ReRAM is a nonlinear passive device related to the combination of charge and magnetic flux[30,31]. A 600 μm-thick heavily doped n-type Si wafer was used as the substrate and bottom electrode. To remove the surface defects (metallic defects, organic particles), SPM cleaning for 60 m at 90 °C was performed with a solution of sulfuric acid and deionized water at a 3:1 ratio. To produce an insulation membrane on the Si bottom electrode, TiO$_2$ was deposited using an atomic layer deposition (ALD) system (LUCIA D100, NCD Co., Ltd., Daejeon, South Korea). For the ALD cycle, titanium tetraisopropoxide was injected as a precursor to Ti. One cycle was defined as dinitrogen (N$_2$) purge gas injection for 10 s, water (H$_2$O) injection for 1 s, and N$_2$ purge gas injection for 10 s. Then, a 20 nm-thick TiO$_2$ thin film was formed by repeating 1,000 cycles with 0.2 Å deposition per cycle.

To form an oxide semiconductor, a 20 nm-thick a-IGZO thin film was deposited using a radio frequency (RF) magnetron sputtering process based on a target composed of In:Ga:Zn at a composition ratio of 1:1:1 mol%. After the deposition was complete, heat treatment was applied for approximately 1 h in a furnace to control interface defects and improve crystallinity, thus reducing the interface resistance and increasing the charge concentration and electron mobility[32–34]. To determine the temperature for optimizing the characteristics of a-IGZO-based ReRAM, the furnace temperature was evaluated, and heat treatment was applied for approximately 1 h at temperatures of 200, 300, 400, and 500 °C. After that, a 100 nm-thick MoW source/drain electrode was deposited using DC magnetron sputtering with a shadow mask on top of the a-IGZO. The finally formed upper MoW electrode had a square shape with a length and width of 100 × 100 μm, and four ReRAM devices were put on one wafer. To examine the electrical performance of the finally manufactured a-IGZO/TiO$_2$ ReRAM, the current-voltage (I-V) curve was measured. In addition, composition and surface analysis was performed to determine the optimal post-heat-treatment temperature of the a-IGZO oxide semiconductor applicable to ReRAM, and the memory characteristics were checked through C-V measurement.

Results and Discussion

Figure 2 shows the transfer curve graph of the TiO$_{2-x}$ thin-film transistor and a-IGZO TFT formed in a top-contact-bottom-gate structure. The insets in Fig. 2a,b show schematics of the TiO$_{2-x}$ TFT and a-IGZO TFT from which the transfer curves were extracted. A 600 μm-thick heavily doped n-type Si wafer was used as the substrate and gate bottom electrode. For the TFT, 100 nm-thick SiO$_2$ was used as an insulation membrane. The thickness of the TiO$_{2-x}$ was 30 nm, and after deposition with ALD, rapid thermal annealing was applied at 700 °C for 5 min. The a-IGZO had a thickness of 50 nm, and after deposition with RF magnetron sputtering, it was heat-treated at 350 °C for 1 h in a furnace. Every electrode was 100 nm-thick aluminum (Al), and the channel length and width were 200 μm and 2,000 μm, respectively.

Bias voltage was applied at 30 V of V_{ds}, and the I_{ds} value was examined when V_{gs} was applied from −10 V to 30 V in increments of 0.2 V. According to Table 1, the electron mobility of the a-IGZO TFT was 11.02 cm^2/Vs, which is excellent, compared with the 0.15 cm^2/Vs of the TiO$_{2-x}$ TFT. Furthermore, the on/off current ratio values showed a large difference at 6.2 × 10^6 and 7.2 × 10^3, respectively. The off-current level of the a-IGZO TFT was approximately 1.0 × 10^{-10}, which is similar to that of the TiO$_{2-x}$ TFT, but the on-current level was approximately
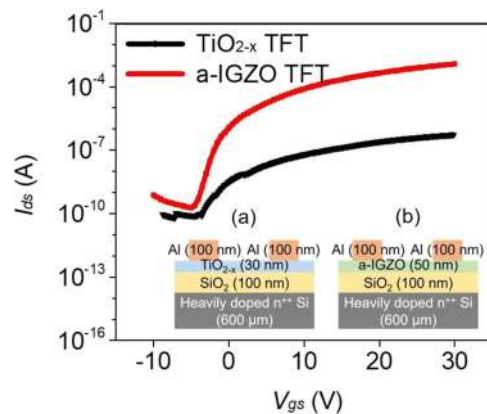
Figure 2. Transfer characteristics of the TiO_{2-x} TFT and the a-IGZO TFT with $V_{ds} = 30\,V$. (inset: structures of the (**a**) TiO_{2-x} TFT and (**b**) a-IGZO TFT).
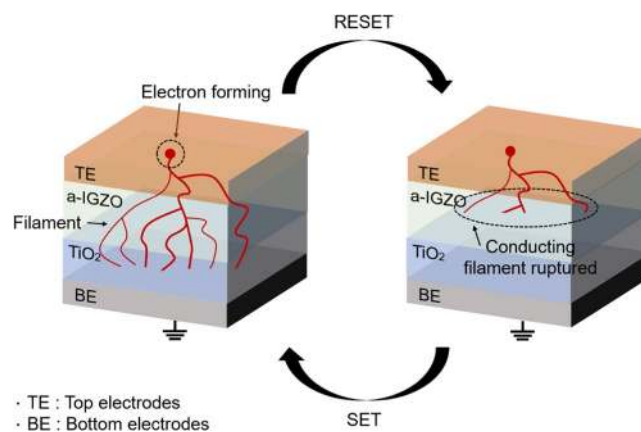

Figure 3. Typical switching mechanism of a-IGZO/TiO_2-based ReRAM.

Active-layer materials	μ_{sat} (cm²/Vs)	On/off current ratio	V_{th} (V)	S/S (V/dec)
TiO_{2-x}	0.15	7.2×10^3	0.40	0.31
a-IGZO	11.02	6.2×10^6	4.94	0.87

Table 1. Comparison of the electrical parameters of the TiO_{2-x} TFT and the a-IGZO TFT.

1.0×10^{-3}, in contrast to the 7.0×10^{-7} of the TiO_{2-x} TFT. Thus, the a-IGZO TFT is expected to be excellent for implementing high- and low-resistance states (HRS/LRS) characteristic of ReRAM.

Figure 3 illustrates the typical switching mechanism of the a-IGZO/TiO_2-based ReRAM. For measurement of the ReRAM, a heavily doped n-type Si wafer substrate was used as the bottom electrode, and operation of the a-IGZO ReRAM was checked by applying a voltage to the upper MoW electrode. At first, the current was low when a positive (+) voltage was applied from the a-IGZO oxide active layer to the positive bias area, but the current increased sharply when a specific threshold voltage was applied. This process is called the SET operation[35–37]. By contrast, when a voltage is applied from the positive bias area to the negative bias area, the device reaches the (−) threshold voltage, and the current decreases sharply. This process is called the RESET operation[35,36]. When the state of the a-IGZO thin film reaches the (+) threshold voltage for this process in ReRAM, a conducting pathway is generated because of filament formation[38–40]. However, when a (−) voltage is applied, the oxygen trap of the TiO_2 insulation layer blocks the electron movement, causing a rupture of the filament[39,40]. Through this process, the resistance state changes according to the applied bias, which induces hysteresis[41–43] and drives the a-IGZO/TiO_2 ReRAM.

Figure 4 shows the measurements of electrical performance from the a-IGZO/TiO_2-based ReRAM when post-heat treatment was applied at 200, 300, 400, and 500 °C after deposition of the a-IGZO oxide semiconductor layer. For the measurement device, a System 4200 Source Meter (Keithley) was used to measure the I-V curve when −2 V to 4 V was applied. Figure 4a shows the I-V curve of the ReRAM when post-heat treatment was applied at 200 °C. At voltages from 0 V to 4 V, an HRS was observed. Then, at 4 V, which is a reverse sweep, a
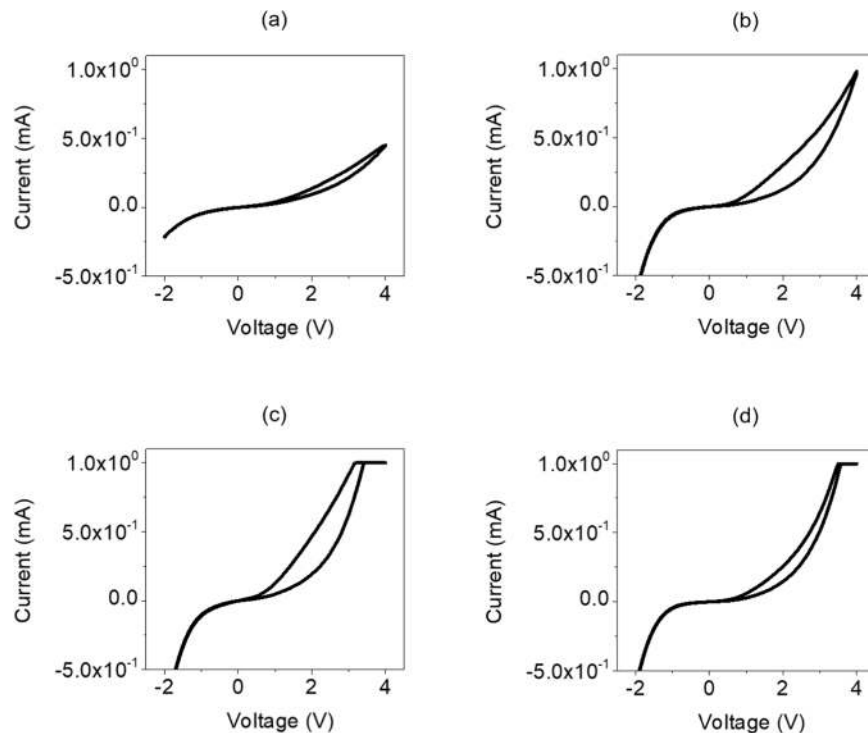
Figure 4. I-V curves for -2 V to 4 V in the a-IGZO layers manufactured with post annealing in a furnace at (**a**) 200 °C, (**b**) 300 °C, (**c**) 400 °C, and (**d**) 500 °C.

current of approximately 2.83×10^{-4} was recorded, creating an LRS. After reaching the write state, the ReRAM changed again to an HRS after -2 V was applied, and then it changed to the erase state. Figure 4b shows the I-V curve of the ReRAM that underwent post-heat treatment at 300 °C. The current was approximately 9.82×10^{-4} at 4 V. In Fig. 4c,d, which are the I-V curves of the ReRAM that underwent post-heat treatment at 400 °C or more, the current increased to 1.00×10^{-3}, which is set as compliance.

In addition, as the post-heat-treatment temperature of ReRAM was increased, the current level of the LRS increased due to crystallization of the a-IGZO thin film. Through this, it was confirmed that the hysteresis curve characteristics of the memory had been implemented. The ReRAM that underwent post-heat treatment at 200 °C did not show the perfect shape of the hysteresis curve in the $(+)$ area. Using 300 °C created a hysteresis shape with a small width. By contrast, when the post-heat-treatment temperature was 400 °C, the best hysteresis shape was seen. However, the I-V curve of the ReRAM that underwent post-heat treatment at 500 °C reached the compliance current in Fig. 4d, but the hysteresis characteristic decreased as the off-current level increased, and the gap between the HRS and LRS decreased.

In the low range of the post-heat-treatment temperature, electrons were trapped because of interface resistance and the defects on the surface of the a-IGZO thin film. As the temperature increased, the trap density decreased, and as the carrier concentration increased[44–46], the memory characteristics improved. Therefore, when the post-heat-treatment temperature was 400 °C for the a-IGZO oxide active layer deposited at a low temperature by RF magnetron sputtering, the optimal characteristics of the ReRAM were confirmed through the reduction of the carrier concentration and the trap density of electrons. By contrast, when heat treatment was applied at 500 °C or higher, the hysteresis characteristic decreased because of the unstable state that was formed in some crystals in the IGZO thin film[47–49].

Figure 5 shows the x-ray photoelectron spectroscopy (XPS) analysis result of the O1s peaks in the surface after post-heat treatment at 200, 300, 400, and 500 °C after deposition of the a-IGZO oxide semiconductor layer. When post-heat treatment was applied at 400 °C, which is the temperature condition that showed the best electrical performance, the proportion of the oxygen vacancy peaks (O_1) among the O1s peaks was the highest at approximately 78.2%, and the proportion of hydroxide peaks (O_3) was the lowest at approximately 2.6%, as shown in Fig. 5c,e. By contrast, in the composition of the a-IGZO thin film that underwent post-heat treatment at 200 °C, the proportions of O_1 and O_3 among all O1s peaks were approximately 53.0% and 11.6%, respectively, as shown in Fig. 5a,e. Furthermore, in the composition of the a-IGZO thin film that underwent post-heat treatment at 300 °C, the proportion of O_1 among the O1s peaks was approximately 49.0%, as shown in Fig. 5b,e. When compared with the 200 °C condition, the proportion of O_1 decreased slightly from approximately 53.0% to 49.0%, and the proportion of O_3 increased from approximately 11.6% to 14.5%.

As shown above, when the O_1 peak is small and the O_3 peak is large, oxygen vacancies remain without sufficient recovery of the metal-oxygen bonds, and the overall electrical performance of the ReRAM decreases because of the increase in leakage current[50–52]. Furthermore, when the O_3 peak increases, hydrogen ions are combined with oxygen vacancies, and oxygen traps that are relatively strongly bonded with hydrogen increase. As a
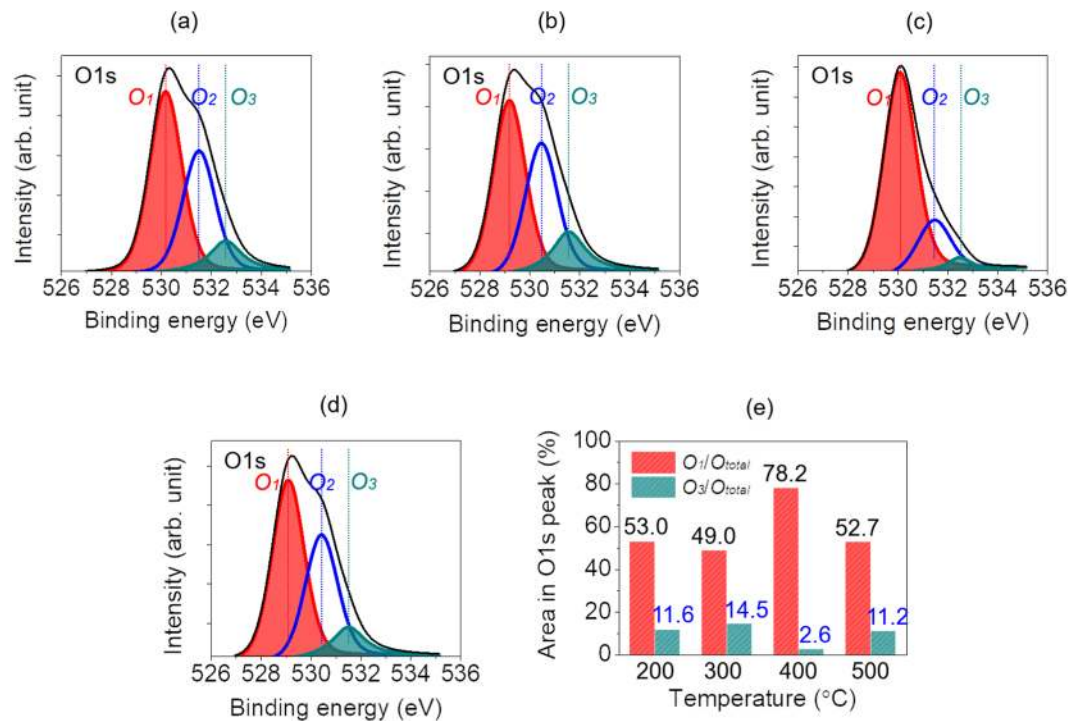
Figure 5. XPS spectra O1s patterns of a-IGZO layers manufactured with post annealing in a furnace at (**a**) 200 °C, (**b**) 300 °C, (**c**) 400 °C, and (**d**) 500 °C, respectively, and (**e**) an area in the O1s peak curve.
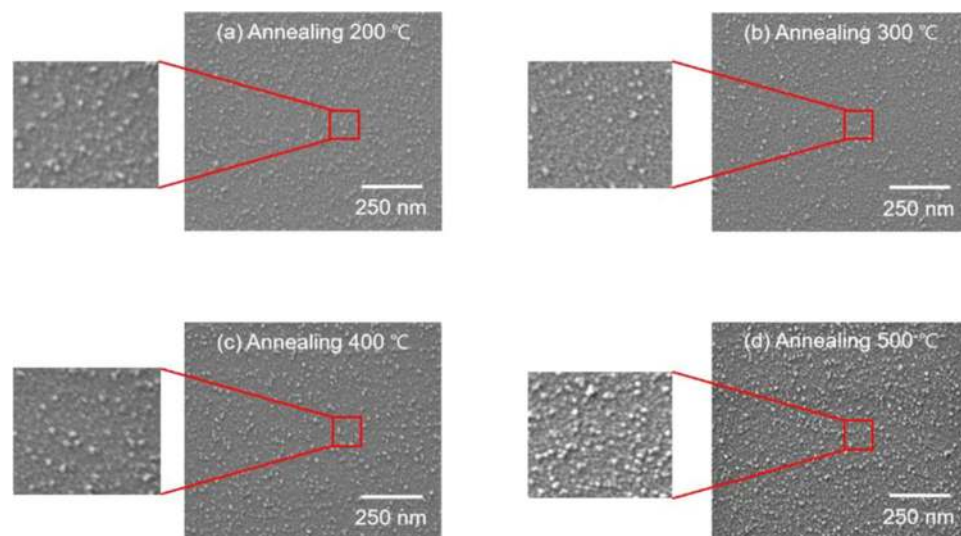

Figure 6. SEM images (50k× magnification) of the a-IGZO layers manufactured by post annealing in a furnace at (**a**) 200 °C, (**b**) 300 °C, (**c**) 400 °C, and (**d**) 500 °C. (inset: enlarged SEM images).

result, more interface trap charge phenomena that interfere with electron movement occur[53–55]. This is a cause for reduced electron mobility in memory devices while assisting the generation of leakage current, thus lowering the electrical performance of the ReRAM[56–58].

Meanwhile, when the post-heat-treatment temperature was higher than 500 °C, as shown in Fig. 5d,e, the proportion of O_1 among the O1s peaks in the composition of the a-IGZO thin film decreased significantly (to approximately 52.7%) while the proportion of O_3 increased again to approximately 11.2%. When the proportion of O_1 decreases and the proportion of O_3 increases, the oxygen molecules released from the metal-oxygen bonds quickly diffuse outside the thin film, where the concentration is relatively low, thus causing a decrease in the electrical performance of the ReRAM[50,59,60]. Consequently, this is the same as the electric experiment result that proved the post-heat-treatment temperature of 400 °C is optimal, and it can also be a basis for proving it.
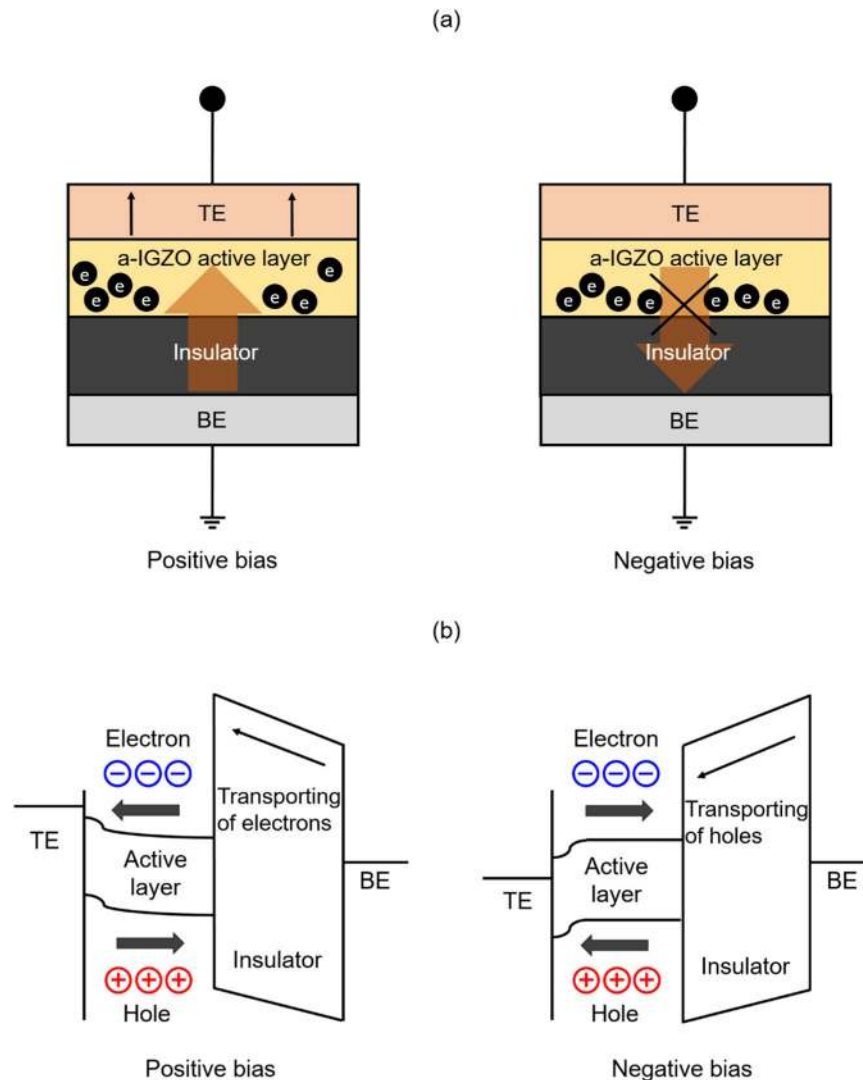
(a)

(b)

Figure 7. (**a**) Schematics to show that the excited charge carriers in the a-IGZO layer with thermal annealing contribute to the current rise; and (**b**) energy band diagrams representing electron transfer by excited electrons when each positive or negative bias is applied to the upper electrode in the MIOS structure.

Figure 6 shows measurements using scanning electron microscopy (SEM) with the electron high tension set to 1.0 kV, the I probe set to 1.0 nA, and the working distance set to 2.5 mm in order to analyze the surface area performance of a-IGZO that underwent post-heat treatment at 200, 300, 400, and 500 °C. As shown in Fig. 6a–c, as the post-heat-treatment temperature gradually increased from 200 °C to 400 °C, the grain boundary of the small oval grains grew in size with random curved shapes. However, when post-heat treatment was performed at 500 °C, as shown in Fig. 6d, the large and small grains coexisted on the same surface, and secondary recrystal-lization[61,62] was observed[63,64]. This implies that specific grains coarsen more quickly than others in the growing process. This occurs often when there are many impurities or crystals on the surface, and this ultimately causes a decrease in the electrical performance of the ReRAM[7,64,65].

Furthermore, as the post-heat-treatment temperature increases, the grain boundary becomes more distinct. In the a-IGZO thin film that underwent post-heat treatment at 500 °C, many hillocks were observed on the surface of the thin film. It is presumed that, because of the high post-heat treatment of 500 °C, the degree of relaxation in the compressive stress that the a-IGZO thin film received increased, and small deformations increased, thus increasing the size of the hillocks[66,67]. Therefore, in the a-IGZO thin film that underwent post-heat treatment at 500 °C, the roughness of the surface also increased significantly, because many hillocks were generated. When the surface roughness of the oxide semiconductor is large, a large current leakage occurs because of the interface trap charge phenomenon that interferes with electron movement, resulting in a large, adverse effect on the general electrical properties of the device[68–70]. Consequently, when a high post-heat-treatment temperature like 500 °C is applied after deposition of the a-IGZO oxide semiconductor layer, an aggravated surface state can be seen, which suggests that post-heat treatment at 500 °C or higher has a significant effect on performance degradation of the ReRAM.
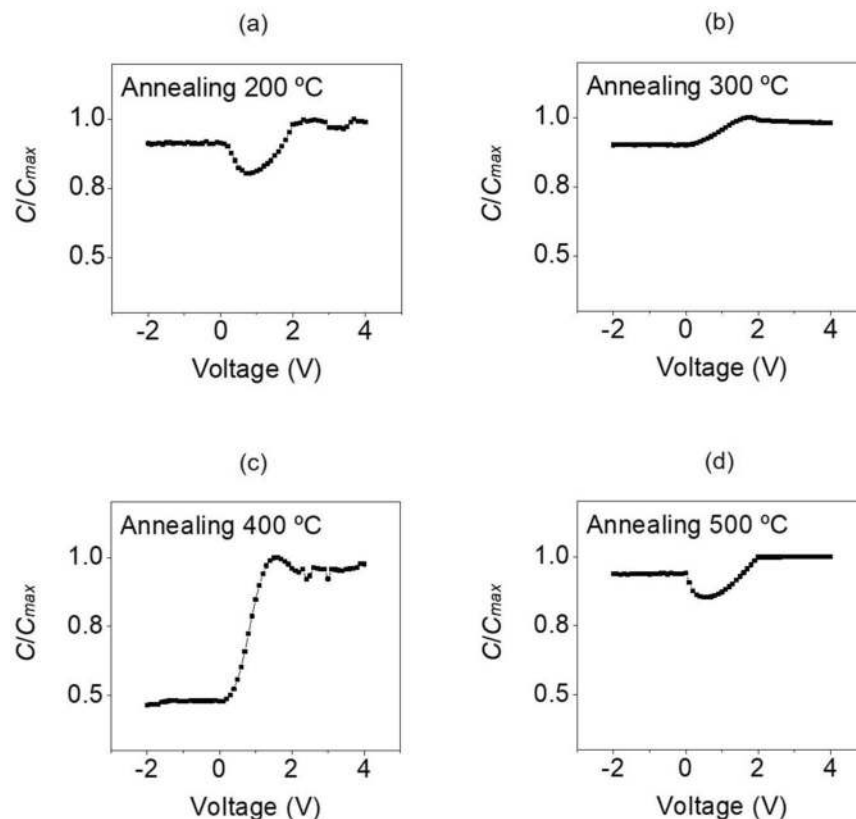
Figure 8. C-V curves for -2 V to 4 V in the a-IGZO layers manufactured with post annealing in a furnace at (**a**) 200 °C, (**b**) 300 °C, (**c**) 400 °C, and (**d**) 500 °C.

Figure 7a shows schematics of the electron movement mechanism in the MIOS structure, analyzing the effect of post-heat treatment of the a-IGZO. The current's size and direction in the C-V characteristics of the ReRAM that was post-heat treated for a-IGZO depend greatly on the state of the active layer[71]. In a typical MIM device, the electrons injected through the interface of the insulation layer from the top/bottom metal electrodes flow in two directions, and the direction is determined by the applied bias voltage[72–74]. However, the MIOS device flows in a single direction toward the a-IGZO active layer from the metal to which the positive bias voltage is applied[75,76].

First, the a-IGZO active layer creates an electron movement path by moving the electrons injected by positive voltage applied to the upper MoW metal electrode, and electrons are injected from the interface of the a-IGZO/TiO_2 through the accumulation area of electrons[77]. The injected electrons form a filament, owing to the conductivity of the bottom electrode, and drive the memory[14,78]. By contrast, when a negative bias voltage is applied to the upper electrode, the electron movement path for the electrons delivered by the TiO_2 insulating film from the bottom electrode is blocked by the depletion of electrons acting as a capacitor for the TiO_2-SiO_2 interface[79,80]. Consequently, the current is halted by the negative bias without flowing, and the filament of the TiO_2/a-IGZO is ruptured[12,81]. Figure 7b represents the movement of excited electrons as an energy band when a positive or negative bias is applied to the MIOS structure. The electrons and holes changed to an excited state by the voltage applied to the upper electrode, and the excited electrons or holes have the energy for tunneling the TiO_2 insulating film[82,83].

Figure 8 shows the measurement results of the C-V curves in the range of –2 V to 4 V in 0.1 V increments for the a-IGZO/TiO_2-based ReRAM that underwent post-heat treatment at 200, 300, 400, and 500 °C after deposition of the a-IGZO oxide semiconductor layer. The frequency was set to 1 kHz, and the y-axis represents C/C_{max}, which is the capacitance divided by the maximum capacitance for the applied voltage. As shown in Fig. 8a, the C/C_{max} value was approximately 0.91 in the inversion area for the ReRAM that underwent post-heat treatment at 200 °C, but it was approximately 0.99 in the accumulation area, thus showing a very small difference. Furthermore, in Fig. 8b,d, which show the ReRAM that underwent post-heat treatment at 300 °C and 500 °C, respectively, the C/C_{max} value was approximately 0.90 in the inversion area and 0.98 in the accumulation. Thus, there was little difference from post-heat treatment at 200 °C. Figure 8a,b,d show that the C-V characteristics were not realized due to the inability to optimize the carrier concentration and electron trap density of the a-IGZO thin film caused by a lack of and excess heat treatment. This is because the electrical properties of the memory due to the interfacial trap deteriorate when the recovery of the metal-oxygen bond by heat treatment is not sufficiently achieved. The C-V characteristics of MIOS do not appear to be implemented under 200, 300, and 500 °C because of the inappropriate post-heat treatment temperatures.

However, as shown in Fig. 8c, for the ReRAM that underwent post-heat treatment at 400 °C, the C/C_{max} value was approximately 0.45 when −2 V to 0 V was applied to the upper MoW electrode, indicating that the current state was the inversion section. At this time, the electric field that penetrated through the oxide layer became large enough to induce a small number of carriers to the semiconductor surface. The electron concentration of the semiconductor surface remained relatively constant, because it cannot respond to the high-frequency signals[84,85]. When 0 V to 2 V was applied, because the applied voltage changed from negative (−) to positive (+), the electron energy in the MoW electrode decreased, and (+) charges gathered at the interface between the electrode and oxide. As a result, corresponding (−) charges gathered near the interface between the semiconductor and oxide, which drove out holes or recombined with them, and the interface became a depletion area with no carriers[86,87]. When 2 V to 4 V was applied, the C/C_{max} value became approximately 0.98, and electrons gathered at the interface between the metal and the oxide semiconductor layer, reaching the accumulation area, where the capacitance value increased[88,89]. In conclusion, we verified through the C-V value that the memory characteristics are optimized when a positive or negative bias voltage is applied to the MoW electrode of the a-IGZO-based ReRAM that underwent post-heat treatment at 400 °C.

Conclusions

MoW/a-IGZO/TiO$_2$/n-type Si-based ReRAM was manufactured using ALD and a DC/RF magnetron sputtering system. To analyze the effect of the change in temperature for post-heat treatment using a furnace after depositing a-IGZO (an oxide semiconductor layer) on the a-IGZO/TiO$_2$-based ReRAM, the ReRAM was heat-treated for approximately 1 h at 200, 300, 400, and 500 °C. The measurement of the I-V curve showed that the a-IGZO/TiO$_2$-based ReRAM that underwent post-heat treatment at 400 °C showed the most perfect hysteresis curve. Furthermore, when the O1s peaks of the a-IGZO thin film were checked through XPS, the a-IGZO thin film that underwent post-heat treatment at 400 °C showed the largest increase in the O_1/O_{total} value at approximately 78.2%, and the largest decrease in the O_3/O_{total} value at approximately 2.6%. As a result, the a-IGZO/TiO$_2$-based ReRAM that underwent post-heat treatment at 400 °C showed a decrease in conductivity, and prevented the increase in leakage current because the metal-oxygen bonds sufficiently recovered. SEM analysis showed that hillocks are generated on the a-IGZO surface at the high post-heat treatment temperature of 500 °C, thus greatly increasing the surface roughness, and worsening the surface area performance. Finally, measurement of the C-V curve in the range of −2 V to 4 V for the a-IGZO/TiO$_2$-based ReRAM confirmed that the memory characteristics were optimized. Therefore, the results of this study prove that when post-heat treatment is applied to the a-IGZO oxide active layer, 400 °C produces the best electrical performance in the ReRAM, and the best composition and surface state in the a-IGZO thin film.

References

1. Park, J. B., Davis, W. R. & Franzon, P. D. 3-D-DATE: A Circuit-Level Three-Dimensional DRAM Area, Timing, and Energy Model. *IEEE Trans. Circuits Syst. I, Reg.* Papers. **66**, 756–768 (2019).
2. Cho, Y. *et al.* Suppression of the Floating-Body Effect of Vertical-Cell DRAM With the Buried Body Engineering Method. *IEEE Trans. Electron Devices* **65**, 3237–3242 (2018).
3. Yu, E. *et al.* A Band-Engineered One-Transistor DRAM With Improved Data Retention and Power Efficiency. *IEEE Electron Device Lett.* **40**, 562–565 (2019).
4. Tehranipoor, F. *et al.* DRAM-Based Intrinsic Physically Unclonable Functions for System-Level Security and Authentication. *IEEE Trans. Very Large Scale Integr. VLSI Syst.* **25**, 1085–1097 (2017).
5. Kim, S. M., Song, B. & Jung, S. Sensing Margin Enhancement Technique Utilizing Boosted Reference Voltage for Low-Voltage and High-Density DRAM. *IEEE Trans. Very Large Scale Integr. VLSI Syst.* **27**, 2413–2422 (2019).
6. Sahay, S. & Strukov, D. A Behavioral Compact Model for Static Characteristics of 3D NAND Flash Memory. *IEEE Electron Device Lett.* **40**, 558–561 (2019).
7. Yoon, K. J., Kim, Y. & Hwang, C. S. What Will Come After V-NAND-Vertical Resistive Switching. *Memory? Adv. Electron. Mater.* **5**, 1800914 (2019).
8. Yoon, J. W. *et al.* Nanophotonic identification of defects buried in three-dimensional NAND flash memory devices. *Nat. Electron.* **1**, 60–67 (2018).
9. Chien, T. *et al.* Low-Power MCU With Embedded ReRAM Buffers as Sensor Hub for IoT Applications. *IEEE Trans. Emerg. Sel. Topics Circuits Syst.* **6**, 247–257 (2016).
10. Chang, Y. *et al.* Guest Editorial: IEEE Transactions on Computers Special Section on Emerging Non-Volatile Memory Technologies: From Devices to Architectures and Systems. *IEEE Trans. Comput.* **68**, 1111–1113 (2019).
11. Dai, G. *et al.* HyVE: Hybrid Vertex-Edge Memory Hierarchy for Energy-Efficient Graph Processing. *IEEE Trans. Comput.* **68**, 1131–1146 (2019).
12. Rodriguez-Fernandez, A. *et al.* Switching Voltage and Time Statistics of Filamentary Conductive Paths in HfO$_2$-Based ReRAM Devices. *IEEE Electron Device Lett.* **39**, 656–659 (2018).
13. Vescio, G. *et al.* Low-Power, High-Performance, Non-volatile Inkjet-Printed HfO$_2$-Based Resistive Random Access Memory: From Device to Nanoscale Characterization. *ACS Appl. Mater. Interfaces* **11**, 23659–23666 (2019).
14. Huang, T.-K. *et al.* Ni/NiO/HfO$_2$ Core/Multishell Nanowire ReRAM Devices with Excellent Resistive Switching Properties. *Adv. Electron. Mater.* **4**, 1800256 (2018).
15. Shahrabi, E. *et al.* Switching Kinetics Control of W-Based ReRAM Cells in Transient Operation by Interface Engineering. *Adv. Electron. Mater.* **5**, 1800835 (2019).
16. Rathore, B. P. S., Prakash, R. & Kaur, D. Effect of AlN layer on the resistive switching properties of TiO$_2$ based ReRAM memory devices. *Curr. Appl. Phys.* **18**, 102–106 (2018).
17. Ge, J. & Chaker, M. Oxygen Vacancies Control Transition of Resistive Switching Mode in Single-Crystal TiO$_2$ Memory Device. *ACS Appl. Mater. Interfaces* **9**, 16327–16334 (2017).
18. Xiao, M. *et al.* Reliable and Low-Power Multilevel Resistive Switching in TiO$_2$ Nanorod Arrays Structured with a TiO$_x$ Seed Layer. *ACS Appl. Mater. Interfaces* **9**, 4808–4817 (2017).
19. Kim, W. *et al.* Multistate Memristive Tantalum Oxide Devices for Ternary Arithmetic. *Sci. Rep.* **6**, 36652 (2016).

20. Baek, I.-J. & Cho, W.-J. Resistive switching characteristics of solution-processed organic-inorganic blended films for flexible memory applications. *Solid State Electron.* **140**, 129–133 (2018).
21. Choi, K.-H., Chung, K.-B. & Kim, H.-K. d-orbital ordering of oxygen-deficient amorphous and anatase TiO_{2-x} channels for high mobility thin film transistors. *Appl. Phys. Lett.* **102**, 153511 (2013).
22. Kim, T.-W., Baek, I.-J. & Cho, W.-J. Resistive switching characteristics of solution-processed Al-Zn-Sn-O films annealed by microwave irradiation. *Solid State Electron.* **140**, 122–128 (2018).
23. Kang, D. Y., Lee, T.-H. & Kim, T. G. Improved characteristics of amorphous indium-gallium-zinc-oxide-based resistive random access memory using hydrogen post-annealing. *Appl. Phys. Lett.* **109**, 073105 (2016).
24. Wu, Q. *et al*. A Dual-Functional IGZO-Based Device With Schottky Diode Rectifying and Resistance Switching Behaviors. *IEEE Electron Device Lett.* **40**, 24–27 (2019).
25. Tiwari, N., Shieh, H.-P. D. & Liu, P.-T. Structural, optical, and photoluminescence study of ZnO/IGZO thin film for thin film transistor application. *Mater. Lett.* **151**, 53–56 (2015).
26. Kumar, N., Kumar, J. & Panda, S. Enhanced pH sensitivity over the Nernst limit of electrolyte gated a-IGZO thin film transistor using branched polyethylenimine. *RSC Adv.* **6**, 10810–10815 (2016).
27. Yao, R. *et al*. Low-temperature fabrication of sputtered high-k HfO_2 gate dielectric for flexible a-IGZO thin film transistors. *Appl. Phys. Lett.* **112**, 103503 (2018).
28. Lin, C.-C. *et al*. Effects of two-stage post-annealing process on microstructure and electrical properties of sol-gel derived non-stoichiometric NKN thin films. *Appl. Surf. Sci.* **428**, 199–206 (2018).
29. Kim, T. *et al*. Exploring oxygen-affinity-controlled TaN electrodes for thermally advanced TaO_x bipolar resistive switching. *Sci. Rep.* **8**, 8532 (2018).
30. Yang, X., Khandelwal, S. & Jabir, A. Secure memristor replicator architecture with physical uncloneability. *Elect. Lett.* **55**, 1275–1277 (2019).
31. Hassan, A. M., Fahmy, H. A. H. & Rafat, N. H. Enhanced Model of Conductive Filament-Based Memristor via Including Trapezoidal Electron Tunneling Barrier Effect. *IEEE Trans. Nanotechnol.* **15**, 484–491 (2016).
32. Arulkumaran, S. *et al*. Enhancement of both direct-current and microwave characteristics of AlGaN/GaN high-electron-mobility transistors by furnace annealing. *Appl. Phys. Lett.* **88**, 023502 (2006).
33. Sun, J. *et al*. Improved mobility of sol-gel method processed transparent tin sulfide thin films. *Mater. Lett.* **178**, 231–234 (2016).
34. Lu, M.-P., Dai, X.-Y. & Lu, M.-Y. Probing Electron Mobility of Monolayer MoS_2 Field-Effect Transistors in Aqueous Environments. *Adv. Electron. Mater.* **4**, 1700418 (2018).
35. Chen, S. *et al*. An Artificial Flexible Visual Memory System Based on an UV-Motivated Memristor. *Adv. Mater.* **30**, 1705400 (2018).
36. Chen, J.-Y. *et al*. Switching Kinetic of VCM-Based Memristor: Evolution and Positioning of Nanofilament. *Adv. Mater.* **27**, 5028–5033 (2015).
37. Yoon, J. H. *et al*. Truly Electroforming-Free and Low-Energy Memristors with Preconditioned Conductive Tunneling Paths. *Adv. Funct. Mater.* **27**, 1702010 (2017).
38. Wakrim, T. *et al*. From MEMRISTOR to MEMImpedance device. *Appl. Phys. Lett.* **108**, 053502 (2016).
39. Nguyen, V. C. & Lee, P. S. Coexistence of Write Once Read Many Memory and Memristor in blend of Poly(3,4-ethylenedioxythiophene): polystyrene sulfonate and Polyvinyl Alcohol. *Sci. Rep.* **6**, 38816 (2016).
40. Kumar, S. *et al*. Direct Observation of Localized Radial Oxygen Migration in Functioning Tantalum Oxide Memristors. *Adv. Mater.* **28**, 2772–2776 (2016).
41. Cooper, D. *et al*. Anomalous Resistance Hysteresis in Oxide ReRAM: Oxygen Evolution and Reincorporation Revealed by *In Situ* TEM. *Adv. Mater.* **29**, 1700212 (2017).
42. Seo, J. *et al*. Automatic ReRAM SPICE Model Generation From Empirical Data for Fast ReRAM-Circuit Coevaluation. *IEEE Trans. Very Large Scale Integr. VLSI Syst.* **25**, 1821–1830 (2017).
43. Zhang, H. *et al*. Understanding the Coexistence of Two Bipolar Resistive Switching Modes with Opposite Polarity in $Pt/TiO_2/Ti/Pt$ Nanosized ReRAM Devices. *ACS Appl. Mater. Interfaces* **10**, 29766–29778 (2018).
44. Abbaszadeh, D. *et al*. Elimination of charge carrier trapping in diluted semiconductors. *Nat. Mater.* **15**, 628–633 (2016).
45. Ji, H. *et al*. Thickness-dependent carrier mobility of ambipolar $MoTe_2$: Interplay between interface trap and Coulomb scattering. *Appl. Phys. Lett.* **110**, 183501 (2017).
46. Kesavan, A. V., Rao, A. D. & Ramamurthy, P. C. Interface Electrode Morphology Effect on Carrier Concentration and Trap Defect Density in an Organic Photovoltaic Device. *ACS Appl. Mater. Interfaces* **9**, 28774–28784 (2017).
47. Rosa, J. *et al*. Memristors Using Solution-Based IGZO Nanoparticles. *ACS Omega* **2**, 8366–8372 (2017).
48. Ishizu, T. *et al*. An Energy-Efficient Normally Off Microcontroller With 880-nW Standby Power, 1 Clock System Backup, and 4.69-μs Wakeup Featuring 60-nm CAAC-IGZO FETs. *IEEE Solid State Circuits Lett.* **2**, 293–296 (2019).
49. Oh, S., Woo, J. & Jang, J. Comparative Studies of Long-Term Ambiance and Electrical Stress Stability of IGZO Thin-Film Transistors Annealed Under Hydrogen and Nitrogen Ambiance. *IEEE Trans. Electron Devices* **63**, 1910–1915 (2016).
50. Skaja, K. *et al*. Reduction of the forming voltage through tailored oxygen non-stoichiometry in tantalum oxide ReRAM devices. *Sci. Rep.* **8**, 10861 (2018).
51. Park, J. *et al*. Multi-layered $NiO_y/NbO_x/NiO_y$ fast drift-free threshold switch with high I_{on}/I_{off} ratio for selector application. *Sci. Rep.* **7**, 4068 (2017).
52. Sivan, M. *et al*. All WSe_2 1T1R resistive RAM cell for future monolithic 3D embedded memory integration. *Nat. Commun.* **10**, 5201 (2019).
53. Wei, H. *et al*. Sensitive X-ray detectors made of methylammonium lead tribromide perovskite single crystals. *Nat. Photonics* **10**, 333–339 (2016).
54. Dong, B. W. *et al*. High resistance ratio of bipolar resistive switching in a multiferroic/high-K $Bi(Fe_{0.95}Cr_{0.05})O_3/ZrO_2/Pt$ heterostructure. *Appl. Surf. Sci.* **434**, 687–692 (2018).
55. Wang, Z. *et al*. Poly(vinylidene fluoride) Flexible Nanocomposite Films with Dopamine-Coated Giant Dielectric Ceramic Nanopowders, $Ba(Fe_{0.5}Ta_{0.5})O_3$, for High Energy-Storage Density at Low Electric Field. *ACS Appl. Mater. Interfaces* **9**, 29130–29139 (2017).
56. Kaushik, J. K. *et al*. Investigation of surface related leakage current in AlGaN/GaN High Electron Mobility Transistors. *Thin Solid Films* **612**, 147–152 (2016).
57. Xu, N. *et al*. Gate leakage mechanisms in normally off p-GaN/AlGaN/GaN high electron mobility transistors. *Appl. Phys. Lett.* **113**, 152104 (2018).
58. Narita, T., Wakejima, A. & Egawa, T. Local gate leakage current induced by inhomogeneous epitaxial growth in AlGaN/GaN high-electron-mobility transistors. *Appl. Phys. Express* **9**, 031002 (2016).
59. Razi, P. M. & Gangineni, R. B. Compliance current and film thickness influence upon multi-level threshold resistive switching of amorphous $BaTiO_3$ (am-BTO) films in Ag/am-BTO/Ag cross point structures. *Thin Solid Films* **685**, 59–65 (2019).
60. Ishibe, T. *et al*. Epitaxial iron oxide nanocrystals with memory function grown on Si substrates. *Appl. Phys. Express* **9**, 055508 (2016).
61. Zhu, H., Liu, A. & Noh, Y. Transparent Inorganic Copper Bromide (CuBr) p-Channel Transistors Synthesized From Solution at Room Temperature. *IEEE Elect. Device Lett.* **40**, 769–772 (2019).
62. Joo, W.-J. *et al*. Realization of continuous Zachariasen carbon monolayer. *Sci. Adv.* **3**, e1601821 (2017).

63. Tian, H. *et al.* Growth Dynamics of Millimeter-Sized Single-Crystal Hexagonal Boron Nitride Monolayers on Secondary Recrystallized Ni (100) Substrates. *Adv. Mater. Interf.* **6**, 1901198 (2019).

64. Vannozzi, A. *et al.* Growth of Biaxially-Textured La$_2$Zr$_2$O$_7$ and Zr-doped CeO$_2$ on Cold-Rolled Ni-W Substrate by CSD. *IEEE Trans. Appl. Supercond.* **28**, 1–5 (2018).

65. Burr, G. W. *et al.* Recent Progress in Phase-Change Memory Technology. *IEEE Trans. Emerg. Sel. Topics Circuits Syst.* **6**, 146–162 (2016).

66. Powers, M. *et al.* Hillock formation in co-deposited thin films of immiscible metal alloy systems. *Thin Solid Films* **693**, 137692 (2020).

67. Barda, H. & Rabkin, E. Hillocks formation in the Cr-doped Ni thin films: growth mechanisms and the nano-marker experiment. *J. Mater. Sci.* **55**, 2588–2603 (2020).

68. Zhang, F. *et al.* Interface studies of well-controlled polymer bilayers and field-effect transistors prepared by a mixed-solvent method. *RSC Adv.* **8**, 11272–11279 (2018).

69. Hashemi, A. & Bahari, A. Synthesis and characterization of silanized-SiO$_2$/povidone nanocomposite as a gate insulator: The influence of Si semiconductor film type on the interface traps by deconvolution of Si$_{2s}$. *Curr. Appl. Phys.* **18**, 1546–1552 (2018).

70. Latrach, S. *et al.* Trap states analysis in AlGaN/AlN/GaN and InAlN/AlN/GaN high electron mobility transistors. *Curr. Appl. Phys.* **17**, 1601–1608 (2017).

71. Jia, K. *et al.* Transient Current Correlation based Protection for DC Distribution System. *IEEE Trans. Ind. Electron* 1–1 (2019).

72. Urcuyo, R. *et al.* High Performance Graphene-Oxide-Metal Diode through Bias-Induced Barrier Height Modulation. *Adv. Electron. Mater.* **2**, 1600223 (2016).

73. Padovani, A. *et al.* A Sensitivity Map-Based Approach to Profile Defects in MIM Capacitors From I-V, C-V, and G-V Measurements. *IEEE Trans. Electron Devices* **66**, 1892–1898 (2019).

74. Jabbar, S. *et al.* Effect of Ag and Ti electrodes on capacitance tunability of oxygen-deficient SrTiO$_3$ based MIM varactors prepared by plasma sputtering. *Mater. Res. Express* **4**, 046401 (2017).

75. Lee, J. *et al.* Vertical Transport Control of Electrical Charge Carriers in Insulator/Oxide Semiconductor Hetero-structure. *Sci. Rep.* **8**, 5643 (2018).

76. Lee, D. *et al.* Verification of Charge Transfer in Metal-Insulator-Oxide Semiconductor Diodes via Defect Engineering of Insulator. *Sci. Rep.* **9**, 10323 (2019).

77. Siao, M. D. *et al.* Two-dimensional electronic transport and surface electron accumulation in MoS$_2$. *Nat. Commun.* **9**, 1442 (2018).

78. Wei, Z. & Eriguchi, K. Analytic Modeling for Nanoscale Resistive Filament Variation in ReRAM With Stochastic Differential Equation. *IEEE Trans. Electron Devices* **64**, 2201–2206 (2017).

79. Feng, Z. *et al.* Fluorination-Enabled Monolithic Integration of Enhancement- and Depletion-Mode Indium-Gallium-Zinc Oxide TFTs. *IEEE Electron Device Lett.* **39**, 692–695 (2018).

80. Xu, H. *et al.* Low-Power Transparent RFID Circuits Using Enhancement/Depletion Logic Gates Based on Deuterium-Treated ZnO TFTs. *IEEE Electron Device Lett.* **38**, 1383–1386 (2017).

81. Al-Mamun, M. *et al.* Impact of the Heat Conductivity of the Inert Electrode on ReRAM Performance and Endurance. *ECS Trans.* **85**, 207–212 (2018).

82. Ueba, H. *et al.* Action spectra associated with inelastic two-electron tunneling through a single molecule: Propene on Cu(211). *Surf. Sci.* **678**, 206–214 (2018).

83. Liu, S., Wolf, M. & Kumagai, T. Plasmon-Assisted Resonant Electron Tunneling in a Scanning Tunneling Microscope Junction. *Phys. Rev. Lett.* **121**, 226802 (2018).

84. Tang, K. *et al.* Interface Defect Hydrogen Depassivation and Capacitance-Voltage Hysteresis of Al$_2$O$_3$/InGaAs Gate Stacks. *ACS Appl. Mater. Interfaces* **9**, 7819–7825 (2017).

85. Zhang, J. W. *et al.* Two-peak capacitance-voltage behavior in devices based on electron transport materials. *Org. Electron.* **28**, 239–243 (2016).

86. Pham, T. T. *et al.* Deep depletion concept for diamond MOSFET. *Appl. Phys. Lett.* **111**, 173503 (2017).

87. Chaganti, V. R. S. K. *et al.* Demonstration of a Depletion-Mode SrSnO$_3$ n-Channel MESFET. *IEEE Electron Device Lett.* **39**, 1381–1384 (2018).

88. Vais, A. *et al.* A New Quality Metric for III-V/High-k MOS Gate Stacks Based on the Frequency Dispersion of Accumulation Capacitance and the CET. *IEEE Electron Device Lett.* **38**, 318–321 (2017).

89. Naitou, Y. Carrier accumulation and depletion in point-contact capacitance-voltage measurements. *AIP Adv.* **7**, 115218 (2017).

Acknowledgements

Author contributions

K.-J. Heo and H.-S. Kim wrote the main manuscript text. J.-Y. Lee organized the data and drew figures. All authors reviewed the results and implications and commented on the manuscript at all stages. The project was guided by S.-J. Kim.

Competing interests

The authors declare no competing interests.

Additional information

Correspondence and requests for materials should be addressed to S.-J.K.

Reprints and permissions information is available at www.nature.com/reprints.

Publisher's note Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.