Purdue University
Purdue e-Pubs

Open Access Theses | Theses and Dissertations

2013

Finfet Device Optimization at 15NM for Near-threshold Operation

Jolene Singh
Purdue University, jolenesingh@gmail.com

Follow this and additional works at: https://docs.lib.purdue.edu/open_access_theses

Part of the Electrical and Computer Engineering Commons

Recommended Citation

Singh, Jolene, "Finfet Device Optimization at 15NM for Near-threshold Operation" (2013). *Open Access Theses*. 72.
https://docs.lib.purdue.edu/open_access_theses/72

This document has been made available through Purdue e-Pubs, a service of the Purdue University Libraries. Please contact epubs@purdue.edu for additional information.

Graduate School ETD Form 9
(Revised 12/07)

PURDUE UNIVERSITY
GRADUATE SCHOOL
Thesis/Dissertation Acceptance

This is to certify that the thesis/dissertation prepared

By Jolene Singh

Entitled
Finfet Device Optimization at 15NM for Near-threshold Operation

For the degree of Master of Science in Electrical and Computer Engineering

Is approved by the final examining committee:

KAUSHIK ROY
Chair

BYUNGHOO JUNG

MICHAEL D. ZOLTOWSKI

To the best of my knowledge and as understood by the student in the *Research Integrity and Copyright Disclaimer (Graduate School Form 20)*, this thesis/dissertation adheres to the provisions of Purdue University's "Policy on Integrity in Research" and the use of copyrighted material.

Approved by Major Professor(s): KAUSHIK ROY

Approved by: V. Balakrishnan 04-17-2013
Head of the Graduate Program Date

FINFET DEVICE OPTIMIZATION AT 15NM FOR NEAR-THRESHOLD OPERATION

A Thesis

Submitted to the Faculty

of

Purdue University

by

Jolene Singh

In Partial Fulfillment of the

Requirements for the Degree

of

Master of Science in Electrical and Computer Engineering

May 2013

Purdue University

West Lafayette, Indiana

Dedicated to my family, Brig (Retd.) Mohan Singh Gujral, Mrs. Suninder Kaur, Gurmeet Singh Gujral and Manraj Singh Gujral.

ACKNOWLEDGEMENTS

I would like to thank Prof. Kaushik Roy for giving me this learning opportunity under his guidance. I truly appreciate his efforts to ease my fear and inhibitions towards research and giving me direction on how to work on a problem. Through this thesis, I have learnt so much more than just the subject of my research.

I would also like to thank so many of my fellow researchers for helping me along during different stages of this thesis. I would like to thank Dr. Sumeet Gupta for helping me learn the tools and simulate my first FinFET. I am also very thankful to Sri Harsha Choday for helping me resolve convergence issues with my scripts and truly being available for each and every question I had. I would like to thank Arun Akkala and Karthik Yogendra for helping me understand the scripts and models used in earlier studies. I would also like to thank Selin Mungan for being my go-to person for all questions regarding Sentaurus.

There are many people who were not directly involved with this work, but who worked extra hard to work around my schedule in other aspects of my life to help me accommodate maximum time for my thesis. I am truly grateful to Donald E. Brier, my supervisor at Graduate School, who readjusted the timelines for his project around my

availability and had so much faith in my capabilities that he gave me full freedom to work as and when I like, so that I could confidently give enough time for both my thesis and my job.

TABLE OF CONTENTS

Page

LIST OF TABLES vii
LIST OF FIGURES viii
LIST OF ABBREVIATIONS xi
ABSTRACT xii
1. INTRODUCTION 1
 1.1 Current in an FET 1
 1.2 Delay 2
 1.3 Energy curves 3
 1.4 Near threshold computing (NTC) 6
2. FINFET DEVICE DESIGN 7
 2.1 FinFET Parameter Variables 8
 2.2 Parameter Sweep 9
 2.3 Simulation Framework 10
3. DEVICE PARAMETER VARIATION 12
 3.1 Oxide Thickness Variation 12
  3.1.1 Superthreshold parameter selection 13
  3.1.2 Near-threshold parameter selection 16
 3.2 Spacer Width Variation 18
  3.2.1 Superthreshold parameter selection 19
  3.2.2 Near-threshold parameter selection 21
 3.3 Fin thickness variation 23
  3.3.1 Volume Inversion 23
  3.3.2 Super-threshold parameter selection 26
  3.3.3 Near-threshold parameter selection 30
 3.4 Source/Drain Extension Variation 32
  3.4.1 Superthreshold parameter selection 32

Page

3.4.2 Near-threshold parameter selection 34

3.5 Source/Drain Doping Variation... 36

3.5.1 Superthreshold parameter selection 36

3.5.2 Near-threshold parameter selection 38

4. FINAL RESULTS 41
5. CONCLUSION 44
5.1 Take-away points 44

LIST OF REFERENCES 45
A. SENTAURUS STRUCTURE EDITOR CODE... 47
B. SENTAURUS DEVICE CODE – CG PLOT 52
C. SENTAURUS DEVICE CODE – IV PLOT... 60

LIST OF TABLES

Table Page

1.1 Drain current for FET 1

2.1 Parameter Variation value-set 10

3.1 Optimized device parameters -Tox 17

3.2 Optimized device parameters -Tsp 22

3.3 Optimized device parameters - Tsi 31

3.4 Optimized device parameters -Text 35

3.5 Optimized device parameters –S/D Doping 40

4.1 Optimized device parameters 41

4.2 Results – Tsi=7nm 42

4.3 Results – Tsi=5nm 43

LIST OF FIGURES

Figure Page

1.1 Id (orange) and ln(Id) versus Vgs [13] 2

1.2 NFET with a capacitive load........ 3

1.3 Inverter........ 4

1.4 Energy curves for 45nm MOSFET (50 stage inverter)........ 5

2.1 3D FinFET [Source: cadence.com]........ 7

2.2 MOSFET cross-section [Source: University of Cambridge]........ 7

2.3 FinFET crosssection........ 8

2.4 Simulation Framework........ 11

3.1 Currents versus oxide thickness........ 13

3.2 Gate capacitance and delay versus Tox at VDD=1V........ 14

3.3 Gate leakage versus oxide thickness........ 15

3.4 Energy curves for oxide thickness variation........ 16

3.5 Subthreshold characteristics for oxide thickness variation........ 17

3.6 Capacitance components........ 18

3.7 Increase in Energy barrier with spacer........ 19

3.8 Gate capacitance and gate current versus spacer thickness........ 19

3.9 On current and off current versus spacer thickness........ 20

3.10 Delay versus spacer thickness........ 20

Page

3.11 Energy curves for spacer thickness variation ... 21

3.12 Subthreshold characteristics for spacer thickness variation ... 22

3.13 An example of band bending in Double Gate FET ... 23

3.14 Volume Inversion (a) ... 24

3.15 Volume Inversion(b) ... 25

3.16 Band Bending of DGMOS for different body thicknesses ... 25

3.17 Gate capacitance and gate leakage versus fin thickness ... 26

3.18 On current and off current versus fin thickness ... 26

3.19 Delay versus fin thickness ... 27

3.20 Quantum confinement ... 28

3.21 Ultra thin body (UTB) ... 29

3.22 Inversion Carrier Distribution ... 29

3.23 Energy curves for fin thickness variation ... 30

3.24 Subthreshold characteristics for fin thickness variation ... 30

3.25 Gate capacitance and gate current versus extension thickness ... 32

3.26 FinFET ... 32

3.27 On current and off current versus extension thickness ... 33

3.28 Delay versus extension thickness ... 34

3.29 Energy curves for extension thickness variation ... 34

3.30 Subthreshold characteristics for Text variation ... 35

3.31 Gate capacitance versus doping ... 36

3.32 On current versus doping ... 37

Page

3.33 Delay versus doping 37

3.34 Energy curves for doping variation 38

3.35 Gate capacitance versus doping at VDD=0.45V 39

3.36 Subthreshold characteristics for Doping variation 39

4.1 Energy Curves 42

LIST OF ABBREVIATIONS

Cds	Drain to Source Capacitance
Cg	Gate Capacitance
CV Characteristics	Capacitance-Voltage Characteristics
Edyn	Dynamic Energy
Eleak	Leakage Energy
Etotal	Total Energy
FET	Field Effect Transistor
FinFET	Fin Field Effect Transistor
Ioff	Off Current
Ion	On Current
IV Characteristics	Current-Voltage Characteristics
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
Text	Extension Thickness
Tox	Oxide Thickness
Tsi	Fin Thickness
Tsp	Spacer Thickness
VDD	Supply voltage

ABSTRACT

Singh, Jolene. M.S.E.C.E., Purdue University, May 2013. FinFET Device Optimization at 15nm for Near-threshold Operation. Major Professor: Kaushik Roy.

Much of the current research in the electronic industry focuses on reducing power consumption of digital circuits. Towards the same many attempts are being made to reduce the operating voltage of the circuits. It has been shown through device and circuit analysis that a circuit consumes minimum energy when operated near threshold voltage. In this thesis I vary device parameters and study their effects on energy consumption and delay of the device for the two regions of operation – superthreshold and near-threshold, using LUTs of IV and CV characteristics, verilogA and hSpice. Finally, device parameters are obtained for an optimum superthreshold optimized device which acts as the baseline device, and for a near-threshold optimized device. The savings in energy are calculated when near-threshold optimized devices are used instead of baseline devices for circuits that are being operated near threshold voltage.

1. INTRODUCTION

For circuit applications which need to consume less energy, for instance, portable battery-operated devices, a lot of research is being conducted to understand the parameters which contribute to total energy consumed and incorporate designs to reduce energy consumption of the circuit. Let us first look at different components of energy in a circuit and their relationships to the total energy and operating voltage.

1.1 Current in an FET

For a field effect transistor, the drain current can be related to gate voltage by the following relationships:

Table 1.1 Drain current for FET

1.	**V_G < V_{th}**	$I_d = I_0 e^{\frac{V_{GS}}{m v_T}}\left(1 - e^{\frac{-V_{DS}}{n v_T}}\right)$
2.	**V_G > V_{th} and V_{DS} < (V_{GS} – V_{th})**	$I_d = K' \frac{W}{L}\left[(V_{GS} - V_{Th})V_{DS} - \frac{V_{DS}^2}{2}\right](1 + \lambda V_{DS})$
3.	**V_G > V_{th} and V_{DS} > (V_{GS} – V_{th})**	$I_d = \frac{1}{2} K' \frac{W}{L}(V_{GS} - V_{Th})^2(1 + \lambda V_{DS})$

where ‘m’ represents the fraction of voltage drop across the gate oxide, ‘n’ is a device fitting parameter, ‘v_T’ is thermal voltage (it is the same as kT/q) and λ is the DIBL factor. K’ is a constant equaling μC_{ox}, where μ is the mobility of major charge carriers and C_{ox} is the oxide capacitance.

Equation 1 is for subthreshold current of a transistor. Equation 2 corresponds to Linear region of superthreshold current while equation 3 is for Saturation region of superthreshold current. As we can see, drain current is a polynomial function of gate voltage when gate voltage is above threshold voltage. This relationship becomes an exponential function when gate voltage reduces below threshold voltage.

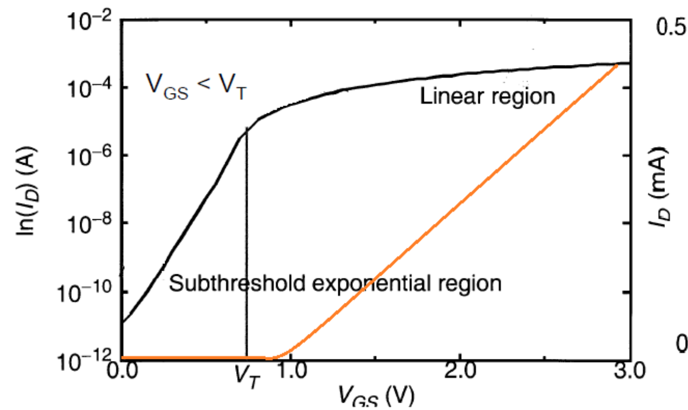

Figure 1.1 Id (orange) and ln(Id) versus Vgs [13]

Figure 1.1 shows Id-Vgs characteristics of an NFET with a threshold voltage of 0.75V. The orange curve plots drain current on a linear scale while black curve plots drain current on a logarithmic scale. On a linear scale, the characteristics look much like that of a diode. We can see the exponential nature of current below threshold voltage on the logarithmic plot.

1.2 Delay

Now, let us see how current affects delay through a circuit. From the definition of current, we can write delay as

$$Delay, \Delta t = \frac{Q}{I} \tag{1}$$

Consider the following NFET

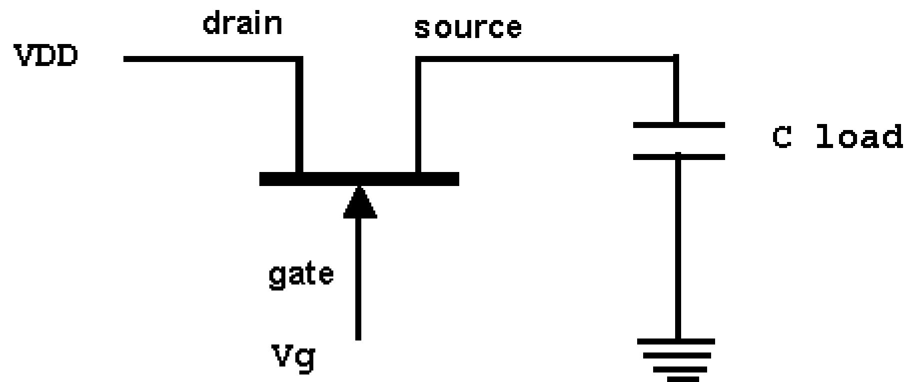

Figure 1.2 NFET with a capacitive load

The charge stored on capacitor, Q = CV. For most digital circuits the gate of the subsequent stages acts as a capacitive load along with a load capacitor that may be used at the output. Therefore, delay can be re-written as

$$Delay, \Delta t = \frac{CV}{I} \tag{2}$$

Thus, as operating voltage is reduced, or V_{GS} is reduced, delay initially increases linearly as current reduces linearly (approximately, actual relationship is polynomial in nature). After threshold voltage (as operating voltage continues to decrease), current starts to reduce exponentially, causing an exponential increase in delay.

1.3 Energy curves

Consider a simple inverter

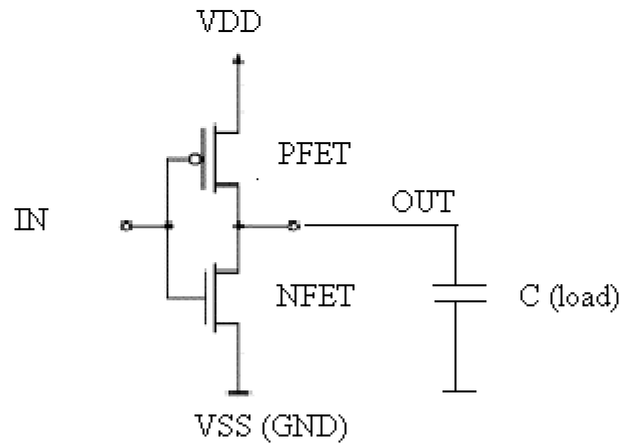

Figure 1.3 Inverter

For any circuit, there are two components of energy – leakage energy and dynamic energy. Dynamic energy is the energy consumed every time the output switches. For an ideal inverter this is equal to CV^2, corresponding to the energy that is consumed from the supply when the output changes from 0 to 1.

Leakage energy is the energy consumed by continuous flow of leakage current from VDD to VSS. The key factor to note here is that leakage energy is also a function of frequency or delay of the circuit, while dynamic energy is purely a function of the operating voltage.

$$Dynamic\ energy = \alpha CV^2 \quad (3)$$

$$Leakage\ energy = VI_{leak} \times delay \quad (4)$$

where, α is the activity factor (<1) indicating the fraction of cycles when the output switches. This relationship of dynamic energy and leakage energy is shown in the figure below:

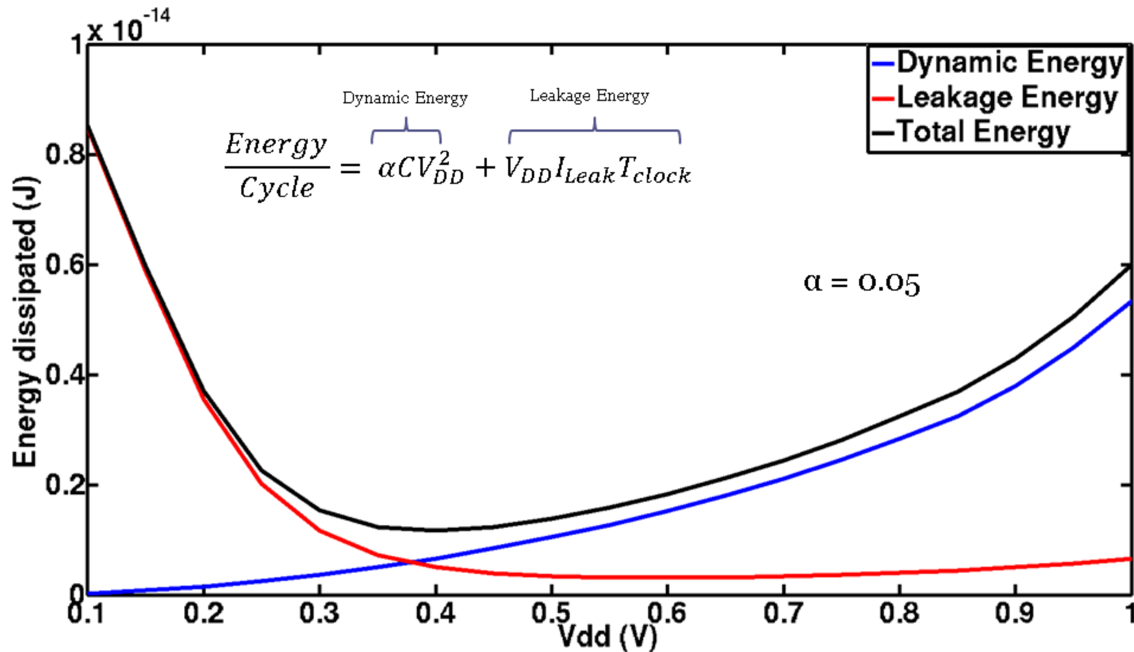

Figure 1.4 Energy curves for 45nm MOSFET (50 stage inverter)

Dynamic energy (blue) is a quadratic function of operating voltage and increases monotonously as operating voltage is increased. Leakage energy (red) initially increases linearly as operating voltage is reduced from VDD=1V to threshold voltage of 0.35V. This linear increase in delay is mainly due to a linear decrease in drain current as voltage is reduced. However, below threshold voltage, drain current reduces exponentially, causing the delay and subsequently, the leakage energy, to increase exponentially.

If we were to observe the total energy in a circuit (sum of dynamic energy and leakage energy), as shown by the black curve, we see a decrease in total energy as operating voltage is reduced till threshold voltage. After threshold voltage, total energy starts to increase again. This curve indicates that to consume least energy, a circuit should be operated at the minimum energy point. This minimum energy point is of great interest to circuit designers. A point to bear in mind is that this minimum energy voltage is a

function of the logic depth of the circuit (a factor which is not easily noticeable in the figure). In the figure above, a chain of 50 inverters with a fan-out of 1 has been used. If the number of inverter stages is decreased, the minimum energy point will shift to the left as delay (and thus, the leakage energy) will reduce.

1.4 Near threshold computing (NTC)

For a sufficiently large logic depth, the minimum energy point for a circuit lies around the threshold voltage of the FETs. This is why reducing operating voltage of a circuit near to its threshold voltage is an idea that we would like to look into to reduce the operating energy of the circuit.

The question that arises is that as we already have a device optimized for superthreshold operation, do we need to re-optimize the device for near-threshold voltage? As we shall see at the end of this thesis, a device optimized for superthreshold operation is not the most optimum choice for near-threshold operation for least energy. A superthreshold optimized device is optimized for maximum performance, while a near-threshold optimized device is optimized for least energy. The device parameter value-set required for the two regions/requirements are different. We shall show that not only do we need to optimize the device for near-threshold region, the parameter value-set is mutually exclusive. This means that a device optimized for near-threshold region is not optimum for superthreshold region even in terms of energy and vice versa.

2. FINFET DEVICE DESIGN

Unlike planar MOSFETs, FinFET is a 3D Field Effect Transistor. The channel is grown like a fin on top of oxide and is wrapped by gate on two sides. A 3D view of FinFET is shown below.

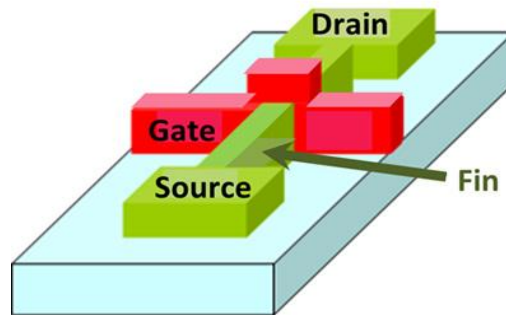

Figure 2.1 3D FinFET [Source: cadence.com]

Due to two gates, a FinFET has better channel control than a planar MOSFET. The real need for a new device structure emerged when the scaling limits of MOSFETs (shown below) were realized due to parasitic body effects and poor channel control.

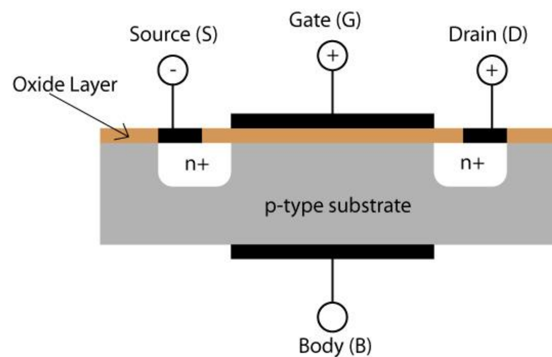

Figure 2.2 MOSFET cross-section [Source: University of Cambridge]

A FinFET can be designed to have both gates tied together or act as independent gates. Independent gates allow for better threshold voltage control through electrostatic interaction between the two gates. Symmetric tied gates offer more on current since both gates create an inversion layer once gate voltage exceeds threshold voltage. In our simulations, we have used a symmetric tied-gate FinFET. The channel in a FinFET is undoped/intrinsic. Since the volume of the channel is so small, it is very difficult to dope it accurately. For instance, in the current technology node, the gate length is 15nm, fin thickness is 5nm and fin height is 30nm. For a doping of 1e18/cm^3, we would need 2.25 dopants in the entire channel. An intrinsic channel gives better threshold control, an almost ideal subthreshold swing of about 60mV/dec and zero random dopant fluctuation. Thus, for a symmetric tied-gate FinFET, threshold voltage is controlled by the flatband voltage of the gate. For our analysis, we have used Aluminum, modified to have a mid-gap workfunction yielding a threshold voltage of 0.45V.

2.1 FinFET Parameter Variables

If we were to take a cross section of a FinFET, we would see a 2D view as shown below.

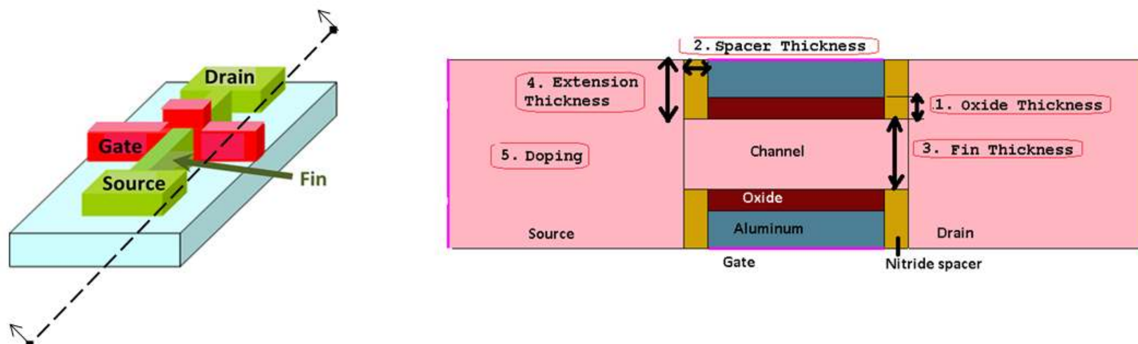

Figure 2.3 FinFET cross-section

Five physical parameters of the FinFET structure have been numbered in the figure. These are:

1. Oxide thickness
2. Spacer Thickness
3. Fin Thickness
4. Source/Drain Extension Thickness
5. Source/Drain Doping

We shall sweep these five parameters in a 1D space, i.e., while keeping other parameters constant and observe their effect on performance and energy for a chain of 25 inverters with a fan-out of 1. For each parameter, we shall select a value which is optimum for near-threshold operation and another value (could be same, as we shall see later) for optimum superthreshold operation. Finally, we will have a set of parameter values for superthreshold-optimized device and another set for near-threshold-optimized device. Using these parameter values, we shall simulate a chain of 25 inverters and calculate savings in energy when a near-threshold-optimized device is used instead of a superthreshold-optimized device when the operating voltage is reduced to the threshold voltage. We shall also calculate the increase in energy consumption when a near-threshold-optimized device is used in superthreshold region, indicating that the two parameter value sets are mutually exclusive, i.e., device optimized for one region is not suitable to be used in the other.

2.2 Parameter Sweep

The following table gives the values over which each parameter is varied.

Table 2.1 Parameter Variation value-set

Parameter	**Default Value SetA**	**Default Value SetB**	**Variation (Start:Step:End)**
Fin thickness (Tsi)	5nm	6nm	5nm : 1nm : 8nm
Source/Drain Extension (Text)	5nm	5nm	5nm : 1nm : 10nm
Spacer Width (Tsp)	2nm	2nm	1nm : 1nm : 6nm
Oxide Thickness (Tox)	1.8nm	1.8nm	1nm : 0.2nm : 2nm
Source/Drain Doping	1e20 / cm^3	1e18 / cm^3	1e^(15 : 1 : 20)
VDD	1V	Variable	0.1V : 0.05V : 1V

There are two columns for the default value for each parameter. As one parameter is being varied, since it is a 1D analysis, the other parameters have to be kept fixed. In this analysis, we chose two such default value sets. The choice for SetA and SetB default values was made solely for ease of convergence/simulation and does not affect the correctness of the analysis. As we had discussed previously, the objective of this analysis is to observe the trends in energy and delay for variation in each parameter one by one. These trends are unaffected by the default values chosen for other variables.

2.3 Simulation Framework

The following flowchart gives a pictorial view of the simulation framework. A simulation framework describes the layout of different tools and how data is transferred amongst them for extracting useful results.

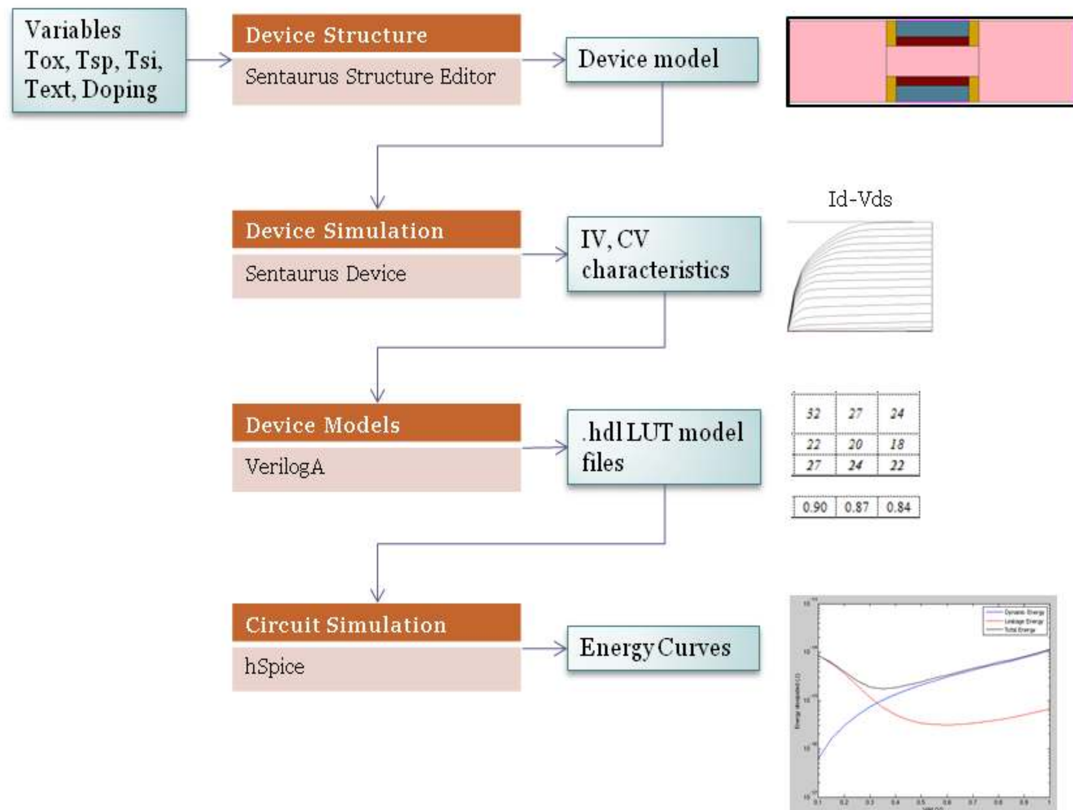

Figure 2.4 Simulation Framework

For each parameter, using Sentaurus Structure Editor, a device model file was created for each value in its sweep range. This structure model file was then used as an input to Sentaurus Device to generate IV and CV curves for the given FinFET. These IV and CV characteristics were reorganized into LUTs and were used through VerilogA for defining .hdl models for hSpice. Finally, the VerilogA .hdl models were used to simulate circuits in hSpice from which energy curves were plotted.

3. DEVICE PARAMETER VARIATION

Let us now begin to analyze the results for variation in each of the five selected parameters. In each figure you might notice the words “SetA” and “SetB”. Recall from section 2.2, these are the default value-sets for the five parameters. They’ve been mentioned on the figures for reference.

3.1 Oxide Thickness Variation

Oxide thickness variation changes the control of the applied gate voltage on the channel energy bands. The oxide acts as the insulating layer in an FET and is the major component of the gate capacitance above threshold voltage. As gate voltage is varied, the energy bands in the silicon moves along with the energy band in the metal, tied across the oxide. However, a thin oxide can lead to leakage due to very high electric field across the oxide. It can also lead to breakdown of the insulator. Let us now view the effect of change in oxide thickness on the device energy and performance.

3.1.1 Superthreshold parameter selection

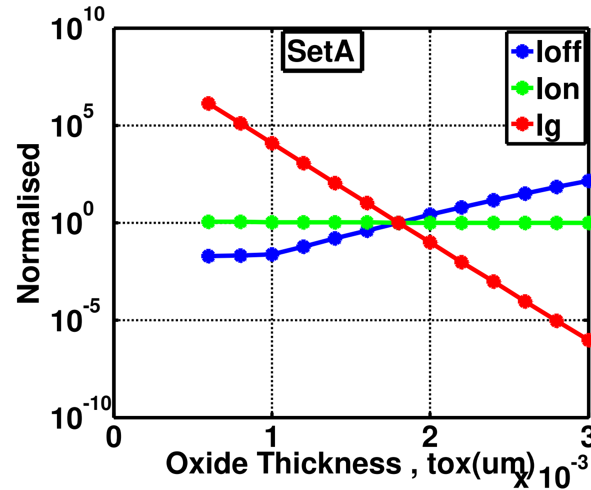

Figure 3.1 Currents versus oxide thickness

In this figure, on current, off current and gate leakage current have been plotted on a semi log graph. As can be observed, this is not an iso-Ioff analysis as iso-Ioff analysis requires that we vary threshold voltage or gate voltage to obtain values of on current and gate leakage for the same value of off current. In this analysis, however, we are keeping the threshold voltage constant. We observe that with increase in oxide thickness, the subthreshold leakage current increases exponentially. This increase in subthreshold current indicates a poorer channel control. This conforms with our intuitive understanding that a thinner oxide provides better channel control. In fact, a lot of research is being done to create high-k dielectrics so that oxide thickness can be further reduced. SiO_2, as the current oxide, results in extremely high tunneling leakage at low thickness and is susceptible to breakdown at high voltages. This increase in gate leakage is also shown in the figure above.

Let us now consider effect of oxide variation on delay.

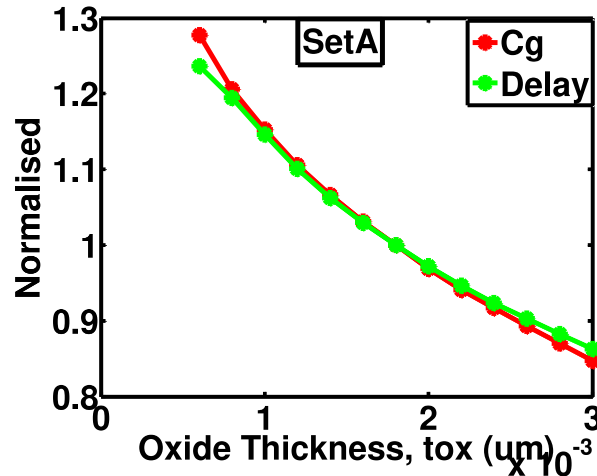

Figure 3.2 Gate capacitance and delay versus Tox at VDD=1V

Delay shows a 1:1 relationship with the gate capacitance. Gate capacitance is inversely related to oxide thickness (recall basic two plate capacitor, C=Aε /d). As this is not an iso-Ioff analysis, we see constant on current as oxide thickness is varied (conversely, in iso-Ioff analysis, we would see declining on current as oxide thickness is increased, which in turn can affect your results/graph for delay), and thus delay is directly affected only by gate capacitance. This trend suggests that increase in oxide thickness would be optimal for low delay. However, the main reason why we should be willing to accept increased subthreshold leakage is because of exponential decrease in gate leakage. The figure below shows how gate leakage scales when operating voltage is decreased.

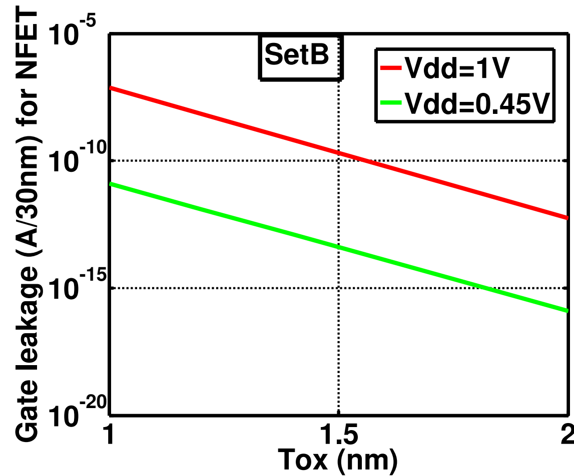

Figure 3.3 Gate leakage versus oxide thickness

For the same oxide thickness, gate leakage increases by a factor of ~1e4 as voltage is increased from 0.45V to 1V (vertical displacement). We can also rephrase this observation as follows, for the same gate leakage, as voltage is scaled down, oxide thickness can also be scaled down correspondingly. We shall look at near-threshold optimization in the next section. From this section, we shall bear in mind that gate leakage plays a very important role for oxide scaling and though a thinner oxide provides better channel control, at higher voltages we want to keep the oxide thick enough to reduce gate leakage.

3.1.2 Near-threshold parameter selection

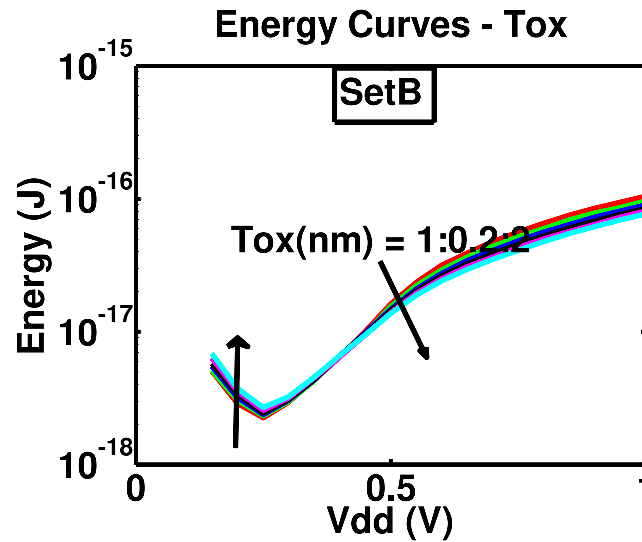

Figure 3.4 Energy curves for oxide thickness variation

Oxide thickness shows a cross-over point in its energy characteristics. A smaller oxide consumes lower energy at minimum energy point and is most optimal from energy perspective at low voltage. However, the characteristics cross over and smaller oxide ends up consuming maximum energy at higher voltages. This crossover point or more precisely, increase in energy at higher voltages is mainly due to high gate leakage for thinner oxides. Thus, from minimum energy point of view, we would like to reduce our oxide thickness provided our operating voltage is low enough to be on the left side of the crossover point.

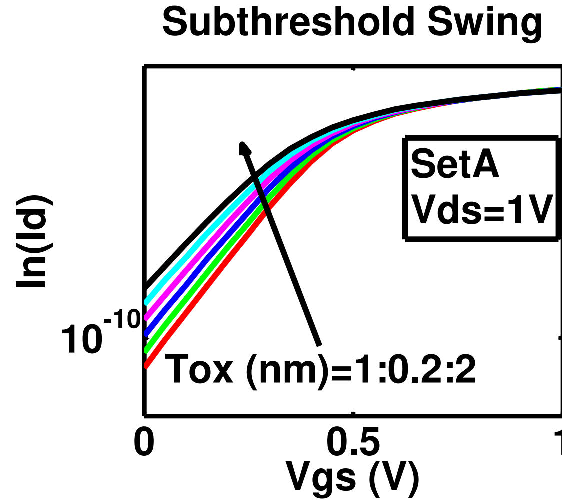

Figure 3.5 Subthreshold characteristics for oxide thickness variation

A smaller oxide provides better channel control. A better channel control means that the energy band bending in the channel on the inside of the gate oxide is tightly coupled to the energy bands of the gate contact. A smaller subthreshold swing (given in units of mV/dec) implies that a smaller change in gate voltage is needed to increase drain current by the same factor, which is a desirable quality for subthreshold circuits.

Thus, for near threshold operation we would like to reduce our oxide thickness for two very important reasons – firstly, it provides a better subthreshold swing, secondly it gives us the minimum energy point. For superthreshold operation however, we will have to increase our oxide thickness to keep gate leakage in control. We also observed improvement in delay at thicker oxides due to reduction in gate capacitance.

Table 3.1 Optimized device parameters -Tox

	Lg	S/D Doping	Text	Tox	Tsi	Tsp	Vthn	Vthp
Super-th.	15nm			2nm			0.45V	0.45V
Near-th.	15nm			1nm			0.45V	0.45V

3.2 Spacer Width Variation

Spacers introduce an underlap in the channel. Consider a planar MOSFET figure shown below which highlights all the parasitic capacitances in an NFET.

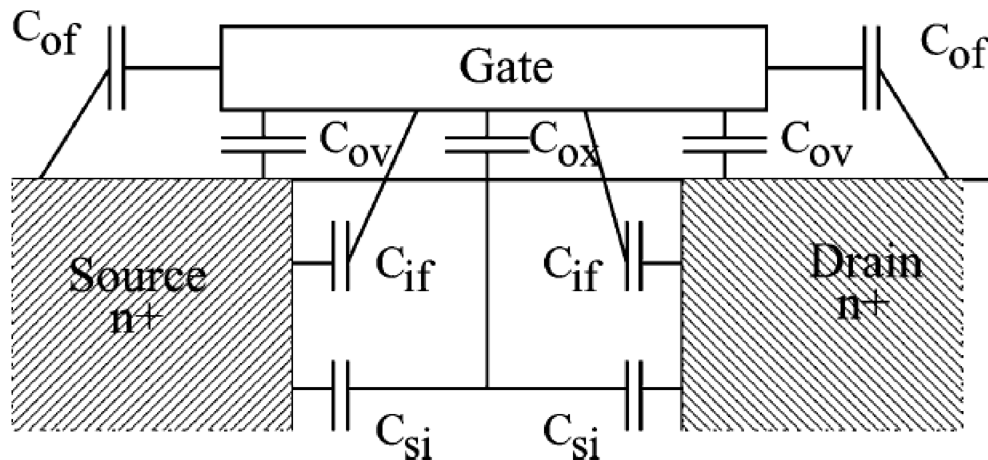

Figure 3.6 Capacitance components. [3]

An underlap occurs when the Source and Drain do not lie under the gate; in fact, a portion of channel lies outside the physical length of the gate. As source and drain move further apart keeping the gate length constant,

1. the effective channel length increases
2. fringe capacitance reduces due to a thicker spacer
3. overlap capacitance reduces

Effects 2 and 3 above can be seen by the trends in gate capacitance with increasing spacer thickness. Effect 1 above along with change in energy bands (refer figure below) causes a drop in on current as spacer thickness is increased.

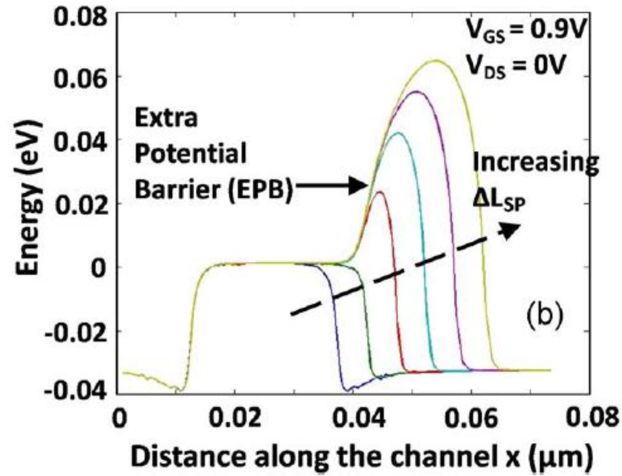

Figure 3.7 Increase in Energy barrier with spacer. [14]

Let us now see the effect of spacer thickness on our FinFET.

3.2.1 Superthreshold parameter selection

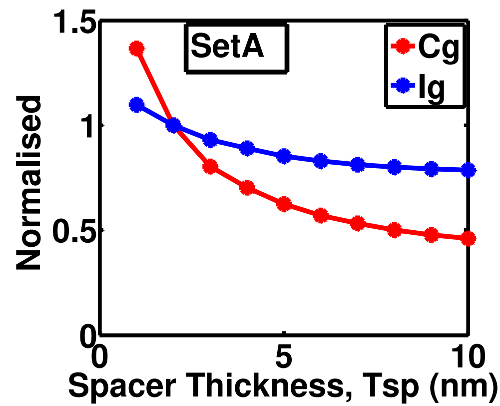

Figure 3.8 Gate capacitance and gate current versus spacer thickness

The figure above shows the trends for gate leakage and gate capacitance as spacer thickness is varied. We can notice that as spacer thickness is increased, initially gate capacitance decreases rapidly after which the rate of decrease decays and eventually gate

capacitance is almost constant. This trend of gate capacitance plays an important role in affecting the delay through the circuit.

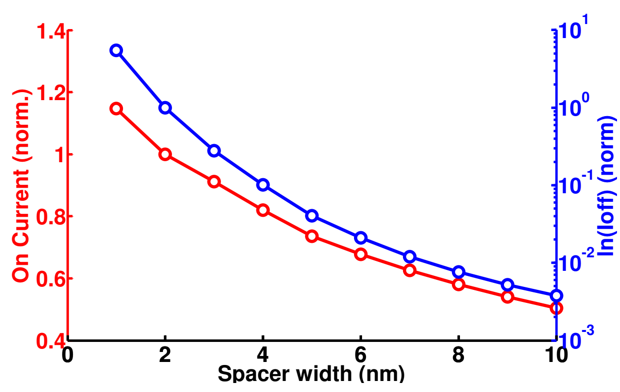

Figure 3.9 On current and off current versus spacer thickness

As described earlier, on current reduces as spacer thickness is increased. There is also an exponential decrease in leakage current. The leakage current is largely affected by the increased energy bump due to spacers.

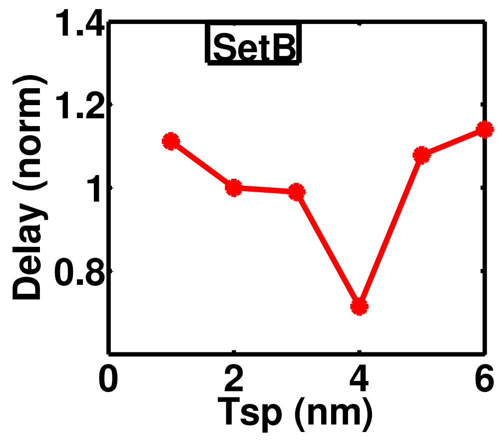

Figure 3.10 Delay versus spacer thickness

Delay is being affected by both gate capacitance and on current. Initially, as spacer thickness is increased, gate capacitance reduces by a larger margin as compared to the decrease in on current, because of which we actually see an improvement in delay. Eventually, decrease in gate capacitance saturates as on current continues to decrease, causing the delay to finally catch up and start increasing. This is why we see a U- shaped curve for delay. Thus, when optimizing for least delay for superthreshold operation, we should look for an optimum value of spacer thickness for which we obtain least delay. In our analysis, it appears to be around 4nm.

3.2.2 Near-threshold parameter selection

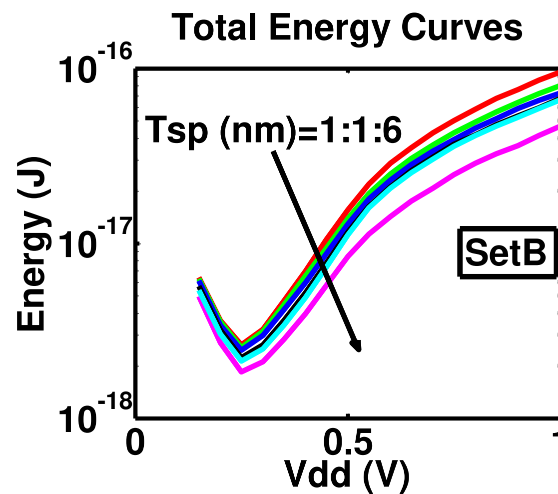

Figure 3.11 Energy curves for spacer thickness variation

From energy perspective, both leakage current and load capacitance decrease as spacer thickness is increased, causing an overall decrease in total energy. Thus, for near-threshold operation, a thicker spacer is better for least energy.

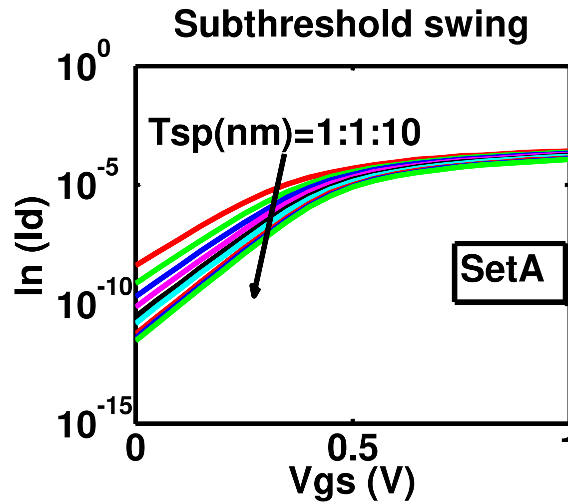

Figure 3.12 Subthreshold characteristics for spacer thickness variation

We had observed in figure 3.9 that on current reduces linearly while leakage current reduces exponentially as spacer thickness is reduced. This means, our Ion/Ioff ratio is improving as spacer thickness is increased. This is essentially, what we see in figure 3.12. Subthreshold swing improves as spacer thickness is increased. As mentioned earlier, smaller subthreshold swing is better because we can observe large gain in current for the same increase in gate voltage.

Thus, for near-threshold optimization, increase in spacer thickness appears to be an out-and-out choice.

Table 3.2 Optimized device parameters -Tsp

	Lg	S/D Doping	Text	Tox	Tsi	Tsp	Vthn	Vthp
Super-th.	15nm			2nm		4nm	0.45V	0.45V
Near-th.	15nm			1nm		6nm	0.45V	0.45V

3.3 Fin thickness variation

As fin thickness is varied, we are essentially increasing the volume of the channel. When the thickness of the film is large enough, the two gates' depletion regions do not interact and the FinFET acts as two parallel transistors. As fin thickness continues to reduce, the depletion regions merge and we essentially have a fully depleted channel. Volume inversion in thin channel leads to increase in the number of charge carriers as the energy bands across the width of the channel move in accordance with the gate voltage. Before we proceed further, we should revise the concept of "volume inversion".

3.3.1 Volume Inversion

Taking example of an NFET, when a positive gate voltage is applied, the energy bands on the metal side of the oxide get pulled down. Coupled with this, the energy bands in the channel also bend near the oxide.

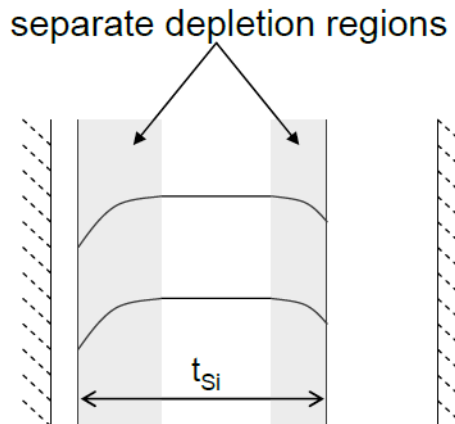

Figure 3.13 An example of band bending in Double Gate FET [11]

If the fin thickness is small enough, for an undoped channel, the band doesn't just bend near the oxides; the entire bulk of the channel gets pulled down. For instance, in the

figure below, the dotted line represents the conduction band in unbiased state. When positive gate voltage is applied, the entire energy band gets pulled down. This is known as “volume inversion”.

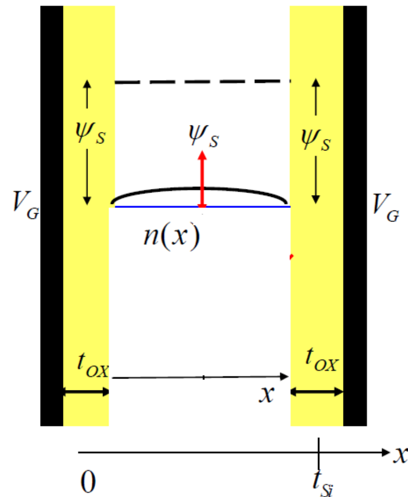

Figure 3.14 Volume Inversion (a) [11]

For volume inversion, the fin thickness should satisfy the relationship

$$t_{Si} \ll \sqrt{\frac{8\varepsilon_{Si}k_BT}{q^2N_A}} \tag{5}$$

where for an intrinsic channel N_A is approximately 1e15/cm^3 and RHS is approximately $2\sqrt{2} \times 130nm$. At such low fin thickness, at threshold voltage the band structure looks as shown below. In the figure below, if equation 5 was satisfied then $\Delta\psi \ll k_BT/q$ and charge density is fairly constant across the entire thickness of the fin.

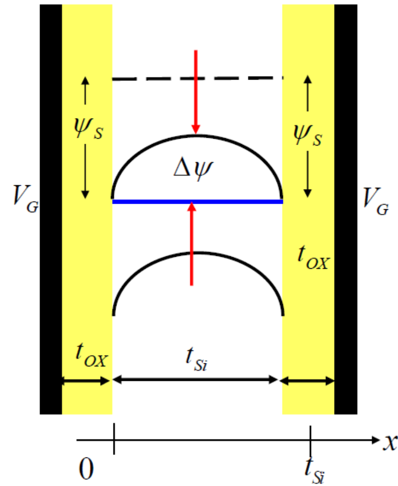

Figure 3.15 Volume Inversion (b) [11]

The following figure gives a fair comparison of band bending for different fin thicknesses.

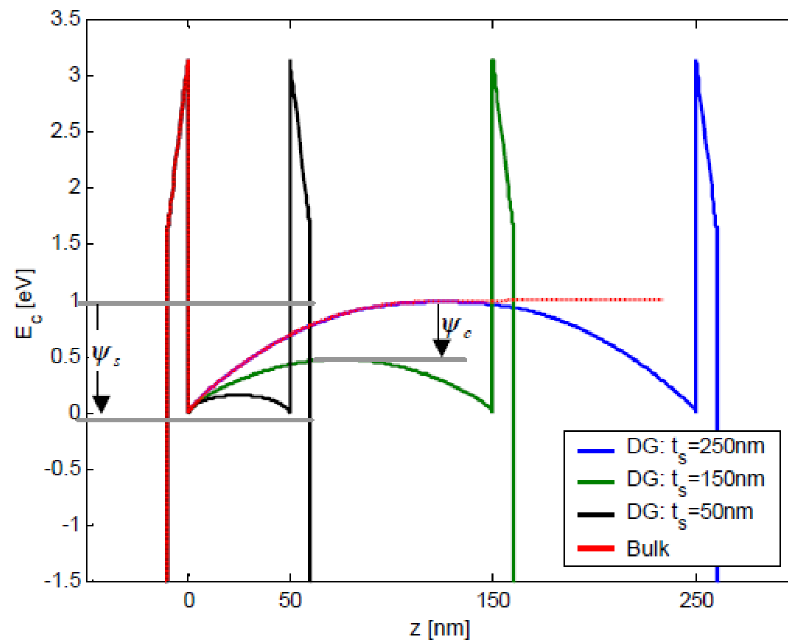

Fig. 14. Band-diagram of DGMOS capacitors of different body thickness at same V_G. Also shown the band diagram of bulk MOSC (red-dashed line). t_{ox} = 10nm, N_A = 1.E17 cm^{-3}, V_G = 1.5v. Classical mode calculation.

Figure 3.16 Band Bending of DGMOS for different body thicknesses [12]

Volume inversion effectively increases the number of carriers in the channel. The instance at which the conduction band of the channel gets pulled down to the conduction band of Source/Drain, we move from subthreshold region to superthreshold region. After this point, we may observe a slight more bending near the oxide surface. Eventually we will have charge sheets under the oxide on both gates which will act as conduction channels.

3.3.2 Super-threshold parameter selection

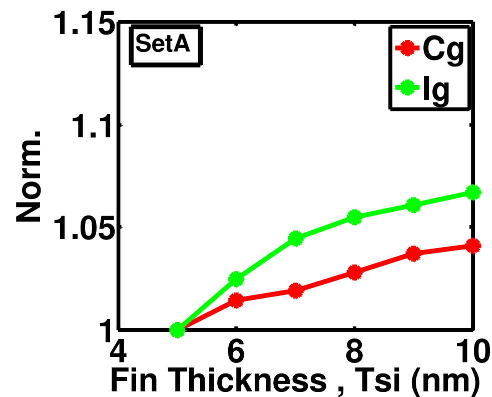

Figure 3.17 Gate capacitance and gate leakage versus fin thickness

Fin thickness does not affect gate capacitance much. Gate capacitance is still primarily a function of oxide and spacer thickness.

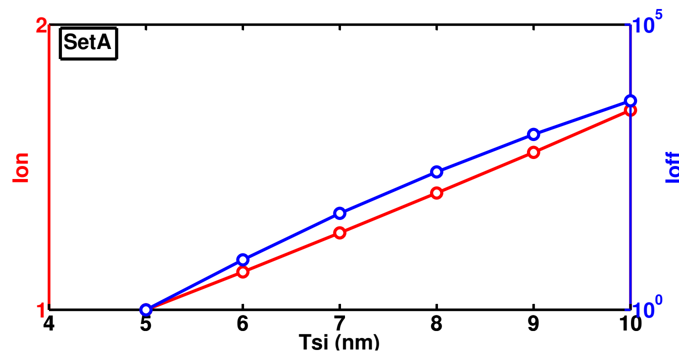

Figure 3.18 On current and off current versus fin thickness

Based on our discussion on volume inversion, we can understand the characteristics shown in the figure above. Subthreshold current increases exponentially as fin thickness is increased due to volume inversion. Similarly, on current increases due to greater charge density.

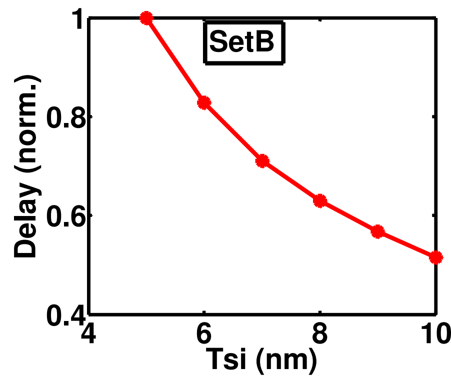

Figure 3.19 Delay versus fin thickness

Delay is a function of both gate capacitance and on current. From the previous two figures, we noted that only on current increases a little with increase in fin thickness which gets proportionately translated to decrease in delay with increase in fin thickness. This trend would suggest that we should increase our fin thickness for lesser delay. However, we must take into consideration the exponential increase in off current too, which makes the Ion/Ioff ratio worse. Most device engineers recommend a thinner fin for better channel control (recall, a better channel control is essentially a better Ion/Ioff ratio). These are two contradictory requirements for superthreshold optimization. We shall at the end of the thesis observe the savings in energy for a minimum fin thickness and for a thicker fin (thicker fin leads to lower delay as seen in the figure above).

One may wonder at this point, if we can go below 5nm fin thickness. Below 5nm we observe quantum confinement effects which shift the centroid of the charge density to the center of the fin.

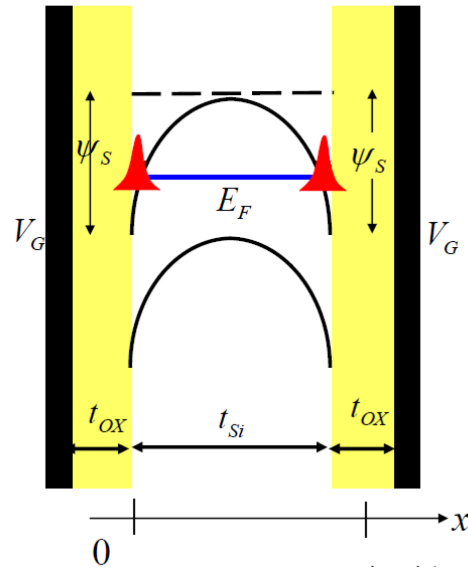

Figure 3.20 Quantum confinement [11]

Essentially in a fully depleted thin body FinFET, the band and the oxide form a quantum well. The actual charge sheet lies a small distance away from the physical oxide layer. When fin thickness is reduced below 5nm, this distance from the oxide is considerable enough to couple the two inversion layers and move the centroid of the charge sheet to the middle of the fin as shown below:

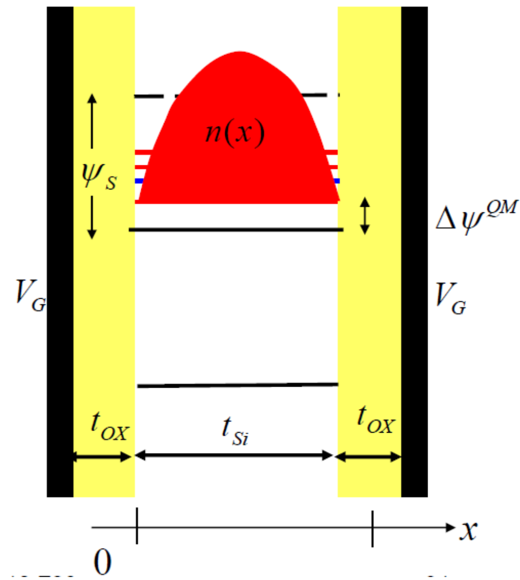

Figure 3.21 Ultra-thin body (UTB) [11]

The following figure shows how the carrier distribution shifts inside a UTB.

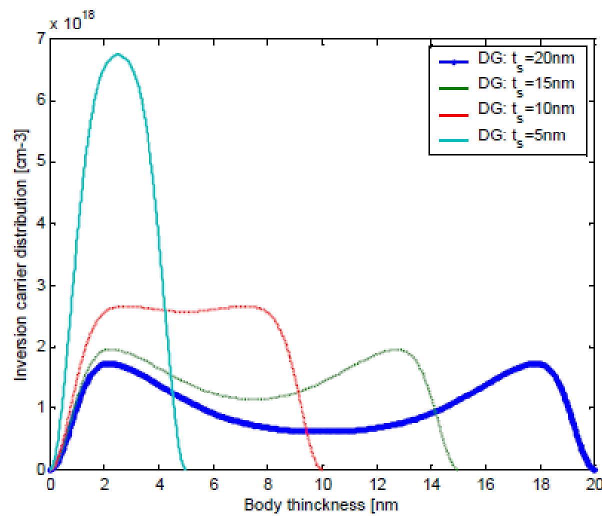

Fig. 20. Inversion carrier distribution inside the DGMOSC, for various body thickness, with t_{ox}=10nm, N_a=1.E17cm-3, V_G = 0.5v.

Figure 3.22 Inversion Carrier Distribution [12]

Below 5nm fin thickness, the analysis has to change to account for these effects.

3.3.3 Near-threshold parameter selection

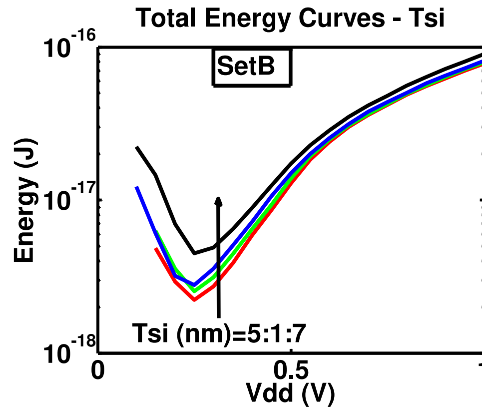

Figure 3.23 Energy curves for fin thickness variation

A thinner fin gives lower energy at minimum energy points. This can mainly be attributed to improvement in leakage energy. As we had discussed earlier, due to volume inversion, leakage current increases exponentially as fin thickness is increased.

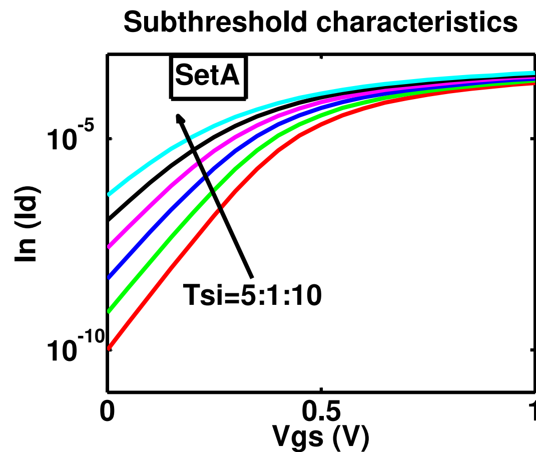

Figure 3.24 Subthreshold characteristics for fin thickness variation

Similar observation can be made regarding subthreshold swing improvement with increase in fin thickness. A better subthreshold swing implies better channel control.

Hence, for near-threshold optimization, decreasing fin thickness appears to be optimal for both least energy as well as better subthreshold characteristics.

Table 3.3 Optimized device parameters - Tsi

	Lg	S/D Doping	Text	Tox	Tsi	Tsp	Vthn	Vthp
Super-th.	15nm			2nm	7nm	4nm	0.45V	0.45V
Near-th.	15nm			1nm	5nm	6nm	0.45V	0.45V

3.4 Source/Drain Extension Variation

Source and Drain extension effectively increase the volume of Source and Drain which should translate to a reduced resistance and higher current. However, we shall see below that increased Source and drain extensions effectively increase gate capacitance due to increased fringe capacitance between the gate and Source/Drain.

3.4.1 Superthreshold parameter selection

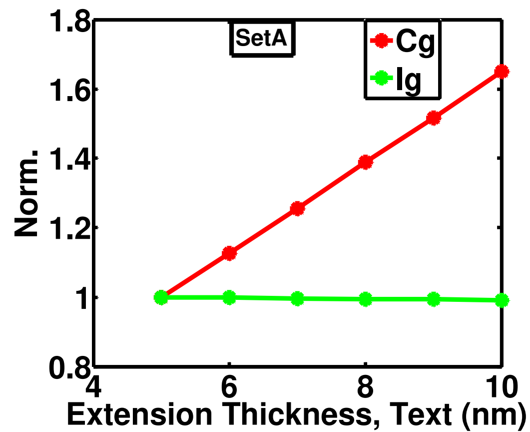

Figure 3.25 Gate capacitance and gate current versus extension thickness

The increase in gate capacitance is quite noticeable. Recall the structure of FinFET.

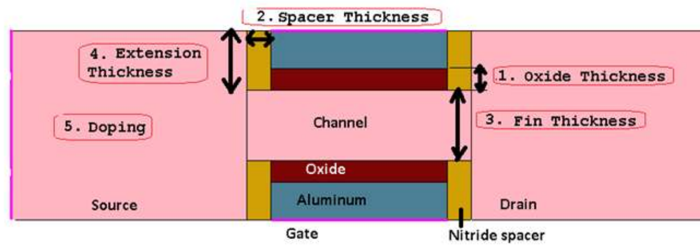

Figure 3.26 FinFET

Gate forms a capacitor with the Source and the Drain through the spacer. As we continue to extend source and drain, the area of the two plate capacitor increases linearly (there is a third dimension, fin height, which is constant here). This linear increase in area, translates to a linear increase in gate capacitance.

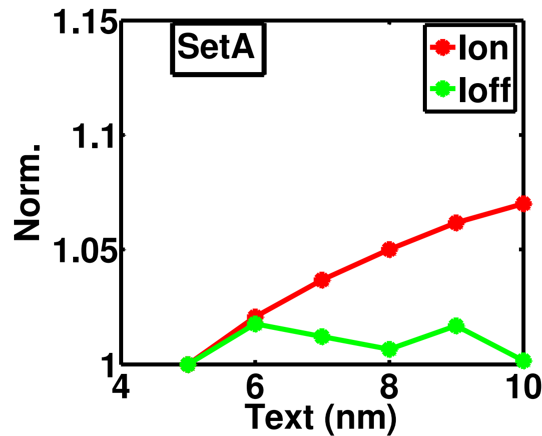

Figure 3.27 On current and off current versus extension thickness

As had been expected initially, on current increases with increased Source/Drain volume, but this comes at the cost of the considerable increase in gate capacitance. The improvement in current is hardly worth the increase in gate capacitance as we can see from the delay curve below.

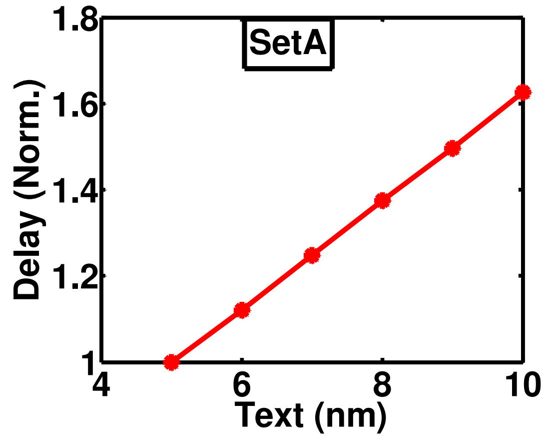

Figure 3.28 Delay versus extension thickness

Delay increases by the same factor as the gate capacitance which masks the little improvement in on current. Hence, for superthreshold optimization for least delay, increasing source/drain extension does not appear to be a suitable choice. We should keep the extensions to the minimum.

3.4.2 Near-threshold parameter selection

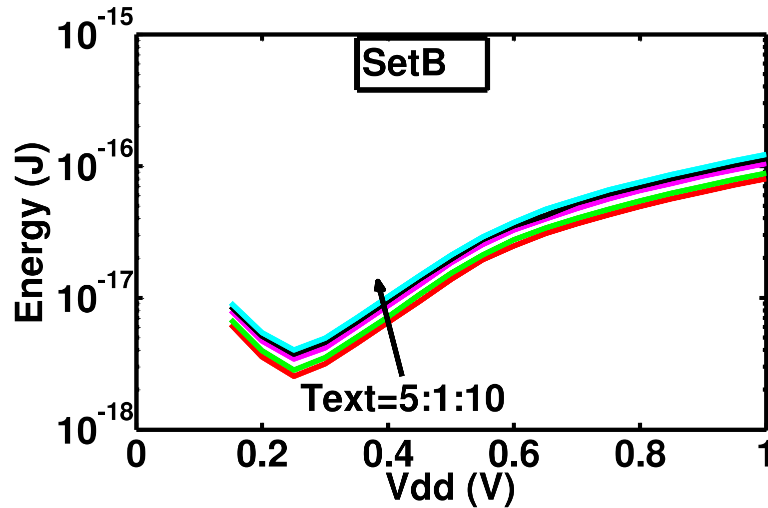

Figure 3.29 Energy curves for extension thickness variation

There is an almost linear vertical translation in the energy curves as the extension increases. This trend can be directly attributed to the increase in gate capacitance which linearly affects the dynamic energy of the circuit.

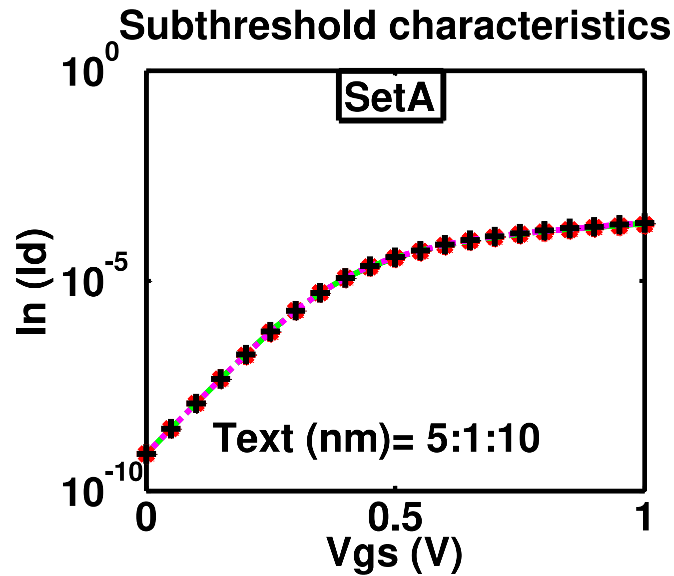

Figure 3.30 Subthreshold characteristics for Text variation

The miniscule improvement in on current and no change in off current imply that the subthreshold characteristics are not affected by the extension thickness. Solely, from energy improvement, we would recommend a smaller extension for least energy. This analysis reveals that for both superthreshold and near-threshold optimized device we would like to keep the extensions to a minimum to reduce gate capacitance.

Table 3.4 Optimized device parameters -Text

	Lg	S/D Doping	Text	Tox	Tsi	Tsp	Vthn	Vthp
Super-th.	15nm		5nm	2nm	7nm	4nm	0.45V	0.45V
Near-th.	15nm		5nm	1nm	5nm	6nm	0.45V	0.45V

3.5 Source/Drain Doping Variation

Doping in source and drain is essentially meant to increase the on current. But, we shall observe later that it does in fact affect the capacitance of the device which may come into picture at lower operating voltages.

3.5.1 Superthreshold parameter selection

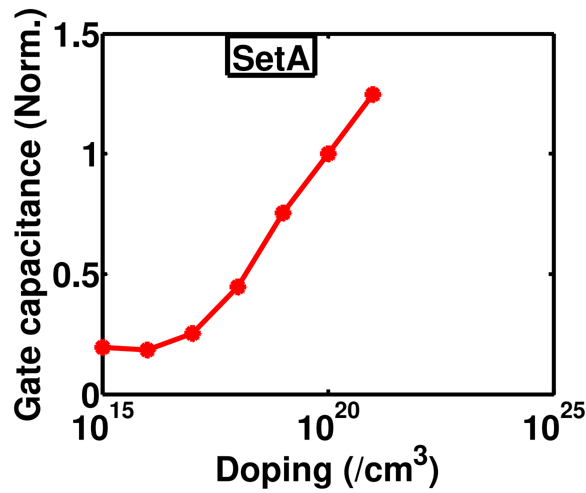

Figure 3.31 Gate capacitance versus doping

We see a small increase in gate capacitance as doping is increased. Here, both fringe capacitance and junction capacitance increase. It is worth noting that in our analysis since source/drain extension was kept to a default of 5nm, fringe capacitance is rather strong. From our analysis in the previous section, we recommended reduced source/drain extension for better performance, as it affects gate capacitance considerably. If we were to reduce extensions to 0nm, then fringe capacitance would reduce considerably.

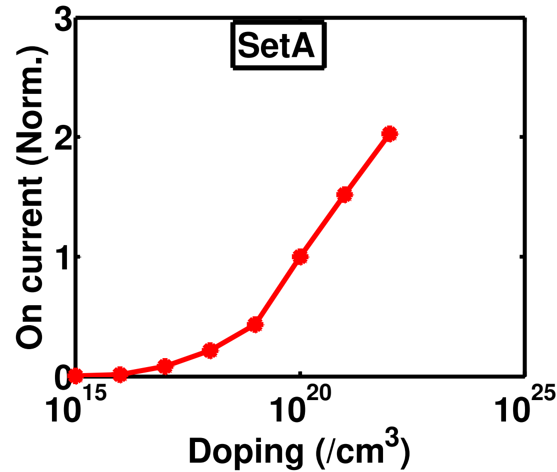

Figure 3.32 On current versus doping

The most important reason why we want to increase source/drain doping is mainly to increase the on current. This trend can be seen in the figure shown above.

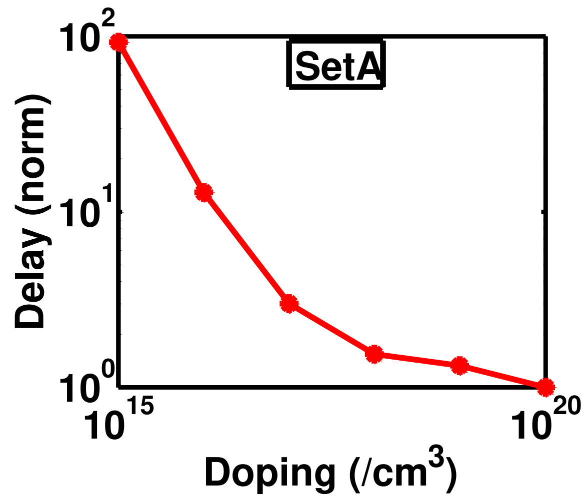

Figure 3.33 Delay versus doping

Clearly, the improvement in on current is considerably large when compared to increase in gate capacitance. The combined effect of the two on delay tilts in favor of

current improvement. Thus, for superthreshold optimization we should increase our Source/Drain doping to obtain least delay.

3.5.2 Near-threshold parameter selection

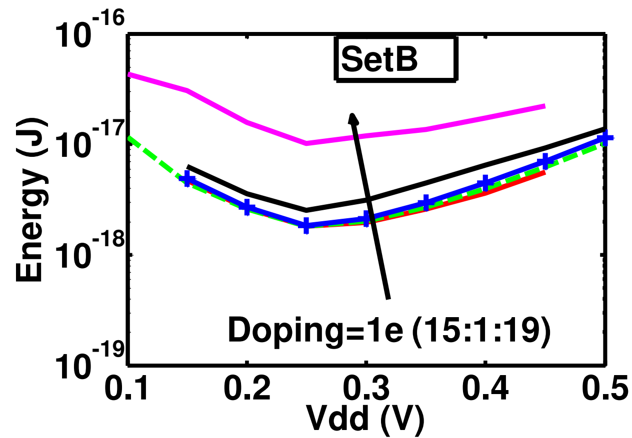

Figure 3.34 Energy curves for doping variation

Energy curves show a trend that favors lower doping. This is largely due to gate capacitance and junction capacitances. The figure below shows how gate capacitance changes with change in doping at low voltage. This trend leads to an increase in dynamic energy which is a linear function of gate capacitance. Hence from energy perspective, a lower doping seems preferable. At low doping, the on current is so low that leakage energy is also dominant. Low doping energy curves appear to overlap as leakage energy reduces while dynamic energy increases with increase in doping.

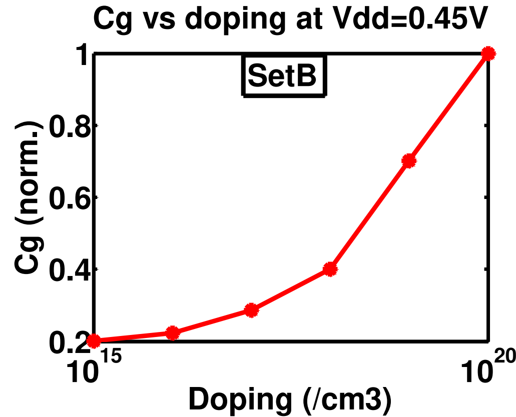

Figure 3.35 Gate capacitance versus doping at VDD=0.45V

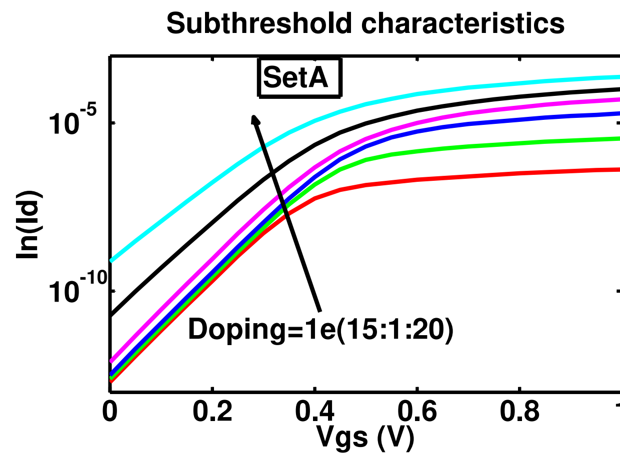

Figure 3.36 Subthreshold characteristics for doping variation

Subthreshold characteristics suggest, again, that a lower doping gives better subthreshold swing. As can be seen from the figure above, initially the improvement in on current is significant as doping is increased after which this improvement reduces. Practically, it is not advised that we reduce the doping below 1e18/cm^3 due to very low on current. Hence, for near-threshold operation, we can reduce doping to take advantage of reduced gate capacitance while keeping doping high enough to maintain a suitably large on current.

Table 3.5 Optimized device parameters –S/D Doping

	Lg	S/D Doping	Text	Tox	Tsi	Tsp	Vthn	Vthp
Super-th.	15nm	$1e18/cm^3$	5nm	2nm	7nm	4nm	0.45V	0.45V
Near-th.	15nm	$1e20/cm^3$	5nm	1nm	5nm	6nm	0.45V	0.45V

4. FINAL RESULTS

We've analyzed the effects of five very important parameters on the performance of FinFETs in different regions of operation. Following table lists the final optimal values for these five parameters.

Table 4.1 Optimized device parameters

	Lg	S/D Doping	Text	Tox	Tsi	Tsp	Vthn	Vthp
Super-th.	15nm	$1e18/cm^3$	5nm	2nm	7nm	4nm	0.45V	0.45V
Near-th.	15nm	$1e20/cm^3$	5nm	1nm	5nm	6nm	0.45V	0.45V

Here, the superthreshold optimized device acts as the baseline device against which energy savings are being calculated. After this we shall re-extract the IV and CV characteristics for these two parameter value-sets and compare savings in energy when a near-threshold optimized device is used instead of a superthreshold optimized device at low voltages.

To work around convergence issues in hSpice, I've used a modified baseline device first, which has S/D doping of $1e18/cm^3$.Please note that as a lower doping leads to lower energy, the calculated savings in energy will be a pessimistic value and hence still applicable for our analysis. Using these parameters, the energy curves are as follows:

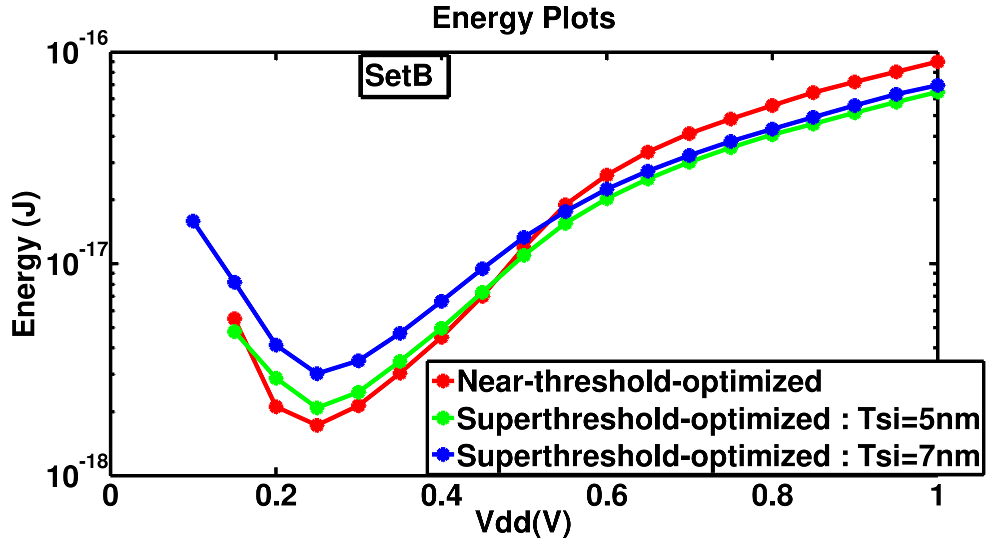

Figure 4.1 Energy Curves.

To calculate savings in energy by operating at minimum energy point, I translated the voltages by 0.2V. So, a comparison of performance between 0.45V and 1V translates to a difference between 0.25V and 0.8V.

Table 4.2 Results – Tsi=7nm

		Delay	**Leakage Energy**	**Dynamic Energy**	**Total Energy**
VDD=0.45V (0.25V)	**Superthreshold**	2.272e-07	8.554e-19	2.165e-18	3.020e-18
	Near-threshold	1.674e-06	3.620e-19	1.366e-18	1.728e-18
	Percentage	636.8% ↑	57.68% ↓	36.9% ↓	42.78% ↓
VDD=1V (0.8V)	**Superthreshold**	1.102e-10	2.576e-21	4.313e-17	4.313e-17
	Near-threshold	2.133e-10	1.904e-22	5.578e-17	5.578e-17
	Percentage	93.55% ↑	92.61% ↓	29.32% ↑	29.32%↑

We note that a near-threshold optimized device performs the best at near-threshold voltages in terms of energy. It is also worst amongst the three shown above at high voltages.

You may notice that two energy curves for a superthreshold device are plotted, one for a fin thickness of 7nm and one for a fin thickness of 5nm. As you may recall from our discussion on fin thickness variation, increase in fin thickness improves delay but simultaneously leads to an exponential increase in subthreshold leakage current. If we were to simply optimize for delay, a 7nm fin thickness can be used, but most device engineers prefer not to lose channel control. The savings in energy when compared against a modified baseline device with 5nm fin thickness are listed below.

Table 4.3 Results – Tsi=5nm

		Delay	**Leakage Energy**	**Dynamic Energy**	**Total Energy**
VDD=0.45V (0.25V)	**Superthreshold**	8.732e-07	5.634e-19	1.523e-18	2.087e-18
	Near-threshold	1.674e-06	3.620e-19	1.366e-18	1.728e-18
	Percentage	~900% ↑	35.75% ↓	10.3% ↓	17.2% ↓
VDD=1V (0.8V)	**Superthreshold**	1.461e-10	4.881e-22	4.064e-17	4.064e-17
	Near-threshold	2.133e-10	1.904e-22	5.578e-17	5.578e-17
	Percentage	~45% ↑	61% ↓	37.25% ↑	37.25%↑

For both values of fin thickness, we observe an improvement in energy by switching to a near-threshold-optimized device.

5. CONCLUSION

We observed trends for different performance parameters of a FinFETs as device parameters are varied.

In the end, we can conclude, that when the region of operation of a device has to be changed from superthreshold to near-threshold, a device optimized specifically for that region of operation is more energy efficient. Considerable savings in energy can be achieved by using a near-threshold optimized device at VDD=Vth, instead of using a superthreshold optimized device.

Similarly, a near-threshold optimized device will not be the most optimum choice when the operating voltage is in the superthreshold region.

5.1 Take-away points

Here, we can finally list the changes that we should make if we are trying to move from superthreshold region to near-threshold region of operation.

1. Decrease oxide thickness
2. Increase spacer thickness
3. Decrease Source/Drain doping

These are the three main take-away points that we can utilize when optimizing a device for near-threshold region of operation.

LIST OF REFERENCES

LIST OF REFERENCES

[1] Design Space Exploration of FinFETs in Sub-10nm Technologies for Energy-Efficient Near-Threshold Circuits. Sumeet Kumar Gupta, Kaushik Roy et al

[2] Underlap DGMOS for Digital Subthreshold Operation. Bipul C. Paul, Aditya Bansal and Kaushik Roy. IEE Transactions on Electronic Devices, Vol.53, No.4, April 2006

[3] Device Optimization for Digital Subthreshold Logic Operation. Bipul C. Paul, Arijit Raychowdhury and Kaushik Roy, IEEE Transactions on Electron Devices, Vol. 52, No.2, Feb 2005

[4] Double Gate-MOSFET Subthreshold Circuit for Ultralow Power Applications Jae-Joon Kim and Kaushik Roy, IEEE Transactions on Electron Devices, Vol 51, No.9, Sep 2004

[5] Threshold voltage and bulk inversion effects in nonclassical CMOS devices with undoped ultra-thin bodies, Vishal Trivedi, Jerry Fossum and Weimin Zhang, Solid State Electronics 51 (2007) 170-178

[6] Threshold Voltage of Thin-Film Silicon-on-Insulator (SOI) MOSFETs, Hyung-Kyu Lim and Jerry Fossum, IEEE Transactions on Electron Devices, Vol ED-30, No.10, Oct 1983

[7] A Continuous, Analytic Drain-Current Model for DG MOSFETs, Yuan Taur, X. Liang, W Wang and H. Lu, IEEE Electron Device Letters, Vol 25, No.2, Feb 2004

[8] PETE: A Device/Circuit Analysis Framework for Evaluation and Comparison of Charge Based Emerging Devices, C. Augustine, A. Raychowdhury, Y. Gao, M. Lundstorm and K. Roy, 10th Int'l Symposium on Quality Electronic Design

[9] Device-Optimization Technique for Robust and Low-Power FinFET SRAM Design in NanoScale Era, A. Bansal, S. Mukhopadhyay, K. Roy, IEEE Transactions on Electron Devices, Vol 54, No.6, June 2007.

[10] Analytic Solutions of Charge and Capacitance in Symmetric and Asymmetric Double-Gate MOSFETs, Yuan Taur, IEEE Transactions on Electroc Devices, Vol 48, No 12, December 2001.

[11] Mark Lundstorm EE612 F06, Purdue University

[12] Schred 2.1 Tutorial, Sayed Hasan, April 2003, Purdue University

[13] Kaushik Roy, ECE559 F11, Purdue University

[14] Asymmetric Drain Spacer Extension (ADSE) FinFETs for Low-Power and Robust SRAMs, Ashish Goel, Sumeet Kumar Gupta and Kaushik Roy, IEEE Transactions on Electron Devices, Vol 58, No 2, Feb 2011

APPENDICES

A. SENTAURUS STRUCTURE EDITOR CODE

```
(sde:clear)

;;NFET

;;define parameters

(define Sx 0.02)

(define Sy (+ (* 2 @Text@) @Tsi@))

(define Chwidth @Tsi@) ;;Tsi

(define Chlength @ChLen@)

(define spacer @Tsp@)

(define tox @Tox@)

(define Dx1 (+ (+ Sx Chlength) (* spacer 2)))

(define Dx2 ( + Dx1 Sx))

(define Dy Sy)

(define Chx1 Sx)

(define Chx2 Dx1)

(define Chy1 ( / (- Sy Chwidth) 2))

(define Chy2 ( / (+ Sy Chwidth) 2))

(define Oxidex1 (+ Sx spacer))

(define Oxidex2 (- Dx1 spacer))

(define Oxidey1 (- Chy1 tox))

(define Oxidey2 (+ Chy2 tox))

(define Metalx1 Oxidex1)

(define Metalx2 Oxidex2)

(define Metaly1 0)
```

```
(define Metaly2 Sy)

(define spacerx1 Sx)

(define spacerx2 Dx1)

(define spacery1 0)

(define spacery2 Sy)

(define mesh_ch_max (/ tox 10))

(define mesh_ch_min (/ mesh_ch_max 2))

(define doping @Doping@)


;;geometry (in um)

(sdegeo:set-auto-region-naming OFF)

(sdegeo:create-rectangle (position 0 0 0.0 )  (position Sx Sy 0.0 ) "Silicon" "source_rgn" )

(sdegeo:create-rectangle (position Dx1 0 0.0 )  (position Dx2 Dy 0.0 ) "Silicon" "drain_rgn" )

(sdegeo:create-rectangle (position Chx1 Chy1 0.0 )  (position Chx2 Chy2 0.0 ) "Silicon"
"channel" )

(sdegeo:set-default-boolean "BAB")

(sdegeo:create-rectangle (position Oxidex1 Oxidey1 0.0) (position Oxidex2 Oxidey2 0.0) "SiO2"
"oxide")

(sdegeo:create-rectangle (position Metalx1 Metaly1 0.0) (position Metalx2 Metaly2 0)
"Aluminum" "metal")

(sdegeo:create-rectangle (position spacerx1 spacery1 0.0) (position spacerx2 spacery2 0) "Si3N4"
"spacer")



;;define contacts
```

```
(sdegeo:define-contact-set "source" 4 (color:rgb 0 0 1)"//")
(sdegeo:define-contact-set "drain" 4 (color:rgb 0 0 1)"##")
(sdegeo:define-contact-set "gate" 4 (color:rgb 1 0 0)"solid")
;(sdegeo:set-current-contact-set "gate")
;(sdegeo:set-contact-edges (list (car (find-edge-id (position 0 (/ Sy 2) 0)))) "source")
;(sdegeo:set-contact-edges (list (car (find-edge-id (position Dx2 (/ Dy 2) 0)))) "drain")
;(sdegeo:set-contact-edges (list (car (find-edge-id (position (+ (/ (- Chx2 Chx1) 2) Chx1)  0.0 0))))
"gate")
;(sdegeo:set-contact-edges (list (car (find-edge-id (position (+ (/ (- Chx2 Chx1) 2) Chx1) Sy 0))))
"gate")

(sdegeo:define-2d-contact (list (car (find-edge-id (position 0 (/ Sy 2) 0)))) "source")
(sdegeo:define-2d-contact (list (car (find-edge-id (position Dx2 (/ Dy 2) 0)))) "drain")
(sdegeo:define-2d-contact (list (car (find-edge-id (position (+ (/ (- Chx2 Chx1) 2) Chx1)  0.0 0))))
"gate")
(sdegeo:define-2d-contact (list (car (find-edge-id (position (+ (/ (- Chx2 Chx1) 2) Chx1) Sy 0))))
"gate")



;;define refeval windows
(sdedr:define-refeval-window "RefWin.Source" "Rectangle" (position 0 0 0) (position Sx Sy 0))
(sdedr:define-refeval-window "RefWin.Drain" "Rectangle" (position Dx1 0 0) (position Dx2 Dy
0))
(sdedr:define-refeval-window "RefLine.Source" "Line" (position Chx1 Chy1 0) (position Chx1
Chy2 0))
```

```
(sdedr:define-refeval-window "RefLine.Drain" "Line" (position Chx2 Chy1 0) (position Chx2
Chy2 0))
(sdedr:define-refeval-window "RefWin.Global" "Rectangle" (position 0.0 0.0 0.0) (position Dx2
Dy 0.0))
(sdedr:define-refeval-window "RefWin.Channel" "Rectangle" (position Chx1 Chy1 0.0) (position
Chx2 Chy2 0.0))

;;Doping
;;This is the only segment which is different for a PFET
;;Instead of ArsenicActiveConcentration, use
;;BoronActiveConcentration
(sdedr:define-constant-profile "CPDef.SourceDrain" "ArsenicActiveConcentration" doping)
(sdedr:define-constant-profile-placement "CPPlace.Source" "CPDef.SourceDrain"
"RefWin.Source")
(sdedr:define-constant-profile "CPDef.SourceDrain" "ArsenicActiveConcentration" doping)
(sdedr:define-constant-profile-placement "CPPlace.Drain" "CPDef.SourceDrain" "RefWin.Drain")
(sdedr:define-analytical-profile-placement "APPlace.Source" "APDef.Source" "RefLine.Source"
"Negative" "NoReplace" "Eval")
(sdedr:define-gaussian-profile "APDef.Source" "ArsenicActiveConcentration" "PeakPos" 0
"PeakVal" doping "Length" 0.0002 "Gauss" "Factor" 0.1)
(sdedr:define-analytical-profile-placement "APPlace.Drain" "APDef.Drain" "RefLine.Drain"
"Positive" "NoReplace" "Eval")
(sdedr:define-gaussian-profile "APDef.Drain" "ArsenicActiveConcentration" "PeakPos" 0
"PeakVal" doping "Length" 0.0002 "Gauss"  "Factor" 0.1)
```

```
;;Meshing
(sdedr:define-refinement-size "RefDef.Global" 0.001 0.001 0.0005 0.0005  )
(sdedr:define-refinement-placement "RefPlace.Global" "RefDef.Global" "RefWin.Global" )
(sdedr:define-refinement-size "RefDef.Channel" 0.0005 0.0005  0.00025 0.00025  )
(sdedr:define-refinement-placement "RefPlace.Channel" "RefDef.Channel" "RefWin.Channel" )


(sde:build-mesh "snmesh" "-a -c boxmethod" "./n@node@")
;;End of Code
;;In alum.par change the value of Workfunction
;; WorkFunction           = 4.6     # [eV]
```

B. SENTAURUS DEVICE CODE – CG PLOT

```
Device NFET {
 Electrode {
        { Name="source" Voltage=0.0 }
        { Name="drain" Voltage=0 }
        { Name="gate" Voltage=0 }
 }

 File {
        Grid = "@tdr@"
        Plot = "@tdrdat@"
        Current = "@plot@"
     Parameter = "@parameter@"
 }

 Physics {
        AreaFactor=0.03
        AreaFactor=0.03
        Hydrodynamic  * Hydrodynamic carrier transport model takes into account the
contribution due to the spatial variations of electrostatic
                      * potential, electron affinity, and the band gap,gradient of concentration,
the carrier temperature
                      * gradients, and the spatial variation of the effective masses
        Fermi         * Using the work Fermi activates Fermi-Dirac Statistics
```

```
        Mobility(ThinLayer PhuMob HighFieldSaturation)
        Recombination( SRH(DopingDependence)
        eAvalanche(CarrierTempDrive)
        hAvalanche(Eparallel) )
        EffectiveIntrinsicDensity (BandGapNarrowing (OldSlotboom))
        MultiValley(MLDA)     *Quantization Model
  }

  Plot {
        eDensity hDensity eCurrent hCurrent
        equasiFermi hquasiFermi

        ElectricField eEparallel hEparallel
        Potential SpaceCharge
        SRHRecombination Auger AvalancheGeneration
        eMobility hMobility eVelocity hVelocity
        Doping DonorConcentration AcceptorConcentration

        eDirectTunneling hDirectTunneling
  }
}
Math {
  Extrapolate
  RelErrControl
  Notdamped=50
```

```
  Iterations=60
  AcceptNewtonParameter (
          -RhsAndUpdateConvergence
          RhsMin = 1.0e-5
          UpdateScale = 1.0e-2
  )
}


File {
  Output = "@log@"
  ACExtract = "@acplot@"
}
System {
  NFET trans (drain=d source=s gate=g)
  Vsource_pset vd (d 0) {dc=0}
  Vsource_pset vs (s 0) {dc=0}
  Vsource_pset vg (g 0) {dc=0}
}
Solve {
#-a) zero solution
Poisson
Coupled { Poisson Electron Hole }


#-b) ramp drain to positive starting voltage
Quasistationary (
```

```
 InitialStep=0.1 Increment=1.35 MinStep=1e-24 MaxStep=0.1
 Goal { Parameter=vd.dc Voltage=@vds@ }
){Coupled { Poisson Electron Hole }}

#-c) ramp gate to negative starting voltage
Quasistationary (
 InitialStep=0.1 Increment=1.35 MinStep=1e-24 MaxStep=0.1
 Goal { Parameter=vg.dc Voltage=-0.4 }
){Coupled { Poisson Electron Hole }}

#-d) ramp gate to positive starting voltage
Quasistationary (
 InitialStep=0.05 Increment=1.35 MinStep=1e-24 MaxStep=0.05
 Goal { Parameter=vg.dc Voltage=@vdd@ }
 AcceptNewtonParameter (ReferenceStep = 1.e-6)
){ ACCoupled (
 StartFrequency=1 EndFrequency=1
 NumberOfPoints=1 Decade
 Node(s,d,g) Exclude(vd vs vg)
){ Poisson Electron Hole }
        CurrentPlot (Time =
        ( range = (0 1) intervals = 33)
        )
}
}
```

```
Device PFET {
 Electrode {
           { Name="source" Voltage=0.0 }
           { Name="drain" Voltage=0 }
           { Name="gate" Voltage=0 }
 }

 File {
           Grid = "@tdr@"
           Plot = "@tdrdat@"
           Current = "@plot@"
      Parameter = "@parameter@"
 }
 Physics {
           AreaFactor=0.03
           AreaFactor=0.03
           Hydrodynamic  * Hydrodynamic carrier transport model takes into account the
contribution due to the spatial variations of electrostatic
                         * potential, electron affinity, and the band gap,gradient of concentration,
the carrier temperature
                         * gradients, and the spatial variation of the effective masses
           Fermi         * Using the work Fermi activates Fermi-Dirac Statistics
           Mobility(ThinLayer PhuMob HighFieldSaturation)
           Recombination( SRH(DopingDependence)
           eAvalanche(CarrierTempDrive)
```

```
        hAvalanche(Eparallel) )
        EffectiveIntrinsicDensity (BandGapNarrowing (OldSlotboom))
        MultiValley(MLDA)     *Quantization Model
  }

  Plot {
        eDensity hDensity eCurrent hCurrent
        equasiFermi hquasiFermi
        ElectricField eEparallel hEparallel
        Potential SpaceCharge
        SRHRecombination Auger AvalancheGeneration
        eMobility hMobility eVelocity hVelocity
        Doping DonorConcentration AcceptorConcentration
        eDirectTunneling hDirectTunneling
  }
}
Math {
  Extrapolate
  RelErrControl
  Notdamped=50
  Iterations=20
}
File {
  Output = "@log@"
  ACExtract = "@acplot@"
```

```
}
System {
  PFET trans (drain=d source=s gate=g)
  Vsource_pset vd (d 0) {dc=0}
  Vsource_pset vs (s 0) {dc=0}
  Vsource_pset vg (g 0) {dc=0}
  #-Initialize (vg.dc=0)
}
Solve {
#-a) zero solution
Poisson
Coupled { Poisson Electron Hole }

#-b) ramp source to positive starting voltage
Quasistationary (
  InitialStep=0.1 Increment=1.35 MinStep=1e-21 MaxStep=0.1
  Goal { Parameter=vd.dc Voltage=@vd@ }
)
{ Coupled { Poisson Electron Hole } }

Quasistationary (
  InitialStep=0.1 Increment=1.35 MinStep=1e-21 MaxStep=0.1
  Goal { Parameter=vg.dc Voltage=0.4 }
)
{ Coupled { Poisson Electron Hole } }
```

```
#-c) ramp gate to positive voltage
Quasistationary (
  InitialStep=0.05 Increment=1.35 MinStep=1e-21 MaxStep=0.05
  Goal { Parameter=vg.dc Voltage=@n_vdd@ }
)
{ ACCoupled (
  StartFrequency=1 EndFrequency=1
  NumberOfPoints=1 Decade
  Node(s,d,g) Exclude(vd vs vg)
)
{ Poisson Electron Hole }
CurrentPlot (Time =
        ( range = (0 1) intervals = 33)
        )
}
}
```

C. SENTAURUS DEVICE CODE – IV PLOT

```
*NFET
File {
Grid = "@tdr@"
Plot = "@tdrdat@"
Current = "@plot@"
Output = "@log@"
Parameter = "@parameter@"
}
Electrode {
{ Name="source" Voltage=0.0 }
{ Name="drain" Voltage=0.0 }
{ Name="gate" Voltage=0.0  }


}
Physics {
AreaFactor=0.03
Hydrodynamic  * Hydrodynamic carrier transport model takes into account the contribution due
to the spatial variations of electrostatic
              * potential, electron affinity, and the band gap,gradient of concentration, the
carrier temperature
              * gradients, and the spatial variation of the effective masses
Fermi         * Using the work Fermi activates Fermi-Dirac Statistics
Mobility(ThinLayer PhuMob HighFieldSaturation)
```

```
Recombination( SRH(DopingDependence)
eAvalanche(CarrierTempDrive)
hAvalanche(Eparallel) )
EffectiveIntrinsicDensity (BandGapNarrowing (OldSlotboom))
MultiValley(MLDA)     *Quantization Model
}
Physics(MaterialInterface="Silicon/Oxide") {
GateCurrent( DirectTunneling )
}
Plot {
eDensity hDensity eCurrent hCurrent
equasiFermi hquasiFermi
ElectricField eEparallel hEparallel
Potential SpaceCharge
SRHRecombination Auger AvalancheGeneration
eMobility hMobility eVelocity hVelocity
Doping DonorConcentration AcceptorConcentration
eDirectTunneling hDirectTunneling
}
Math {
Extrapolate
RelErrControl
Iterations=40
NotDamped=50
```

```
}
CurrentPlot {
PMIModel (
Name="EffectiveMobility"
Region="Channel"
)
}
Solve {
# initial gate voltage Vgs=0.0V
*Temperature    * compute a spatially dependent lattice temperature
Poisson
Coupled { Poisson Hole Electron}


Quasistationary
(InitialStep=0.1 Maxstep=0.1 MinStep=1e-8
Goal { name="gate" voltage=@Vg@ } )
{ Coupled { Poisson  Electron Hole} }


Quasistationary
(InitialStep=0.1 Maxstep=0.1 MinStep=1e-21
Goal { name="drain" voltage=-0.4 } )
{ Coupled { Poisson Electron Hole} }


NewCurrentPrefix="Vd_"
```

```
Quasistationary
(InitialStep=0.05 Maxstep=0.1 MinStep=1e-21
Goal { name="drain" voltage=@Vd@ } )
{ Coupled { Poisson Electron Hole}
CurrentPlot (Time = ( range = (0 1) intervals = 33))}
}
****************************************************
*PFET
File {
Grid = "@tdr@"
Plot = "@tdrdat@"
Current = "@plot@"
Output = "@log@"
Parameter = "@parameter@"
}
Electrode {
{ Name="source" Voltage=0.0 }
{ Name="drain" Voltage=0.0 }
{ Name="gate" Voltage=0.0  }
}
Physics {
AreaFactor=0.03
Hydrodynamic  * Hydrodynamic carrier transport model takes into account the contribution due
to the spatial variations of electrostatic
```

```
                    * potential, electron affinity, and the band gap,gradient of concentration, the
carrier temperature
                    * gradients, and the spatial variation of the effective masses
Fermi               * Using the work Fermi activates Fermi-Dirac Statistics
Mobility(ThinLayer PhuMob HighFieldSaturation)
Recombination( SRH(DopingDependence)
eAvalanche(CarrierTempDrive)
hAvalanche(Eparallel) )
EffectiveIntrinsicDensity (BandGapNarrowing (OldSlotboom))
MultiValley(MLDA)     *Quantization Model
}
Physics(MaterialInterface="Silicon/Oxide") {
GateCurrent( DirectTunneling )
}
Plot {
eDensity hDensity eCurrent hCurrent
equasiFermi hquasiFermi
ElectricField eEparallel hEparallel
Potential SpaceCharge
SRHRecombination Auger AvalancheGeneration
eMobility hMobility eVelocity hVelocity
Doping DonorConcentration AcceptorConcentration
eDirectTunneling hDirectTunneling
}
Math {
```

```
Extrapolate
RelErrControl
Iterations=30
NotDamped=50
}
CurrentPlot {
PMIModel (
Name="EffectiveMobility"
Region="Channel"
)
}
Solve {
# initial gate voltage Vgs=0.0V
*Temperature    * compute a spatially dependent lattice temperature
Poisson
Coupled { Poisson Hole Electron}

Quasistationary
(InitialStep=0.1 Maxstep=0.1 MinStep=1e-21
Goal { name="gate" voltage=@Vg@ } )
{ Coupled { Poisson Electron Hole } }

Quasistationary
(InitialStep=0.1 Maxstep=0.1 MinStep=1e-21
Goal { name="drain" voltage=0.4 } )
```

```
{ Coupled { Poisson Electron Hole } }

NewCurrentPrefix="Vd_"

Quasistationary

(InitialStep=0.05 Maxstep=0.05 MinStep=1e-21

Goal { name="drain" voltage=@Vd@ } )

{ Coupled { Poisson Electron Hole }


CurrentPlot (Time =

        ( range = (0 1) intervals = 33)

        )

}

}
```