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# Finite Control Set Model Predictive Direct Power Control of Single-Phase Three-Level PWM Rectifier Based on Satisfactory Optimization

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**ABSTRACT** In this paper, a finite control set model predictive direct power control (FCS-MPDPC) method based on satisfactory optimization, for single-phase three-level PWM rectifier, is proposed to achieve global optimization that takes into account all its objectives and constraints. Satisfaction optimization aims to obtain the satisfactory solution after coordination of multiple goals, instead of the optimal solution of a single goal. By replacing ''optimal'' with ''satisfaction'', more control degrees of freedom are acquired, so that low-priority auxiliary control objectives can participate in the optimization process. Meanwhile, in order to enhance the description accuracy of FCS-MPDPC method for the future trend of PWM rectifier, the prediction time domain is extended from the traditional single-step to multi-step, and the average switching frequency model is established to realize the low switching frequency control. The satisfactory optimized FCS-MPDPC method proposed in this paper is compared, through simulation and experimental results, with the standard FCS-MPDPC method, which verifies the effectiveness and superiority of the proposed algorithm.

**INDEX TERMS** Finite control set model predictive control (FCS-MPC), direct power control (DPC), single-phase PWM rectifier, satisfactory optimization control.

## I. INTRODUCTION

The single-phase PWM rectifier converter can realize the bidirectional flow of electric energy, and maintain high power factor and small current distortion (THD) between the AC and DC output terminals. Therefore, it wins a wide application in photovoltaic grid connection [1], single-phase uninterruptible power supply [2], and single-phase AC-DC-AC converter [3], and it is also the key equipment in the track traction system [4]. With the continuous development of high-speed railways, the demand for higher power levels is even more urgent. Single-phase three-level PWM converters have advantages over single-phase two-level PWM converters in terms of voltage level, power density, and current quality. Therefore, single-phase three-level PWM converters are widely used in high-speed railway traction [5].

High-performance NPC single-phase three-level PWM rectifier systems have relative high complexity due to multiple complex control targets. First of all, the output bridge arm phase voltage and the voltage between two bridges for each switching action cannot generate a voltage jump exceeding half of the DC bus voltage, because the former situation is unfavorable to the rectifier circuit, causing damage to the switching device, and the latter situation is unfavorable to the power grid, causing excessive impact on the power grid [6]. Secondly, power tracking and midpoint potential balance are the main control indicators for single-phase three-level PWM rectifier systems [7], [8]. Finally, the temperature of the switching device needs to be maintained at the maximum allowable range, to ensure that the switching device can work safely. Because the cooling capacity of the converter is

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limited, the temperature limit can be converted into the limit of the maximum tolerable switching loss. An indirect and very effective way to reduce the switching loss is to reduce the average switching frequency [9].

Model predictive control has attracted extensive attention from academic and industrial circles because of its multi-objective optimization ability and fast dynamic response [10], and has been extensively studied in induction motor drive [11], Z source converter [12], matrix converter [13], battery charging [14], photovoltaic power generation [15], wind power generation [16], high voltage direct current transmission [17], inverter power [18], robot control [19], DC/DC converter [20]–[22] and other fields. Literature [4] and [23] respectively proposed predict direct power control, deadbeat prediction control for single-phase three-level PWM rectifiers, and both achieved good results, but they all require carrier modulation to achieve current or power tracking. In the application of high power and low switching frequency, since the switching period is equal to the carrier period, that is, the discrete period. As the discrete time becomes larger, the error of the system discrete model becomes larger, and the system control performance deteriorates. Jose Rodriguez proposed a finite control set model predictive control scheme [24]. Because its discrete time domain is much smaller than its average switching period, it has lower system model discrete error at low switching frequency than carrier modulation, and in the field of low switching and high power, it has a high application prospect [25]–[28] and has been industrially applied in high-power motor drives [29]–[32].

In [33], the single-step FCS-MPC control method for single-phase two-level PWM rectifier is studied. In [34], the NPC single-phase three-level PWM rectifier is used as the control object, and the single-step FCS-MPC method is studied and introduced. The cascading-free prediction method further improves the DC-side dynamic performance of the single-phase three-level PWM rectifier, but its cost function contains only two control targets of current error and midpoint potential deviation, and does not introduce switching frequency optimization control.

The setting process of weight factor in the ''weight method'' is extremely complicated, and it is impossible to describe the designer's operation requirements for single-phase three-level PWM rectifier by quantifying single group of weight factors. The above phenomenon is especially obvious in the low-switching frequency PWM rectifier system [35]. The reasons are as follows:

1) Multiple targets and constraints of single-phase three-level PWM rectifiers often have different measurement units and accuracy requirements (such as power unit is watt, voltage unit is volt, and switching frequency unit is Hertz), and there are even certain time-varying and conflicting feature(such as steady-state error and switching frequency);

2) The single-step Np = 1 prediction link of traditional FCS-MPC method is extremely limited in the description of the future trend of single-phase three-level PWM rectifier. Although the switching state obtained after online optimization satisfies the minimum value of the cost function $J$ at the time of k+1, it may quickly deviate from the error zero in the subsequent short time, resulting in a single-step FCS-MPC falling into local optimum.

Aiming at the above two points, this paper takes a single-phase three-level PWM rectifier as the research object, and proposes an FCS-MPDPC method based on satisfactory optimization. By introducing the concept of priority in the cost function, all the objectives and constraints of the PWM rectifier are realized global optimization. In addition, in order to enhance the accuracy of the FCS-MPDPC method for the future trend of the PWM rectifier, the prediction time domain is extended from the traditional single-step length Np = 1 to the multi-step length Np > 1.

Different from the traditional ''optimal control'' theory, ''satisfaction optimization'' does not pursue the optimal solution of a single target when dealing with multi-objective optimization problems of complex systems, but aims to obtain satisfactory solutions after coordination of multiple targets. Considering the difference in the importance of multiple targets and constraints of a single-phase three-level PWM rectifier, the priority is firstly divided before the design of the satisfactory optimization cost function. Among them, the high priority is the system hard constraint. Once the indicator is broken, the system will be threatened to operate safely. The indicator plays a global role in the whole optimization process. The medium priority is the main control indicator, and the target ''optimal'' is replaced with ''satisfied'' in the optimization process for more control freedom, so that low-priority control targets can participate in the optimization process. The low-priority is auxiliary control indicators. When it comes to low priority, if there still exist multiple control degrees of freedom, the high and medium priority effects are ignored, and the final output of the system is determined directly by the low priority index to ensure the uniqueness of the entire optimization solution. The simulation and experimental verification of the proposed method are carried out, and compared with the standard FCS-MPDPC method. The results verify the effectiveness and superiority of the proposed algorithm.

## II. MATHEMATICAL MODEL OF SINGLE-PHASE PWM RECTIFIER

### A. PREDICTION MODEL

Fig. 1 shows the topology of a single-phase three-level neutral point clamped converter, where the continuous-time dynamic grid-voltage equation is shown as (1).

$$u_g - u_{ab} = L\frac{di_g}{dt} + Ri_g \tag{1}$$

where $i_g$ represents the grid-current, $u_g$ represents the grid-voltage, $u_{ab}$ represents the voltage between bridge arm a and b, L represents the filter inductor and R represents the parasitic resistance on inductor L.

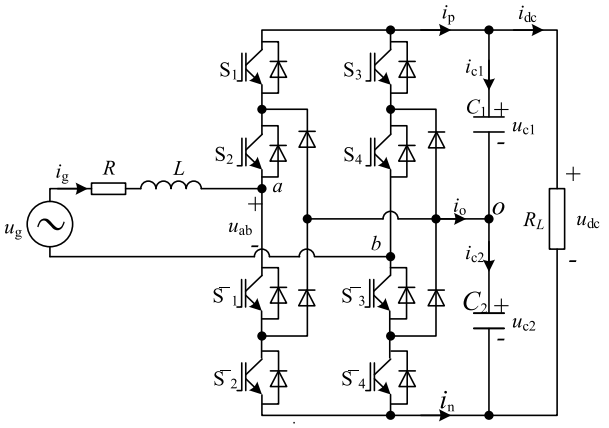


**FIGURE 1.** Single phase three-level NPC converter.

DC-side capacitor voltage is shown as (2).

$$\begin{cases} \dfrac{du_{C1}}{dt} = \dfrac{1}{C_1} i_{C1} = \dfrac{1}{C_1}(i_p - i_{dc}) \\ \dfrac{du_{C2}}{dt} = \dfrac{1}{C_2} i_{C2} = \dfrac{1}{C_2}(-i_n - i_{dc}) \end{cases} \tag{2}$$

where $i_{C1}$, $i_{C2}$ and $i_p$, $i_n$ are respectively the capacitor currents and internal currents of NPC converter, $u_{C1}$, $u_{C2}$ represents the up and down dc bus capacitor voltage, $i_{dc}$ represents the dc-link current and $C_1$, $C_2$ represent the dc-link capacitor value.

According to the switching states in Table 1, $u_{ab}$ can be expressed as (3).

$$u_{ab}^k = u_{C1}^k(S_1 - S_3) + u_{C2}^k(S_2 - S_4) \tag{3}$$

where $S_i$(i = 1,2,3,4) are the switching states.

**TABLE 1.** Switching state.

| $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_A$ | $S_B$ | $u_{ab}$ | state |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 1 | -1 | $u_{C1}+u_{C2}$ | $V_1$ |
| 1 | 1 | 0 | 1 | 1 | 0 | $u_{C1}$ | $V_2$ |
| 0 | 1 | 0 | 0 | 0 | -1 | $u_{C2}$ | $V_3$ |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | $V_4$ |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | $V_5$ |
| 0 | 0 | 0 | 0 | -1 | -1 | 0 | $V_6$ |
| 0 | 1 | 1 | 1 | 0 | 1 | $-u_{C1}$ | $V_7$ |
| 0 | 0 | 0 | 1 | -1 | 0 | $-u_{C2}$ | $V_8$ |
| 0 | 0 | 1 | 1 | -1 | 1 | $-u_{C1}-u_{C2}$ | $V_9$ |

To realize the prediction of the up and down dc bus capacitor voltage, the forward Euler method is adopted to transform (2) into a discrete-time form, i.e.

$$\begin{cases} u_{C1}^{k+1} = \dfrac{T_s}{C_1} i_p^k - \dfrac{T_s}{C_1} i_{dc}^k + u_{C1}^k \\ u_{C2}^{k+1} = -\dfrac{T_s}{C_2} i_n^k - \dfrac{T_s}{C_2} i_{dc}^k + u_{C2}^k \end{cases} \tag{4}$$

where $T_s$ is the sampling period. Based on the direct relation between the switching states of the NPC converter and $i_g$ as [34], the value of $i_p$ and $i_n$ can be calculated as (5).

$$\begin{cases} i_p^k = \dfrac{S_A(S_A+1) - S_B(S_B+1)}{2} i_g^k \\ i_n^k = \dfrac{S_A(S_A\text{-}1) - S_B(S_B\text{-}1)}{2} i_g^k \end{cases} \tag{5}$$

Consequently, according to (3) and (5), the controller can easily derive the estimated values for the predictions of the capacitor voltages.

Convert formula (1) to $\alpha\beta$ coordinate system:

$$\mathbf{u}_{\alpha,\beta} - \mathbf{u}_{ab\alpha,\beta} = L\frac{d\mathbf{i}_{\alpha,\beta}}{dt} + R\mathbf{i}_{\alpha,\beta} \tag{6}$$

$$\mathbf{x}_{\alpha,\beta} = \mathbf{x}_{d,q}e^{j\omega t} \tag{7}$$

Use equation (7) to convert formula (6) to dq coordinates.

$$\mathbf{u}_{d,q} - \mathbf{u}_{abd,q} = L\frac{d\mathbf{i}_{d,q}}{dt} + R\mathbf{i}_{d,q} + jL\omega\mathbf{i}_{d,q} \tag{8}$$

The first-order forward Euler discretization of equation (8) is obtained:

$$\begin{cases} i_d^{k+1} = \dfrac{T_s}{L}\left(u_d^k - u_{abd}^k\right) + \left(1 - \dfrac{T_sR}{L}\right) i_d^k + T_s\omega i_q^k \\ i_1^{k+1} = \dfrac{T_s}{L}\left(u_q^k - u_{abq}^k\right) + \left(1 - \dfrac{T_sR}{L}\right) i_q^k - T_s\omega i_d^k \end{cases} \tag{9}$$

According to the instantaneous power theory, active and reactive power can be expressed as:

$$\begin{bmatrix} p^{k+1} \\ q^{k+1} \end{bmatrix} = \frac{1}{2}\begin{bmatrix} u_d^{k+1} & u_q^{k+1} \\ u_q^{k+1} & -u_d^{k+1} \end{bmatrix}\begin{bmatrix} i_d^{k+1} \\ i_q^{k+1} \end{bmatrix} \tag{10}$$

Assuming a sinusoidal voltage, the grid voltages $u_d$ and $u_q$ can be considered constant during a small sampling period, that is $\mathbf{u}_{d,q}^{k+1} = \mathbf{u}_{d,q}^k$, Also, by using a PLL, the d-axis can be aligned with the fictitious rotating voltage vector $u_\alpha + ju_\beta$ and as a consequence $u_q = 0$. The vector diagram is shown in Fig. 2.

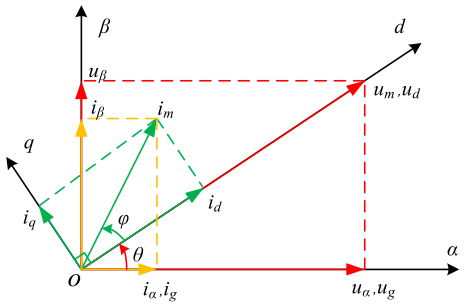


**FIGURE 2.** Vector diagram.

Based on these two assumptions, and substituting (9) into (10), the simplified relations for the fictitious active and reactive powers will be obtained as:

$$\begin{cases} p^{k+1} = \left(1 - \dfrac{T_sR}{L}\right) p^k - T_s\omega q^k + \dfrac{T_s}{L}\left(\left(u_d^k\right)^2 - u_d^k u_{abd}^k\right) \\ q^{k+1} = \left(1 - \dfrac{T_sR}{L}\right) q^k + T_s\omega p^k + \dfrac{T_s}{L}\left(u_d^k u_{abq}^k\right) \end{cases} \tag{11}$$

### B. POWER REFERENCE DESIGN

Obviously, the dc-link power can be expressed as (12).

$$p_{dc}^{k} = p_{C1}^{k} + p_{C2}^{k} + p_{Z_{dc}}^{k} = i_{p}^{k} u_{C1}^{k} - i_{n}^{k} u_{C2}^{k} \tag{12}$$

where $i_p$ and $i_n$ are obtained according to (6).

The power balance at both ends of the rectifier can obtain a reference value synchronized with the control targets on the DC side and the AC side. However, it is impossible to instantaneously compare the AC side power and the DC side power. For example, when $S_A = S_B$, the current $i_p$ and $i_n$ shown in equation (5) become zero, which will cause the DC side power to become zero, that is $p_{dc} = 0$, while the AC side power is not zero, that is $p_g \neq 0$. Therefore, define the average power reference value of the DC side in the power frequency cycle as $p_{dc\_av}^{*}$, and the average active power reference value of the AC side as $p_{g\_av}^{*}$, and analyze the average power balance in the rectifier. Based on the principle of power balance, we can acquire (13).

$$p_{g\_av}^{*k+1} = p_{R\_av}^{k+1} + p_{dc\_av}^{*k+1} \tag{13}$$

where $p_{R\_av}$ represents the filter resistor power loss.

Clearly, it is impossible to get $p_{dc\_av}^{*}$ directly from (12). Consequently, $p_{dc\_av}^{*}$ is derived from the average values for each item in (12). The capacitor voltage is always controlled by its current. However, due to the limitation of the properties of power electronics, the capacitor current is limited. In order to ensure that the capacitor voltage reaches the expected value while maintaining power balance, a reference prediction horizon $N^*$ is introduced. $N^*$ is defined as the expected DC bus voltage $u_{dc} = u_{dc}^{*}$ after $N^*$ sampling times $N^*T_s$.

Therefore, the future average voltage references of capacitor can be obtained according to (14)

$$u_{dc\_av}^{*k+1} = u_{dc}^{k} + \frac{1}{N^*}(u_{dc}^{*k} - u_{dc}^{k}) \tag{14}$$

In addition, the average value of the neutral-point current $i_o$ is approximately zero when neutral point voltage is in a dynamic equilibrium. Hence, the average capacitor current references are deduced as (15)

$$i_{C1\_av}^{*k+1} = i_{C2\_av}^{*k+1} = i_{C\_av}^{*k+1} = \frac{\frac{C_1 C_2}{C_1 + C_2}}{T_s}(u_{\mathrm{dc\_av}}^{*k+1} - u_{dc}^{k}) \tag{15}$$

where $C_1$, $C_2$ represent the dc-link capacitor value.

The average dc-current at this moment can be written as (16).

$$i_{dc\_av}^{*k+1} = \frac{u_{dc\_av}^{*k+1}}{R_{L\_av}^{*k+1}} \tag{16}$$

Assuming that the actual values of $u_{dc}^{k}$ an be measured and the average dc-link power consumption related to $R_{L\_av}$ is a constant within two sampling periods, $R_{L\_av}^{k+1}$ can be expressed as (17).

$$R_{L\_av}^{k+1} = \frac{u_{dc}^{k}}{i_{dc}^{k}} \tag{17}$$

Based on the above analysis, the average dc-power reference $p_{dc\_av}^{*k+1}$ is defined as (18).

$$p_{dc\_av}^{*k+1} = (i_{dc\_av}^{*k+1} + i_{C\_av}^{*k+1}) u_{dc\_av}^{*k+1} \tag{18}$$

Considering a second-order harmonic component existed in the dc-side variables of single-phase converters, a notch-filter centered at 100Hz (2f) is adopted. Moreover, the notch-filter output is used as a reference $p_{dc\_av\_2f}^{*k+1}$.

In addition, it is essential to estimate the resistor power loss to get the filter inductor loss, i.e:

$$p_{R\_av}^{*k+1} = R(\frac{i_m^{k+1}}{\sqrt{2}})^2 = \frac{R}{(u_m^{k+1}/\sqrt{2})^2}\left((p_{g\_av}^{k+1})^2 + (q_{g\_av}^{k+1})^2\right) \tag{19}$$

where $u_m^{k+1} \approx u_m^{k}$ and $i_m^{k+1}$ stand for the peak values of grid-voltage and current respectively and $q_{g\_av}^{k+1}$ is the ac-side average reactive power.

According to (13), (18), and (19), the ac-side power can be calculated. Thus, (11) can be expressed as a quadratic equation of $p_{g\_av}^{k+1}$:

$$\frac{2R}{(u_m^{k})^2}(p_{g\_av}^{*k+1})^2 - p_{g\_av}^{*k+1} + p_{dc\_av\_2f}^{*k+1} + \frac{2R}{(u_m^{k})^2}(q_{g\_av}^{*k+1})^2 = 0 \tag{20}$$

The solution that minimizes the power is given by (21):

$$p_{g\_av}^{*k+1} = \frac{\rho^k}{2}\left(1 - \sqrt{1 - \frac{4}{\rho^k}\left(p_{dc\_av\_2f}^{*k+1} + \frac{(q_{g\_av}^{*k+1})^2}{\rho^k}\right)}\right) \tag{21}$$

where $\rho^k = \frac{(u_m^k)^2}{2R}$.

At this point, the reference value of the active power $p^{*k+1}$ at time k+1 is $p_{g\_av}^{*k+1}$.

## III. STANDARD FCS-MPDPC METHOD

Standard FCS-MPDPC method uses weight factors for multiple control targets to establish a multi-target cost function [10]. These control requirements can be expressed by formulas through the cost function to get the minimum value. The cost function for the NPC single-phase three-level PWM rectifier consists of the following components

$$\begin{cases} J_p = \left|p^{*k+1} - p^{k+1}\right| \\ J_q = \left|q^{*k+1} - q^{k+1}\right| \\ J_{u_o} = \left|u_o^{k+1}\right| \\ J_s = \left|\mathrm{S_A^k\text{-}S_A^{k-1}}\right| + \left|\mathrm{S_B^k\text{-}S_B^{k-1}}\right| \end{cases} \tag{22}$$

$$J = J_p + J_q + k_o J_{u_o} + k_s J_s \tag{23}$$

In the formula, $J_p$ and $J_q$ are the tracking errors of active power and reactive power, $Ju_o$ is the midpoint potential deviation, and $J_s$ is the number of power electronic switch conversions. The weight factors $k_o$ and $k_s$ are used to handle the relationship among reference power tracking, midpoint

voltage balance, and variables that contribute to switching frequency reduction. Some larger weight factors value implies a greater priority for this goal.

## IV. SATISFACTORY OPTIMIZATION PREDICTIVE CONTROL

Different from the traditional ''optimal control'' theory, the so-called ''satisfaction optimization'' does not pursue the optimal solution of a single target when dealing with multi-objective optimization problems of complex systems, but aims to obtain satisfactory solutions after coordination of multiple targets. Considering the difference in the importance of multiple targets and constraints of a single-phase three-level PWM rectifier, prior to the design of the satisfactory optimization cost function, the priority division is firstly shown in Fig. 3. In Fig. 3, the optimization goal of the single-phase three-level PWM rectification system is divided into three priority levels: high, medium and low. Among them, the high priority is the system hard constraint. Once the indicator is broken, the system will be threatened to operate safely. The indicator plays a global role in the whole optimization process; the medium priority is the main control indicator, and in the optimization process, the target ''optimal'' is replaced with ''satisfied'' in exchange for more control freedom, so that low priority control targets can participate in the optimization process; low priority is auxiliary control indicators, and when optimization continues to low priority, if there still exist multiple control degrees of freedom, the high and medium priority effects are ignored. The final output of the system is determined directly by the low priority index to ensure the uniqueness of the entire optimization solution. The multiple priority cost functions of the single-phase three-level PWM rectifier are designed one by one below.

| priority order | Optimizing content | norm |
|---|---|---|
| high | Phase Voltage Jump Limitation<br>Line Voltage Jump Limitation | constraint |
| medium | Power Tracking Reference<br>Neutral Potential Balance | Satisfied |
| low | Reduce switching frequency | optimal |

**FIGURE 3.** The priority of PWM rectifier multi-objective.

### A. HIGH PRIORITY

For the single-phase three-level PWM rectifier NPC topology studied in this paper, the bridge arm phase voltage ($u_{ao}$, $u_{bo}$). That is unfavorable to the rectifier circuit, causing damage to the switching device. Therefore, for a single-phase three-level NPC topology, not all of the nine switch states can be directly actuated each time the switch is actuated, and it needs to be properly constrained. The specific switching state jump rule is shown in Fig.4. In the high priority, when the 9 candidate switching states have excessive voltage du/dt hopping

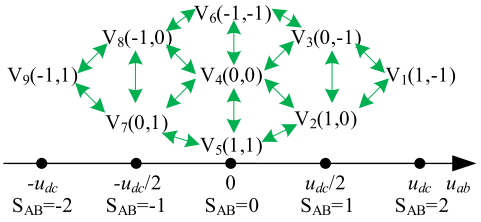


**FIGURE 4.** Switching diagram of switching rules.

problems, they are directly discarded without predicting and evaluating the k+1 value of the corresponding single-phase three-level PWM rectifier.

Power tracking and midpoint potential balance are the main control indicators of single-phase three-level PWM rectifier system. The trade-off of control effect will directly determine the advantages and disadvantages of FCS-MPDPC optimization process. Throughout the medium-priority optimization process, the idea of satisfactory optimization runs through it, pursuing more control freedom by pursuing the ''satisfaction'' rather than ''optimal'' of the control target, and leaving enough control margin for the low priority control target.

### B. MEDIUM PRIORITY

Taking the active power $p$ tracking control as an example, the satisfaction judgment method of the active power prediction result is given in Fig. 5. Let the tracking error be $\Delta p^{k+1} = p^{*k+1}\text{-}p^{k+1}$ and take the active power satisfaction error as $\delta_p > 0$. The satisfactory error function $\mu k+1\ p$ of the active power $p$ can be expressed as a piecewise function as:

$$\mu_p^{k+1} = \begin{cases} 0, & \Delta p^{k+1} \in \left[-\delta_p, \delta_p\right] or \left|\Delta p^{k+1}\right| \le \left|\Delta p^{k}\right| \\ 1, & \text{else} \end{cases} \tag{24}$$

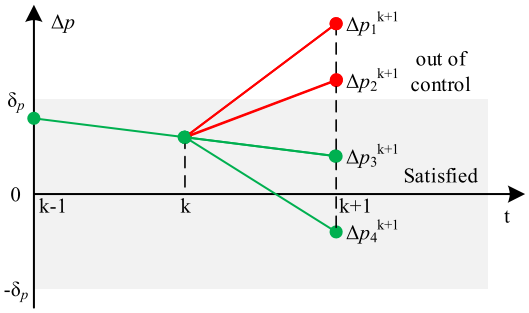


**FIGURE 5.** Satisfaction judgment method of active power predictive result.

Similarly, the satisfaction of reactive power and midpoint potential can be described in the same way as in equation (24), and the corresponding satisfaction levels $\mu_q$ and $\mu u_o$ are obtained as follows.

$$\mu_q^{k+1} = \begin{cases} 0, & \Delta q^{k+1} \in \left[-\delta_q, \delta_q\right] or \left|\Delta q^{k+1}\right| \le \left|\Delta q^{k}\right| \\ 1, & \text{else} \end{cases} \tag{25}$$

$$\mu_{u_o}^{k+1} = \begin{cases} 0, & \Delta u_o^{k+1} \in \left[-\delta_{u_o}, \delta_{u_o}\right] or \left|\Delta u_o^{k+1}\right| \le \left|\Delta u_o^{k}\right| \\ 1, & \text{else} \end{cases} \tag{26}$$

So far, the comprehensive satisfaction error function $\mu$ of the medium priority target can be expressed as:

$$\mu^{k+1} = \mu_p^{k+1} + \mu_q^{k+1} + \mu_{u_o}^{k+1} \tag{27}$$

When $\mu = 0$, it means that the medium priority targets $p$, $q$, and $u_o$ are all within the expected satisfaction error range, and the PWM rectifier should continue to output the optimal switching state obtained by the k-1 cycle; when $\mu > 0$, it means that there exit one or more of the medium priority targets $p$, $q$, $u_o$ are beyond the satisfaction error range, and at this time, the PWM rectifier needs to switch to the new optimal switching state to maintain the stability of PWM rectifier. When the feasible switching state number N is greater than 0, it indicates that there is still a control margin for low priority target optimization, and the optimization process will be further performed to the low priority; when the feasible switching state number N is equal to 0, the optimization process will stop at the medium priority. In order to make the PWM rectifier recover quickly and stabilize, the feasible switching state that can eliminate the tracking error of the mid-priority targets $p$, $q$, $u_o$ will be selected as soon as possible. The tracking errors of $p$, $q$ and $u_o$ corresponding to different switch states are sorted from small to large, and the switch state with the smallest weighted sequence number is selected as the output [36].

### C. LOW PRIORITY

Lower switching frequency is an auxiliary control indicator for a single-phase PWM rectifier system, which reflects more of the designer's design preferences for high-power single-phase PWM rectifier systems. If there are still several possible switching states, namely N > 0, when the optimization proceeds here, all optimization targets of high and medium priority are ignored, and the average switching frequency becomes the only optimization content. For this purpose, a multi-step average switching frequency model will be built.

#### 1) ACTIVE POWER REFERENCE PREDICTION

In the single-step FCS-MPDPC rectification system, the sampling period $T_s$ takes a small value (usually less than 100 $\mu$s). Therefore, even in the dynamic process, the expected value of the active power $p^{*k+1}$ at time k+1 and the expected value of the active power $p^{*k}$ at time k is close, and can generally be considered as $p^{*k+1} \approx p^{*k}$.

However, as the prediction step size $N_p$ increases, the active power expectation value $p^{*k+Np}$ at $k + N_p$ time changes significantly compared to the expected value $p^{*k}$ at time k. Linear extrapolation can be used to calculate the active power expected value trajectory, as follows

$$p^{*k+N_p} = p^{*k} + \left(p^{*k} - p^{*k-1}\right) N_p \tag{28}$$

#### 2) SYSTEM STATE PREDICTION

The traditional FCS-MPDPC algorithm is based on the limited switching state of the power electronic system. When the prediction step size is extended to $N_p > 1$, the finite switching state set is extended to a finite switching sequence set. Taking the prediction step size $N_p = 2$ as an example, the number of combinations of switching sequences sharply increases to $9^2 = 81$ when ignoring the switching state du/dt jump constraint condition.

The multi-step FCS-MPDPC discrete prediction model refers to predicting the state of the future Np sampling periods of the PWM rectification system at time k. Taking the prediction step size $N_p = 2$ as an example, it is necessary to predict the state of the single-phase three-level PWM rectifier at the time of k+1 and k+2 in the control period k. The model prediction process of the multi-step FCS-MPDPC system is carried out step by step in a progressive manner.

Firstly, according to the system state at time k, the system state prediction at time k+1 is completed according to the discrete prediction model in equations (4) and (11); On this basis, based on the system state prediction value at time k+1, the system state prediction value at time k+2 is calculated, and then gradually moves forward according to this.

Further analysis that when the switching state of the PWM rectification system remains unchanged in the previous cycle, the active power, the reactive power, and the midpoint potential are directly extrapolated. If the above three still meet the set error range, other switching states in the cycle can be directly judged as invalid.

Therefore, for the multi-step optimization FCS-MPDPC system, the switching state's switching point can be set directly at the time when the system state is close to the error boundary, that is, the switching is kept unchanged while the system state is within the set error range.

A schematic diagram of the switching sequence of the multi-step FCS-MPDPC system is shown in Fig.6. A switch of switching state occurs when the error boundary is approached, and the system state is extrapolated for the rest of the time. System state trend extrapolation can be solved by linear extrapolation, as follows

$$N_y = \begin{cases} \dfrac{y^{*k} + \delta_y - y^k}{y^{k+1} - y^k}, & y^{k+1} > y^k \\ \dfrac{y^{*k} - \delta_y - y^k}{y^{k+1} - y^k}, & y^{k+1} < y^k \end{cases} \tag{29}$$

where $N_y$ is the extrapolation step size when the controlled variable y reaches the error boundary, and $\delta_y$ is the allowable error of variable y.

So far, the PWM rectifier state at the time $k + N_y$ can be expressed as:

$$y^{k+N_y} = \left(y^{k+1} - y^k\right) N_y + y^k \tag{30}$$

It should be noted that the system's "prediction step size $N_p$" and "prediction time domain $T_p$" do not satisfy the relationship of $T_p = N_p T_s$ due to the constraint that the

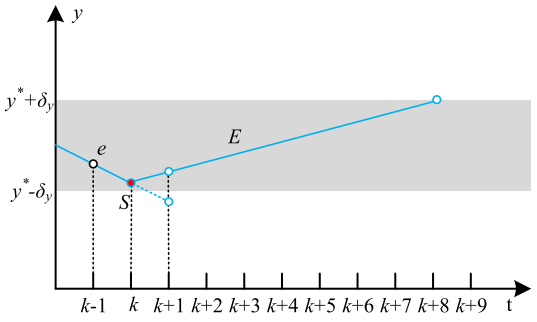


**FIGURE 6.** Multi-step FCS-MPDPC system switching sequence diagram.

switching state remains unchanged within the error range.

$$T_p = N_y T_s > N_p T_s \tag{31}$$

Taking the "eSE" switching sequence in Fig.6 as an example, the implementation steps of the multi-step FCS-MPDPC system based on satisfactory optimization are introduced as follows:

1) Firstly, keep the output switching state of k-1 cycle unchanged, and complete the "e" trend extrapolation according to the discrete prediction models of equations (4) and (11). If the corresponding $k+1$ times $p^{k+1}$, $q^{k+1}$, and $u_o^{k+1}$ are all within the set satisfactory error range, the optimal switching state corresponding to the k-cycle is consistent with the k-1 period. The multi-step FCS-MPDPC online optimization is terminated, and the corresponding switching state of the k-1 cycle is directly applied to the PWM rectification system; If any value of $p^{k+1}$, $q^{k+1}$, and $u_o^{k+1}$ at corresponding $k+1$ exceeds the set error range, it indicates that one of the values $p^{k+1}$, $q^{k+1}$, and $u_o^{k+1}$ has reached satisfactory error boundaries, and a new switch sequence needs to be selected to adjust it.

2) According to the optimal switching state $V_{OPT}^{k-1}$ corresponding to the period k-1, determine all "SE" switching sequences that satisfy the satisfactory optimization FCS-MPDPC high priority criterion.

3) According to equations (30) and (31), predict the state of the PWM rectifier that meets the "SE" law, and store all the "SE" switch states that satisfy the satisfactory optimization FCS-MPDPC medium priority criterion into the candidate switch sequence set M;

4) Calculate an average switching frequency $f_{SW}^{k+N_y}$ corresponding to all candidate switching sequences in the set of candidate switch sequences M, namely:

$$f_{SW}^{k+N_y} = \frac{\left|S_A^k - S_A^{k-1}\right| + \left|S_B^k - S_B^{k-1}\right|}{T_p} \tag{32}$$

where the prediction time domain $T_p$ takes the extrapolated time domain minimum of $p$, $q$, $u_o$ under the "SE" switch sequence, namely:

$$T_p = \min\left\{T_{p\_p}, T_{p\_q}, T_{p\_u_o}\right\} \tag{33}$$

where $T_{p\_p}$, $T_{p\_q}$, and $T_{p\_u_o}$ are active power, reactive power, and midpoint potential extrapolation time domains, respectively.

It can be seen that each candidate switch sequence prediction time domain $T_p$ is not the same. The average switching frequency $f_{SW}^{k+N_y}$ is proportional to the number of switching switches, and inversely proportional to the extrapolation time domain of the switching sequence. Finally, the switch sequence that satisfies the average switching frequency value $f_{SW}^{k+N_y}$ is the smallest, and is selected as the optimal switch sequence $V_{\mathrm{OPT}}^{\mathrm{k}}$. The multi-step FCS-MPDPC online optimization is terminated.

5) It needs to be explained again that the multi-step FCS-MPDPC is based on the rolling optimization principle to complete the switch state output, that is, only the first switch state of the obtained optimal switch sequence is applied to the PWM rectification system.

So far, the multi-step FCS-MPDPC online optimization is completed, and the optimization process of 1), 2), 3), 4) is repeated in the next control cycle.

## V. SIMULATION ANALYSIS AND EXPERIMENTAL VERIFICATION

In order to verify the effectiveness and superiority of the proposed satisfactory optimization of FCS-MPDPC control strategy, the simulation analysis and experimental verification were carried out. The simulation and experimental parameters are shown in Table 2.

**TABLE 2.** The main parameters of the simulation and experimental set up.

| Parameters | Symbol | value |
|---|---|---|
| Filter inductor | L | 12mH |
| Filter resistance | R | 0.1Ω |
| DC bus capacitor | $C_1$, $C_2$ | 2200μF*2 |
| RMS of grid-voltage | $u_g$ | 230V |
| DC bus voltage | $u_{dc}$ | 400V |
| Load resistance | $R_L$ | 25Ω |
| Reactive power reference | $q^*$ | 0 |
| Active power satisfaction error | $\delta_p$ | 500W |
| Reactive power satisfaction error | $\delta_q$ | 500W |
| Midpoint potential satisfaction error | $\delta u_o$ | 20V |
| Average switching frequency | $f_{SW}$ | ≤1000Hz |
| Sampling time | $T_s$ | 100μs |

### A. SIMULATION RESULTS AND ANALYSIS

Simulation studies are carried out by Matlab/Simulink software to validate the effectiveness of the proposed satisfactory optimization of FCS-MPDPC control algorithm.

Fig.7 and Fig.8 show the simulation results of the control effect of the satisfactory optimization of FCS-MPDPC method and the standard FCS-MPDPC method at full load. The satisfaction error $\delta_p$, $\delta_q$, $\delta u_o$ in the satisfactory optimization FCS-MPDPC algorithm are as shown in Table 2, and the average switching frequency is about 300Hz at this time. The standard FCS-MPDPC method selects the weight coefficient so that the average switching frequency can be

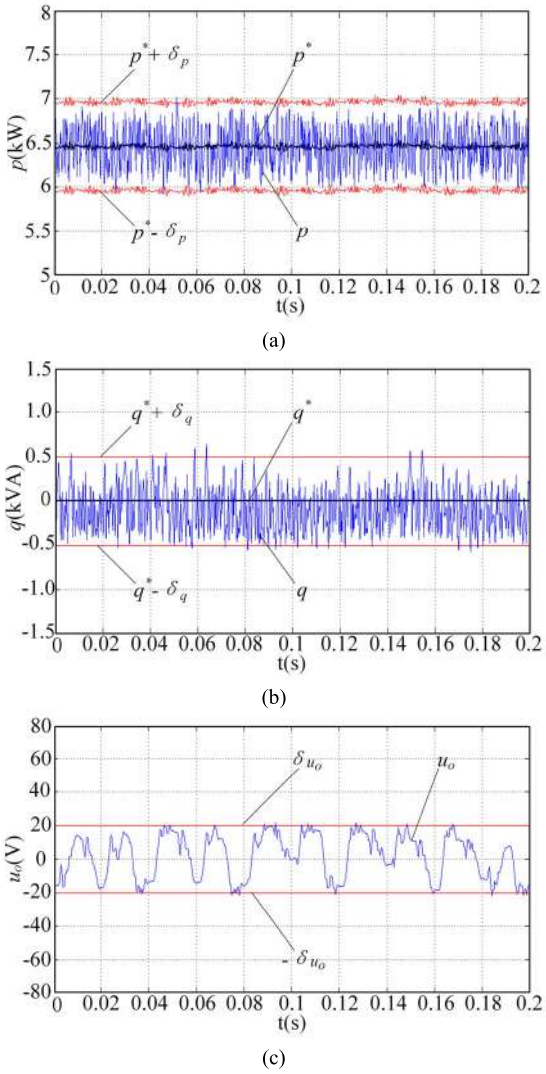


**FIGURE 7.** Simulation results of satisfactory optimization FCS-MPDPC control strategy, (a) Active power, (b) Reactive power, (c) Midpoint potential.

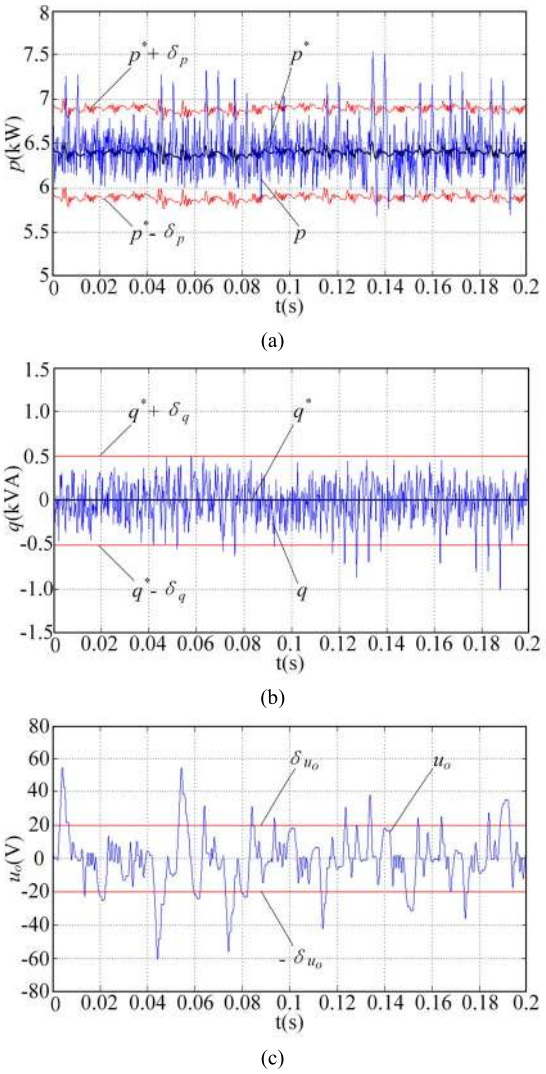


**FIGURE 8.** Simulation results of standard FCS-MPDPC control strategy, (a) Active power, (b) Reactive power, (c) Midpoint potential.

also close to 300Hz. In Fig.7, in the satisfactory optimization FCS-MPDPC method, $p$, $q$, and $u_o$ are strictly limited to the set error band, which shows that the FCS-MPDPC satisfaction error parameter under satisfactory optimization is more physical. In contrast, in Fig.8, the standard FCS-MPDPC method exhibits large fluctuations in $p$, $q$, and $u_o$, and the PWM rectifier operation quality obviously cannot meet the designer's requirements.

It can be seen from above Figures that the satisfactory optimization FCS-MPDPC is not required to carry out the complicated weighting coefficient configuration process compared with the standard FCS-MPDPC. The setting parameters are the satisfaction errors $\delta_p$, $\delta_q$, $\delta u_o$ with clear physical meaning. Considering the transient over-voltage characteristics of IGBT power devices, in order to avoid over-voltage breakdown of IGBT devices, it is necessary to limit the maximum fluctuation of the midpoint potential. In engineering applications, 5% of the DC bus voltage is usually configured.

At this point, the variable parameters are only $\delta_p$, $\delta_q$, which are related to the grid-current quality of the satisfactory optimization FCS-MPDPC method. Considering the consistency of the active power and reactive power measurement units, $\delta_p = \delta_q$ is usually taken. The simulation results of power satisfaction error and grid-current distortion rate are given in Fig.9. The set values of power satisfaction error $\delta_p$ and $\delta_q$ are gradually increased from 250W to 1000W. It's obvious that with the gradual increase of power error, the total current distortion rate THD of the grid side gradually increases correspondingly, the minimum is 2.21% and the maximum is 10.82%, and the whole process is quasi-linear. Based on this characteristic, the designer can easily complete the parameters $\delta_p$, $\delta_q$ configuration according to the requirements of the PWM rectifier system.

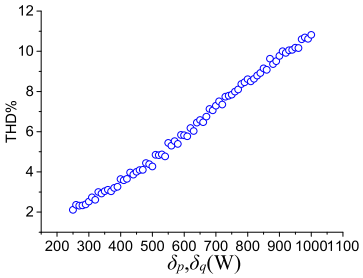


**FIGURE 9.** Satisfaction error $\delta_p$, $\delta_q$ and current distortion rate curve at full load.

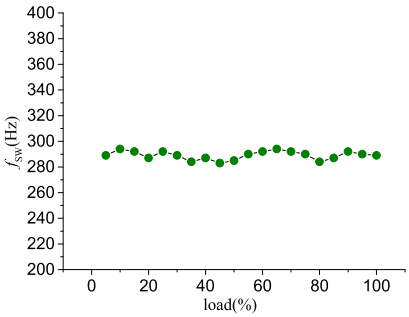


**FIGURE 10.** Average switching frequency versus load curve.

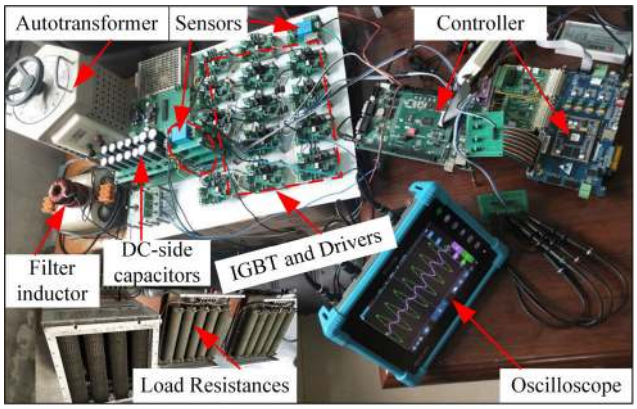


**FIGURE 11.** Experimental setup.

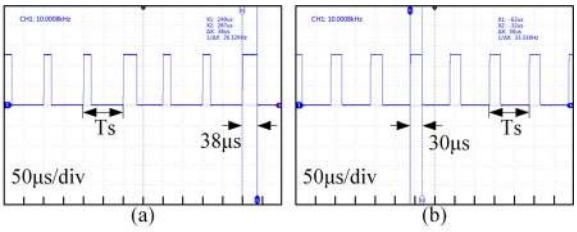


**FIGURE 12.** DSP operation time, (a) satisfactory optimization FCS-MPDPC control strategy, (b) standard FCS-MPDPC control strategy.

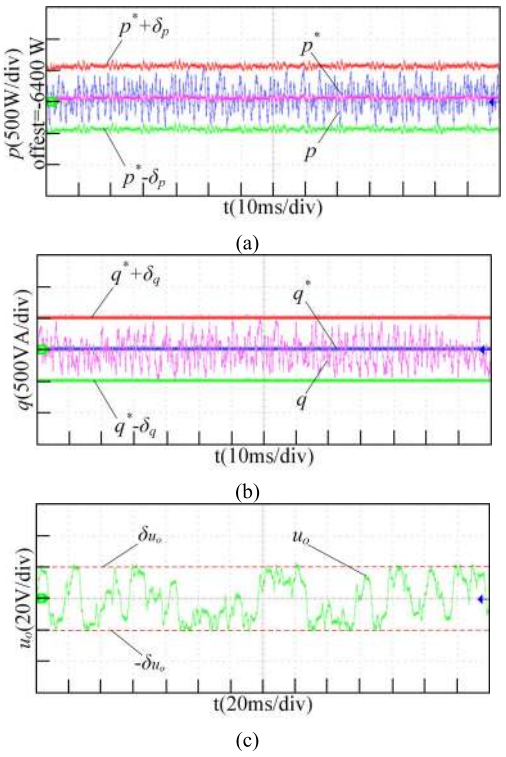


**FIGURE 13.** Experimental results of satisfactory optimization FCS-MPDPC control strategy, (a) Active power, (b) Reactive power, (c) Midpoint potential.

In order to further analyze the optimized FCS-MPDPC average switching frequency characteristics, the average switching frequency statistics of single-phase PWM rectifiers from no load to full load are shown in Fig.10. The load power is gradually changed from no load to full load, and the change step is 5% full load. Similarly, taking $\delta_p = 500$W, $\delta_q = 500$W, $\delta u_o = 20$V, the average switching frequency $f_{SW}$ of the single-phase PWM rectifier is statistically described. As can be seen from Fig.10, the average switching frequency $f_{SW}$ of the PWM rectifier from idling to full load fluctuates around 280-300 Hz. The above phenomenon indicates that the satisfactory optimization FCS-MPDPC is set at a low priority because of its lower switching frequency optimization target, and the switching frequency of the PWM rectifier can be maintained at any load power. It can be concluded that the satisfactory optimization FCS-MPDPC can achieve effective control of the average switching frequency $f_{SW}$.

### B. EXPERIMENTAL VALIDATION

In order to verify the effectiveness and superiority of the proposed satisfactory optimization FCS-MPDPC control method, an experimental prototype of NPC single-phase three-level PWM rectifier is established as shown in Fig. 11. The device uses a TMS320C28346 digital signal processor (DSP), XC7A100T-2FGG484I FPGA and FGY75N60SMD IGBT. The load is changed by controlling the number of resistors connected in parallel to the DC bus. Parameter configuration and simulation part of satisfactory optimization FCS-MPDPC and standard FCS-MPDPC method are consistent.

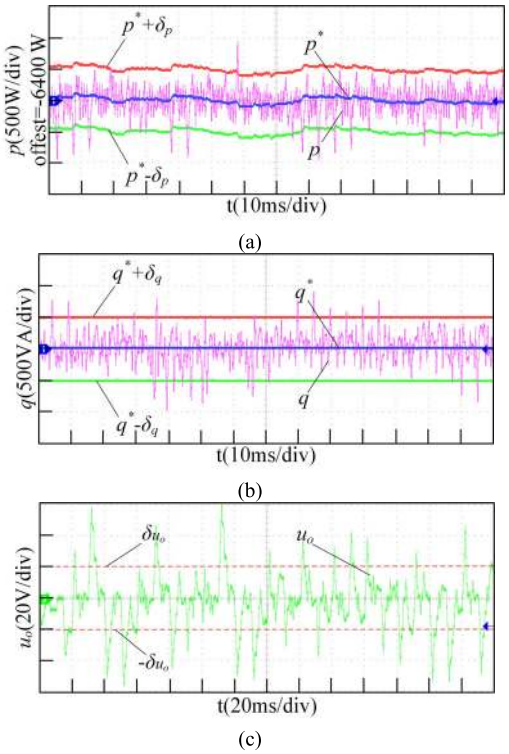


**FIGURE 14.** Experimental results of standard FCS-MPDPC control strategy, (a) Active power, (b) Reactive power, (c) Midpoint potential.

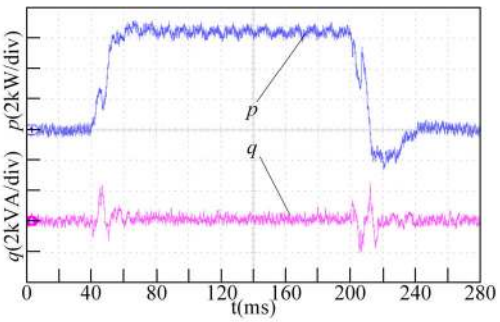


**FIGURE 15.** Experimental waveform diagram of active power and reactive power on grid side.

Fig. 12 shows the DSP operation time required by the two control strategies. The maximum operation time of the satisfactory optimization FCS-MPDPC control strategy is 38$\mu$s, and the maximum operation time of the standard FCS-MPDPC control strategy is 30$\mu$s. The proposed control strategy is more computational cost than the standard FCS-MPDPC, but most of the current DSP chips can meet the computational needs.

Fig.13 and Fig.14 show the control effect comparison between the satisfactory optimization FCS-MPDPC method and the standard FCS-MPDPC method at full load. Fig.15-18 show the satisfactory optimization FCS-MPDPC dynamic experiment, with 0-40ms and 200-280ms with no load and 40-200ms with full load.

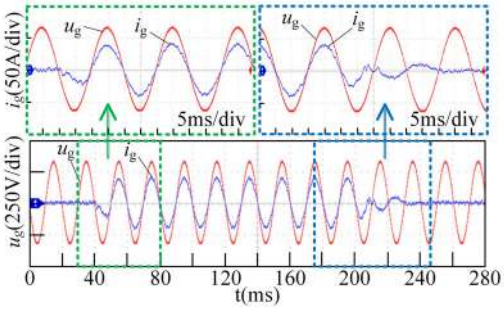


**FIGURE 16.** Experimental waveform diagram of grid-voltage and grid-current.

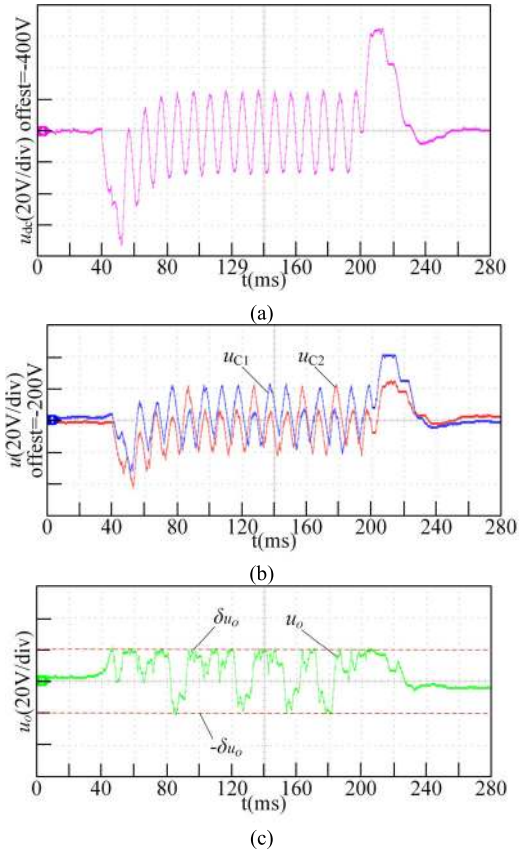


**FIGURE 17.** Experimental waveform diagram of DC-side dynamic response, (a) DC bus voltage, (b) DC side upper and lower bus capacitor voltage, (c) midpoint potential.

Fig.15 is a waveform diagram of active power and reactive power on the grid side, showing that the active reactive power of the dynamic process can track the reference value. Fig.16 is a waveform diagram of the grid-voltage and grid-current, showing that unity power factor control can be achieved. As can be seen from Fig.16, the dynamic response time is about 10ms, and Fig.15 shows that the dynamic response is about 20ms. The oscillation of active power and reactive power in the dynamic process is due to the error in the dynamic process of the $\alpha\beta$-axis and the dq-axis current. The actual grid side response time of the system is about 10ms.

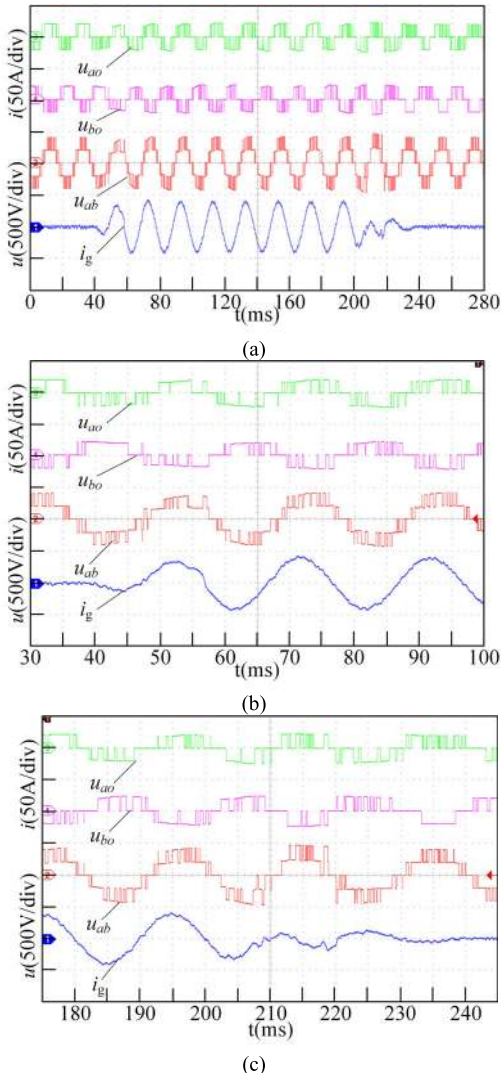


**FIGURE 18.** Experimental waveform diagram of $u_{ao}$, $u_{bo}$, $u_{ab}$ and $i_g$ dynamic response.

Fig.17 shows the DC-side dynamic response waveform of the system, where Fig.17(a) is the DC bus voltage waveform, Fig.17(b) is the DC-side upper and lower bus capacitor voltage waveform, and Fig.17(c) is the midpoint potential waveform. As can be seen DC bus voltage can effectively track the reference value when the load is changed, the upper and lower bus capacitor voltages can be effectively controlled, and the midpoint potential is controlled within the set range. Therefore, effectiveness of the satisfactory optimization FCS-MPDPC method for midpoint potential control is proved.

Fig.18 shows the input voltage and grid-side current waveform of a single-phase three-level PWM rectifier, where Fig.18 (b) and Fig.18 (c) are a partial enlarged view of Fig.18 (a). As can be seen from Fig.18, there is no cross-level jump of the bridge arm phase voltage and the voltage between the two bridges during dynamic and steady state processes, and the highest priority setting for satisfactory optimization FCS-MPDPC method is realized eventually.

## VI. CONCLUSION

Taking single-phase three-level PWM rectifier as the research object, this paper proposes a FCS-MPDPC method based on satisfactory optimization. By introducing the concept of priority into the cost function, the global optimization that combines all objectives and constraints of PWM rectifier is realized. In addition, in order to enhance the description accuracy of FCS-MPDPC method for the future trend of PWM rectifier, the prediction time domain is extended from the traditional single-step to multi-step. The control scheme is novel in that it can optimize the average switching frequency of NPC single-phase three-level PWM rectifier when the active power, reactive power and midpoint potential control are within a given error range, and the performance is better than that of standard FCS-MPDPC. Simulation and experimental results show that the proposed scheme is effective, and has certain reference significance in the design of high power single-phase PWM rectifier controller.

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