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First Demonstration of Short-Circuit Capability for a 1.2 kV SiC SWITCH-MOS

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ABSTRACT In this paper, the authors report a unique short circuit failure mechanism of a 1.2 kV silicon carbide (SiC) SBD-wall-integrated trench MOSFET (SWITCH-MOS), using numerical simulations and experimental validation. When the Schottky barrier height in the SWITCH-MOS was set at 1.20 eV, the short-circuit withstand time was roughly half that of a conventional SiC trench MOSFET. This is because, in the SWITCH-MOS, the thermionic-field emission electrons passing through the embedded SBD continue flowing into the high electric field in the n− drift region, even after the gate is turned off. This causes heat generation in the device, resulting in thermal runaway. Using a novel methodology for improving the short-circuit capability, it was confirmed that metal with a high Schottky barrier height of 1.75 eV can significantly improve the SWITCH-MOS short-circuit capability, making it comparable to that of conventional SiC trench MOSFETs, and suggesting SWITCH-MOS devices may be superior power devices for use in high frequency inverters.

INDEX TERMS Silicon carbide, SWITCH-MOS, short-circuit capability, thermionic-field emission, Schottky barrier height.

I. INTRODUCTION

A 1.2kV 4H-silicon carbide (SiC) trench metal-oxide-semiconductor field-effect-transistor (MOSFET) with embedded trench Schottky barrier diode (SBD), known as an SBD-wall-integrated trench MOSFET (SWITCH-MOS), has been proposed and fabricated [1]. The SWITCH-MOS is a unique device consisting of a trench-SBD-integrated trench MOSFET with a small cell pitch, enabling the device to achieve both low on-resistance and inactivation of the body pin diode for reliable operation [2], [3]. Also, the device features superior fast switching characteristics even at high temperature. This is because of small recovery current when the drain current is turned on, owing to the operation of the embedded SBD and the extremely high dV/dt both in the turn-on and turn-off state, due to the smaller reverse transfer capacitance [4]. A further significant benefit of the SWITCH-MOS is that the MOSFET and SBD share not only the forward conduction layer but also the edge termination regions, resulting in a significant reduction in SiC wafer area. This also reduces the number of dies which must be assembled in the SiC MOSFET module, and reduces their assembly time, resulting in reduced module cost [5]–[12].

In power inverter applications, there is a particularly strict requirement for SiC MOSFETs to be capable of withstanding the high-current flow that occurs during the short-circuit state, so that the devices must withstand a high current flow while supporting high voltage being applied to the drain electrode. Based on experimental and numerical analysis, the present study investigated the short-circuit capability and a failure mechanism of the SWITCH-MOS. Further, it proposes and verifies a novel methodology for enhancing the device's short-circuit capability.

II. SHORT CIRCUIT EXPERIMENTS

A. THE TESTED DEVICE

Figure 1 shows a schematic cross section of a fabricated 1.2 kV SWITCH-MOS with a cell pitch of 5 μm and a die

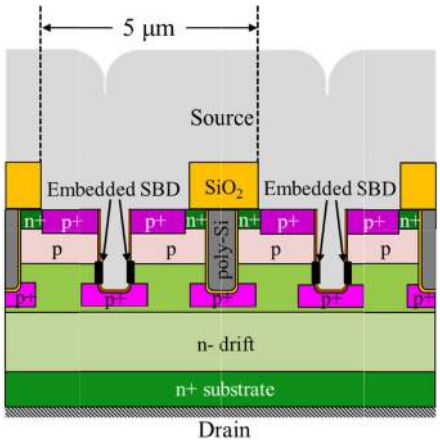

FIGURE 1. Schematic cross section of SWITCH-MOS.

size of 3 mm × 3 mm. The fabrication process is summarized in [1].

Titanium was used as the Schottky metal (embedded SBD as shown in Fig. 1), and its measured barrier height was 1.20 eV on the $(1\bar{1}00)$-face (m-face) of the 4H-SiC wafer. The static device characteristics of the 1.2-kV SWITCH-MOS and a conventional trench MOSFET, the IE-UMOSFET [13], were measured, and are summarized in Table 1. The IE-UMOSFET is a SiC trench gate power MOSFET with low on-resistance; IE stands for implantation and epitaxial growth, the processes involved in the p-base formation. High channel mobility was achieved in an epitaxially grown channel region with a low acceptor concentration. In the fabrication of both the SWITCH-MOS and IE-UMOSFET, the buried p+ and trench bottom p+ shielding regions, which together function as the gate shielding structure, were formed using high-dose aluminum-ion (Al^+) implantation. Thickness and doping concentration of the n− drift layer were 10 μm and 8×10^{15} cm^{-3}, respectively, and the gate oxide thickness was 80 nm. In addition to these, a relatively high-dose n region was inserted between the p− base and n− drift region, as a current spreading layer. Both devices were assembled in TO-247 packages. In the SWITCH-MOS, the breakdown voltage and specific on-resistance were 1576 V (with a drain current (I_d) of 0.1 mA at room temperature) and 3.3 mΩcm^2 (gate-to-source voltage (V_{gs}) of 20 V at room temperature), respectively. The SWITCH-MOS was identical to the IE-UMOSFET in structure and dimensions, except for the presence of an embedded trench SBD, so that the corresponding values for the IE-UMOSFET were 1605 V and 3.3 mΩcm^2. It was found that the drain leakage current in the SWITCH-MOS was successfully suppressed, and roughly the same as in the IE-UMOSFET, comparable to a number of commercialized SiC trench MOSFETs. For example, the measured leakage current of the Infineon 1.2 kV SiC trench MOSFET (DF23MR12W1M1_B11) was 157 nA at a drain voltage of 1200 V. This means that the embedded Schottky diode regions in the SWITCH-MOS were sufficiently shielded

TABLE 1. Measured static characteristics of SWITCH-MOS and IE-UMOSFET.

	SWITCH-MOS	IE-UMOSFET
Die size	3.0 × 3.0 mm^2	
Breakdown voltage (V, @I_d = 0.1 mA)	1576	1605
Leakage current (nA, @V_{ds}=1200 V, R.T.)	310	410
Threshold voltage (V, @R.T.)	3.7	3.2
Specific on resistance (mΩcm^2, @V_{gs} = 20 V, R.T.)	3.3	3.2

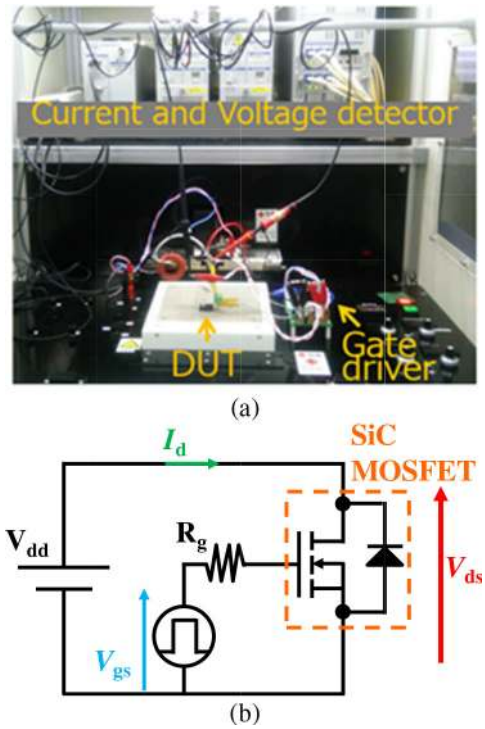

FIGURE 2. (a) Short-circuit measurement hardware and (b) diagram of the equivalent circuit. The gate resistance was set at 47 Ω.

via the p− base and p+ regions, which act as the JBS (junction barrier-controlled Schottky) structure in forward blocking mode [14]. The substrate resistivity and thickness in both the SWITCH-MOS and IE-UMOSFET were 20 mΩcm and 350 μm, so the specific on-resistance of these devices could be improved of as small as less than 3.0 mΩcm^2, in the case of 150 μm substrate. The gate threshold voltages were 3.7 V for the SWITCH-MOS and 3.2 V for the IE-UMOSFET, at room temperature.

B. MEASUREMENTS FOR SHORT-CIRCUIT CAPABILITY

Figure 2 shows the experimental setup for the short-circuit test, and a diagram of the equivalent circuit. There are three main types of short-circuit test configurations mainly for silicon insulated gate bipolar transistors (IGBTs); 1) a direct turn-on of the IGBT to a short circuit, 2) a short circuit during the IGBT conduction mode, and 3) a short circuit across the load during the freewheeling diode conduction mode [15]. Configuration 1) was used in this study. Before turning on the SiC MOSFETs, a high DC voltage of 800 V was applied to the devices, while a negative voltage of −4 V was applied

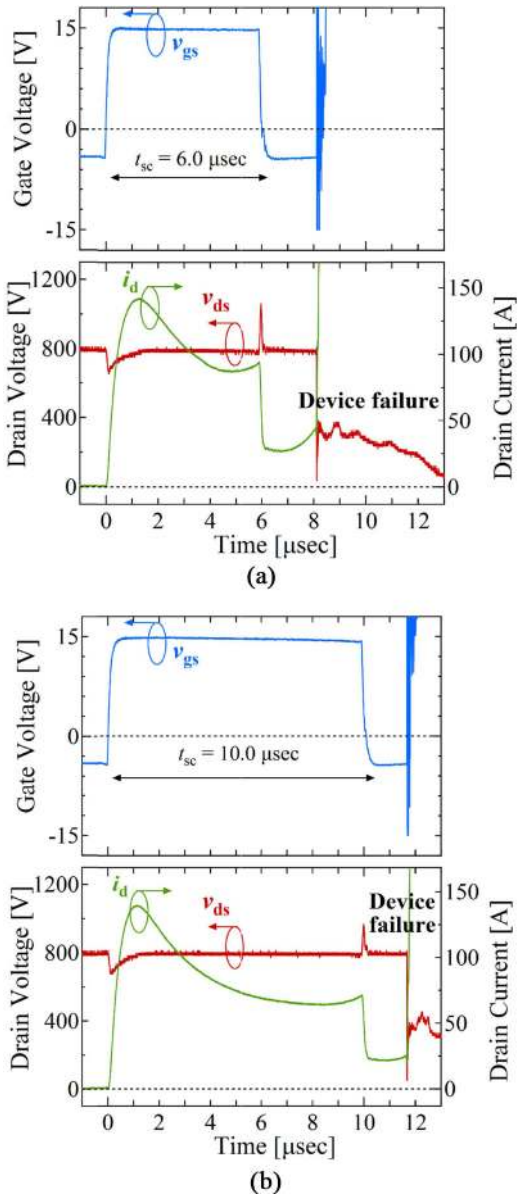

FIGURE 3. Measured short-circuit waveforms of (a) SWITCH-MOS and (b) IE-UMOSFET at a DC bus voltage of 800 V ($@V_{gs}$ = +15V/−4 V, R.T.).

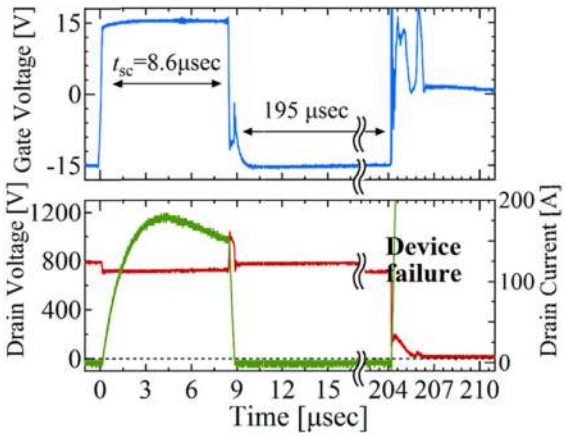

FIGURE 4. Measured short-circuit waveforms of state-of-the-art silicon 1.2 kV trench FS-IGBT at DC bus voltage of 800 V ($@V_{gs}$ = +15/−15 V, R.T.).

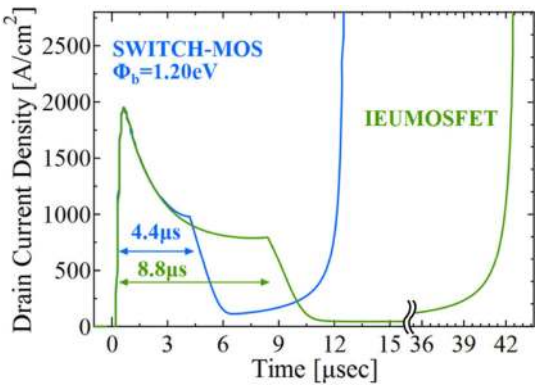

FIGURE 5. Simulated drain current of (a) SWITCH-MOS ($\varnothing_b$ = 1.20 eV) and (b) IE-UMOSFET in the short-circuit state, at a DC bus voltage of 800 V (V_{gs} = +15 V/−4 V, R.T.).

at the gate electrode. The measurement was performed at a positive gate voltage of +15 V. The pulse duration time was increased at intervals of 0.5 µsec until failure of the device under the test (DUT). According to [16], a high drain surge voltage in a MOSFET after device turn-off can trigger an avalanche failure. Therefore, in this study, a gate resistor providing a relatively high gate resistance (R_g) of 47 Ω was connected to the gate electrode, to limit dI/dt for soft turn-off when measurements were taken. In this paper, all the measurements were performed at room temperature (R.T.).

III. INVESTIGATION OF A SHORT CIRCUIT FAILURE MECHANISM AND DEVICE IMPROVEMENT

Figure 3 shows the measured short-circuit current and voltage waveforms of the SWITCH-MOS and IE-UMOSFET. It reveals that the drain current increases to more than 130 amperes (current density J~2300 A/cm^2) in both devices, and then decreases with time. The decrease in drain current was caused by the reduction in electron mobility, due to self-heating of the devices. The SWITCH-MOS failed at 6.0 µsec, 40 % sooner than the IE-UMOSFET. Further, it can be seen that the SWITCH-MOS failed about 2 µsec of after the gate was turned off. Hence, the SWITCH-MOS showed less short-circuit withstand capability. Figure 4 shows the measured short-circuit capability of a state-of-the-art 1.2 kV silicon trench field-stop (FS) IGBT. The trench FS-IGBT failure occurred 195 µsec after turn-off, when an 8.6 µsec gate pulse was applied. Precise experimental and numerical analysis of the failure mechanism has shown that significant increases in the device temperature result in thermal runaway during the blocking state, just after the short-circuit turn-off [17]. Thus, two-dimensional electro-thermal mixed-mode device simulations using Sentaurus TCAD are deployed to reveal the internal dynamics of the SWITCH-MOS [18]. Device structures used for the simulation analyses included backside thermal resistance of 0.052 cm^2 K/W to model the solder layer and packaging materials used in a conventional TO-247 package to take the transient heat flow into

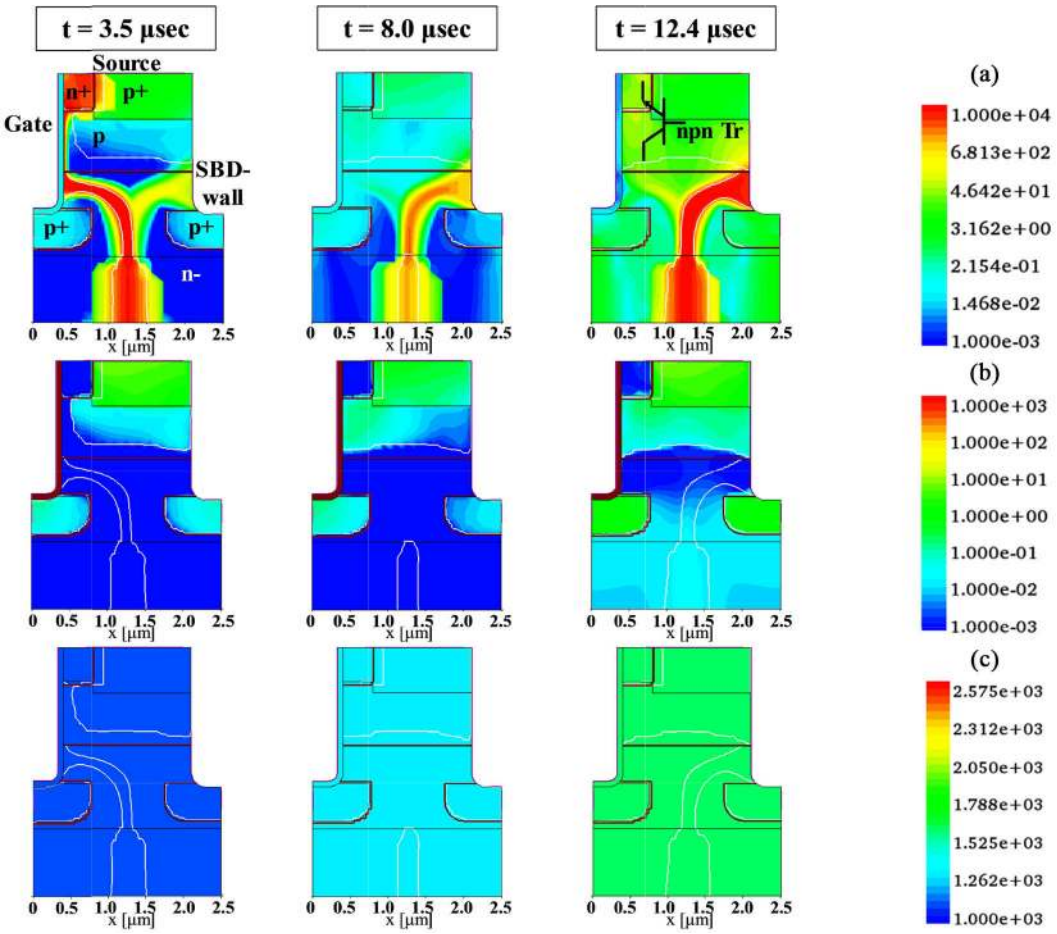

FIGURE 6. Simulated (a) total current density, (b) hole current density, and (c) lattice temperature distribution of the SWITCH-MOS ($\varnothing_b = 1.20$ eV), with varying short-circuit period, when the 4.4 µsec gate pulse was applied. The time $t = 3.5$ µsec corresponds to the time just before gate turn-off; $t = 8.0$ µsec to the time just after gate turn-off; and $t = 12.4$ µsec to the time just after the drain current rapidly increased. The results correspond to the calculated waveforms shown in Fig. 5.

account. In the present study, the thermal boundaries for the device were placed both on its front surface and backside. Figure 5 shows the simulated drain current waveforms of the SWITCH-MOS and the IE-UMOSFET in the short-circuit state, at a DC bus voltage of 800 V. As aforementioned, the Schottky barrier height in the SWITCH-MOS was set at 1.20 eV, which corresponds to the measured results for titanium as Schottky metal. It was found that the short-circuit withstand time of SWITCH-MOS was 50% less than in the simulation results. Figure 6 shows the total current, hole current density and temperature distribution for the SWITCH-MOS, which correspond to the results shown in Fig. 5. Figures 6 (b) and (c) show that, unlike in previous research results for SiC trench MOSFETs [19], just before the device is turned off ($t = 3.5$ µsec), hardly any hole current flows in the n− drift region. This is because of the low level of generated power dissipation in the device, owing to the relatively small short-circuit time. The figure reveals that the lattice temperature and current density in the SBD region increased to 1070 K and 61.8 A/cm^2, respectively, at $t = 3.5$ µsec. Furthermore, it was found from the simulation results that the electric field in the SBD region was limited to roughly 0.41 MV/cm, owing to the pinch-off effect of the depletion layer around the SBD. Thus, estimating the leakage current through the SBD with such high temperature and relatively low electric field, using Equation (1) (based on the thermionic-field emission theory [20], [21]), the calculated leakage current density J_{TFE} is 18.4 A/cm^2, which is comparable to the simulation value;

$$J_{\mathrm{TFE}} = \frac{A^* T q \hbar E}{k}\sqrt{\frac{\pi}{2m_n^* kT}} \times \exp\left[-\frac{1}{kT}\left(\varnothing_{\mathrm{b}} - \Delta\varnothing_{\mathrm{b}} - \frac{(q\hbar E)^2}{24m_n^*(kT)^2}\right)\right] \quad (1)$$

where $\hbar$ is the reduced Planck's constant ($= h/2\pi$), m_n^* is the electron effective mass in 4H-SiC ($= 0.33 \times m_0$) [22], and E is the electric field at the Schottky interface. The effective Richardson constant A^* is set at 146 (A/cm^2/K^2) [23], with a barrier height $\varnothing_{\mathrm{b}}$ of 1.20 eV, temperature T of 1070 K, and electric field E of 0.41 MV/cm, which come from the

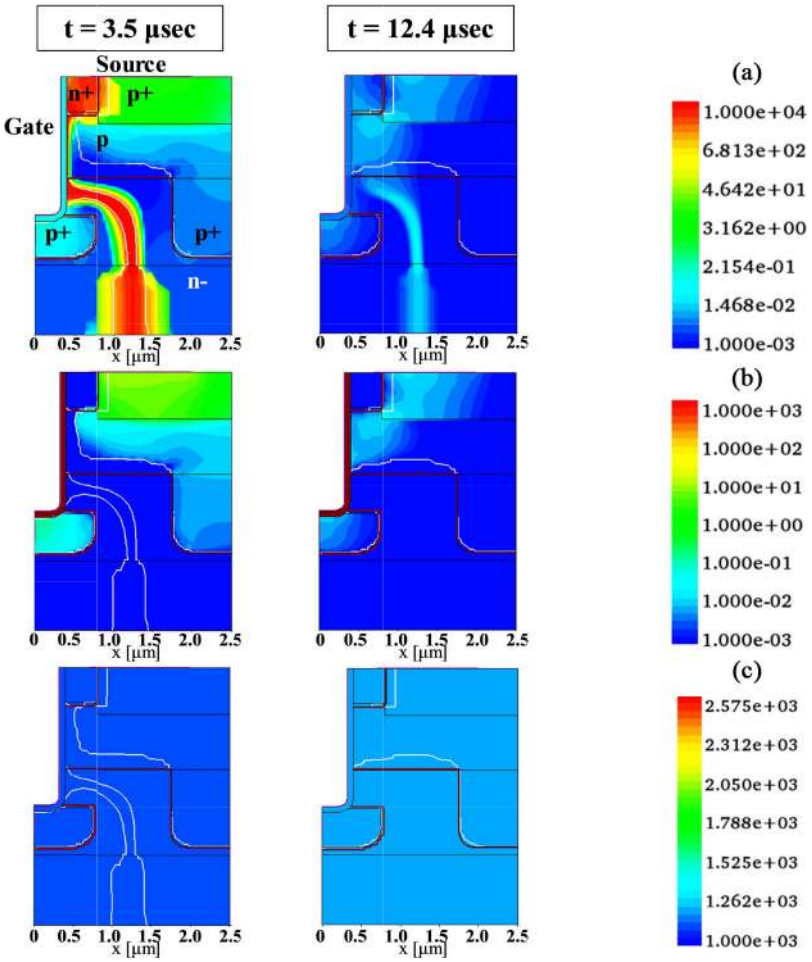

FIGURE 7. Simulated (a) total current density, (b) hole current density, and (c) lattice temperature distribution in the IE-UMOSFET, with varying short-circuit period, when a 4.4 µsec gate pulse was applied. The time $t = 3.5$ µsec corresponds to the time just before gate turn-off; and $t = 12.0$ µsec to the time just after gate turn-off. The results correspond to the calculated waveforms shown in Fig. 8.

simulation results at $t = 3.5$ µsec (Fig. 6). The $\Delta\varnothing_b$ represents the potential barrier lowering owing to the image charge induced in the Schottky metal under the zero bias. Interestingly, the figure reveals that the large emission of thermionic-field electrons does not stop, even after the gate is turned off ($t = 8.0$ µsec), so that the heat generation continues in the device, though the drain current decreases. By $t = 12.4$ µsec, the lattice temperature and total current density at the embedded SBD region increased to 1605 K and about 1200 A/cm^2, respectively (Fig. 6). The calculated leakage current density J_{TFE}, based on Equation (1), is 850 A/cm^2, with a temperature T of 1605 K and electric field E of 0.38 MV/cm, as in the simulation results at $t = 12.4$ µsec (Fig. 6). Notably, it can be seen that the parasitic npn transistor was not activated in the SWITCH-MOS, even after the rapid increase in the drain current. This is mainly because the calculated short-circuit withstand time in the SWITCH-MOS was so short (4.4 µsec) that the power dissipation to generate holes became small, resulting in reduced hole current passing through the p base near the n+ source, and thus the npn transistor did not activate.

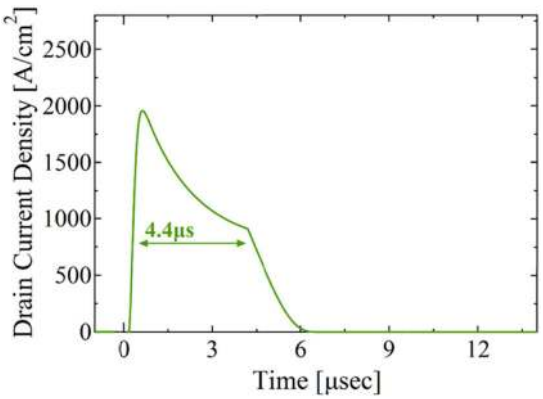

FIGURE 8. Simulated drain current of the IE-UMOSFET in the short-circuit state at DC bus voltage of 800 V when the 4.4 µsec gate pulse was applied (@V_{gs} = +15/−4 V, R.T.).

Since the high lattice temperature near the SBD region in the SWITCH-MOS was higher than the SBD processing temperature, and thus could damage the Schottky interface, the leakage current in the forward blocking state was measured,

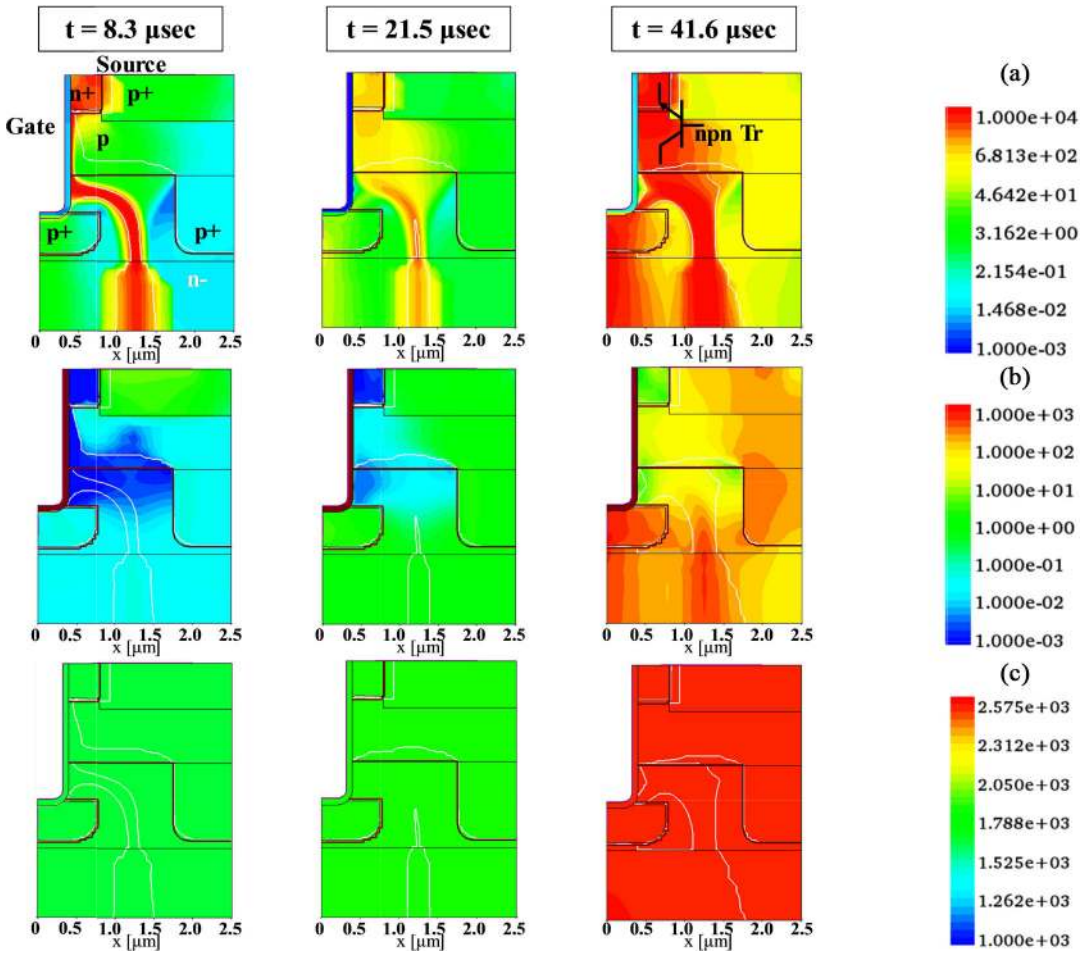

FIGURE 9. Simulated total current, hole current density, and lattice temperature distribution of the IE-UMOSFET, with varying short-circuit period, when an 8.8 µsec gate pulse was applied. The time $t = 8.3$ µsec corresponds to the time of just before gate turn-off; time $t = 21.5$ µsec to the time of just after gate turn-off and $t = 41.6$ µsec to the time just after the drain current rapidly increased. The results correspond to the calculated waveforms shown in Fig. 5.

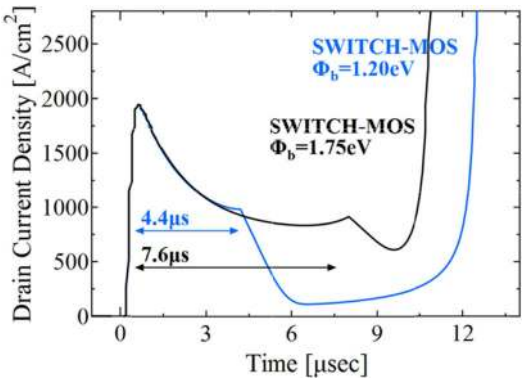

FIGURE 10. Comparison of the simulated drain current in the short-circuit state in SWITCH-MOSs with higher ($\varnothing_b = 1.75$ eV) and lower ($\varnothing_b = 1.20$ eV) Schottky barrier metal, at a DC bus voltage of 800 V (R.T.).

by using the SWITCH-MOS just after measuring the short circuit waveforms with gate pulse duration of 5.4µsec. This pulse duration corresponds to 90 % of the short-circuit capability of the SWITCH-MOS (see Fig. 3), so the lattice temperature near the SBD region could feasibly reach roughly 1070 K. The measured leakage current was 348 nA, similar to the result shown in Table 1; therefore, there is little possibility that the Schottky interface was damaged during the short-circuit test. Figure 7 shows the total current, hole current density, and lattice temperature distribution in the IE-UMOSFET, when a 4.4 µsec gate pulse was applied. The calculated drain current in the IE-UMOSFET, corresponding to Fig. 7, is shown in Fig. 8. Comparing the respective results for the total current, hole current density and lattice temperature distribution just before turning off the IE-UMOSFET and SWITCH-MOS (both at $t = 3.5$ µsec), it is clear that the results was almost identical to each other, except for the presence of the leakage current through the SBD in the SWITCH-MOS. After the gate turn-off, the MOS channel current stops flowing into the n− drift region, and the IE-UMOSFET can be successfully turned off. These results suggest that the short-circuit capability of the SWITCH-MOS with a $\varnothing_b$ of 1.20 eV is less that of the IE-UMOSFET, because the thermionic-field emission electrons passing through the embedded SBD do not stop flowing into the high electric field in the n− drift region,

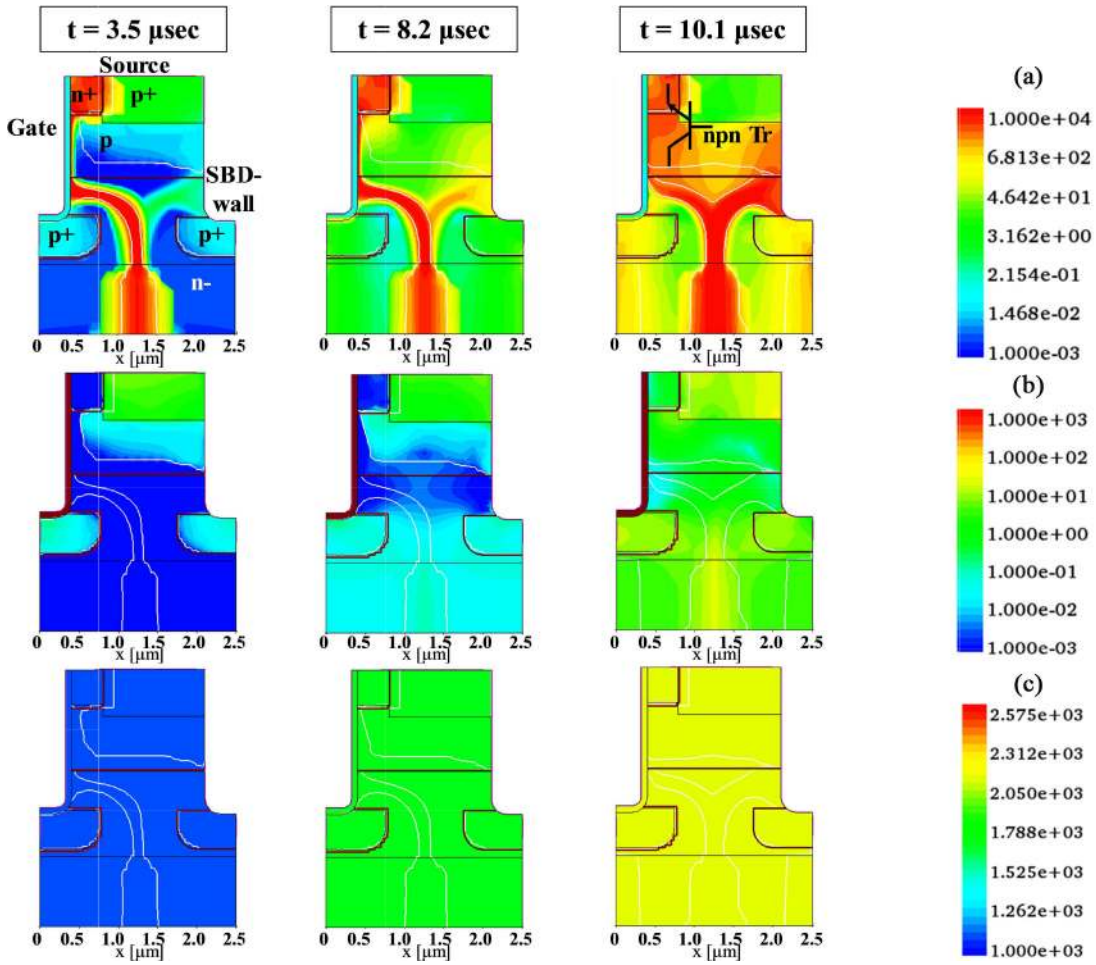

FIGURE 11. Simulated total current, hole current density, and lattice temperature distribution of the SWITCH-MOS ($\varnothing_b$ = 1.75 eV), with varying short-circuit period. The time t = 3.5 µsec corresponds to the same time in Fig. 7, for comparison t = 8.2 µsec to the time of just after the gate turn-off; and t = 10.1 µsec to the time just after the drain current rapidly increased. The results correspond to the calculated waveforms shown in Fig. 10.

owing to the high lattice temperature near the SBD region. Hence, unlike in the case of IGBT, the SWITCH-MOS leakage current as a tail current after device turn-off is caused by not the electron-hole recombination but the thermionic-field emission electrons passing through the embedded SBD described above. Further, it should be noted that the time delay between the SWITCH-MOS turn-off and device failure (as in Fig. 3) corresponds to the time required for heat to generate in the n− drift region, diffuse to the embedded SBD, and finally act to increase the emission of thermionic-field electrons. This positive feedback loop is a failure mechanism known as thermal runaway, and unique to the SWITCH-MOS. Figure 9 shows the total current, hole current density, and lattice temperature distribution for the IE-UMOSFET, when an 8.8 µsec gate pulse was applied. This corresponds to the results shown in Fig. 5. As the figure shows, the simulated lattice temperature and hole current density in the n− drift layer of the IE-UMOSFET increased more than the SWITCH-MOS, reaching roughly 1658 K and 0.05 A/cm^2, respectively, just before the gate turn-off at t = 8.3 µsec. As a result, the generated hole current being collected and passing through the p base near the n+ source region increased, activating the parasitic npn bipolar transistor at 21.5 µsec and 41.6 µsec. This mechanism is identical to that reported in [19].

TABLE 2. Dependence of calculated J_{TFE} on the barrier height $\varnothing_b$ under high temperatures using eq. (1) (@E = 0.41 MV/cm).

J_{TFE} [A/cm^2]		Temperature [K]		
		1000	1070	1140
Φ_b [eV]	1.20	8.1	18.4	38.0
	1.75	1.38×10^{-2}	4.76×10^{-2}	1.41×10^{-1}

Table 2 shows that the leakage current J_{TFE} is strongly dependent on the Schottky barrier height $\varnothing_b$, and can be reduced by more than 1/100 when $\varnothing_b$ is set at 1.75 eV, a value corresponding to the measured result for nickel on the $(1\bar{1}00)$ face of 4H-SiC wafer [24].

Figure 10 shows a comparison of the simulated drain current in the short-circuit state in a SWITCH-MOS with $\varnothing_b$ of 1.75 eV and 1.20 eV, respectively, at a DC bus voltage

of 800 V. The short-circuit capability of the SWITCH-MOS with $\varnothing_b$ of 1.75 eV was improved, and nearly comparable to that of the IE-UMOSFET shown in Fig. 5. Figure 11 shows the total current, hole current density, and lattice temperature distribution of the SWITCH-MOS with $\varnothing_b$ of 1.75 eV, which correspond to the results shown in Fig. 10. The figure reveals that the thermionic-field emission electrons passing through the SBD can be successfully suppressed. For example, at a high lattice temperature about 1085 K, at 3.5 μsec during the short-circuit transient, the thermionic-field emission leakage current can be reduced to 0.16 A/cm^2, which is only 0.26 % of the SWITCH-MOS with $\varnothing_b$ of 1.20 eV, as shown in Fig. 6. Notably, the calculated short-circuit withstand time of the SWITCH-MOS with higher $\varnothing_b$ improved to 8.2 μsec, resulting in greater power dissipation and hole generation, which increased the hole current passing through the p base near the n+ source, and finally activated the parasitic npn transistor. From these results, it can be concluded that the SWITCH-MOS short-circuit withstand capability will improve with the use of metals with a higher Schottky barrier height $\varnothing_b$. Further, it should be noted that the time delay between the high-$\varnothing_b$ SWITCH-MOS turn-off and device failure (shown in Fig. 10) corresponds to the time required for heat to generate in the n− drift region, diffuse to the embedded SBD and p base/n+ source junction in the parasitic npn transistor, and finally act to increase the emission of thermionic-field electrons and activate the npn transistor. This positive feedback loop is the failure mechanism in the SWITCH-MOS with higher $\varnothing_b$.

IV. CONCLUSION

In the present study, for the first time, an experimental and numerical investigation of a SWITCH-MOS short-circuit failure mechanism was conducted. The measured results revealed that a SWITCH-MOS with titanium as the Schottky metal had 40 % less withstand capability than an IE-UMOSFET. Further, the study showed that the thermionic-field emission electrons passing through the embedded SBD do not stop flowing into the high electric field in the n− drift region, due to the high lattice temperature near the SBD region, even after the gate is turned off; and as a result, heat generation continues to take place in the device. This heat diffuses to the embedded SBD region, and finally acts to increase the emission of thermionic-field electrons. This positive feedback loop, known as thermal runaway, is the failure mechanism of the short-circuit state, and unique to the SWITCH-MOS. Finally, it was numerically verified that the use of Schottky metals with higher barrier height can effectively improve the short-circuit capability of a SWITCH-MOS, enabling the device to be utilized in inverters with high frequency operation.

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