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First Demonstration of Ultra-Thin SiGe-Channel Junctionless Accumulation-Mode (JAM) Bulk FinFETs on Si Substrate with PN Junction-Isolation Scheme

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ABSTRACT A SiGe-channel junctionless-accumulation-mode (JAM) PMOS bulk FinFETs were successfully demonstrated on Si substrate with PN junction-isolation scheme for the first time. The JAM bulk FinFETs with fin width of 18 nm exhibits excellent subthreshold characteristics such as subthreshold swing of 64 mV/decade, drain-induced barrier lowering (DIBL) of 40 mV/V and high I_{on}/I_{off} current ratio ($>1 \times 10^5$). The change of substrate bias from 0 to 5 V leads to the threshold voltage shift of 53 mV by modulating the effective channel thickness. When compared to the Si-channel bulk FinFETs with fin width of 18 nm, Si and SiGe channel devices exhibits comparable subthreshold swing and DIBL. For devices with longer fin width, SiGe channel devices exhibits much lower DIBL, indicating superior top-gate controllability and robustness to substrate bias compared to the Si channel devices. A zero temperature coefficient point was observed in the transfer curves as temperature increases from −120 to 120°C, confirming that mobility degradation is dominantly affected by phonon scattering mechanism.

INDEX TERMS Junctionless (JL) field-effect transistor (FET), junctionless-accumulation-mode (JAM) FET, SiGe bulk FinFET, junction-isolation.

I. INTRODUCTION

THE recent scaling down of CMOSFETs poses a challenge to industrial fabrication of ultra-shallow and abrupt source/drain (S/D) junctions [1]. In response, a junctionless (JL) FET was proposed [2] and demonstrated [3] with unique features of a uniformly and homogeneously doped channel from the source to the drain. The JL FET is well known to have stronger immunity against short-channel effect (SCE) than inversion-mode (IM) FETs because it has a longer effective channel length than the physical channel length [4]–[6].

To alleviate the problems arising from the heavily doped channel of JL FET such as increased ionized impurity scattering, random dopant fluctuation, and subthreshold swing (SS), the channel concentration needs to be lowered. Such measures, however, result in an increase of the S/D parasitic resistance and a reduction of the drain current. Therefore, a junctionless accumulation-mode (JAM) FET has been developed by introducing additional S/D implantation into a JL FET [7]–[9].

To obtain a fully-depleted channel at the off state, most JL FETs have been evaluated on an ultra-thin body FET based on either a silicon-on-insulator (SOI) substrate or as a nanowire FET [10]–[12]. Although our group has demonstrated a Si-channel JAM bulk FinFET aimed at attaining threshold voltage (V_{th}) control by substrate bias (V_b), low substrate cost compared to SOI and compatibility with the standard CMOS process [13], isolated junction of Si-channel devices suffered junction breakdown under high substrate bias ($V_b > 3$ V).

Meanwhile, there have been some reports on Ge-channel JL FETs upon consideration of higher hole mobility and

improved gate electrostatics owing to higher dielectric constant of Ge in a multi-gate scheme [14]. Despite such merits of Ge channel, reported subthreshold characteristics are severely degraded due to the low quality of Ge epitaxial layer on Si substrate and inferior interface property between dielectric and channel.

In this work, a SiGe-channel JAM bulk FinFET was demonstrated on Si substrate for the first time to make use of the advantages resulting from high mobility and high dielectric constant of SiGe while achieving relatively mitigated density of the interface trap compared to that of Ge. Also, lower diffusivity of boron in SiGe makes SiGe channel a promising PMOS channel candidate beyond Si channel for JAM bulk FinFET from the viewpoints of improved SCE and robustness to substrate bias.

II. DEVICE FABRICATION

The key fabrication processes have been described including the schematic view of our JAM FET in the previous work [13]. Starting with 8-inch n-type bulk Si substrate, an undoped 15-nm-thick SiGe epi-layer was grown to be Ge composition of 30% using ultra-high-vacuum CVD. Phosphorus ion implantation for a channel-stop was performed to obtain a phosphorus concentration of 1×10^{17} cm^{-3} in the uppermost region of the underlying n-type Si. Boron ion implantation was then carried out for SiGe channel doping with a concentration of 1×10^{18} cm^{-3}. Both implant energies of the above-mentioned implantations were targeted to make a 15-nm-thick p-type SiGe channel. A photo-resist trimming technique was applied to reduce the fin width and gate length, varied from 12 to 43 nm and from 120 to 1000 nm, respectively. After gate patterning, additional S/D implantation of boron was performed for the formation of heavily doped S/D $(>1 \times 10^{20}$ cm$^{-3})$, followed by spike annealing at 1020°C for 1 second in N_2 ambient. The equivalent oxide thickness of hafnium oxide (HfO_2) and titanium nitride (TiN) gate stacks was extracted to be ~1.4 nm from a MOS capacitor as described in our previous report [13].

III. RESULTS AND DISCUSSION

Fig. 1 shows cross-sectional transmission electron microscope (TEM) images of the JAM SiGe bulk FinFETs. When the fin width (W_{fin}) was defined as the bottom width of the p-type SiGe fin, W_{fin} was measured to be ~23 nm and ~43 nm, in Fig. 1(a) and (b), respectively. Partial exposure of the underlying n-type fin was inevitable for tri-gate scheme. The fin height of the underlying n-type Si fin ranges were controlled from ~23 to ~28 nm by the wet dip process of high density plasma oxide. The total physical thickness of ALD-HfO_2 was found to be ~8 nm, comprising the HfO_2 layer of ~7 nm and interfacial oxide of ~1 nm. The secondary ion mass spectroscopy data shows a junction-isolated doping profile with a p-type channel having average boron concentration of 1×10^{18} cm^{-3} and an underlying n-type

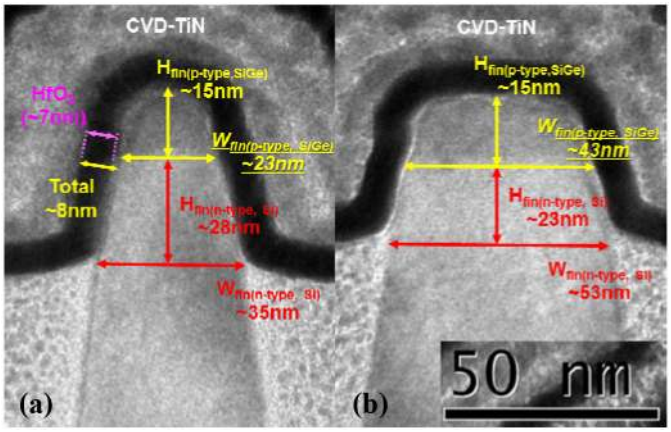

FIGURE 1. Cross-sectional TEM images of the fabricated JAM PMOS SiGe bulk FinFETs with various fin widths. (a) W_{fin} = 23 nm and (b) W_{fin} = 43 nm.

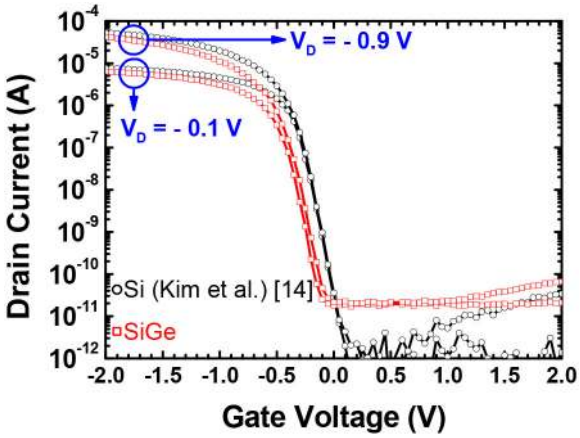

FIGURE 2. Transfer curves of the SiGe JAM device with W_{fin} = 18 nm and L_G = 180 nm compared to previously reported Si JAM device with the same physical dimension by Kim *et al.* [13].

Si of phosphorus concentration of 1×10^{17} cm^{-3} although it is not shown in this paper.

The performance of SiGe-channel JAM FinFETs was measured at room temperature using a semiconductor device analyzer (Agilent Technologies, Model B1500). Fig. 2 shows the transfer curves of the JAM SiGe device with W_{fin} = 18 nm and L_G = 180 nm, providing superior transfer characteristics such as SS_{min} = 64 mV/dec., DIBL = 40 mV/V, and I_{on}/I_{off} ratio > 1×10^5. The SS extracted from Fig. 2 remains less than ~90 mV/decade over three decades of drain current, as shown in Fig. 3.

Figs. 4 and 5 show the effect of the channel dimensions on the device characteristics. Here, $\Delta V_{th} = V_{th} - V_{th}$ (at W_{fin} = 12nm). The increase of fin width weakened the gate controllability, resulting in the increases of SS and DIBL as shown in Fig. 4. SS was relatively higher in SiGe device, because of relatively higher interface trap density than Si device. Si and SiGe channel devices shows comparable levels of DIBL for small fin width. However, SiGe channel device shows much lower DIBL for larger fin width. Such lower

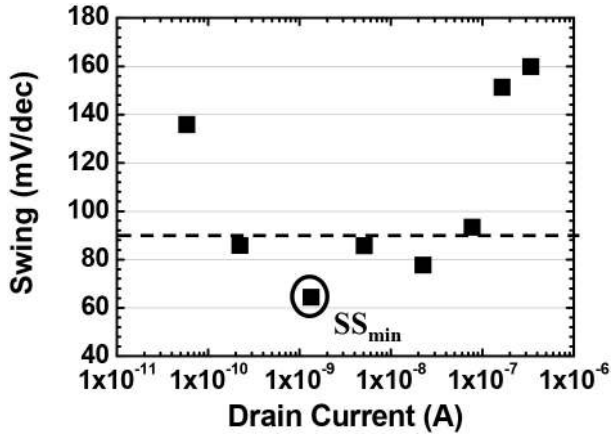

FIGURE 3. Distribution of SS measured from SiGe JAM device in Fig. 2.

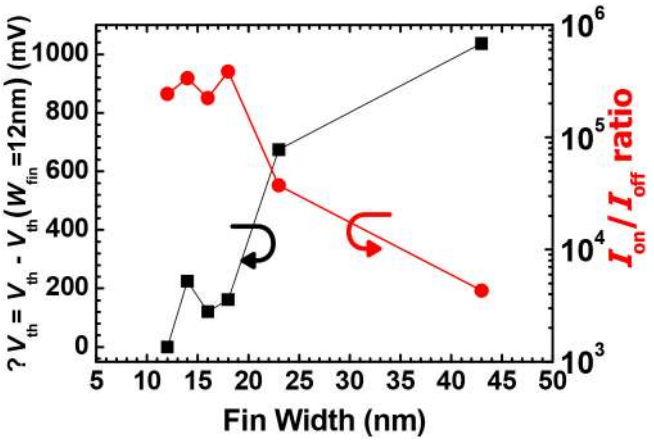

FIGURE 5. Dependency of ΔV_{th}, I_{on}/I_{off} ratio as a function of fin width at a fixed L_G = 180 nm.

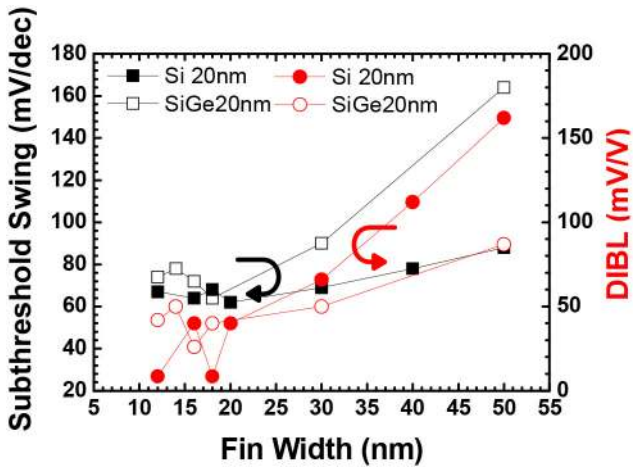

FIGURE 4. Dependency of SS, DIBL, and as a function of fin width at a fixed L_G = 180 nm.

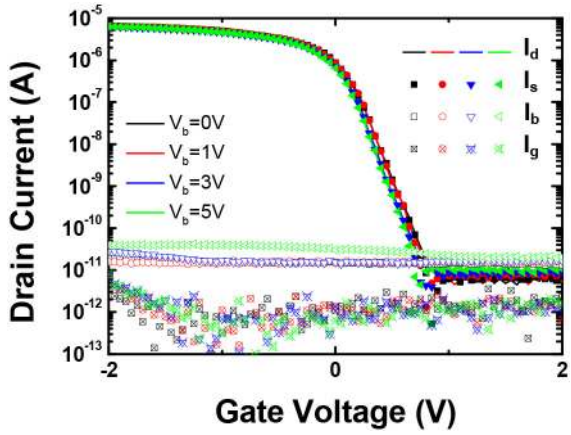

FIGURE 6. Effect of substrate bias (V_b) on transfer curves of the device with L_G = 180 nm and W_{fin} = 45 nm.

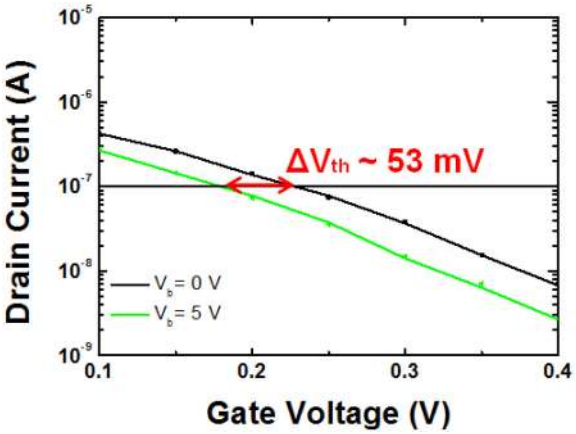

FIGURE 7. Enlarged plot of the transfer curves corresponding to V_b = 0, 5 V, respectively in Fig. 6.

DIBL in SiGe channel is explained by the higher dielectric constant of SiGe than that of Si as a channel material in FinFET structure. Also, the increase of the fin width results in a decrease of PMOS V_{th} (i.e. the increase in the amount of positive V_{th} shift) and a decrease of the I_{on}/I_{off} ratio due to an increase of SS and I_{off} current as shown in Fig. 5. The JAM devices with fin widths less than 18 nm give I_{on}/I_{off} ratio $>1 \times 10^5$. Here, SS_{min} was measured at drain voltage (V_d) = −0.1 V. DIBL has been extracted from the gate voltages corresponding to drain current (I_d) = 10^{-9} A. V_{th} was defined as the gate voltage measured at $I_d = 10^{-7}$ A. I_{on} and I_{off} have been measured at $V_{g,on} = V_{th} + 0.7 \times V_d$ and $V_{g,off} = V_{th} - 0.3 \times V_d$, where V_d = −0.9 V.

Figs. 6 and 7 show the V_b-induced behavior of the transfer curves, indicating that the increase of positive V_b causes an increase of V_{th}, reflecting a decrease of the effective channel thickness by widening the depletion width in the SiGe channel isolated by pn junction, unlike SOI or nanowire FETs. The amount of V_{th} shift by changing V_b from 0 V to 5 V is ∼53 mV as shown in Fig. 7. Here, the V_b was applied to the underlying n-type Si substrate by chuck-biasing on the backside of the wafer. The JL FET has been reported to be more sensitive to substrate bias than an IM FET because of bulk conduction mechanism [15]. It was observed that both the substrate current (I_b) and the gate leakage current (I_g) were negligible in Fig. 6. Given that I_b was less than 1×10^{-10} A, the partially exposed underlying n-type

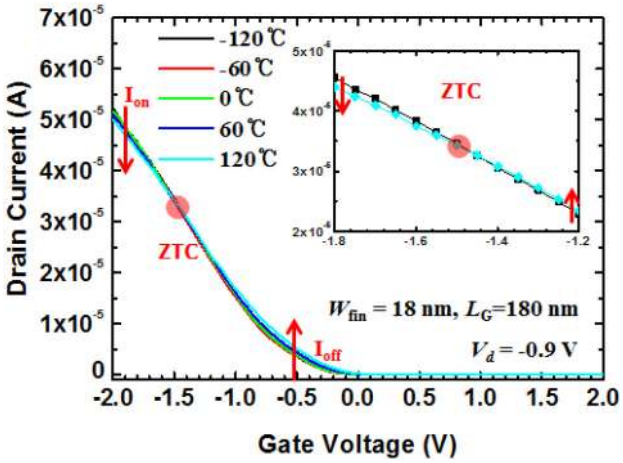

FIGURE 8. Transfer curves of the device with L_G = 180 nm and W_{fin} = 18 nm when temperature is varied from −120 to 120°C. Inset shows the transfer curves of the same device at −120 and 120°C for clear presentation of the ZTC.

TABLE 1. Parameters extracted for JAM FinFETs on bulk silicon

Channel Material	W_{fin} (nm)	L_G (nm)	SS_{min} (mV/dec.)	ΔV_{th} at $V_b = 2V$	ΔV_{th} at $V_b = 5V$
Si [13]	18	180	68	110 mV	Junction breakdown
SiGe (This Work)	18	180	64	20 mV	53 mV

Si fin did not form any parasitic channel. When compared to our previous work [13], shown in Table 1, SiGe channel device shows much lower threshold voltage variation at higher substrate bias, indicating superior top-gate controllability of SiGe device because of SiGe channel's higher dielectric constant compared to Si channel in a FinFET structure. Also, the robust junction-isolation of SiGe channel withstands over 5 V of substrate bias, much higher than that of Si channel reported in our previous work [13].

Fig. 8 shows that an increase of temperature leads to both a V_{th} decrease and SS increase, presenting the existence of a zero temperature coefficient (ZTC) point, contrary to the absence of a ZTC point in previously reported JL FETs [16], [17]. The temperature dependent performance of SiGe channel FinFETs was measured with chamber probe station (MS Probe Station, Model MST-1000B). Here, the ZTC point is the gate voltage where the drain current does not change by varying temperature, and it is important for analog circuit design with temperature stability and reliable circuit operation [17]. The conventional JL FETs with channel doping concentration of more than 1×10^{19} cm^{-3} have been reported to show temperature-independent mobility because of enhanced Coulomb scattering comparable to phonon scattering [16]. Meanwhile, the relatively low doping channel concentration $\left(1 \times 10^{18}\ cm^{-3}\right)$ of our JAM bulk FinFET was found to give rise to mobility degradation dominated by phonon scattering rather than Coulomb scattering at high temperature.

When compared with JAM Si-channel FinFETs in our previous work [13], JAM SiGe-channel FinFETs in this work show improved DIBL characteristics and low I_b under high V_b (5 V) because of their superior top-gate electrostatics and more robustness to substrate bias, respectively. As further works, gate length scaling of our SiGe-channel JAM bulk FinFETs can be reinforced by tuning either the S/D additional implant process conditions or the gate spacer material/sidewall thickness, given that JAM FETs with normal transfer characteristics have been reported down to L_G = 20 nm despite abrupt degradation of SS and DIBL [10], [11].

IV. CONCLUSION

In conclusion, SiGe-channel JAM bulk FinFETs were successfully demonstrated on Si substrate for the first time. Outstanding transfer characteristics were achieved from the JAM devices with W_{fin} of less than 18 nm. The JAM devices with various fin width give superior subthreshold characteristics resulted from enhanced top gate controllability and robustness to substrate bias compared to Si-channel-based devices. The substrate bias allowed modulation of V_{th} owing to the virtue of a body-tied FET with suppressed I_b of less than 1×10^{-10} A. A zero temperature coefficient point was observed, confirming that mobility degradation was dominantly affected by phonon scattering mechanism.

REFERENCES

[1] R. H. Dennard, F. H. Gaensslen, V. L. Rideout, E. Bassous, and A. R. LeBlanc, "Design of ion-implanted MOSFET's with very small physical dimensions," *IEEE J. Solid-State Circuits*, vol. 9, no. 5, pp. 256–268, Oct. 1974.
[2] C. W. Lee *et al.*, "Junctionless multigate field-effect transistor," *Appl. Phys. Lett.*, vol. 94, no. 5, pp. 053511–053512, Feb. 2009.
[3] J. P. Colinge *et al.*, "Nanowire transistors without junctions," *Nat. Nanotech.*, vol. 5, no. 3, pp. 225–229, Feb. 2010.
[4] J. P. Colinge *et al.*, "Junctionless nanowire transistor (JNT): Properties and design guidelines," *Solid-State Electron.*, vol. 65–66, pp. 33–37, Nov.–Dec. 2011.
[5] M. Wu, X. Jin, R. Chuai, X. Liu, and J. H. Lee, "Simulation study on short channel double-gate junctionless field-effect transistors," *J. Semiconductors*, vol. 34, no. 3, pp. 034004–034008, 2013.
[6] M. H. Han, C. Y. Chang, H. B. Chen, Y. C. Cheng, and Y. C. Wu, "Device and circuit performance estimation of junctionless bulk FinFETs," *IEEE Trans. Electron Devices*, vol. 60, no. 6, pp. 1807–1813, Jun. 2013.
[7] C.-W. Lee *et al.*, "Performance estimation of junctionless multigate transistors," *Solid-State Electron.*, vol. 54, no. 2, pp. 97–103, 2010.
[8] R. Rios *et al.*, "Comparison of junctionless and conventional trigate transistors with L_g down to 26 nm," *IEEE Electron Device Lett.*, vol. 32, no. 9, pp. 1170–1172, Sep. 2011.
[9] D. Y. Jeon *et al.*, "Low-temperature electrical characterization of junctionless transistors," *Solid-State Electron.*, vol. 80, pp. 135–141, Feb. 2013.
[10] S. Barraud *et al.*, "Scaling of trigate junctionless nanowire MOSFET with gate length down to 13 nm," *IEEE Electron Device Lett.*, vol. 33, no. 9, pp. 1225–1227, Sep. 2012.
[11] C. H. Park *et al.*, "Electrical characteristics of 20-nm junctionless Si nanowire transistors," *Solid-State Electron.*, vol. 73, pp. 7–10, Jul. 2012.
[12] D. I. Moon, S. J. Choi, J. P. Duarte, and Y. K. Choi, "Investigation of silicon nanowire gate-all-around junctionless transistors built on a bulk substrate," *IEEE Trans. Electron Devices*, vol. 60, no. 4, pp. 1355–1360, Apr. 2013.

[13] T. K. Kim *et al*., "First demonstration of junctionless accumulation-mode bulk FinFETs with robust junction isolation," *IEEE Electron Device Lett*., vol. 34, no. 12, pp. 1479–1481, Dec. 2013.
[14] R. Yu *et al*., "Device design and estimated performance for p-type junctionless transistors on bulk germanium substrates," *IEEE Trans. Electron Devices*, vol. 59, no. 9, pp. 2308–2313, Sep. 2012.
[15] S. J. Park *et al*., "Back biasing effects in tri-gate junctionless transistors," *Solid-State Electron.*, vol. 87, pp. 74–79, Sep. 2013.
[16] C. W. Lee *et al*., " High-temperature performance of silicon junctionless MOSFETs," *IEEE Trans. Electron Devices*, vol. 57, no. 3, pp. 620–625, Mar. 2010.
[17] R. D. Trevisoli *et al*., "The zero temperature coefficient in junctionless nanowire transistors," *Appl. Phys. Lett*., vol. 101, no. 6, pp. 062101–062103, Aug. 2012.

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