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First fabrication of full 3D-detectors at SINTEF

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ABSTRACT: 3D-detectors, with electrodes penetrating through the entire substrates have drawn great interests for high energy physics and medical imaging applications. Since its introduction by C. Kenney et al in 1995, many laboratories have begun research on different 3D-detector structures to simplify and industrialise the fabrication process. SINTEF MiNaLab joined the 3D collaboration in 2006 and started the first 3D fabrication run in 2007. This is the first step in an effort to fabricate affordable 3D-detectors in small to medium size production volumes. The first run was fully completed in February 2008 and preliminary results are promising. Good p-n junction characteristics have been shown on selected devices at the chip level with a leakage current of less than 0.5 nA per pixel. Thus SINTEF is the second laboratory in the world after the Stanford Nanofabrication Facility that has succeeded in demonstrating full 3D-detectors with active edge. A full 3D-stacked detector system were formed by bump-bonding the detectors to the ATLAS readout electronics, and successful particle hit maps using an Am-241 source were recorded. Most modules, however, showed largely increased leakage currents after assembly, which is due to the active edge and p-spray acting as part of the total chip pn-junction and not as a depletion stop. This paper describes the first fabrication and the encountered processing issues. The preliminary measurements on both the individual detector chips and the integrated 3D-stacked modules are discussed. A new lot has now been started on p-type wafers, which offers a more robust configuration with the active edge acting as depletion stop instead of part of the pn-junction.

KEYWORDS: Solid state detectors, Pixelated detectors and associated VLSI electronics

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1 Introduction

Near term and future experiments in high-energy physics and molecular biology will require radiation hard and fast detectors with sensitive border to cope with the increasingly stringent research requirements. Silicon 3D-detectors, with vertical electrodes penetrating through the entire silicon substrate (figure 1) have drawn high interests for these applications due to their unique advantages such as ultra-fast time response, edgeless capability and radiation hardness [1]–[9]. In addition, the through-wafer electrode technology can provide the possibility to connect 3D-detectors on a wafer level via 3D interconnects [10, 11].

The 3D-detector structure was first proposed by C. Kenney and S. Parker in 1995 [10]. Its fabrication has been possible by the developments of MEMS and VLSI technologies and the first 3D detectors was successfully fabricated by C. Kenney et al in 1997. However, the combination of 3 dimensional processing, wafer bonding and thick polysilicon deposition implies a great challenge to produce 3D-detectors in large volumes. The feasibility to transfer the technology to a production environment is therefore of great interest, but yet to be explored. SINTEF MiNaLab has several state-of-the-art Deep Reactive Ion Etching (DRIE) tools, and well-established in-house silicon processing facilities with robotic tools for cassette-to-cassette handling. This is the basis for the SINTEF MiNaLab effort to explore the possibility of small to medium size affordable 3D-detector production. The first fabrication began in 2007 at SINTEF MiNaLab after the 3D-Collaboration was established in 2006.

2 The 3D-detector structure and principle of operation

The distance between the n and p electrodes in a conventional planar silicon detector is determined by the wafer thickness. In simple terms, the induced signal generated by an ionising particle is proportional to the detector thickness traversed by the particle. In a planar detector the electrode distance equals the detector thickness, which for most applications ranges between 300 and 500 μm in order to achieve an acceptable signal-to-noise-ratio. The advantage of the 3D-detector structure shown in figure 1 is that the inter-electrode distance is independent of the wafer thickness and can be made to be as short as 50μm, resulting in much shorter average drift lengths for the generated electrons and holes upon incident radiation. Moreover, the ionisation path of the incident particle is also parallel to the collecting electrodes as shown in figure 2. Ignoring some diffusion spreading, the arrival of all charges is simultaneous, and combined with a much shorter drift length, the induced signal is much faster when compared to that in a planar silicon detector [14].

The short drift length also implies radiation hardness. Upon irradiation, the silicon lattice is damaged and defects are formed, which act as trapping sites for mobile charge carriers that are generated by the incident radiation. The effective drift length of the generated carriers therefore reduces to less than 50 μm after heavy irradiation [9], and the induced signal becomes smaller and could be lost in a conventional planar detector where the electrode spacing is typically 300 to 500 μm. In contrast to planar detectors, the inter-electrode spacing in a 3D- detector is comparable to the reduced effective drift length, while keeping the wafer thickness at 250-300 μm to maintain a good signal-to-noise ratio [9]. As a result, the signal efficiency measured on a 3D ATLAS chip with 4 electrodes per pixel (4E-configuration) is still $\approx$ 55% after irradiation to a fluence of $1.5{\cdot}10^{15}$n/cm^2, which compares to $\approx$ 25% for diamond detectors, and $\approx$ 10% for n-on-p detectors [20].

The smaller inter-electrode distance, however, implies the disadvantage of higher capacitance compared to planar detectors. For a 50x400 μm^2 ATLAS 3D pixel with 2, 3, or 4 electrodes (2E, 3E and 4E configurations, see section 4.1), the capacitances are calculated to 47 fF, 98 fF and 165 fF, respectively, for a 250 μm thick chip [21]. In comparison the corresponding capacitance for a 250 μm thick planar pixel would only be 8.4 fF. As a consequence the 3E configuration offers better signal-to-noise ratio than 4E even after irradiation to $1.5{\cdot}10^{15}$n/cm^2, but both configurations show superior performance both to corresponding diamond and planar n-on-p detectors [20].

The availability of deep reactive ion etching offers the possibility of through-wafer trenches as well as through-holes. A 3D-detector can therefore be made surrounded by a polysilicon filled and doped through-wafer electrode which provides sensitivity right up to its physical edge. In a conventional planar detector a guard ring is necessary to maintain a uniform electric field and to prevent breakdown at the chip edges, forming up to several mm of dead area. In applications where radiation hardness is not the primary concern, active edges can be used to replace the guard ring also in a conventional planar detector (planar 3D) [12].

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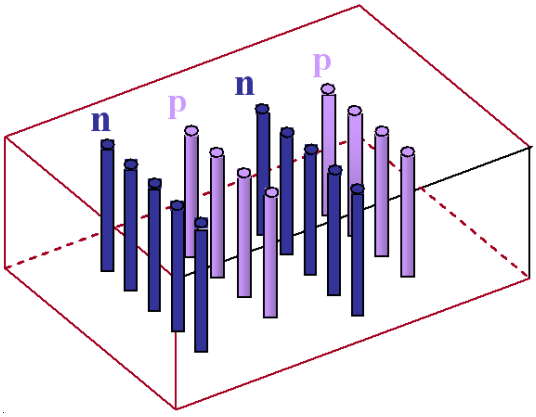

Figure 1. The concept of the 3D detector structure is to have the p and n electrodes penetrating through the entire substrate.

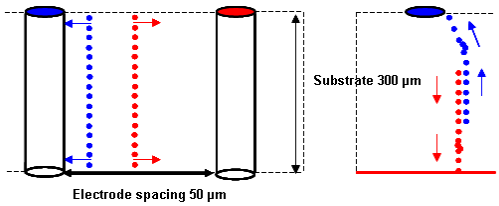

Figure 2. Collecting electrodes in 3D detectors (left) are almost parallel to the particle track and all charges generated from the track have similar collection times, while in a planar device the induced signal is spread out in time.

3 Detector fabrication

3.1 Fabrication overview

The 3D-detector structure was proposed by C. Kenney and S. Parker in 1995, and was successfully fabricated in 1997 [2]. The first 3D-detector prototype run at SINTEF MiNaLab was started in 2007, after collaboration with C. Kenney et al was established in 2006. The process developed by C. Kenney et al [2] for the full 3D structure with polysilicon filled electrodes and active edge was adapted with some modifications. The first run was started on 25 n- type (100) wafers with specific resistivity of 2000 Ωcm. The use of n-type wafers, however, is not optimal for making n-readout devices with p-type active edge, and the choice was motivated from availability at the time and the wish to start the process development.

The process consists of p-spray implant, wafer bonding, 7 lithography steps and 2 separate DRIE steps followed by polysilicon filling and doping of the electrodes. Direct fusion bonding was used to bond the process wafer to a support wafer [13], which is necessary for maintaining the wafer integrity after the trench etching. First the n-type electrodes were etched and filled, and then protected by a 3000Å thermal oxide barrier prior to the processing of the p-type electrodes. Once the electrodes were formed, a metal layer was deposited and patterned. A passivation layer consisting of 0.5 μm oxide and 0.25 μm thick nitride was then deposited by PECVD and patterned as the final step. Figure 3 summarises the full fabrication process.

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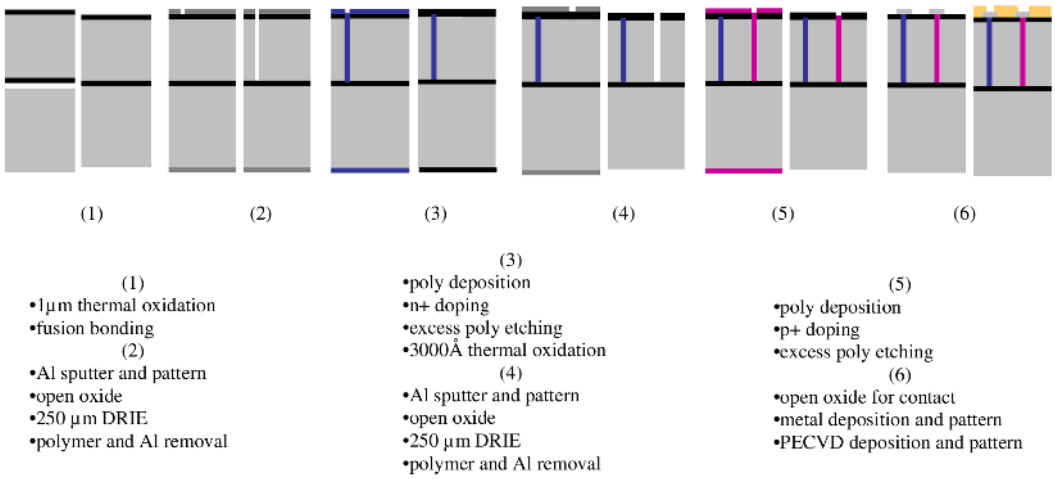

Figure 3. Summary of the fabrication process used in the first 3D-detector prototype run at SINTEF.

3.2 Deep Reactive Ion Etching (DRIE)

Deep reactive ion etching (DRIE) is the key technology in 3D-detector processing. At SINTEF MiNaLab, through-wafer holes with aspect ratios of 15 and larger were previously demonstrated [15] using an Alcatel AMS-200 etcher [16] with a modified Bosch Process [17]. The process parameters are usually tuned according to the requirements for each specific application. The 3D detector design has circular through-wafer electrodes with a diameter of 14μm. Aluminium, 1.5μm thick was used as the etch mask and was patterned using standard lithography. Once patterned, the holes in the aluminium mask became 16 μm wide due to the isotropic nature of a wet chemical etch. The holes were further widened to 18 μm after the DRIE process, giving an overall aspect ratio of 14. Figure 4a shows a SEM image of 250 μm deep through holes in a 500μm thick test wafer. Considering the measurement error, both the bottom and the top of the holes had a diameter of approximately 18 μm, with satisfactory cylindrical profiles. All polymer residues from the etching process were removed by O_2 plasma stripping and the aluminium mask was removed by a piranha rinse.

The same process was then applied to a 250 μm thick process wafer bonded to a 350 μm thick support wafer. The etching profiles were similar (figure 4b) to those obtained in the test wafers, except at the bottom of the holes. Once the process wafer was etched through, the 1 μm oxide situated between the process wafer and the support wafer was charged up by excess ions. The oxide charge then deflected the etching ions, and the ions began etching the sidewalls. This excessive lateral over-etching resulted in severe notching at the hole bottoms, as shown in figure 5b. Such notching could form regions of high electric field, and could easily result in high leakage current and low breakdown voltage. Several test runs were necessary to tune the process parameters, and it was also necessary to modify the etch gas control system. Figure 5a shows how the notching was reduced in the final process.

3.3 Polysilicon deposition

The n and p-type electrodes were formed by filling the through-holes with highly doped polysilicon. A layer of 1 μm thick polysilicon was first deposited at SINTEF and doped from a gas-phase

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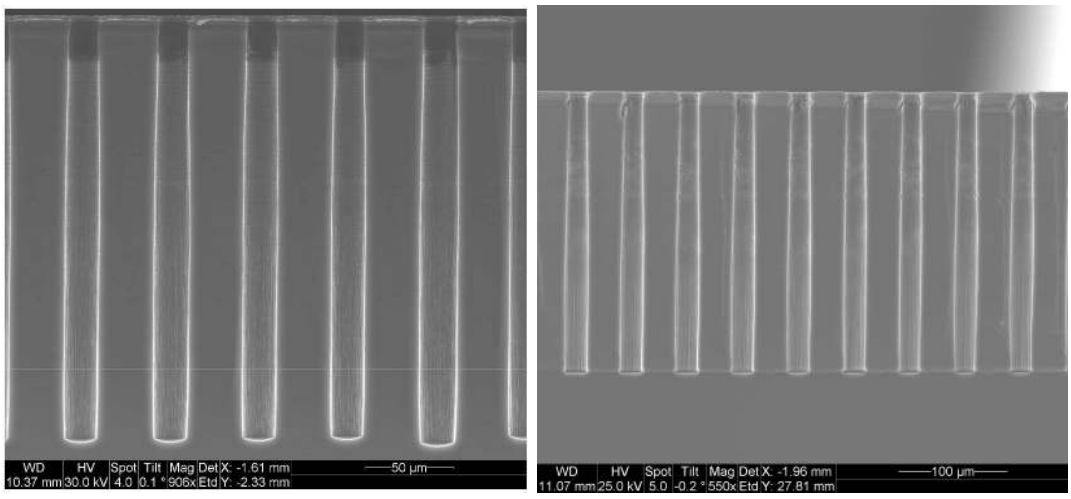
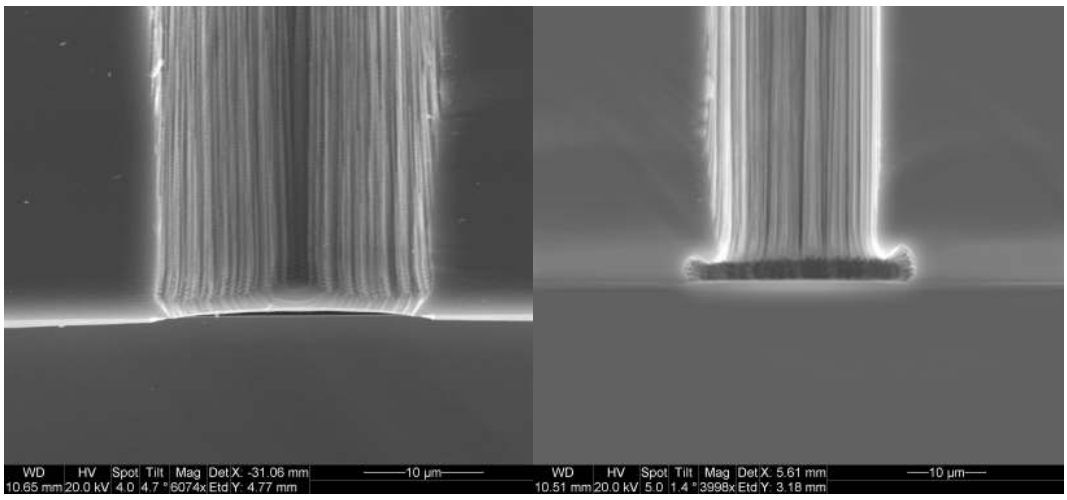


(a) (b)

Figure 4. (left): Cross section of 250 μm deep circular holes in a 500 μm thick test wafer. (right): Cross section of through holes in a 250μm thick wafer bonded to a support wafer.



(a) (b)

Figure 5. (left): A very smooth profile at the bottom of the hole attached to the support wafer after process tuning. (right): Severe notching was observed before process tuning.

source. The facilities at SINTEF MiNaLab is currently limited to deposit polysilicon layers of ≤ 1 μm thickness at a time, and the time for the complete electrode filling was estimated to a minimum of 70 hours. The completion of the n- and p-electrode filling was therefore done at the Stanford Nanofabrication Facility where our collaborators are able to deposit polysilicon layers up to 2 μm at a time. Figure 6 shows the cross sections of the filled electrodes. Although the polysilicon deposition is known to be rather conformal, voids and keyholes are seen, mostly caused by the variation in the etching profiles.

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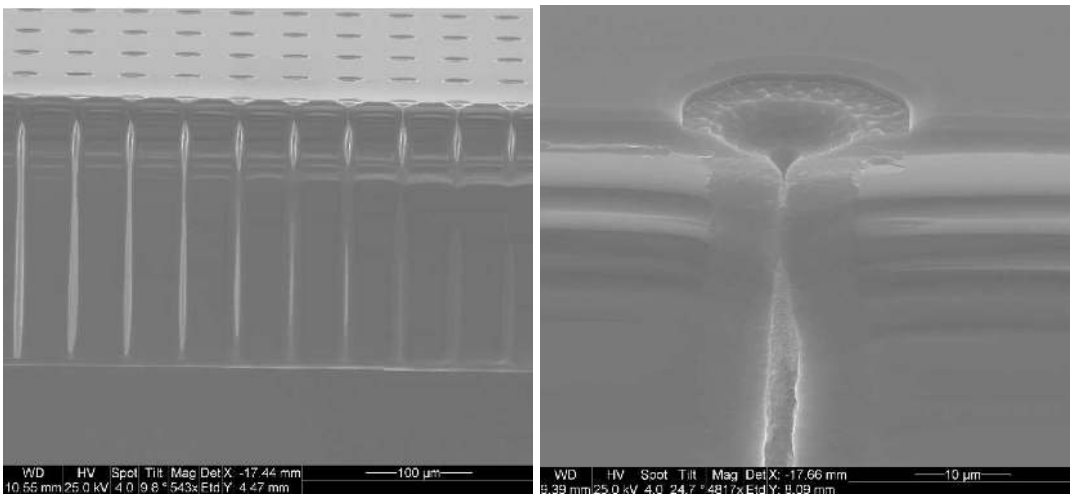
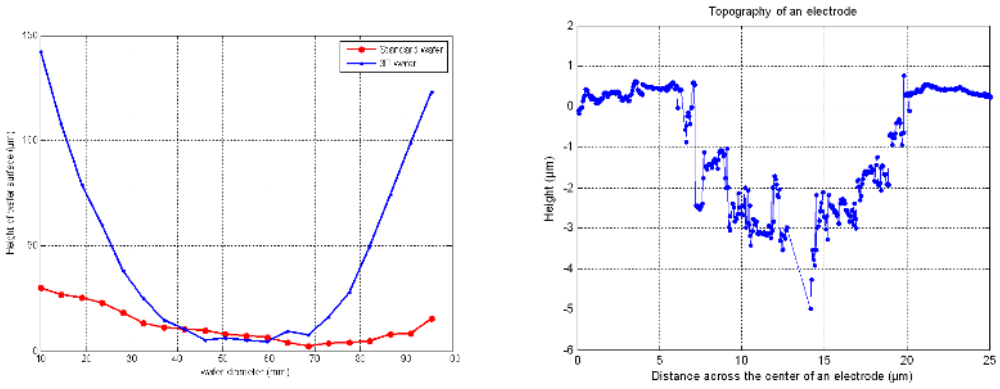


(a) (b)

Figure 6. (left): Due to the holes profile, a void in the poly is observed in the cross section of the filled through holes. (right): A cross section which shows the topography on the top of the hole after the removal of poly on the surface using plasma etching. The void in the poly is also clearly observed.



(a) (b)

Figure 7. (left): A 3D wafer after polysilicon deposition bowed at a curvature 10 times larger than a pre-processed standard silicon wafer. (right): The profile of a filled hole was measured by a laser interferometer, showing the lowest point of the hole is about 5 μm below the surface of the wafer.

3.4 Fabrication issues

The most serious fabrication issue was high mechanical stress induced in the wafers during electrode filling due to an uneven oxide distribution between the front and the back sides. It follows from figure 7a that the warping of a 3D wafer compared to a standard pre-processed wafer is about 10 times larger. Handling excessively warped wafers using robotic tools is difficult with the result of several damaged wafers and significantly reduced yield. Thus we had to resort to manual handling. Another problem caused by warping was the difficulty in achieving accurate alignment in subsequent lithographic steps as demonstrated in figure 8.

Besides the warping issue, lithography also became a challenge after the polysilicon deposition due to the difficulty in spinning a conformal layer of resist over a surface with high topography,

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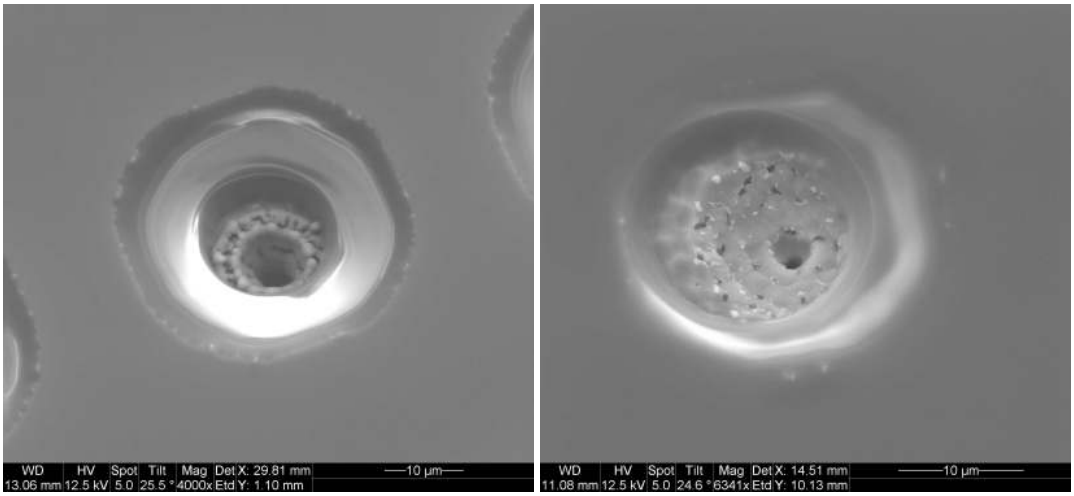

(a) (b)

Figure 8. (left): The resist opening was well-aligned with the wafer pattern in certain area of the wafer. (right): The curvature of the wafer made alignment quality vary across the wafer. Misalignment was clearly observed on the same wafer while some area was well aligned.

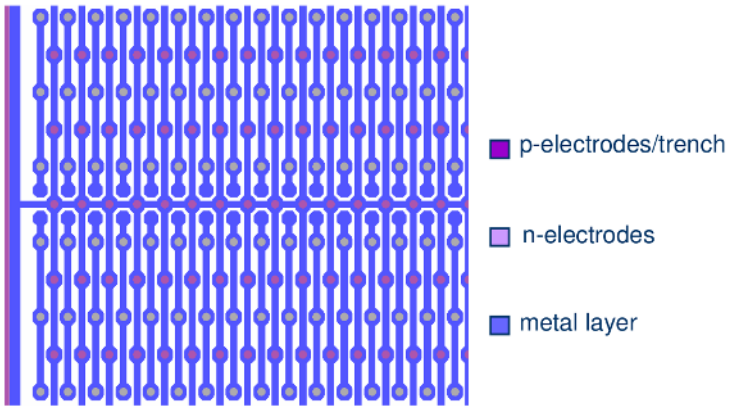

Figure 9. A sketch showing the layout of a 3E chip. The pixel is formed by a metal line joining 3 n-type electrodes together. The wafer included 3 different electrode configurations, with 2, 3 or 4 electrodes per pixel (2E, 3E, 4E). The IV characteristics can vary depending on the number of electrodes per pixel.

as shown in figure 7b. The topography was measured using a laser interferometer and the lowest point of the poly-filled electrode was about 5 μm below the wafer surface (figure 7b).

4 Results and measurements

4.1 IV measurements

Despite the fabrication issues and the required process developmemt, the first run of 3D-detectors was fully completed by February 2008. As these are n-readout devices made on n-type wafers, the p-electrodes and the active edge on one chip are all connected, and when probing on one pixel the total chip dark current is measured. Thus IV measurement was made by simply connecting

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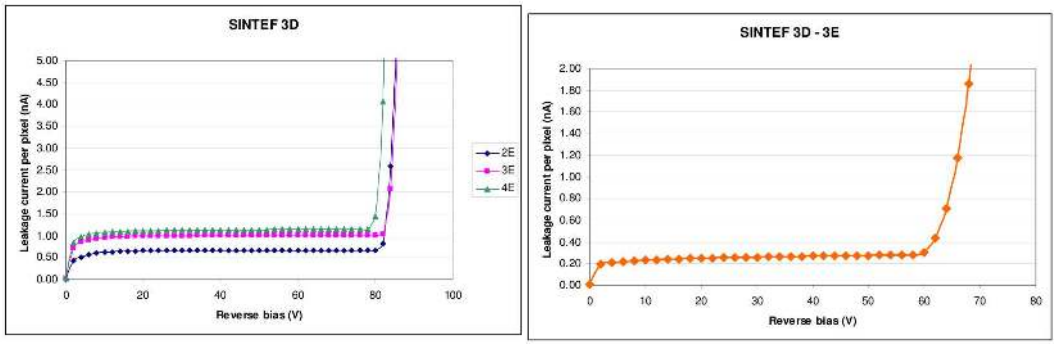

(a) (b)

Figure 10. (left): IV curves measured on 3 detectors with different electrode configurations. The leakage current varies between 0.5 and 1.2 nA per pixel once fully depleted. (right): An IV curve measured on a pixel consists of 3 electrodes and the leakage current is lower than 0.5 nA.

the p-type electrodes including the active edge to ground and applying high voltage to one n-type electrode. However, the disadvantage is that defect pixels can not be directly identified.

The IV characteristics at the wafer stage have been measured on detectors with 3 different electrode configurations. These are ATLAS type chips with 50 x 400 μm^2 pixel size, and each pixel may include 2, 3 or 4 n-electrodes. Accordingly, the chips are termed 2E, 3E or 4E, with n- to p-electrode distances of 106, 76 or 54 μm. The corresponding calculated depletion voltages for devices made on the wafers used in the first run are $\leq$ 27 V, $\leq$ 13 V and $\leq$ 7.5 V. The layout of a 3E device is shown in figure 9.

The IV characteristic can vary depending on the number of electrodes per pixel. Figure 10a shows the IV curves measured on one 2E, one 3E and one 4E device. The measured leakage currents is the average over all 2700 pixels on one chip and varies between 0.5 and 1.2 nA per pixel including possible bad elements. The breakdown voltage is about 80V for all 3 devices, which is $>$ 10 times the depletion voltage for the 4E device. Figure 10b shows the IV characteristic of a particularly good detector with a leakage current of less than 0.5nA.

4.2 Inter-pixel resistance

The inter-pixel resistance between neighboring pixels was measured at 60V bias, which ensures that the devices are over-depleted. The bias voltage was applied to three pixels, with the p-type electrodes and active edge connected to ground. A small voltage of 0.2V was superimposed on the bias voltage on two of the biased pixels, and the inter-pixel resistance was then calculated from the resulting lateral current. Table 1 summaries the measured inter-pixel resistance for the 3 different electrode configurations, and for a test baby strip structure on the same wafer. The results are encouraging as high inter-pixel resistances were measured for all four structures. It follows that the inter pixel resistance depends on the electrode separation and the pixel pitch.

4.3 3D Stacking — Preliminary results

10 detector chips were selected for further characterisation using the standard readout electronics for the ATLAS experiment [18]. Each chip was bump-bonded to the ATLAS FE-I3 readout chip

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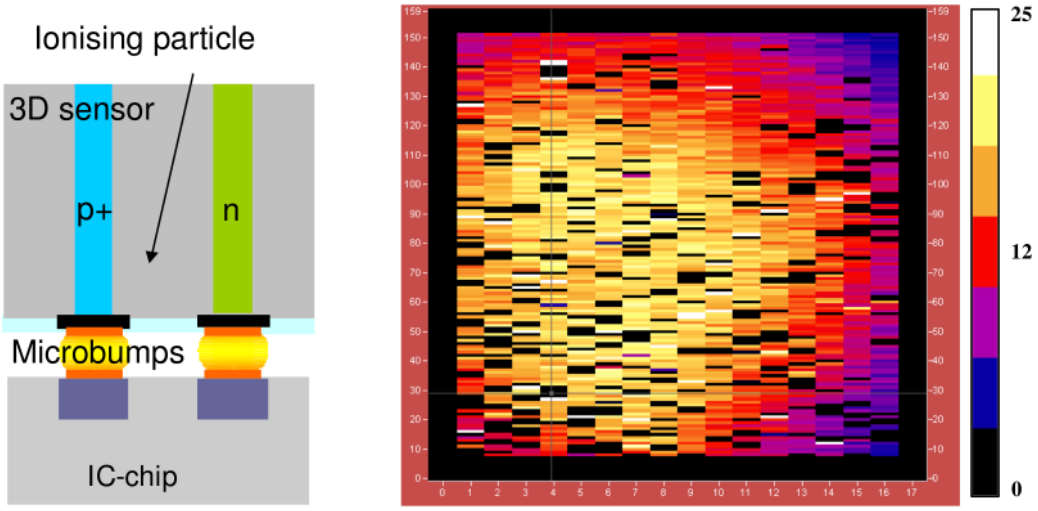
Table 1. The inter-pixel resistance measured on different structures.

Pixel Arrangement	n- to p-electrode separation (μm)	pixel pitch (μm)	Inter-pixel resistance (MΩ)
2E	106	50	600-800
3E	76	50	300-500
4E	54	50	100-300
Test structure	100	200 (strip pitch)	6000-7000



(a) (b)

Figure 11. (left): Sketch of 3D detector chip mounted on top of a readout IC using micro-bumps. Every p+ and n+ channel is interconnected directly to the readout circuit. (right): A particle hit map recorded by a 3D detector bump-bonded to the ATLAS readout chip using an Am-241 radioactive source. The colour bar on the right indicates the number of hits recorded in each square, each representing one pixel.

using micro-bump technology [19] as illustrated in figure 11a. The performance of these modules is still under study, but most of the modules showed strongly increased leakage current compared to before bump-bonding. One probable reason is that in the present configuration with n-readout devices made on n-type wafers, the p-doped bias electrodes represent the pn-junction. Thus all the chip pn-junctions are connected and this also includes the p-doped active edge and the surface p-spray. The depletion layer will then spread out from the active edge to the non-passivated saw cut originating from the wafer dicing, and where high leakage current is generated. This assumption is supported by measurements on chips after dicing. Chips with large distance from the active edge to the saw cut showed no significant increase in leakage current, while chips with the saw cut close to the active edge showed largely increased leakage. Thus the increased leakage may be a result primarily of the dicing and not the bump-bonding. The dicing also implies sawing through the p-spray, which is part of the chip pn-junction, and which make the chips even more vulnerable.

One module was tested using an Am-241 source and particle hits were successfully recorded, as shown in figure 11b. The number of particle hits recorded by each pixel is indicated by the colour of the pixel square. The purpose was demonstration only, and no other data was taken.

Surprisingly the bias required to give low noise readout was much higher than expected from the chip calculated depletion voltage. The effect is not fully understood, especially as CV measurements at the chip level show depletion voltages in compliance with the calculated values in section 4.1. As a consequence the module had to be operated at a bias higher than 60 V to give low noise readout signals, and after about one day of operation the module broke down. The same behaviour was seen on other modules.

5 Conclusions and future work

Full 3D-detectors with active edge were successfully fabricated in the first prototype run at SINTEF MiNaLab. Measured results at the wafer stage show good diode characteristics with leakage currents of less than 0.5 nA per pixel on selected devices, and with breakdown voltage typically $\geq$ 80V. Thus SINTEF is the second laboratory in the world after Stanford Nanofabrication Facility that has succeeded in demonstrating full 3D-detectors with active edge.

Detector modules were made using micro-bump technology to mount 3D-detector chips on the ATLAS FE-I3 readout chip. Preliminary particle hit maps using an Am-241 source was successfully recorded. Most modules, however, show, largely increased leakage currents after dicing and bump-bonding. The reason is that the active edge is part of the chip pn-junction such that the depletion region spreads out to the non-passivated saw cut originating from the chip dicing. One surprising result was that the bias required to give low noise readout is much higher than expected from the calculated depletion voltage and CV measurements at chip level. The modules had to be operated higher than 60 V and some modules were irreversibly damaged after several hours of operation.

The results show that fabricating n-read out devices with active edge on n-type substrates is far from optimal. This was also expected from the start, and use of n-type wafers was due to availability at the time and the wish to get started with the process development. A new lot has now been started on p-type wafers, which offers a more robust configuration with the active edge acting as depletion stop instead of part of the pn-junction. In addition to ATLAS devices, the wafer layout includes CMS and Medipix devices. Learning from the first lot, process steps have been implemented to reduce warping and improve the topography. Thus we hope to demonstrate 3D-detector fabrication in a semi-automatic fashion with satisfactory yield. If successful, SINTEF will offer the possibility to produce high-performance and radiation hard 3D-detectors at an affordable cost for large silicon detector systems such as the ATLAS inner tracker at CERN. However, it is still an expensive technology and SINTEF has estimated that the cost of full 3D detectors in medium volume production will be between 2 and 3 times the cost of planar silicon n-on-p detectors in the same production volume.

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