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First operation of a 72 k element hybrid silicon micropattern pixel detector array

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Abstract

We have constructed and tested silicon pixel detector arrays of 96 x 378 (36288) sensor elements with 75 μm x 500 μm area. The low noise signal processing circuit associated with each element occupies an identical area on a bump-bonded readout chip. The pixel cell response for ionizing particles is binary with an adjustable threshold between 4000 e^- and 15000 e^-. Single chips, the array of 6 ladders and a double array have been characterized in particle test beams and in the Omega experiment WA97 at CERN. The two arrays together, staggered by ~4 mm cover hermetically a 53 mm x 55 mm area with 72576 pixels. The proportion of properly functioning pixels was 98% in the first 36k pixel array and 80% in the second. The ~ 1% "always-on" pixels could be masked electronically. After masking the rate of "spurious noise hits" was $< 10^{-8}$ of the identified particle hits while with beam off no hits at all were recorded. With a beam trigger most events consist of a single cluster with a single hit. At the 8000 e^- threshold an efficiency > 99% was measured. Tracks were reconstructed with a precision of 22 μm. The proportion of double hits (~ 11%) depends only slightly on threshold and detector bias voltage, and for these double hits a precision of 10 μm on the particle position was obtained.

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1. INTRODUCTION

The first fully operational hybrid silicon micropattern particle detector assemblies with 1006 sensitive pixels, which contain a low-noise signal processing circuit within the 75 μm x 500 μm area of every single pixel have been used already at the end of 1991 in the 'Omega-Ion' experiment WA94 at CERN [1] which was the predecessor of the current experiment Omega WA97. Now we have constructed two detector arrays each with 96x378 i.e. 36288 pixel cells, covering a 53 mm x 55 mm area.

The silicon detector chips and the chips with the readout circuits are made on separate silicon wafers and are connected in a "hybrid" assembly using solder bump bonding. The readout chip consists of a matrix with 16 columns and 63 rows together with a test row at the top and some peripheral electronics at the bottom. Such a readout chip can be assembled with a single high resistivity silicon detector chip with identically corresponding geometry, or six readout chips can be placed side by side on a common detector matrix called "ladder". This ladder has 96 columns and 63 rows of detecting elements. A complete array with 6 ladders is illustrated in fig. 1 and it carries 36 readout chips. Two such arrays together, staggered by ~4 mm cover hermetically the 29.15 cm^2 area with a total of 72576 detector elements.

First we have separately studied the performance of the new single chip assemblies with 1008 cells using a telescope arrangement in the CERN H6 120 GeV pion beam. In the following step we have tested the arrays of 6 ladders, using the test row with electrical input on each chip. Then we have used electrons from a radioactive source to study the response of the pixel cells and we have measured efficiency and overall performance in the CERN T9 test beam. Finally, a complete detector plane of two arrays has been operated in WA97.

The driving force behind pixel detector development is the high intensity, high rate particle physics experiments which are expected around the year 2000 [2], e.g. at the proposed Large Hadron Collider LHC, where a true 2-dimensional microdetector will enable efficient and fast pattern recognition and can provide a desirable improvement in selectivity for various types of reactions. Our aim is first to prove the feasibility of the micropattern detector concept in the Omega WA97 heavy ion fixed target experiment rather than pushing immediately for the more demanding designs for such future experiments. It is important to encounter and solve practical problems associated with building a micropattern detector in a real particle physics application. A second reason for the cautious approach is to increase the level of confidence and support in the particle physics community for what is still considered an exotic detector. At the same time, if the micropattern detector is shown to function well, it could provide easier access to various types of more immediate phycics research in beauty factories, heavy ion colliders, etc. Finally, the concept of the micropattern detector looks very promising for applications like high speed or energy-resolved X-ray imaging [3].

2. DESCRIPTION OF THE HYBRID PIXEL ARRAY

The photograph in fig. 1 shows the pixel array together with the intermediate readout electronics card and the VME readout module. This system was installed in October 1993 in the T9 test beam and in November in the WA97 Omega heavy ion experiment.

2.1 The silicon detector ladders

The detector "ladder" is the building block of the array and consists of a "chip" of high resistivity n-type silicon (~5 kΩcm) with dimensions 54 x 6 mm^2 and ~300 μm thick. It is organized as a matrix of 96 columns and 64 rows of independent, ion-implanted rectifying diodes of rectangular shape. The dimensions of most of these diodes are 500 μm x 75 μm. The cells in the columns which correspond to the left and right edges of the readout chips are twice as long, 1000 μm instead of 500 μm, in order to "stitch" the two regions of coverage together. This is illustrated in the photograph of fig. 2 which shows the right-hand one-third of the front side of the detector chip. Each diode can be DC connnected by a tiny solder bump to a virtual ground via its front-end amplifier circuit on the associated readout chip. The complete matrix is surrounded by an ion-implanted guard ring diode which also is grounded via the readout chips. The rear side of the detector wafer is ion-implanted in order to obtain a common n+ ohmic contact without segmentation. The bias voltage, typically 40 to 70 V is applied to this rear side of the ladder and the usual bias filter network is placed on the ceramic substrate besides each of the ladders. The layout of this ceramic support for 6 ladders is shown in fig. 3.

Ten detector ladders are manufactured on a 100 mm diameter wafer, together with detectors with only 1024 diode cells for a single readout chip, and a few test structures. The reverse diode leakage current for the detector ladders is typically a 5 nA cm^{-2} at 50 V applied bias and can be measured only after assembly of the ladder. It is virtually impossible to make reliable contacts to all ~6000 diodes on a ladder without bump-bonding. The detector wafer quality, however, was checked before the bump-bonding step by measuring several test diodes of 1 cm^2 .

2.2 Assembly by bump-bonding

The deposition of the various metal layers and the forming of the Pb-Sn solder bumps on the readout wafers was performed by GEC-Marconi Materials Ltd at Caswell [4]. Reflow results in hemispherical bumps with a diameter of 38 μm [1]. After dicing of the wafers, previously selected readout chips are aligned with the detector chip on a flip-chip bonding machine and the components stick together temporarily. The definitive bonding is achieved by heating the chips in an oven above the eutectic temperature of the solder (183 °C). The precise alignment of the chips is facilitated by the surface tension in the molten solder which adheres to the wettable metal pads on both sides but does not wet elsewhere on the chips. After bonding the height of the

bumps is ~13 μm. The averaged amount of solder between the chips represents 0.4 μm of Pb-Sn or 0.006% of a radiation length which is a small fraction of the total thickness of 1.2 mm or 1.15% radiation length of the present array. Development is under way which aims at reducing the thickness of the array.

During the development of the detector arrays already over 500 chip placements have been made involving the production and inspection of over a million bumps. The failure rate in the bonding is better than 10^{-3} and could be further improved by enhancing the already existing quality inspections at critical steps. Some of the observed failures were related to debris or dust particles deposited well outside the matrix of bumps and which prevented the chips to mate properly. We have not yet found means to distinguish a faulty electronic pixel circuit from a faulty bump connection and therefore the yield numbers represent the combination of both phenomena.

2.3 Mechanical construction and electrical connections of the array

The pixel detector array has to provide hermetic coverage of an area of 5 x 5 cm^2 but this is difficult to achieve with a single plane because of the need for electrical connections to each of the readout chips. We have chosen to cover the full "logical" plane using 2 staggered arrays as illustrated in fig. 4. The support plate for each array is a 380 μm thick ceramic substrate with thin-film metal conductors which act as the connection lines for all readout chips, already shown in fig. 3. The building block for the array, the detector "ladder" carries 6 readout chips which are bump-bonded to the individual detector diodes as described before. The common electrical connection supplying Vss to the rear side of these readout chips is provided by a 55 mm long and 250 μm thick ceramic slab which is metallized facing the readout chips. The slab isolates the chips from the conductors on the ceramic support and provides a homogeneous surface for glueing the ladder in place. A schematic drawing with one complete ladder-assembly and its connections is shown in fig. 5. The 6 ladder-assemblies are placed side by side on the thin-film ceramic substrate with a space of a few mm in between. Using a special table with x, y, z and rotational movements one achieves a precision of ±10 μm. After positioning the ladder is secured in place by temporary fixtures. The epoxy glue is cured in an oven at 60 °C for several hours. A ceramic support with the first ladder positioned and secured can be seen in fig. 6. In this way the mounting of a full array took ~one week.

After all 6 ladders have been glued the external electrical connections are made between the buslines on the ceramic and the bonding pads on the readout chips using ultrasonic wirebonding as can be seen in fig. 7. In this close-up one may see the readout chips just stick out from underneath the detector ladders. The bias connections to the detector ladders are made by wirebonding to the rear side of the ladders. A photograph of a completed array is shown in fig. 8.

Finally, each array is fixed on a U-shaped, 1 mm thick ceramic plate of outer dimensions 132 mm x 132 mm. This U is the handling unit that is placed on the optical bench for the silicon detectors in the Omega spectrometer. The smaller, thin ceramic support plate braces the 7 cm wide, open center of the U and a flexible, multilayer circuit is glued onto the lower part of the U-ceramic, clearly visible in fig. 1. This flexible circuit brings the supply voltages and the 32-bit data bus lines from the intermediate readout card onto the ceramic. Some of the distribution and decoupling of the voltage supplies is situated on this flexible circuit. A flat cable provides the connection between the intermediate readout card and the VME card in the control room, about 30 m away. This VME card will be described in sect. 2.5.

2.4 Frontend electronics, threshold calibration and timing

The electronics readout chip is named Omega2 and it operates at low power, ±1.5 V. As shown in the schematic of fig. 9 each pixel cell contains a low-noise frontend amplifier followed by a comparator with adjustable threshold, a delay line, coincidence circuit and memory element. This stores the bit that indicates a particle "hit" during the time frame that was selected using an external strobe signal in coincidence with the presence of this "hit". Schematic and layout are similar to the Omega-D chip for which the details have been described earlier [1]. Several parameters of this readout circuit can be adjusted externally and usual operational values are indicated in table 1. Both integrated circuits have been made in the 3 μm Self-Aligned Contact CMOS (SACMOS3) technology of Faselec, Zurich, which offers a very dense layout, actually comparable to an effective 1.5 μm circuit technology.

Table 1 Normal operational parameters of Omega2 readout chip

Externally adjustable parameter	Symbol	V/ μA
ground reference	gnd	1.5 V
+ supply voltage	Vdd	3.0 V
- supply voltage	Vss	0.0 V
frontend amplifier bias	Iqa	- 80. μA
frontend amplifier bias	Idis1	30. μA
comparator threshold	Idis2	36. μA
internal "pipeline" delay	Idn	8. μA
leakage current compensation	Ifn	-3.5 μA
detector bias voltage	Vb	50. V

The comparator threshold setting in each pixel depends on the current source Idis2 which can be adjusted via an external bias voltage. Because this current source also supplies the frontend amplifier its response varies at the same time and this causes non-linearity in the threshold as a function of bias voltage. Realistic average values for the threshold are between 4000 and 15000 equivalent electrons at the amplifier input. In fig. 10 the threshold for a single chip is shown as a function of the effective value of the current Idis2. The threshold curve (at 50% response) is measured for single pixels, using the row of 16 test pixels at the top of each matrix which can be pulsed via a built-in capacitor. In the same fig. 10 absolute calibration points are shown which are obtained from normal pixels connected to the detector matrix using photon-emitting radioactive sources of ^{109}Cd, ^{241}Am and ^{57}Co. A good correspondence between the electrical test and the absolute calibration is found if we assume an injection capacitor value of 30 fF which is 50% higher than the designed value of this parasitic field oxide capacitor. At the same time an absolute calibration of the noise of the complete detector with associated electronics could be performed with the ^{109}Cd source and 170 e^- r.m.s. or 1.4 keV FWHM has been measured [5].

From the layout of the ceramic support illustrated in fig. 3 one can see that the 6 chips in a column of the detector array have common power supplies for all the functions, like gain, threshold, delay, etc. It can be expected that if a bad chip would corrupt a supply line all the other chips on the same line may misbehave. In fact, externally on the VME card there is only a single settable value provided for each parameter for the whole array. Therefore, prior to bump-bonding all chips have been tested on wafer in order to ascertain that the DC values are compatible within small tolerances as will be discussed in sect. 2.6.

The threshold for a 6-ladder array is plotted as a function of Idis2 in fig. 11 using the electrical test row. Because here a 100% response has been taken as threshold this curve is shifted towards values that are ~3000 e^- higher than in fig. 10. Threshold data obtained during irradiation tests of the 6-ladder array will be discussed in sect. 4.1.

If a particle signal exceeds the threshold the bit resulting from this "hit" is delayed in a "pipeline" in the pixel such that a logic coincidence can be made with the external strobe signal which is derived from a positive first-level trigger. A schematic diagram of the timing sequence is shown in fig. 12. The internal pipeline delay is adjustable between ~100 ns and ~ 1 μs. If there is coincidence the databit is stored in a local memory in the pixel, otherwise it is lost. It can then be read out via the vertical shift register or it can be reset in case of an abortive higher level trigger. The average delay time of the signals in the pixel pipelines for the 6-ladder array as a function of the adjustable parameter Idn is plotted in fig. 13.

Several improvements have been implemented in the new chip in order to obtain a better matching of the timing between pixel cells [5]. Although the timing uniformity within a single chip has been tightened and a distribution with a standard deviation of ~20 ns r.m.s. has been

measured, it now is found that a non-uniformity exists in the pipeline delays between the chips on the array. In fig. 14 is shown that for the external strobe delay different values are needed for each ladder in order to obtain optimal detection efficiency in a test beam. In the histogram of fig. 15 the internal delay is shown for the separate chips in the array measured with the electrical test rows. In greater detail, a difference of ~200 ns between the top and the bottom of the array is again seen. This effect can be attributed to small voltage drops due to the resistance of the supply lines on the ceramic support. These differences in internal delay may lead to a loss of recognized hits but can be compensated by making the external strobe signal long enough to cover the range of delay values. Therefore, a coincidence strobe signal with a fairly long duration of ~500 ns has been necessary. This external strobe signal is issued with an added delay after the trigger generated by the event. Also for this added delay time an average value had to be determined for the array as a whole, and often a delay of 150 ns was used. For added delay and strobe signal together this corresponds with an overall internal delay of ~800 ns.

2.5 Readout organization and "on-board" intelligence

The schematic diagrams of the readout cards are shown in fig. 16. An intermediate card is placed close to the detector and a VME card in the control room. The readout sequence for the chips in one 6-ladder array is schematically given in fig. 17. The array is split into 2 parts which are read in parallel. In each clock cycle the 16-bit data from a row on 2 chips (e.g. 1A and 1B) are combined into one 32-bit word. Tri-state drivers were included on the Omega2 chip and these allow the different chips in the array to send their data serially via the bus.

In this way, in spite of the large number of sensor elements only one card is needed for an array and data are transmitted as 32-bit words. The readout speed in the laboratory was up to 20 MHz but in the experimental situation with transmission over 30 m only 2 MHz was achieved. The readout time of the array was 576 μs, relatively long but still below the readout time for the other detector systems in the Omega experiment.

The VME card performs data acquisition including masking of noisy pixels and zero suppression as well as various other functions. It only transmits to the data-acquisition computer the non-zero data words with their corresponding address indication. The hardware masking possibility is an essential feature in a pixel detector in view of the large number of sensor elements and the unavoidable occurrence of bad pixels. "Always-on" pixels create problems of dead time and also make on-line histogramming difficult and it is essential to eliminate them from the real time data flow. After it is found which pixels are "always-on" or are abnormally noisy these can be masked and can further be treated as in "off" state. The number of pixels that had to be masked was ~700 (1%), mostly because they were "always-on". It is intended in a future design to bring on-chip both the zero-suppression and the masking. This will be a first step towards an intelligent ("smart") micropattern detector.

2.6 Testing and reliability including preassembly tests

The feasibility of multi-chip arrays depends crucially on the availability of tested, fully functional components. In a 2-step procedure the components are tested before the array construction. The DC parameters have been tested on wafer using a standard probe station with dedicated probe card. Afterwards, these wafers are bumped, diced and bonded to the matching detectors. The second step is the test of finished, bump-bonded 'ladders' before glueing these on a common ceramic support. Pulsing of the test row and irradiation of the detector with an electron source have been performed on the finished ladders, for one readout chip at the time. Acceptance limits for the measured parameters were defined, in order to decide which chips and which ladders can be mounted. The yield of good chips in the wafer test was 70% [5] while the ladder test has not yet been performed in a systematic way. In the first experience it appears that the DC wafer test has eliminated most of the bad chips.

3. TESTING OF A TELESCOPE OF SINGLE CHIP ASSEMBLIES IN A 120 GeV BEAM

A "telescope" test setup of 3 pixel chip assemblies similar to the one described in [1] has been installed in the H6 beam at CERN and a schematic drawing is shown in fig. 18. The beam was operated most of the time with 120 GeV/c negative pions. A large number of events with single beam tracks has been recorded for different values of the electrical parameters. A small proportion shows large clusters in one of the detector planes, each time in 0.15 % of events, followed by multiple tracks downstream as illustrated in fig. 19. This occurrence is compatible with the interaction cross section for pions in the 1.6 mm of material of the detector and its printed circuit board support. The pixel detectors provide an on-line pictorial description of such events. Apparently, nuclear fragments touch quite a number of pixels leading to a considerable extension of the main cluster in the detector plane where the interaction took place. A histogram of the hit distribution over the detector plane is accumulated in fig. 20 and this gives an image of the beam as defined by the scintillators. The background around the peak can be attributed to tracks from interactions as described above. The addition of a veto counter should make it possible to eliminate most of the events with multiplicity due to the interactions in upstream material.

The total statistics of the hits in the middle plane for 99184 beam track events is shown in table 2. These data include some hits from multiple cluster events. If one selects only the clusters which are related to a beam track identified in the upstream and downstream planes the distribution of the cluster size in fig. 21 shows 88% single hits. The efficiency for the middle plane in this sample was determined at 99.8%.

Table 2 Distribution of multiple hits by # of rows and # of columns in 99184 events

# of colmns	1	2	3	4	5	6	7
# of rows							
1	84265	1221	8	1	-	-	-
2	11530	363	3	-	-	-	-
3	816	168	62	2	-	-	-
4	288	79	42	2	2	1	-
5	105	39	15	6	-	-	-
6	60	21	13	6	-	-	-
7	29	9	6	4	1	-	-
8	8	1	1	1	-	-	-
9	-	-	-	-	-	-	-

3.1 Detectors of 150 μm thick

In the H6 beam we also tested the first pixel detector asemblies with a 150 μm thick sensitive silicon layer [6,7]. Because the signal from such a detector is only ~10^4 e-h pairs for minimum-ionizing particles a low threshold of ~4000 e^- is needed in order to achieve 95% efficiency. For higher thresholds there is a loss of efficiency as illustrated in fig. 22.

There are many arguments in favour of using thin pixel detectors in the future high-intensity collider experiments. In particular it may be expected that thin detectors have a longer lifetime under irradiation, mainly because the total depletion voltage scales with the square of the thickness. It has been found for 300 μm thick detectors, e.g. in [7] that after a neutron irradiation dose of 10^{14} cm^{-2} this voltage is increased e.g. from 30 V to 300 V.

3.2 Hit "propagation"

At low thresholds we discovered previously in the OmegaD chip that sometimes "propagation" of a hit occurs on subsequent clock periods from one cell to the adjacent one in the direction of the output periphery of the array, along the column [8]. Such a propagated hit may be seen as background in a following event, and because the propagation always goes in the same direction, accumulation of spurious hits occurs towards one side. This phenomenon was particularly present in the first test of the thin detectors. The propagation was thought to be caused by digital cross-talk into the adjacent pixel from the discriminator reset signal at the end of the internal delay cycle. The use of a shielded reset line has practically eliminated this phenomenon in the Omega2 chip. In fig. 23 data are shown which were taken with a 1-ladder array in the T9 test beam for different delays between the event and the start of the 200 ns strobe width. In fig. 24 similar data have been taken at an exceptionally low threshold level of ~3000 e^- and here a small proportion of "propagated" hits can still be seen at 700-800 ns strobe delay.

4. A 6-LADDER ARRAY IN THE 10 GeV TEST BEAM

The first 6-ladder array has been tested electrically, with a radioactive electron source in the laboratory, and in the T9 beam with 10 GeV/c pions.

4.1 Testing in the laboratory

Prior to testing in the beam, the operational parameters of the array have been studied in the laboratory using a radioactive electron source and an event trigger derived from a single scintillator placed behind the pixel detector array. A comprehensive study was made of the sensitivity of the adjustable parameters. The external voltages are distributed via 6 resistors and each current source then supplies the 6 chips on the corresponding vertical bus. Several of the results concerning threshold and delay timing have already been shown in sect. 2.4. The efficiency and the average number of hit pixels per triggered event caused by a traversing electron from a radioactive source are plotted in fig. 25 as a function of the comparator threshold setting Idis2. Up to a value of 40 μA the efficiency is ~100% and goes down gently for higher thresholds. The proportion of double hits decreases steeply above 33 μA but only a gradual loss occurs from 40 μA upwards. It should be mentioned that all hits are counted in these data, without checking for "always-on" pixels that may occur at low threshold. Only a single pixel of this kind could already explain the "hump" below 33 μA.

The efficiency and proportion of double hits as a function of the applied detector bias voltage are plotted in fig. 26. The total depletion voltage of the detector is 30 V and close to 100% efficiency is achieved from there upwards. There is a slight increase of double hits at higher bias.

4.2 Beam test

The 6-ladder array was positioned between 4 high-precision wire chambers and several scintillator planes which provided coincidence and position information for the beam events generated by 10 GeV/c particles. This beam could cover a fair part of the surface of the array as is shown in the scatter plot of fig. 27 where the hit pixels for 50 000 events are plotted on-line in a histogram with an approximate geometry of the 6 ladders. As was mentioned in sect. 2.1 the detector pixel cells in the "stitching" region between readout chips are 1000 μm wide instead of 500 μm and the double count rate in these cells is visible as a darker band. This double count rate is particularly clear in the histogram of the projection of these data for each ladder in the direction of the columns, fig. 28. A similar set of data, not shown here, has been obtained in the upper part of the array and few columns were found to be "always-on" or dead, as can be seen e.g. in ladder 2, columns 67 and 68 and the upper part of ladder 4, columns 33, 34 and 35.

In the off-line analysis the data have been corrected for the ladder geometry and a fiducial volume selection has been made on the basis of the predicted position using the wirechamber

information. Tracks that are predicted to be within 3 standard deviations from the edge of a ladder have been discarded from the sample. The remaining data are shown in fig. 29. The vertical dark bands have been eliminated by the geometrical correction. In the upper part are plotted the hits that could be associated with the beam tracks in the fiducial volume in 24148 events with only a single cluster of hits. In the lower part are plotted the hits in the not-associated cluster which were found in 757 events with two clusters of which the other one was associated with a good track. From this scatter plot it can be concluded that most of these "spurious" hits also are associated with the beam. Further analysis of these "spurious" particles revealed that there are 2 distinct contributions to the "spurious" hits. Measurement of the distance of the "spurious" hit pixel to the position of the "good" hit resulted in a group of 466 events accumulated in a 3 mm x 3 mm area around the impact point whereas the distances for the other 291 hits were widely distributed over the 50 mm x 50 mm plane. The 466 hits represented 2% of the total number of reconstructed events and given this proportion they can be explained plausibly as separately detected delta electrons, on the basis of the position correlation with the "good" hit.

The other spurious hits were caused by beam particles detected by the pixel array during the 500 ns strobe time but not recorded by the wirechambers because these had only a 40 ns sensitive gate period. With a beam intensity of ~21800 in 300 ms the expected background in the fiducial volume is 405 uncorrelated clusters in 24148 events. This expected background more than compensates for the 291 uncorrelated hits, leaving room for not more than 0±50 "real" noise hits. Therefore, virtually no noise hits can be identified in this sample, for 25000 events and for 36k pixel cells. This gives an upper limit for the incidence of Gaussian noise of $< 10^{-8}$ of the real hits.

A small scintillator allowed the definition of an apparent beam spot, 2 mm high (~30 pixels) and 8 mm wide, across a "stitching area" between readout chips (~16 pixels of 500 μm + 2 pixels of 1000 μm). The sensitive area of a single ladder is 53 mm x 4.7 mm and covers easily this reduced beam spot. The on-line scatter plot is shown in fig. 30 with the corresponding column projection in fig. 31. Some hits found outside the scintillator area are due to triggers generated in the optical fiber which connects the scintillator to the remote photomultiplier tube. The efficiency determined e.g. in ladder 3 was 99.4% and no loss of efficiency can be seen in the "stitching area". The cluster topology is described in table 3 for low, normal and high thresholds. There is only a small influence of the threshold on the incidence of double hits and none at all on the proportion of multiple hits.

These results corroborate essentially those already reported in table 2 for single chip assemblies where a proportion of 85% single hits was found. The performance of the array apparently does not suffer from unexpected interference effects due to the larger number of chips. The double hits consist predominantly of 2 adjacent rows (11.8%). If one supposes that double

Table 3 Cluster Topology 6-ladder Array

		Low threshold 6000 e⁻				Normal threshold 8000 e⁻				High threshold 10 000 e⁻		
	# cols	1	2	> 2		1	2	> 2		1	2	> 2
# rows												
1		84.0	0.8	0		84.1	0.8	0		86.5	0.8	0
2		11.9	0.3	0.12		11.8	0.3	0.15		9.6	0.3	0.14
> 2		2.3	0.4	0.17		2.2	0.4	0.22		2.1	0.3	0.21

hits are caused by particles crossing the boundary of a pixel one finds a sensitive edge region of 4.5 μm on either side. Note that in the test beams the particles cross the detectors under an angle very close to 90°. If double hits are caused by geometry alone there should be 1.6% of double hits with 2 columns and these are, at first sight, with 0.8% under-represented. In the single assembly test 1.2% was found. However, the data in the ladder test are biased because the small scintillator was intentionally placed across the region between two chips (fig. 30) in order to detect any possible inefficiency in the "stitching" region. Therefore there is less boundary between columns, and therefore fewer "double column" hits. Nevertheless, there still may be a slight deficit of "double column" events and this has to be investigated in more detail.

5. FIRST USE OF A DOUBLE ARRAY IN THE OMEGA WA97 EXPERIMENT

A complete detector plane with double array has been installed in the WA97 experiment in the Omega spectrometer in November 1993 during the test run with 200 GeV protons. By defocussing the beam it was possible to "illuminate" practically the complete detector and the less efficient or dead areas became clearly visible in fig. 32 which shows a scatter plot for 50 000 events. The vertical dark bands due to the larger, 1000 μm wide pixels are clearly distinguished, although the statistics from 50 000 events on a total of 72 000 cells cannot be very good. Some dead columns can be seen, but with this limited statistics it would be impossible to recognize single, dead cells. 3 complete readout chips (II-1A,top row, II-10B, I-18B,bottom, see numbers in fig. 17) recorded few hits but they did not disturb the other chips in the array, except II-1A which had to be physically disconnected. Several other chips on the 9th and 11th row of array II (13B, 14B, 15B, 16A, 17A, etc) have a reduced efficiency towards the lower part, maybe due to disconnected bumps. Most of the inefficient chips are on the second array that was less studied in advance. Although several adjustable parameters have been varied during

this run it is possible that an improved operating condition could have been established with sufficient preparation. It was found that with a strobe time of 500 μs two more chips (I-6B and II-2A) had a reduced response, in line with the longer delay found for the top rows. The response could be improved by making the strobe time 1 μs. In total, ~ 10% of the pixels were inoperative, most of them on the second array.

In this development project we are trying to achieve full traceability of the components and this allowed us to determine that all chips on the second array came from a single readout wafer. There are reasons to believe that an incident has occurred during the processing of the solder bumps. This could maybe explain the bad yield on this array. Further analysis is in progress.

The sketch in fig. 33 shows the position of the double array of micropattern pixel detectors between 5 doublets of silicon microstrip detectors in the vertex telescope in Omega. Microstrip detectors with 50 μm and 100 μm pitch allowed track reconstruction in both y and z coordinates with a precision at the pixel plane of respectively 15 μm and 20 μm. The distributions of residuals shown in fig. 34 have standard deviations of 157 μm along y and 30 μm along z. These numbers allow to determine a precision of respectively 156 μm and 22 μm in the pixel detector measurement , and these experimental values agree fairly well with the expected values based on the $1/\sqrt{12}$ rule.

If an event selection is made with only double hits in the pixel plane the distribution of residuals has a standard deviation of 22.6 μm (fig. 35) which indicates a <10 μm precision of the coordinate determined by the pixel detector.

It has been again confirmed that most events with a reconstructed beam particle are characterized by a single cluster with a single hit. The proportion of double hits and of number of clusters has been studied as a function of the threshold adjustment and the applied detector bias voltage. Data have been taken with focussed and defocussed beam and with an interaction trigger which required a large energy deposit in a scintillator placed just in front of the pixel detector plane (fig. 33). A complete analysis of this run will be available in the course of 1994.

6. CONCLUSIONS

For the first time a large, active pixel detector array, consisting of 72576 sensor elements associated with 72 readout chips with binary response has been operated in a particle physics experiment. Crucial to the success of such a device are the integration of the sensors and the design of the electronics functions as well as a careful preliminary characterization of the operational parameters of the finished array.

We have elaborated on the study of threshold adjustments, timing, etc. in order to show the importance of optimization in this multiparameter detector device. The values for gain and threshold have been optimized in a laboratory test using a radioactive electron source and a

scintillator trigger. The determination of the timing delays has been done in a test beam preceding the use in the experiment.

A precision better than 22 μm and an efficiency of >99% were measured on the "good" regions of the detector. Bad regions accounted for 2% of the area in the first array and for 20% of the area in the second one. A major cause for loss of efficiency was found to be improper timing for the various delays. One has to recognize and correct the variations in signal transmission due to the variations in semiconductor chip processing per wafer or per lot. In these first arrays it was found that line resistances on the mechanical support are an important factor influencing the settings of the delays on the chips. This will be easy to remedy in the future arrays. In larger systems it may be necessary to adjust timing and thresholds locally on each "ladder" or even on each chip, using built-in feedback loops.

After corrections for timing and delta rays the incidence of spurious noise hits is found to be $<10^{-8}$, as could be expected from the electrical noise measurements giving 170 e^- r.m.s. Some pixels (here ~1%), however, are "always-on" and hardware masking of these is essential in order to limit the data transmission to manageable proportions, particularly in a large area system which may have $>10^8$ sensor elements.

The future introduction of on-chip timing adjustment, masking, zero suppression, etc. will make the active pixel detector increasingly "intelligent" and at the same time this could widen the acceptance limits for chips from different wafers or different lots, and increase the yield in production.

Acknowledgements

It is a pleasure to acknowledge the effective collaboration with our industrial partners. SMH (Annemasse) helped us at short notice with the ultrasonic wirebonding. We thank J. Séguinot and T. Ypsilantis for the use of their test setup in the T9 beam. The enthusiasm of the Omega community stimulated the progress of this project. The continuous interest of the P. Sharp as the RD19 referee stimulated us through several years.

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Figure Captions

Fig. 1 Photograph of a single array consisting of 6 ladders with the associated local driver card and the VME readout module. This array has 32288 detecting elements and a second, identical array, staggered over the open "slots" completes a full detector plane. The smaller ceramic support with the 6 ladders is mounted on a larger, thicker U-shaped ceramic on which the flexible circuit is glued.

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Fig. 3 Layout of the connecting lines on the thin-film ceramic substrate for the array of 6 detector ladders with altogether 36 readout chips. The + signs are alignment marks for the positioning of the ladder assemblies, the outer lines carry ground and separate bias voltages for the detectors. The readout chip supplies and data buses are grouped in the 6 vertical columns.

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Fig. 7 Close-up of the array. The buslines on the light ceramic plate run vertically underneath the ladders. Bonding wires can be seen connecting the bondpads on the readout chips to these buslines.

Fig. 8 Photograph of a complete array. One can see the dark back side of the detector chips and the bias filter capacitors besides each ladder. The vertical lines are the connecting lines on the ceramic, as shown in fig. 3.

Fig. 9 Schematic of the electronics readout circuit in each pixel cell in the Omega2 chip.

Fig. 10 Threshold at 50% countrate of electrical pulses in a single Omega2 chip as a function of the externally adjustable current Idis2 via a 62 kΩ resistor. Absolute calibration points are shown at 22 keV, 60 keV and 122 keV and these have been used to fit the left-hand vertical scale in electrons. The arrows indicate the low, normal and high threshold values which were used in the beam tests. The non-linearity is caused by the influence of Idis2 on the gain of the preamplifier itself which even collapses completely at low supply current (< 20 μA).

Fig. 11 Average threshold at 100% efficiency for a 6-ladder array measured as a function of the adjustable current source Idis2.

Fig. 12 Timing sequence showing adjustable internal delay and external strobe signal. The strobe is issued with an "added delay" (here e.g. 200 ns) after the trigger signal from the experiment. The bit Qn is stored in memory if there is coincidence between the strobe and the falling edge of the internal delay.

Fig. 13 Average delay for a 6-ladder array as a function of the adjustable current source Idn. The strobe durations were respectively 800 ns, 500 ns and 400 ns.

Fig. 14 The values of the added external strobe delay in the T9 test beam. The "added delay" has been varied but the response is not identical for each ladder. The optimal number of coincidences (or "efficiency") was obtained at the value indicated by the black square. The line indicates the FWHM of the efficiency distribution. The duration of the strobe signal itself was 500 ns. Ladder 1 is at the "top" of the array, furthest away from the supplies.

Fig. 15 Histogram of delays in the pipelines averaged for each chip in the array as measured with the electrical test rows. As in fig. 14 a top (ladder 1)-bottom (ladder 6) non-uniformity can be seen, now in more detail for the separate chips.

Fig. 16 Block diagram for the intermediate readout card at the top and the VME board at the bottom.

Fig. 17 Readout sequence of the chips. 1A and 1B are read in the first 64 clock cycles via the buses in columns 1 and 4, then 2A and 2B in the second 64 via bus columns 2 and 5, etc. The access of each chip to the bus is granted or denied by external switching of tri-state drivers on the chip itself

Fig. 18 Setup of the telescope of 3 single assemblies in the H6 test beam, with various scintillators for beam definition. Beam particles are defined by the coincidence of several small scintillators, in particular 2 crossed scintillating fibers PM3 and PM4. The resulting spot measures only ~1 mm x 2 mm.

Fig. 19 Pictorial representation of the statistics of single, double and multi-hit clusters in the beam test with 3 detector planes. It shows the powerful pattern recognition of the micropattern detector even for large numbers of hits in a cluster.

Fig. 20 Histogram of the beam spot consisting of the coordinates of hits as recorded by a 300 μm thick micropattern detector. The threshold corresponds to 30 μA or ~6000 electrons.

Fig. 21 Histogram of the cluster size for single beam tracks in a 300 μm thick detector.

Fig. 22 Comparison of detector efficiency for a 150 μm and a 300 μm thick detector as a function of the discriminator threshold. The drop in efficiency below 25 μA is related to the influence of Idis2 on the preamplifier gain itself, causing the non-linearity already shown in fig. 10.

Fig. 23 Scan of the added delay time after which the strobe signal of 200 ns duration is issued. Each point represents 5000 event triggers, generated by an electron traversing the single ladder detector. The setting for the threshold was Idis2 =41 μA and Idis1 = 32.5 μA, Iqa = 90 μA, Idn = 4 μA and Vbias=50 V.

Fig. 24 Idem as fig. 23 but with a low threshold of ~3000 electrons: Idis2=24 μA. The ~10% hits detected at 800 ns are likely to be caused by propagation of the reset signal from a previous hit in the adjacent pixel cell.

Fig. 25 Efficiency and number of hits per event for a 6-ladder array as a function of adjustable threshold Idis2. Each point represents 2000 triggers, strobe duration was 500 ns and added strobe delay 50 ns.

Fig. 26 Efficiency and number of hits per event for a 1-ladder array as a function of detector bias voltage Vbias. Idis1=Idis2=30 μA, Idn=4 μA, strobe duration 200 ns, added strobe delay 150 ns.

Fig. 27 On-line scatter plot of approximately 25 000 hits in the 6-ladder array from 50 000 beam triggers. The dark bands are explained in the text.

Fig. 28 Projection of the hits in each ladder in fig. 27 in the direction of the columns. Note the change of the vertical scales from ladder to ladder.

Fig. 29 Top: Off-line representation of selected data from fig. 27, geometrically corrected. Only hits from single cluster events are plotted.
Bottom: Idem for 2-cluster events with only those hits that are not associated with the wirechamber-determined beam track. These hits are nevertheless correlated with the beam position. They can be explained by the longer strobe time of the pixel array and by correlated delta electrons.

Fig. 30 On-line scatter plot of hits with the 8 mm x 2 mm scintillator in the event trigger. The scintillator is covering the "stitching"area between 2 readout chips. The background hits below the scintillator are mostly due to particles which crossed the detector and generated a trigger via Cerenkov light in the optical fiber that connected the scintillator to the remote phototube.

Fig. 31 Projection of the hits of fig. 30 in the direction of the columns.

Fig. 32 Scatter plot of particle positions in 50 000 events for a complete detector with double array, comprising 12 detector ladders and 72 readout chips. The separations between the readout chips are visible as vertical, dark bands. The strobe pulse started immediately after the trigger pulse and the strobe duration was 1 μs.

Fig. 33 Top view of the layout of the pixel detector and 5 doublets of microstrip vertex detectors in the Omega WA97 run in November 1993. 3 of the horizontal microstrip detectors have a pitch of 100 μm instead of 50 μm which leads to a reduced reconstruction precision in the z-coordinate. During the test the vertical magnetic field was not on.

Fig. 34 Histograms of the distribution of residual values between predicted and measured coordinates in the y and z projection (see fig.33). The calculated standard deviations are 157.1 μm (y) and 30.5 μm (z) and these indicate a precision in the pixel detector of 150 μm and 22 μm in the y- resp. z direction.

Fig. 35 Distribution in z as in fig. 34 but for selected events with 2 adjacent hits in cells in the same column. The standard deviation is now only 22.6 μm giving a precision of better than 10 μm in the pixel detector.

Table 1 Normal operational parameters of Omega2 readout chip

Externally adjustable parameter	Symbol	V/ μA
ground reference	gnd	1.5 V
supply voltage	Vdd	3.0 V
supply voltage	Vss	0.0 V
frontend amplifier bias	Iqa	- 80. μA
frontend amplifier bias	Idis1	30. μA
comparator threshold	Idis2	36. μA
internal 'pipeline' delay	Idn	8. μA
leakage current compensation	Ifn	- 3.5 μA
detector bias voltage	Vb	50. V

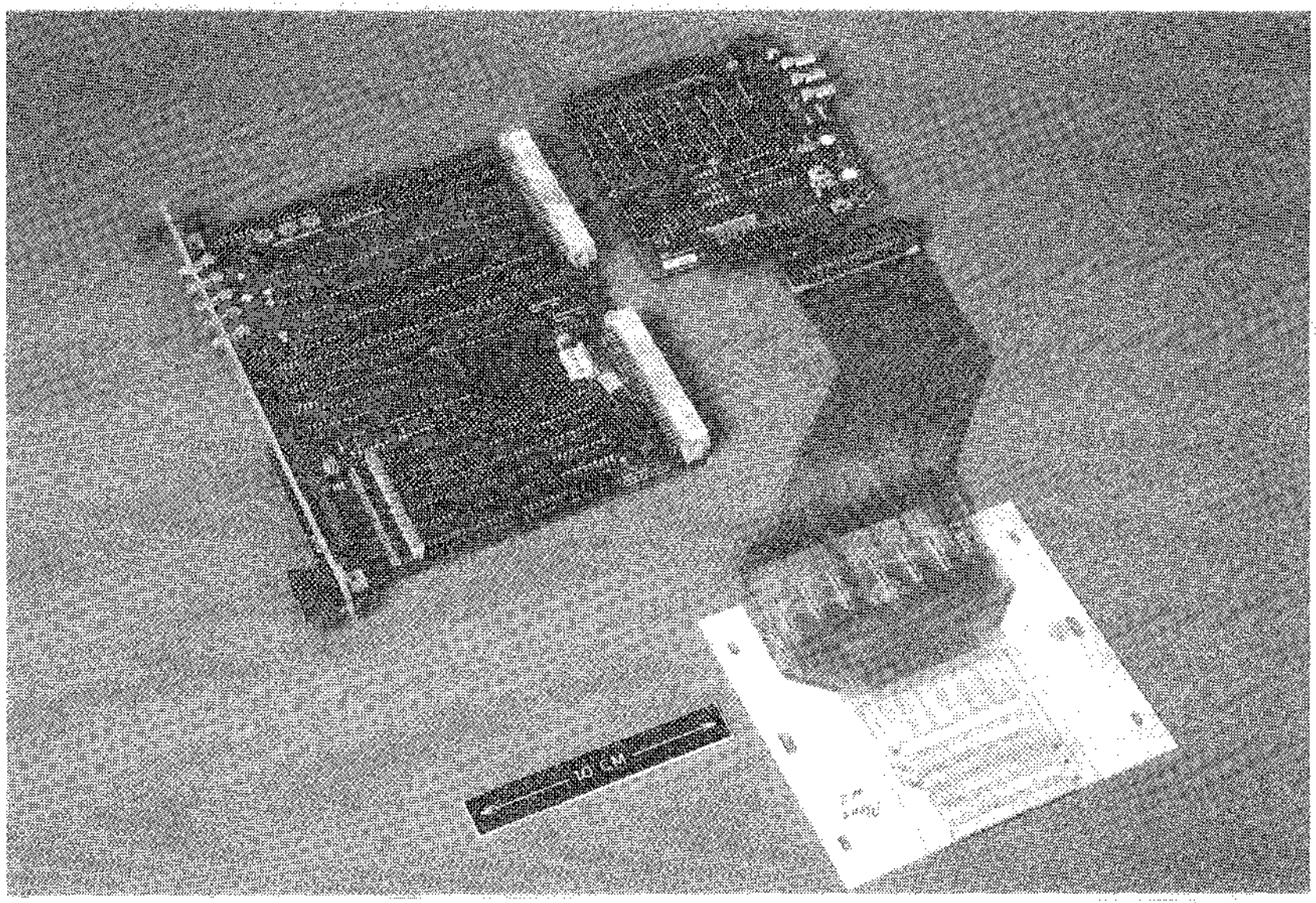
Table 2 Distribution of multiple hits by # of rows and # of columns in 99184 events

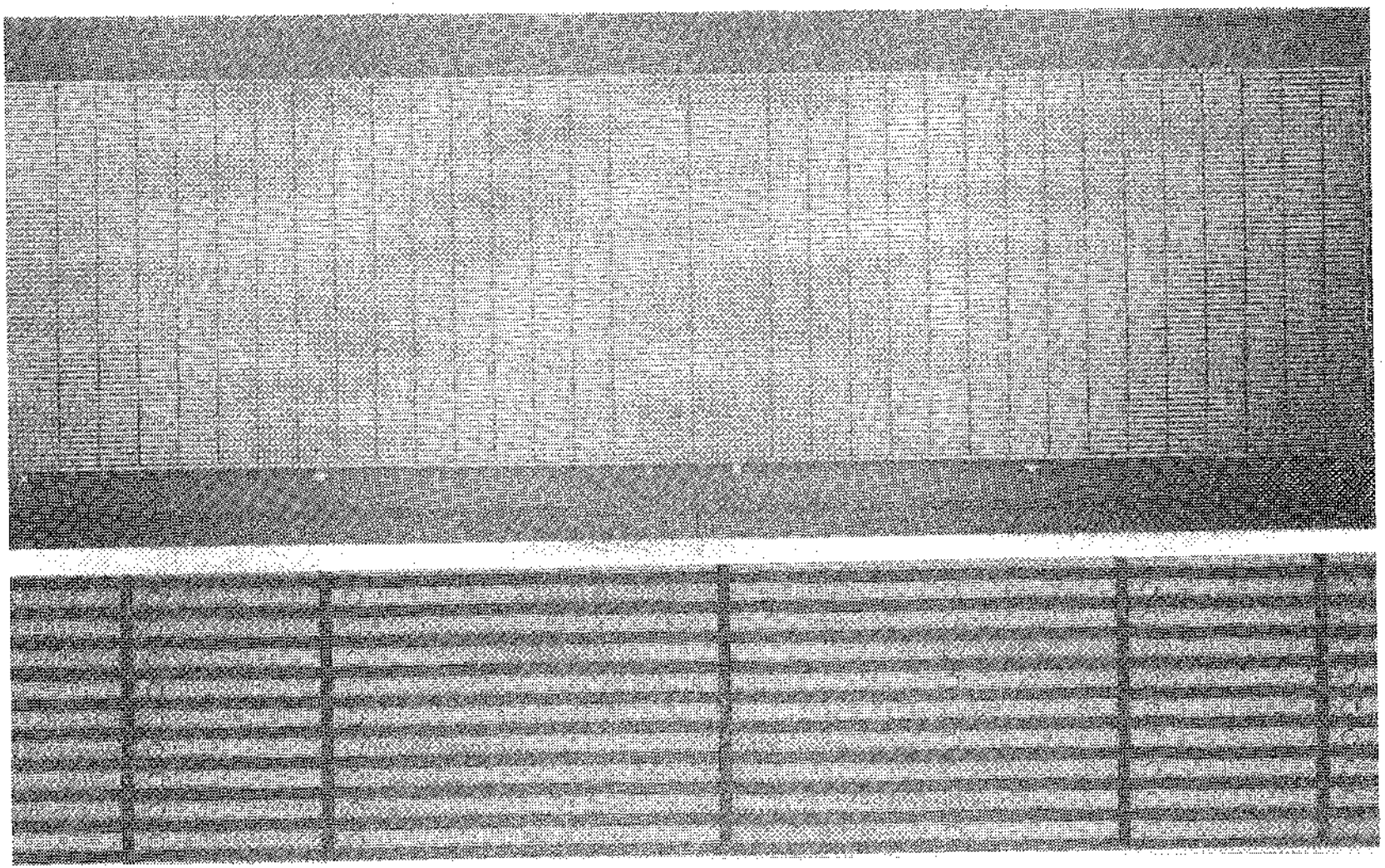
# of colmns	1	2	3	4	5	6	7
# of rows							
1	84265	1221	8	1	-	-	-
2	11530	363	3	-	-	-	-
3	816	168	62	2	-	-	-
4	288	79	42	2	2	1	-
5	105	39	15	6	-	-	-
6	60	21	13	6	-	-	-
7	29	9	6	4	1	-	-
8	8	1	1	1	-	-	-
9	-	-	-	-	-	-	-

Table 3 Cluster Topology 6-ladder Array

		Low threshold 6000 e⁻				Normal threshold 8000 e⁻				High threshold 10 000 e⁻		
	# cols	1	2	> 2		1	2	> 2		1	2	> 2
# rows												
1		84.0	0.8	0		84.1	0.8	0		86.5	0.8	0
2		11.9	0.3	0.12		11.8	0.3	0.15		9.6	0.3	0.14
> 2		2.3	0.4	0.17		2.2	0.4	0.22		2.1	0.3	0.21

Fig. 1 Photograph of a single array consisting of 6 ladders with the associated local driver card and the VME readout module. This array has 32288 detecting elements and a second, identical array, staggered over the open 'slots' completes a full detector plane. The smaller ceramic support with the 6 ladders is mounted on a larger, thicker U-shaped ceramic on which the flexible circuit is glued.





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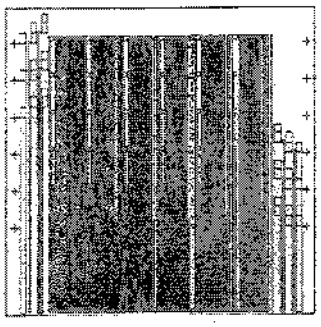

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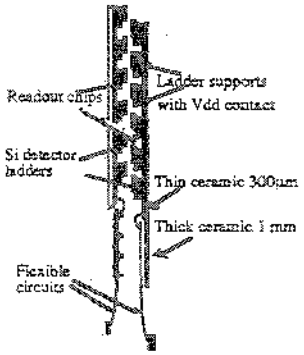

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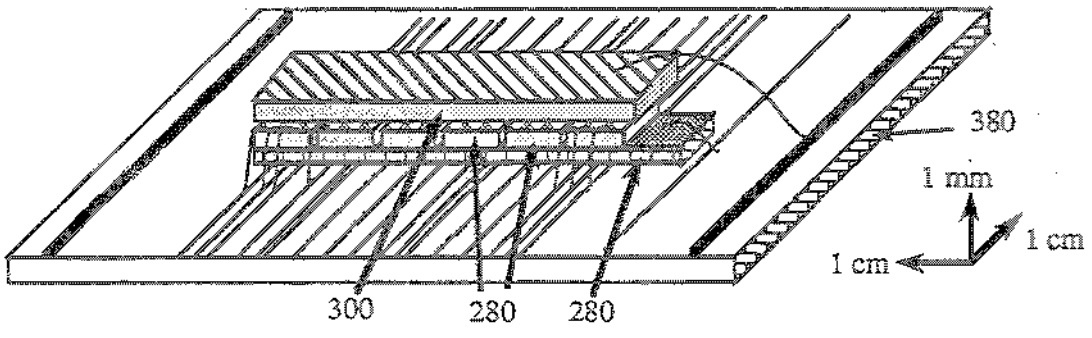
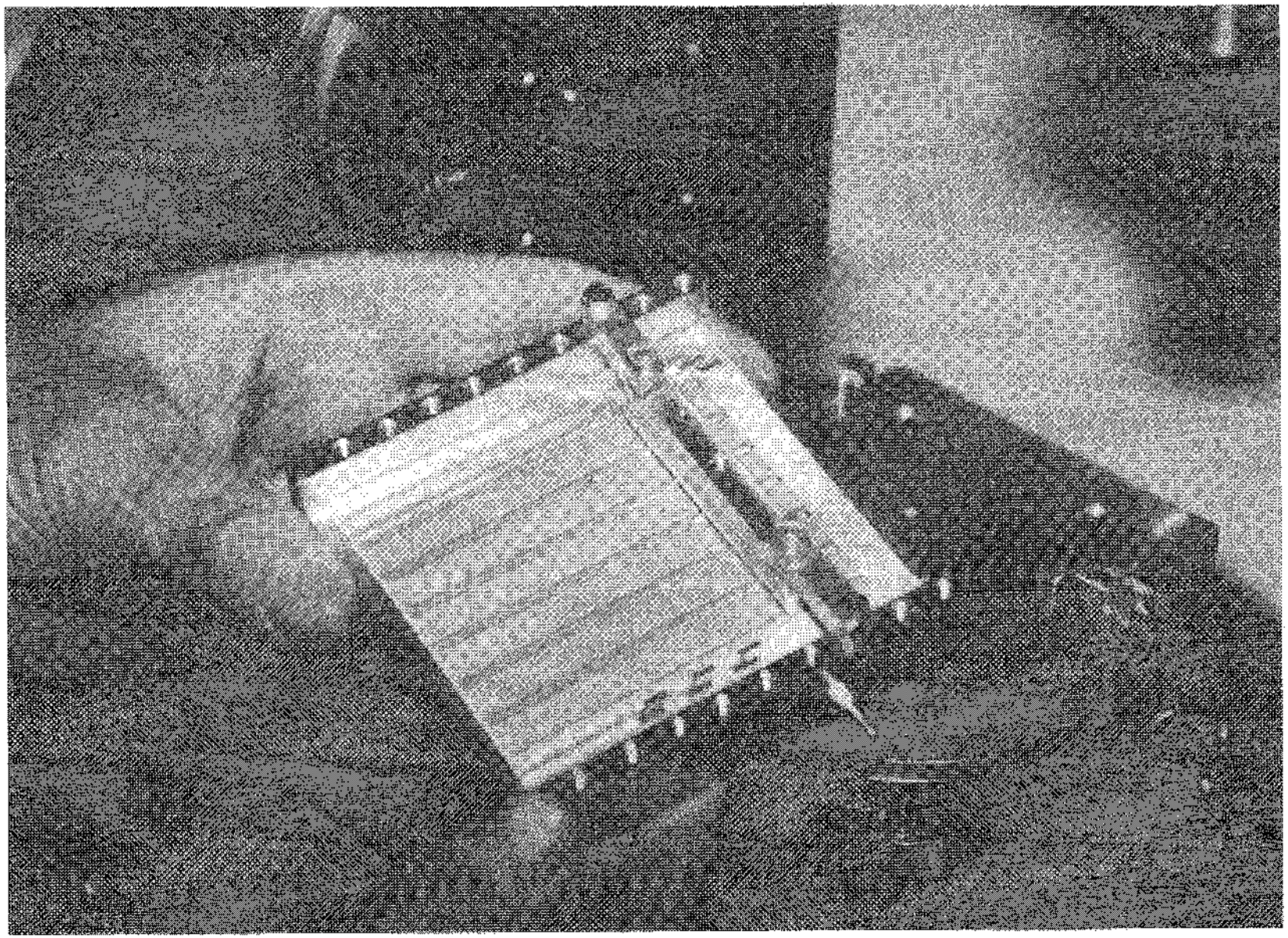


Fig. 5 Drawing of the assembly of ceramic support plate, supply and bus conductors, isolation ceramic, readout chips and detector ladder, from bottom to top. The thicknesses are indicated in µm.



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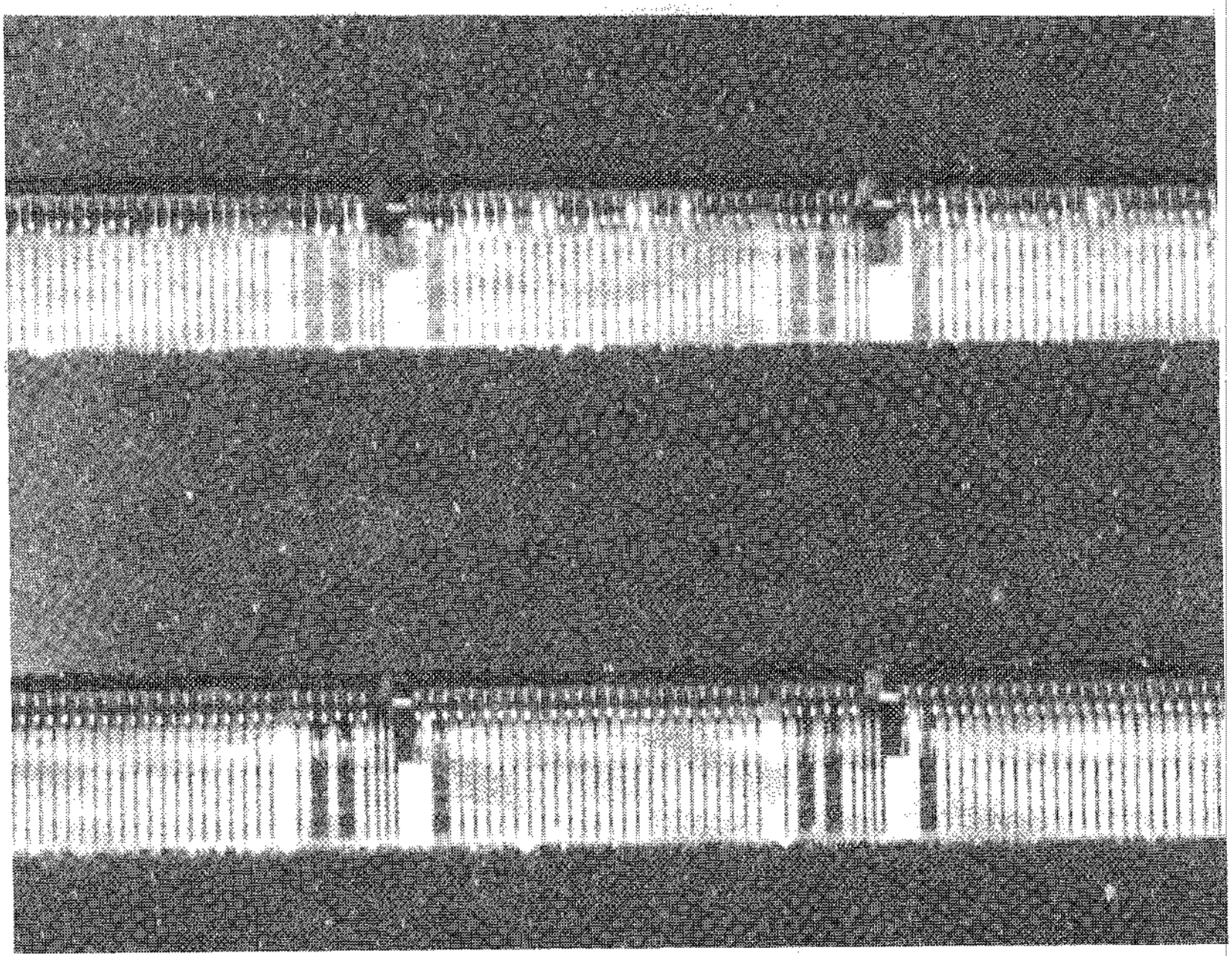

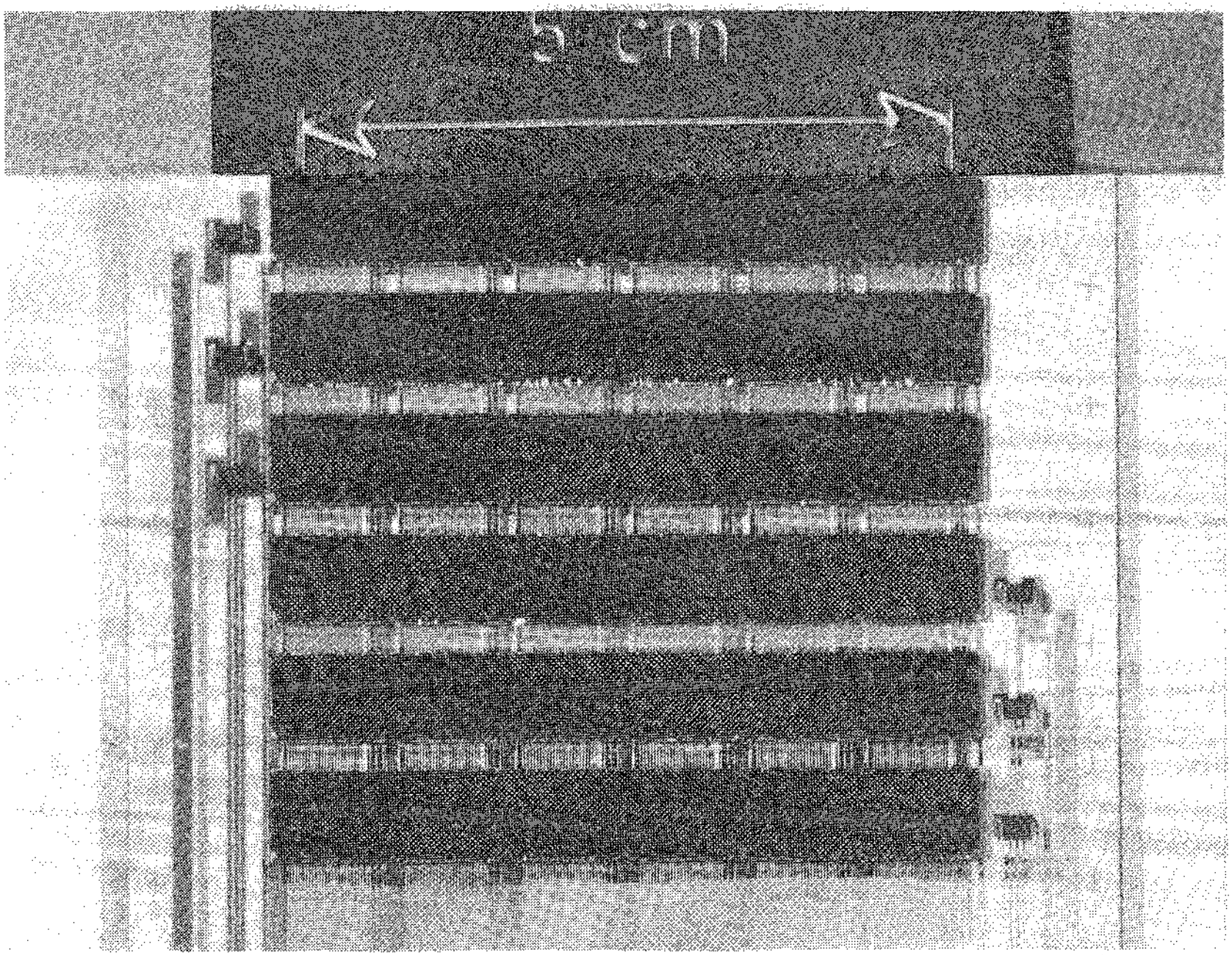

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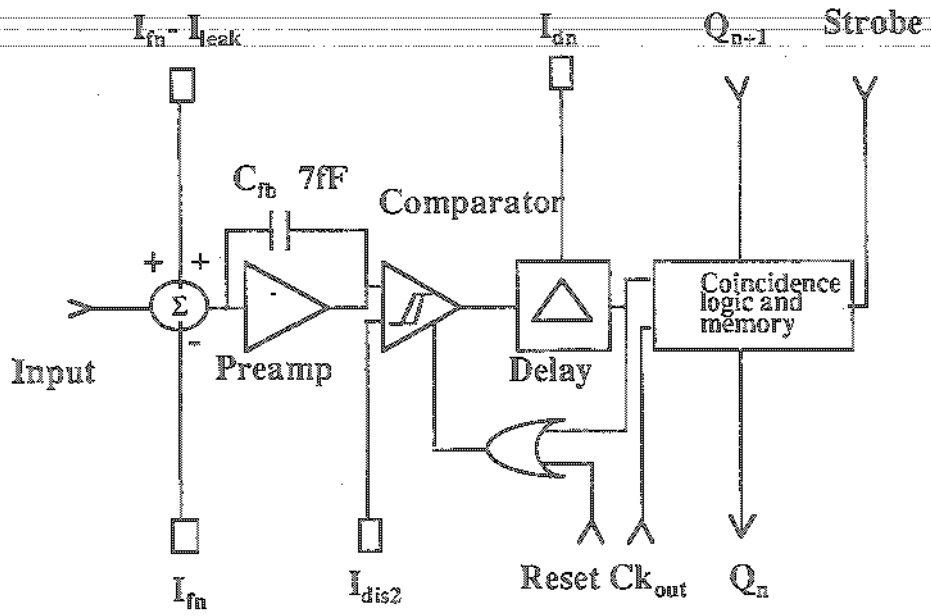

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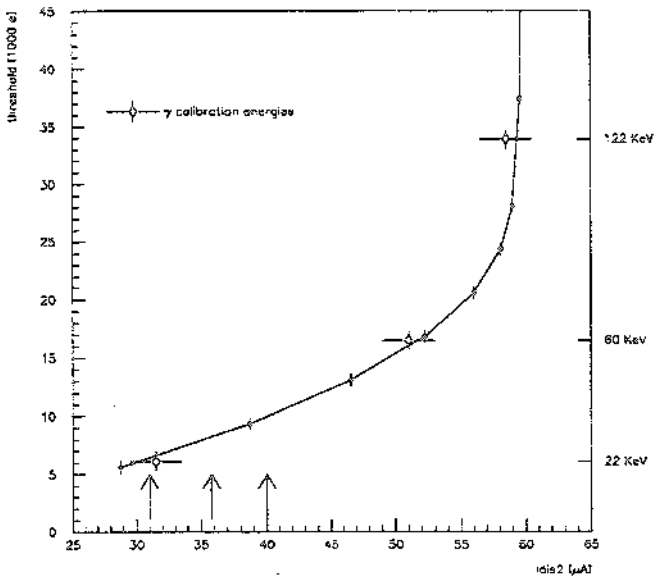

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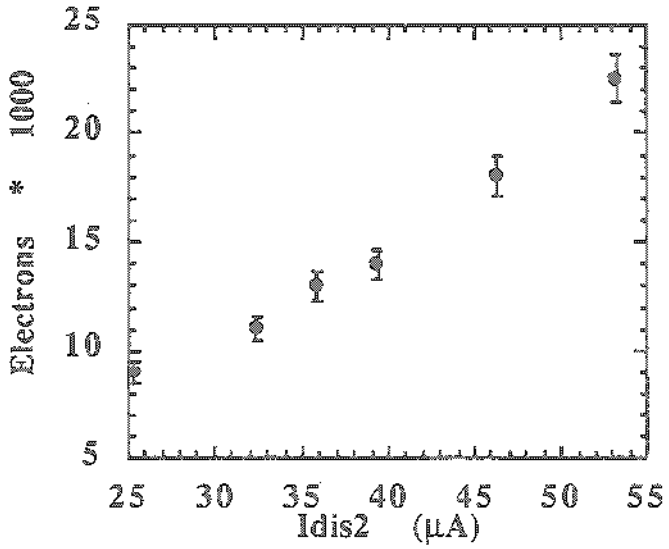
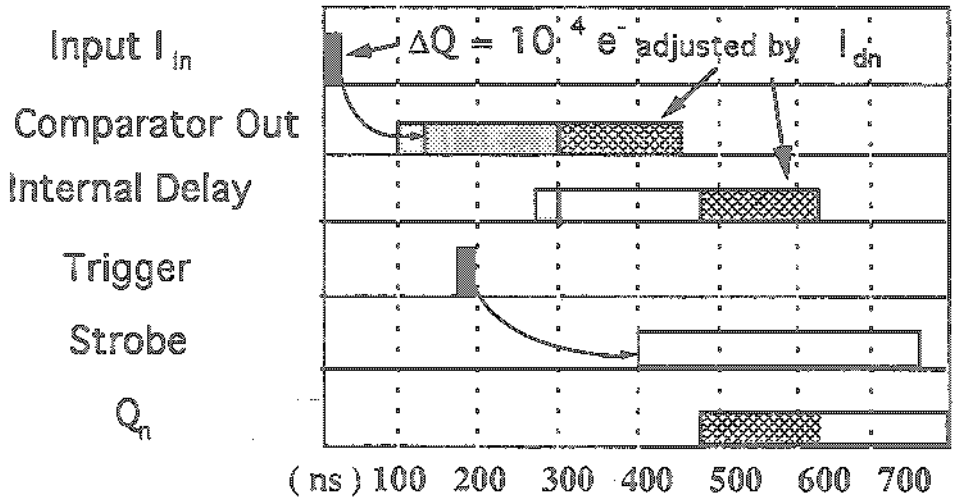


Fig. 11 Average threshold at 100% efficiency for a 6-ladder array measured as a function of the adjustable current source Idis2.



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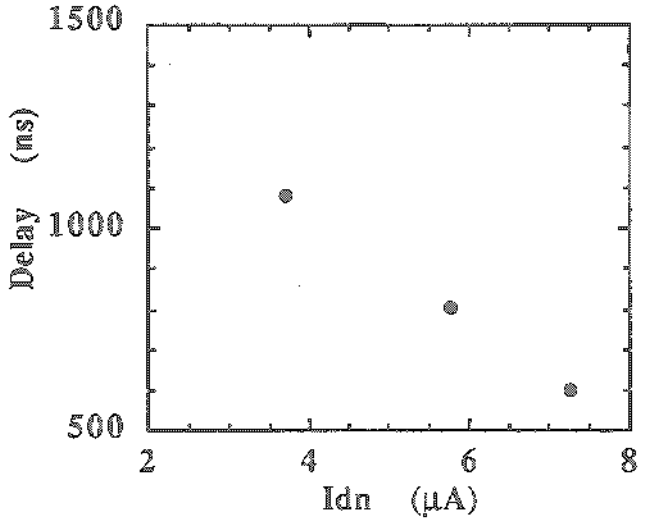

Fig. 13 Average delay for a 6-ladder array as a function of the adjustable current source Idn. The strobe durations were respectively 800 ns, 500 ns and 400 ns.

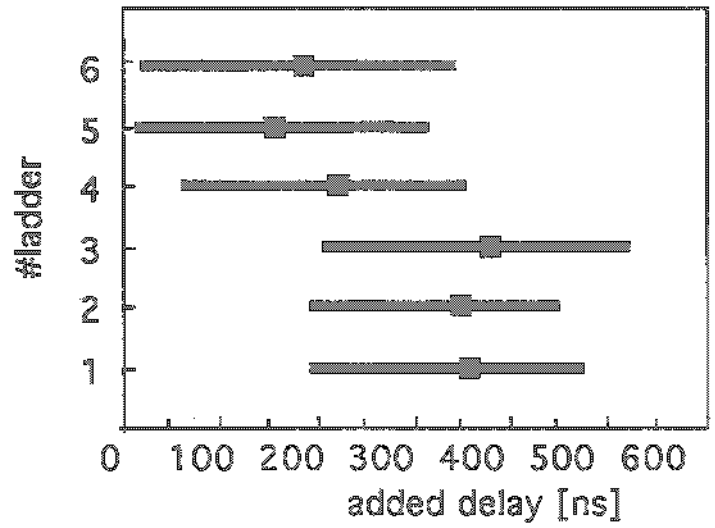

Fig. 14 The values of the added external strobe delay in the T9 test beam. The 'added delay' has been varied but the response is not identical for each ladder. The optimal number of coincidences (or 'efficiency') was obtained at the value indicated by the black square. The line indicates the FWHM of the efficiency distribution. The duration of the strobe signal itself was 500 ns. Ladder #1 is at the 'top' of the array, furthest away from the supplies.

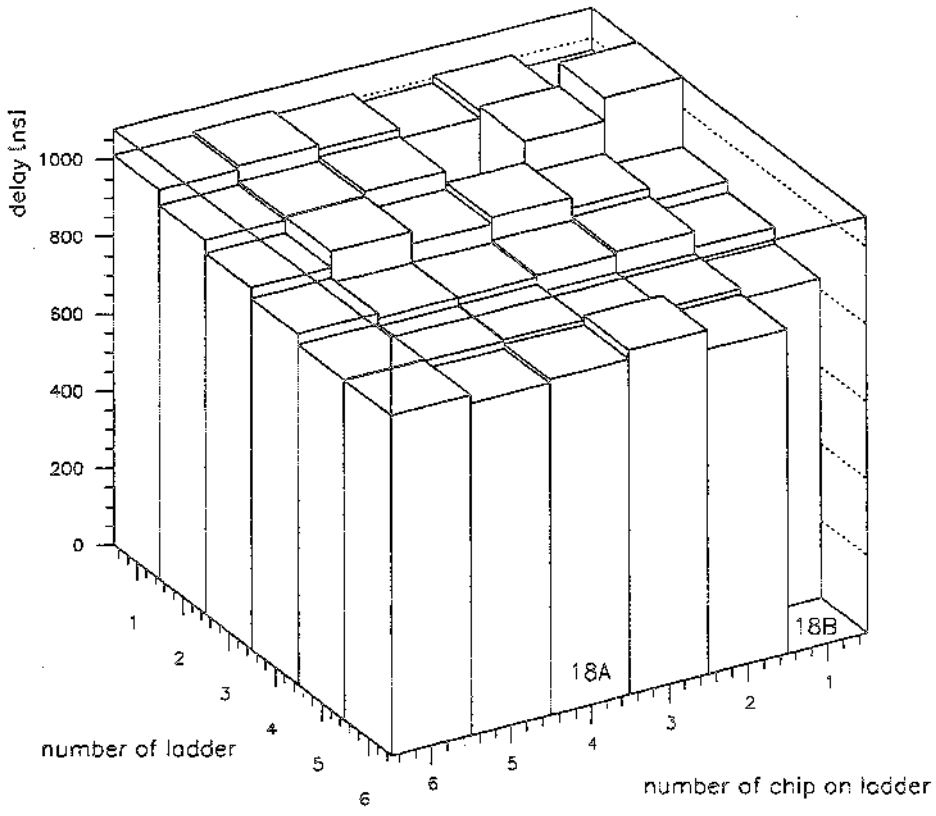

Fig. 15 Histogram of delays in the pipelines averaged for each chip in the array as measured with the electrical test rows. As in fig. 14 a top (ladder 1)-bottom (ladder 6) non-uniformity can be seen, now in more detail for the separate chips.

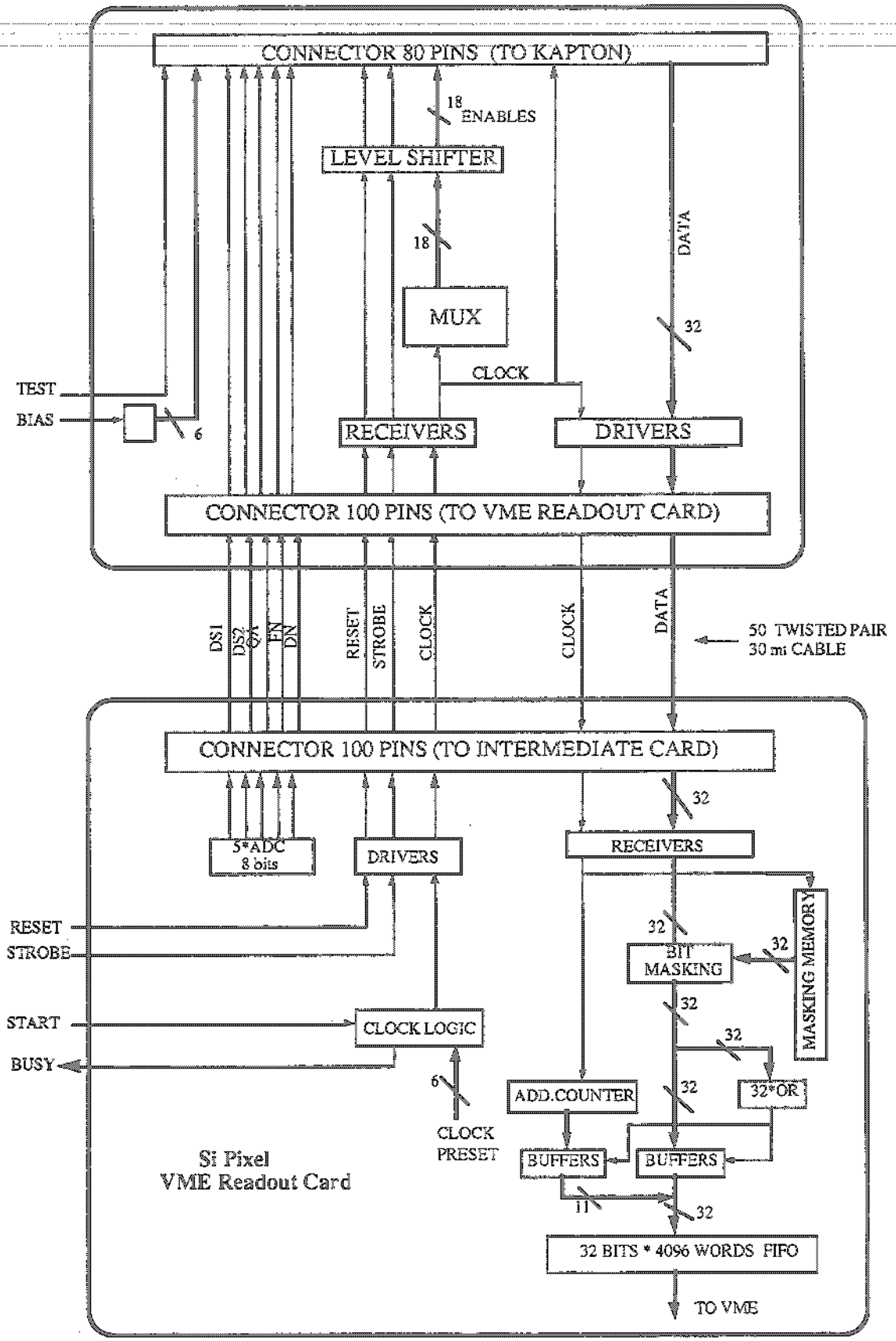

Fig. 16 Block diagram for the intermediate readout card (top) and the VME board at the bottom.

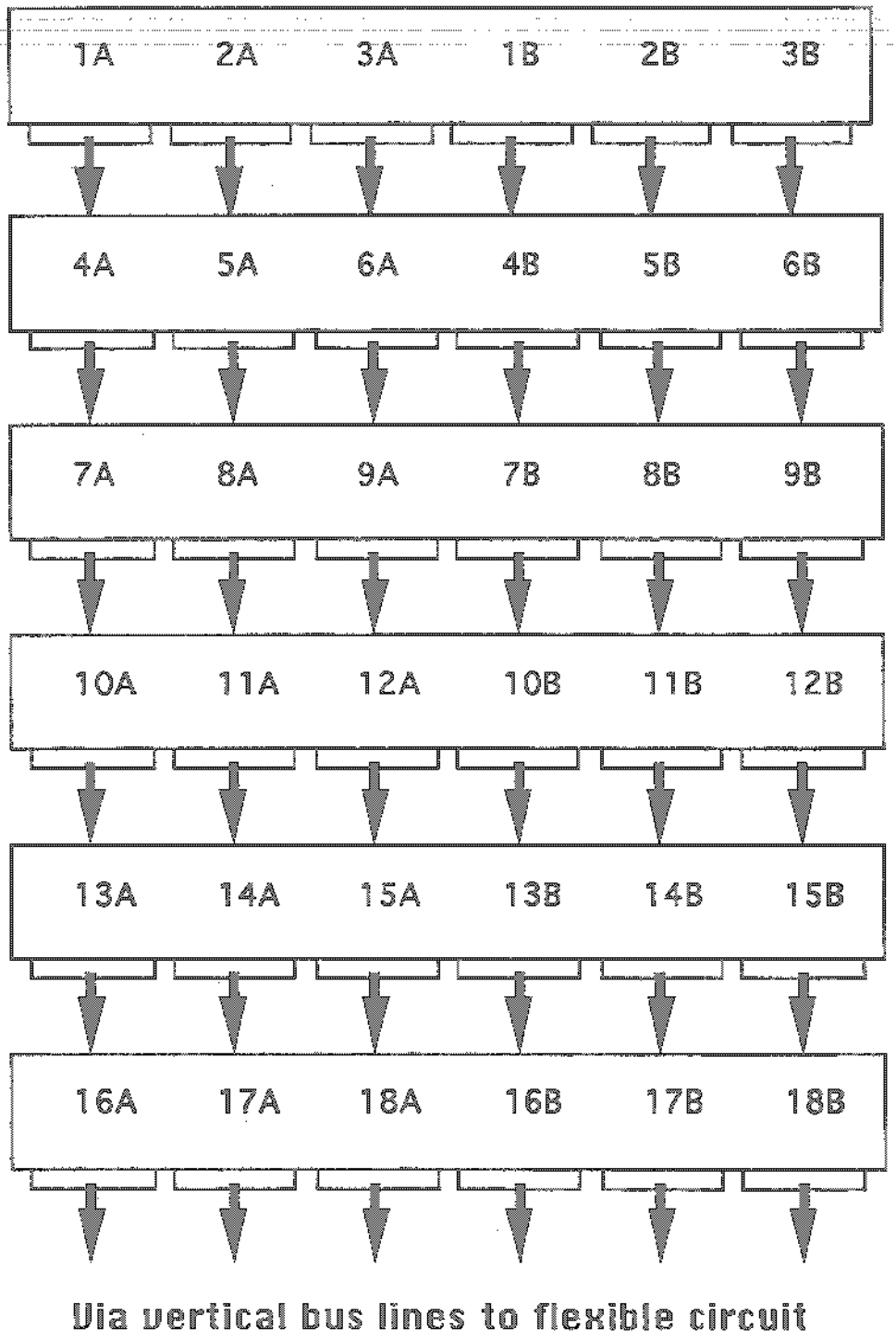

Fig. 17 Readout sequence of the chips. 1A and 1B are read in the first 64 clock cycles via the buses in columns 1 and 4, then 2A and 2B in the second 64 via bus columns 2 and 5, etc. The access of each chip to the bus is granted or denied by external switching of tristate drivers on the chip itself

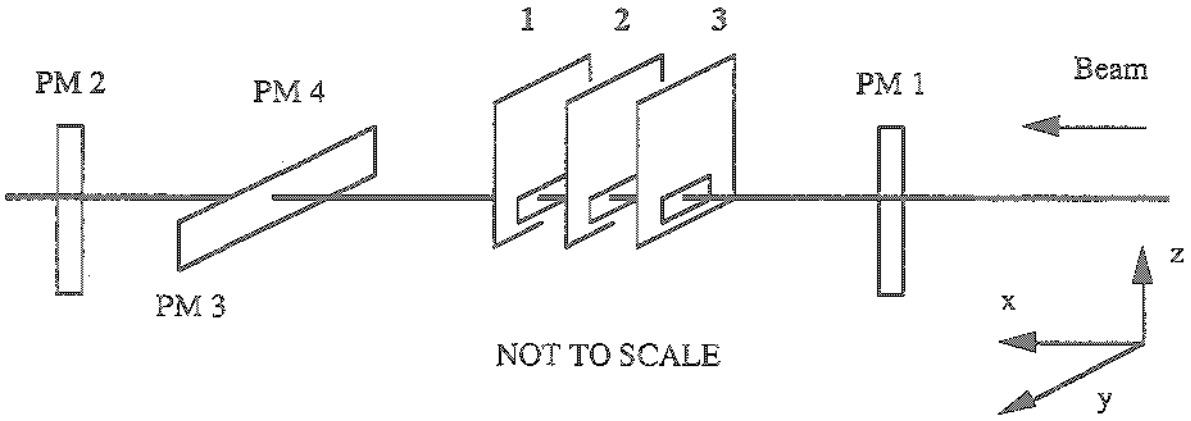

Fig. 18 Setup of the telescope of 3 single assemblies in the H6 test beam, with various scintillators for beam definition. Beam particles are defined by the coincidence of several small scintillators, in particular 2 crossed scintillating fibers PM3 and PM4. The resulting spot measures only ~1 mm x 2 mm.

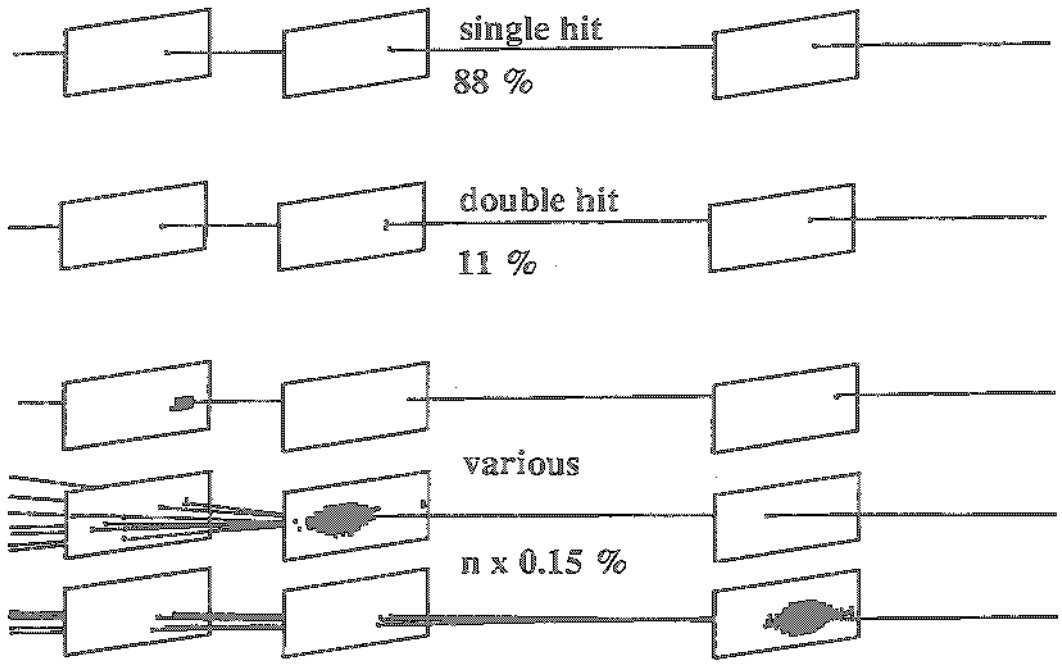

Fig. 19 Pictorial representation of the statistics of single and multi-hit clusters in the beam test with 3 detector planes. It shows the powerful pattern recognition of the micropattern detector even for large numbers of hits in a cluster.

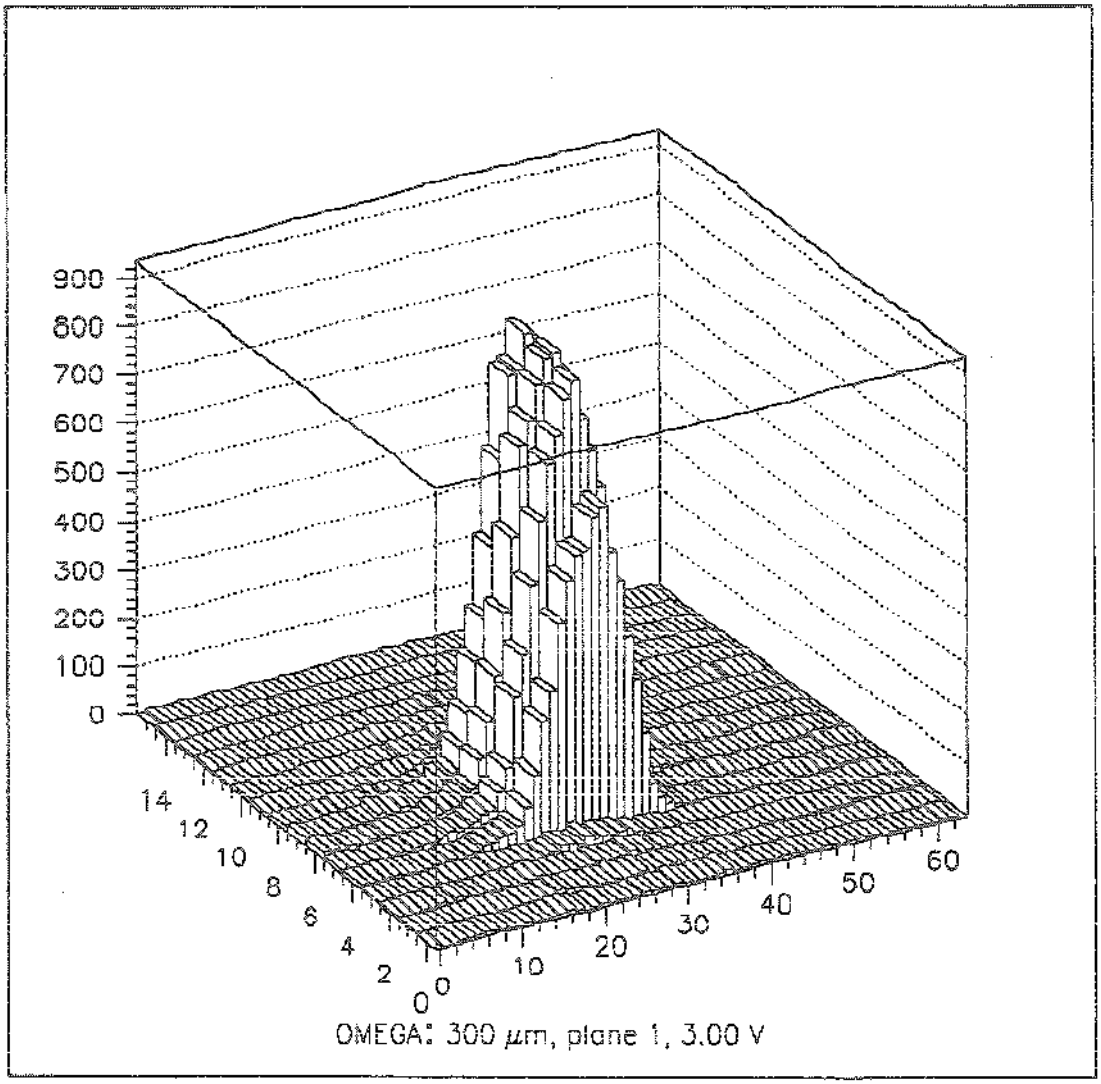

Fig. 20 Histogram of the beam spot consisting of the coordinates of hits as recorded by a 300 μm thick micropattern detector. The threshold corresponds to 30 μA or ~6000 electrons.

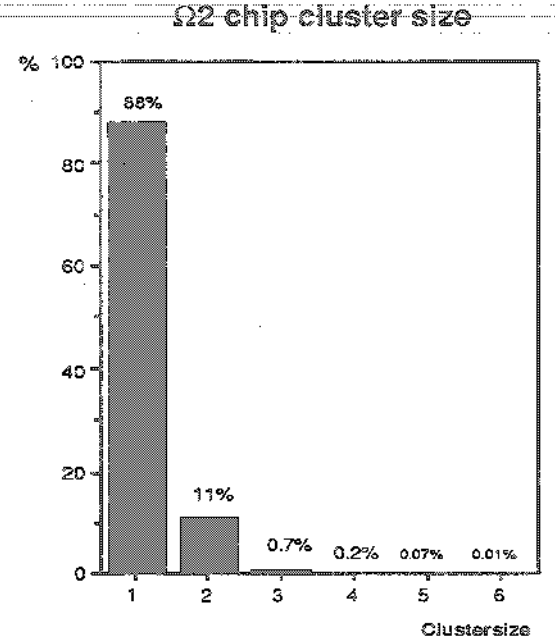

Fig. 21 Histogram of the cluster size for single beam tracks in a 300 µm thick detector.

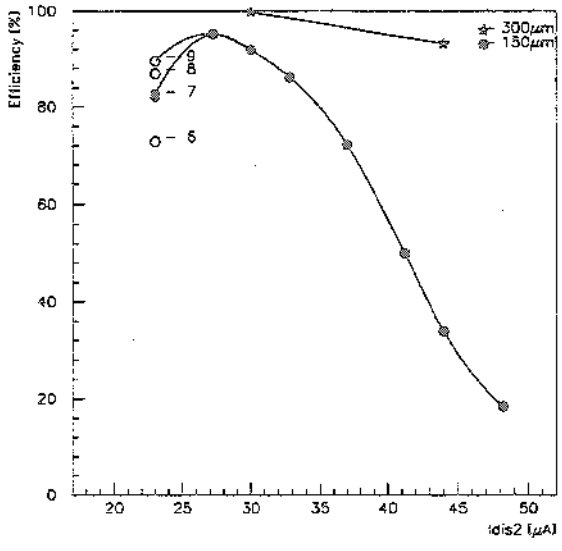

Fig. 22 Comparison of detector efficiency for a 150 µm and a 300 µm thick detector as a function of the discriminator threshold. The drop of efficiency below 25 µA is related to the influence of Idis2 on the preamplifier gain itself, causing the non-linearity already shown in fig. 10.

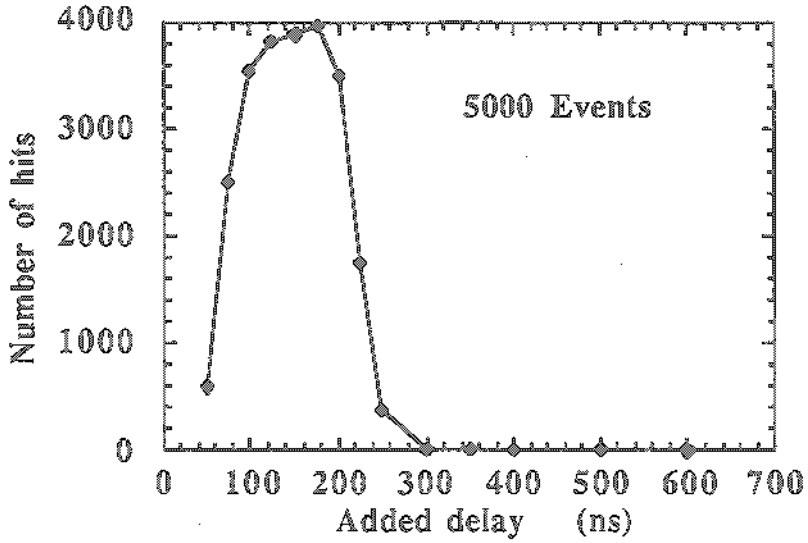

Fig. 23 Scan of the added delay time after which the strobe signal of 200 ns duration is issued. Each point represents 5000 event triggers, generated by an electron traversing the single ladder detector. The setting for the threshold was Idis2 =41 μA and Idis1 = 32.5 μA, Iqa = 90 μA, Idn = 4 μA and Vbias=50 V.

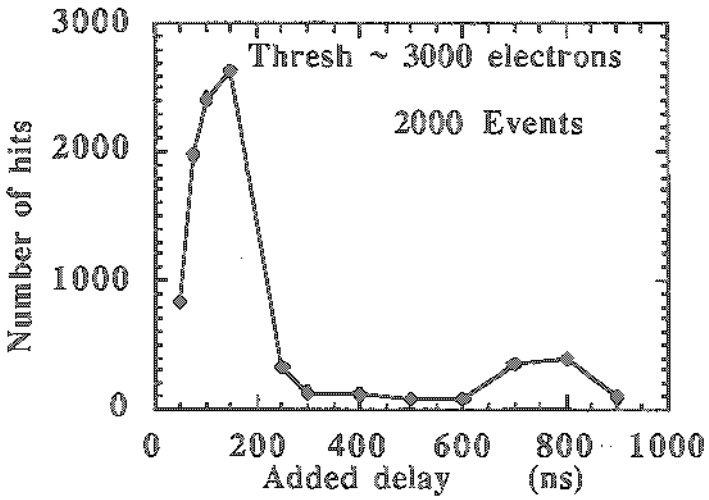

Fig. 24 Idem as fig. 23 but with a low threshold of ~3000 electrons: Idis2=24 μA. The ~10% hits detected at 800 ns are likely to be caused by propagation of the reset signal from a previous hit in the adjacent pixel cell.

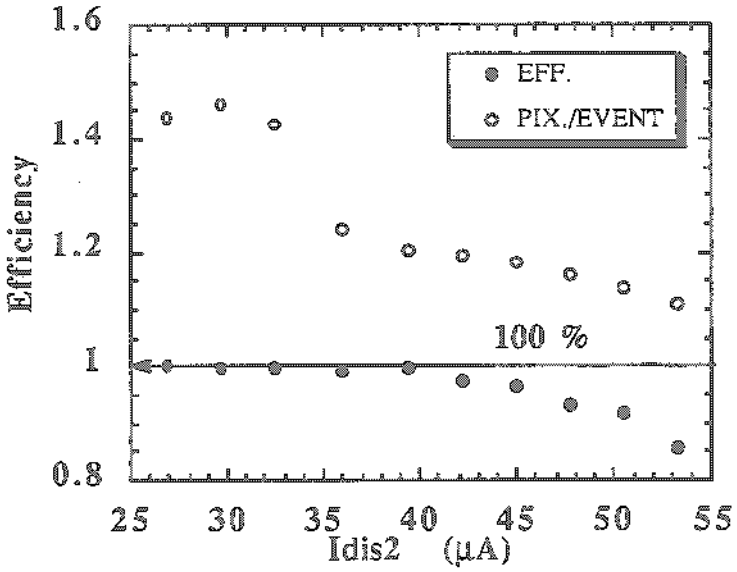

Fig. 25 Efficiency and number of hits per event for a 6-ladder array as a function of adjustable threshold Idis2. Each point represents 2000 triggers, strobe duration was 500 ns and added strobe delay 50 ns.

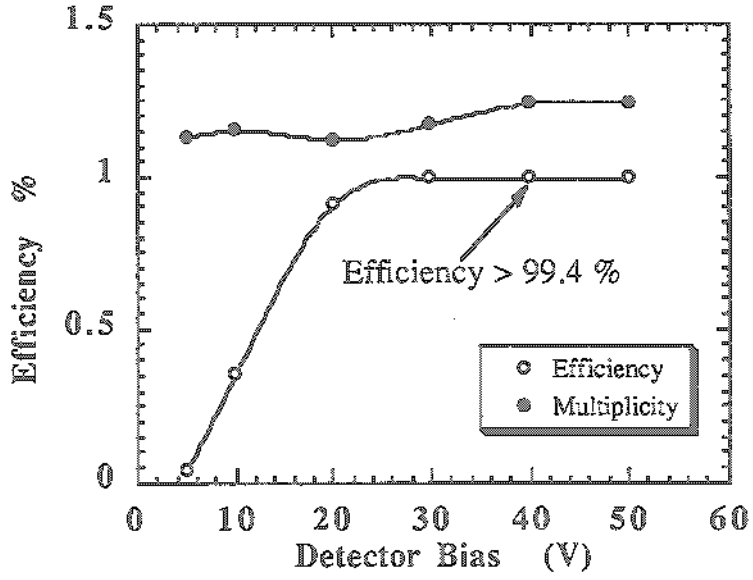

Fig. 26 Efficiency and number of hits per event for a 1-ladder array as a function of detector bias voltage Vbias. Idis1=Idis2=30 μA, Idn=4 μA, strobe duration 200 ns, added strobe delay 150 ns.

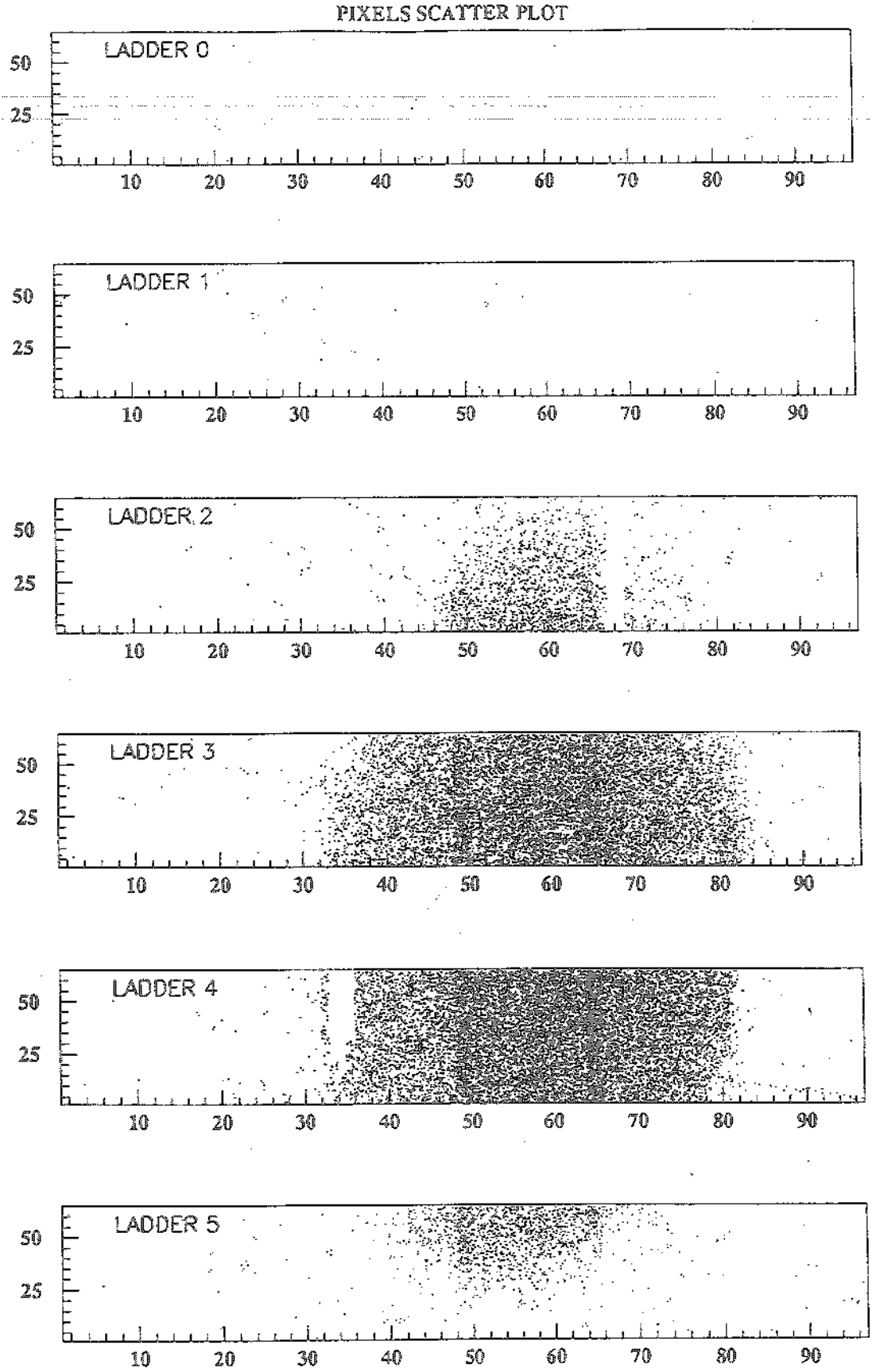

Fig. 27 On-line scatter plot of approximately 25 000 hits in the 6-ladder array from 50 000 beam triggers. The dark bands are explained in the text.

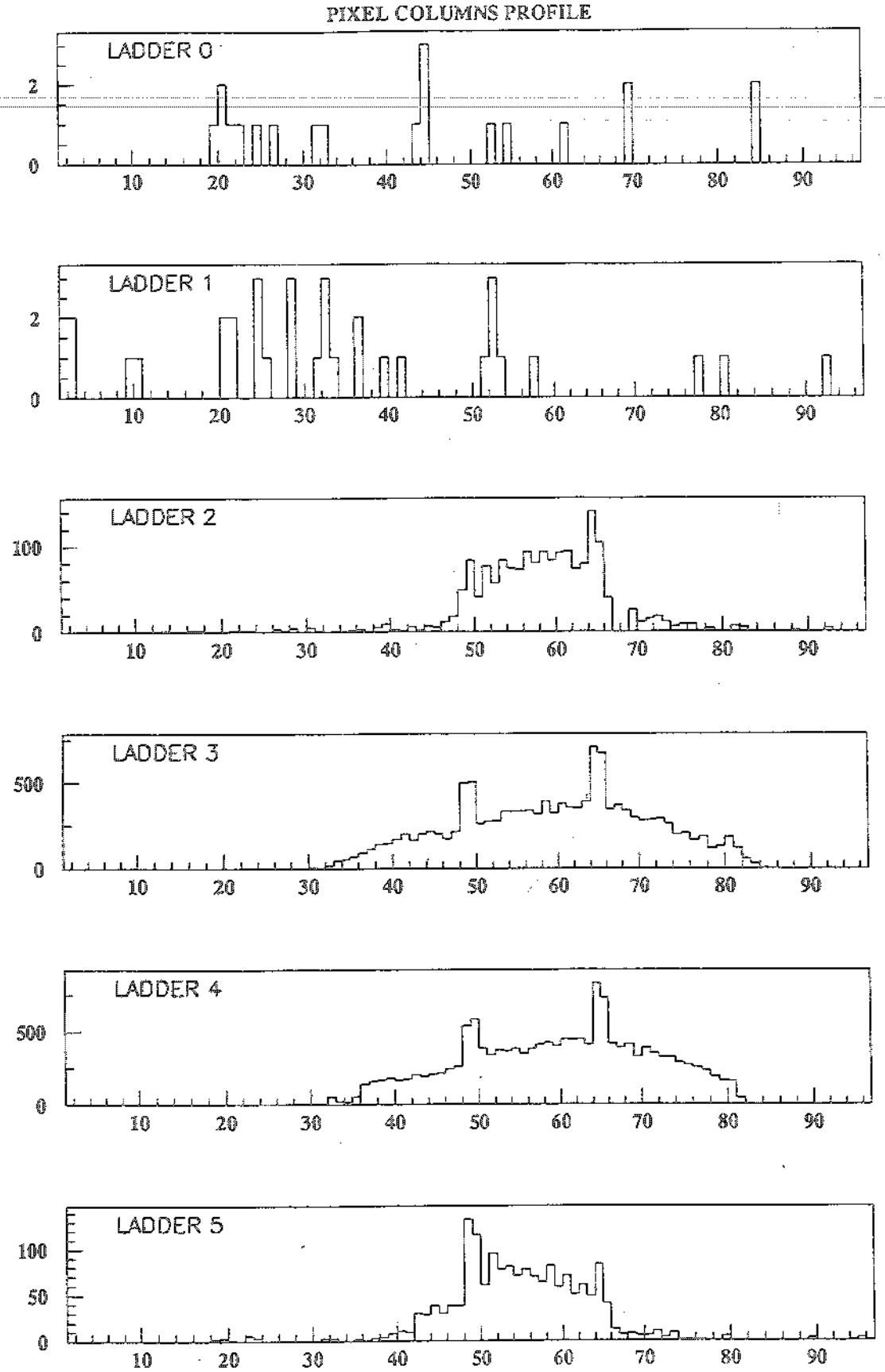

Fig. 28 Projection of the hits in each ladder in fig. 27 in the direction of the columns. Note the change of the vertical scales from ladder to ladder.

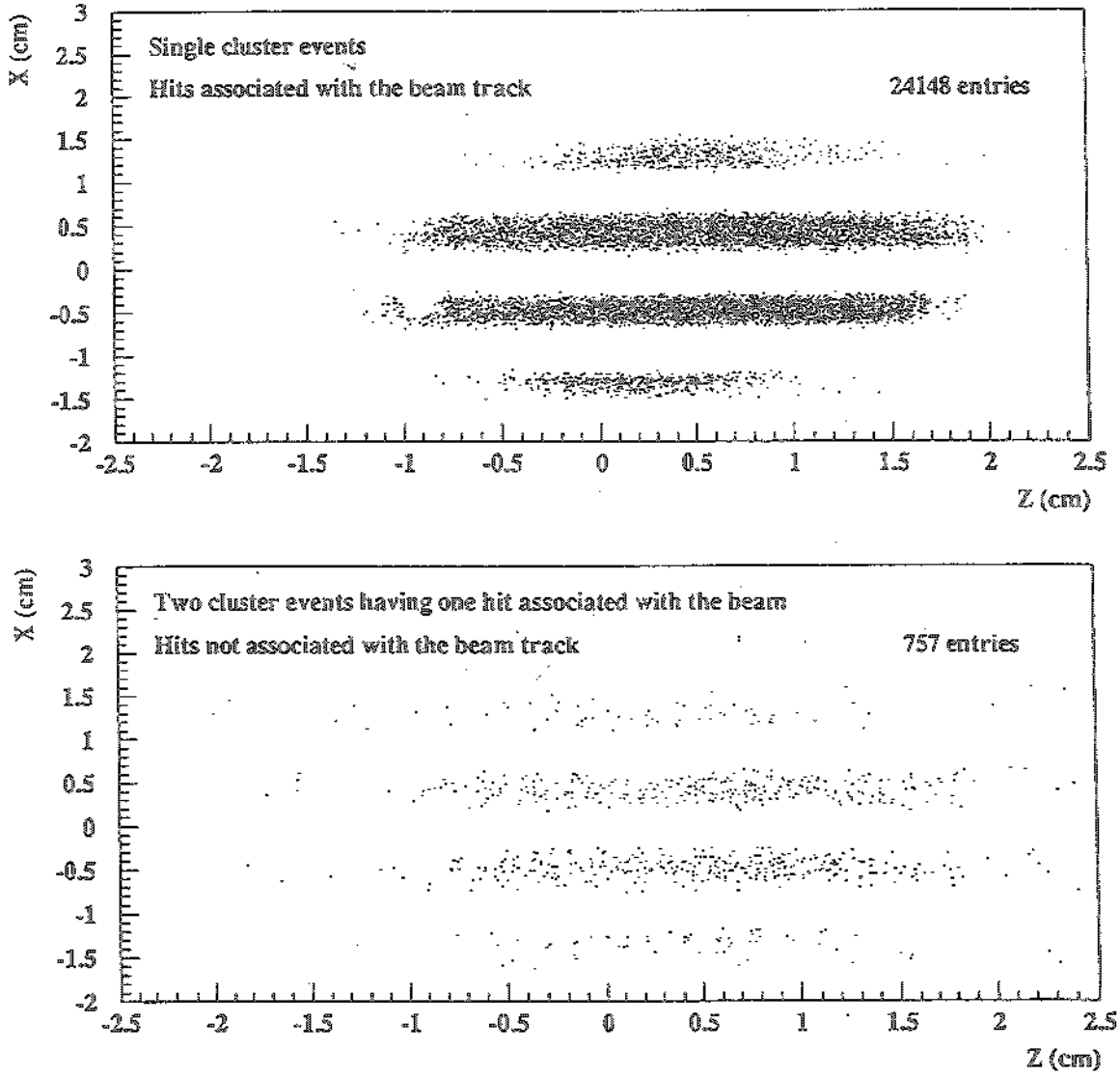

Fig. 29 Top: Off-line representation of selected data from fig. 27, geometrically corrected. Only hits from single cluster events are plotted.

Bottom: Idem for 2-cluster events with only those hits that are not associated with the wirechamber-determined beam track. These hits are nevertheless correlated with the beam position. They can be explained by the longer strobe time of the pixel array and by correlated delta electrons.

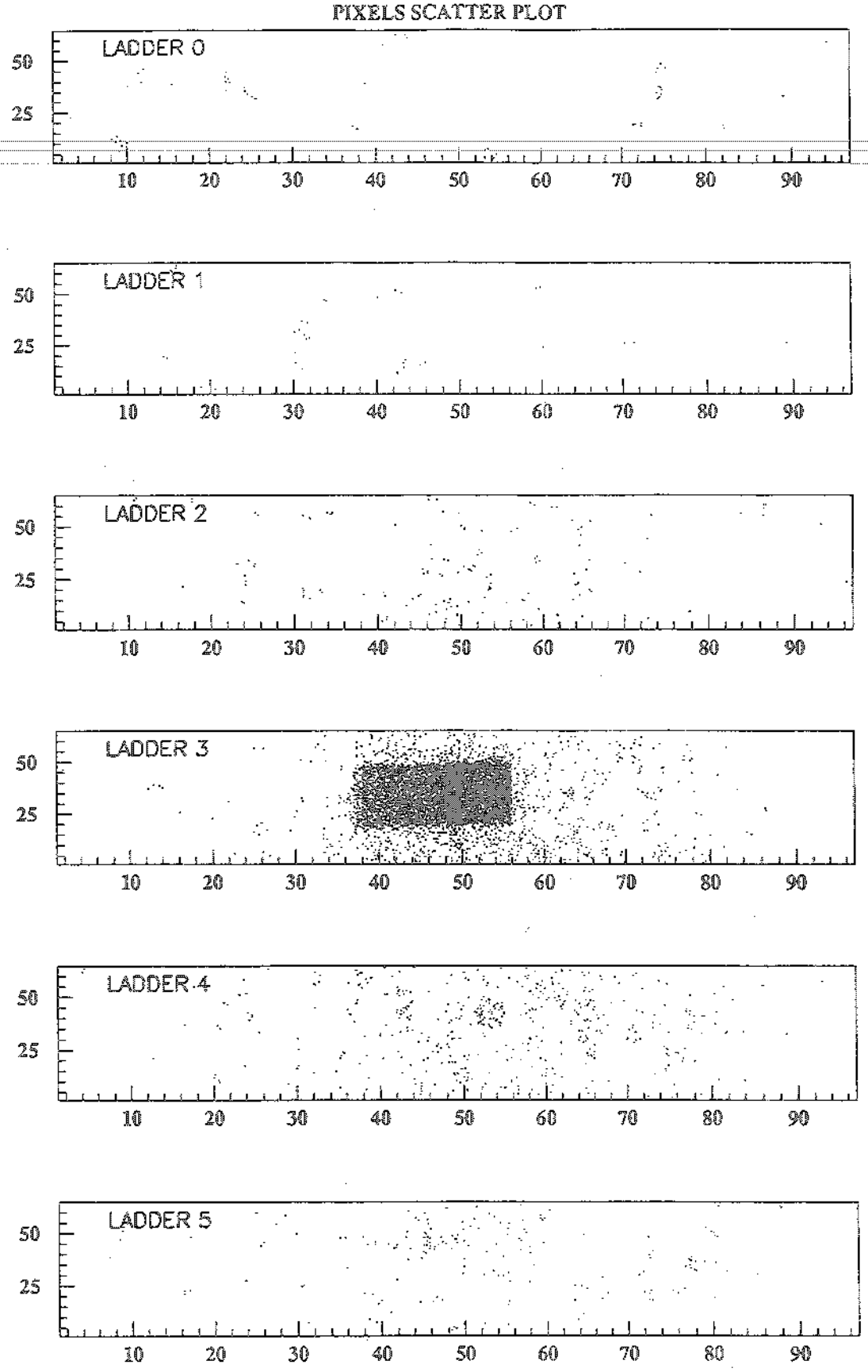

Fig. 30 On-line scatter plot of hits with the 8 mm x 2 mm scintillator in the event trigger. The scintillator is covering the "stitching" area between 2 readout chips. The background hits below the scintillator are mostly due to particles which crossed the detector and generated a trigger via Cerenkov light in the optical fiber that connected the scintillator to the remote phototube.

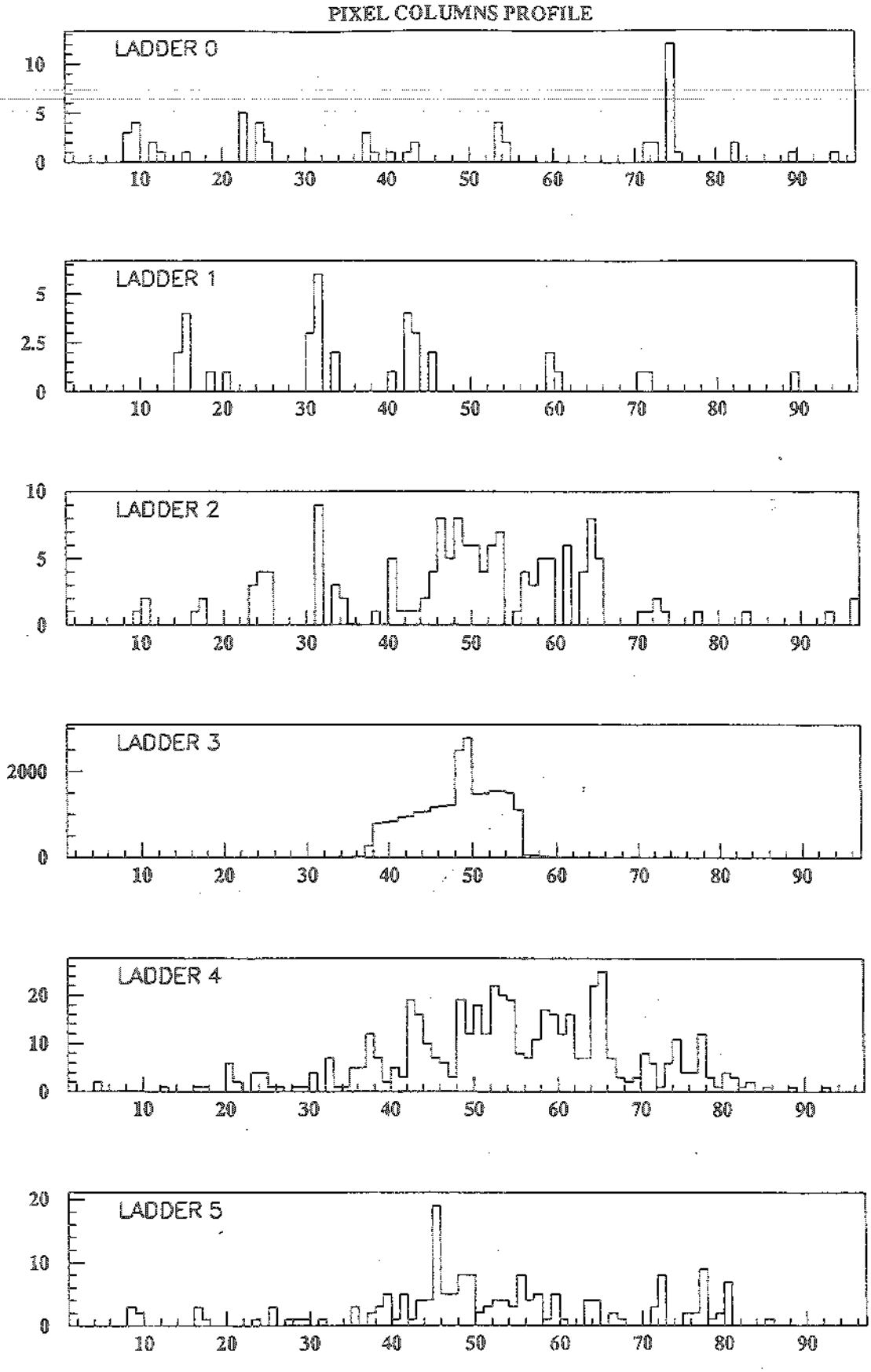

Fig. 31 Projection of the hits of fig. 30 in the direction of the columns.

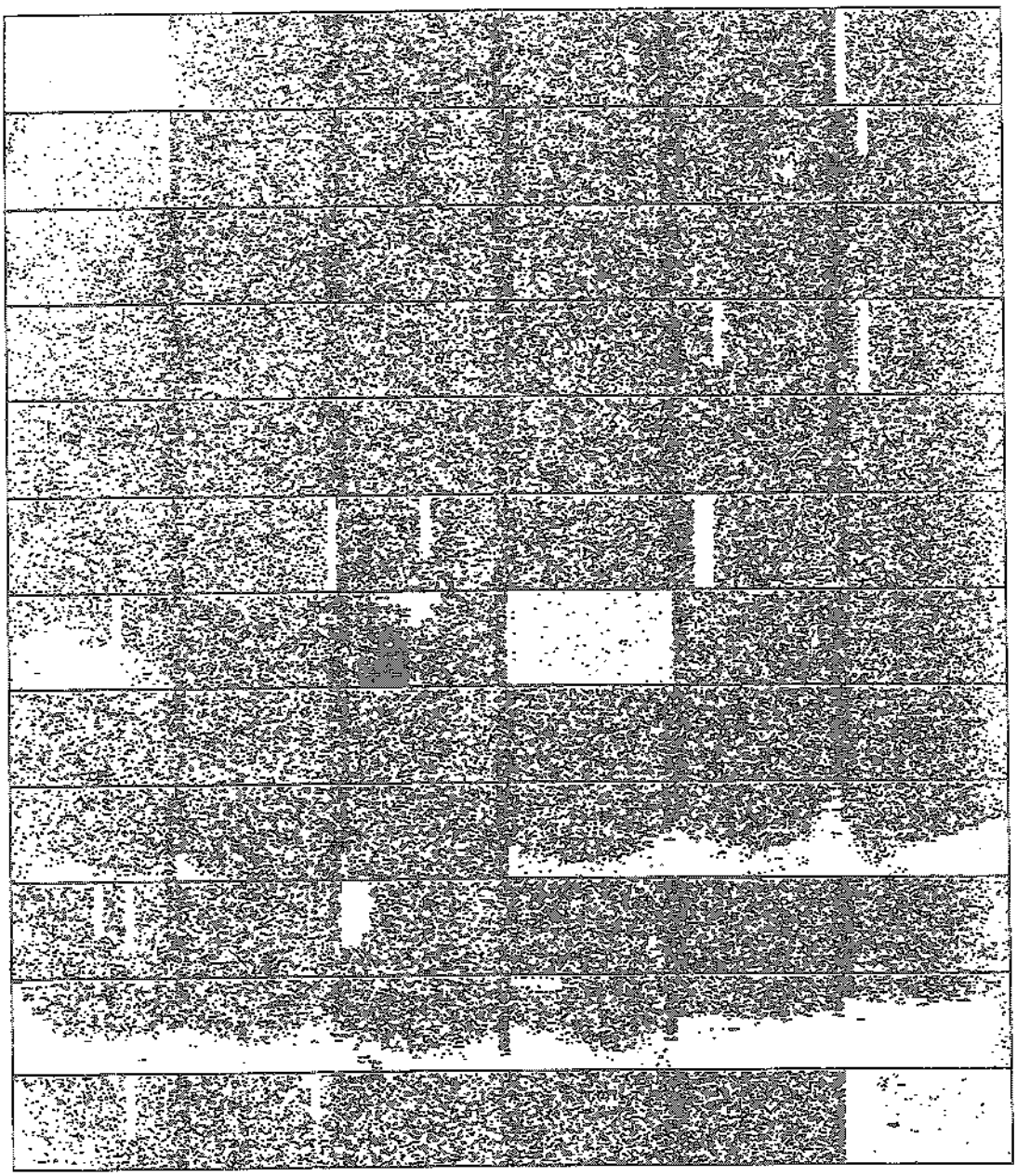

Fig. 32 Scatter plot of particle positions in 50 000 events for a complete detector with double array, comprising 12 detector ladders and 72 readout chips. The separations between the readout chips are visible as vertical, dark bands. The strobe pulse started immediately after the trigger pulse and the strobe duration was 1 μs.

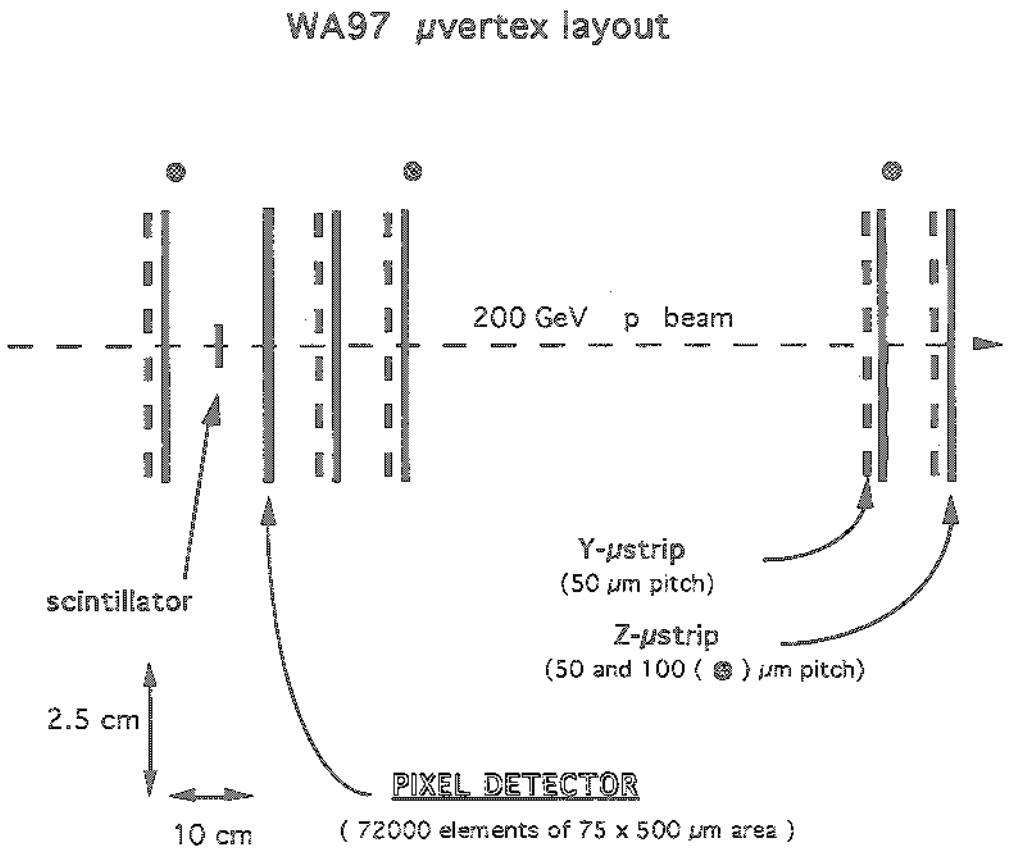

Fig. 33 Top view of the layout of the pixel detector and 5 doublets of microstrip vertex detectors in the Omega WA97 run in November 1993. 3 of the horizontal microstrip detectors have a pitch of 100 μm instead of 50 μm which leads to a reduced reconstruction precision in the z-coordinate. During the test the vertical magnetic field was not on.

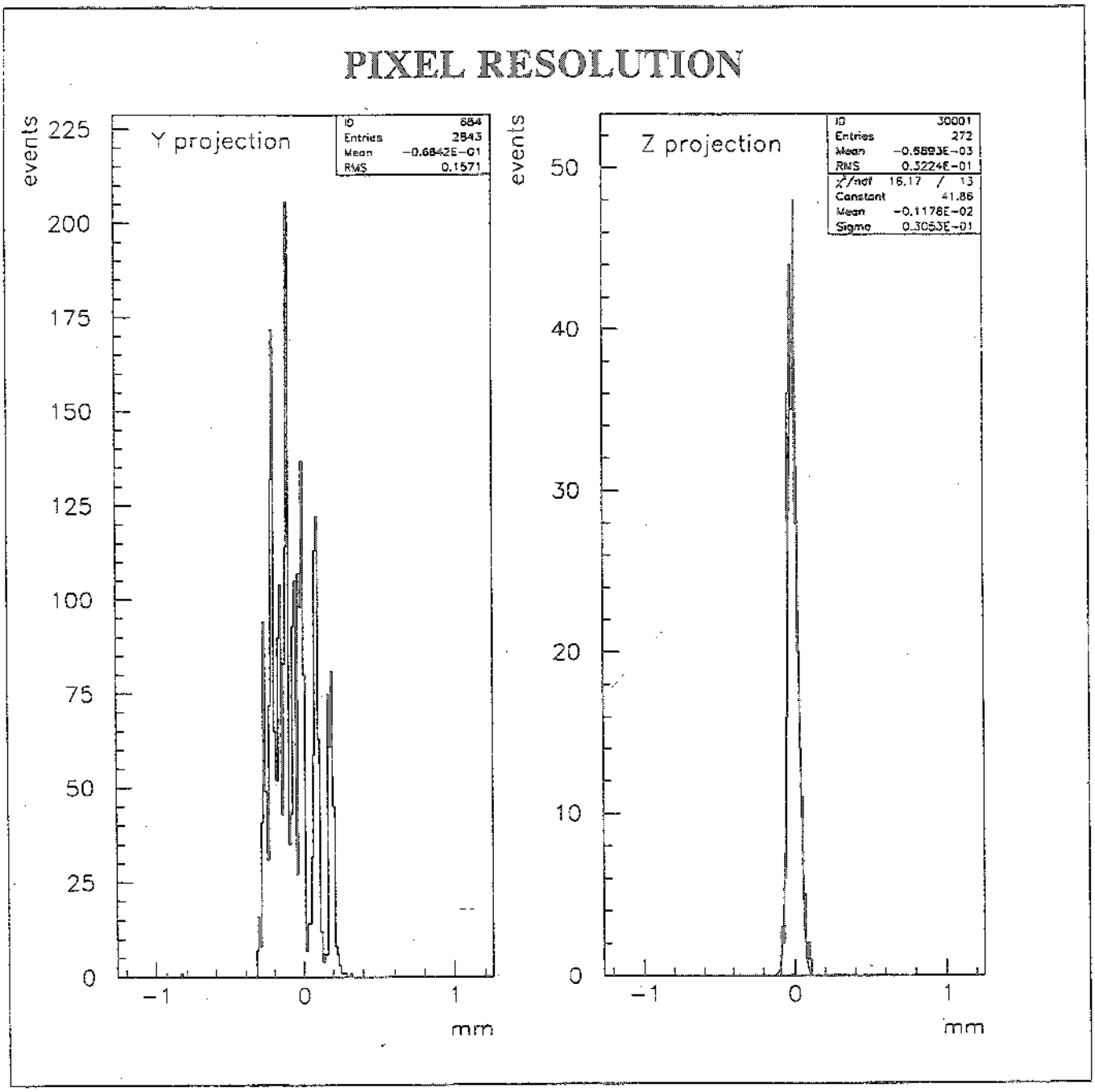

Fig. 34 Histograms of the distribution of residual values between predicted and measured coordinates in the y and z projection (see fig.33). The calculated standard deviations are 157.1 μm (y) and 30.5 μm (z) and these indicate a precision in the pixel detector of 156 μm and 22 μm in the y- resp. z direction.

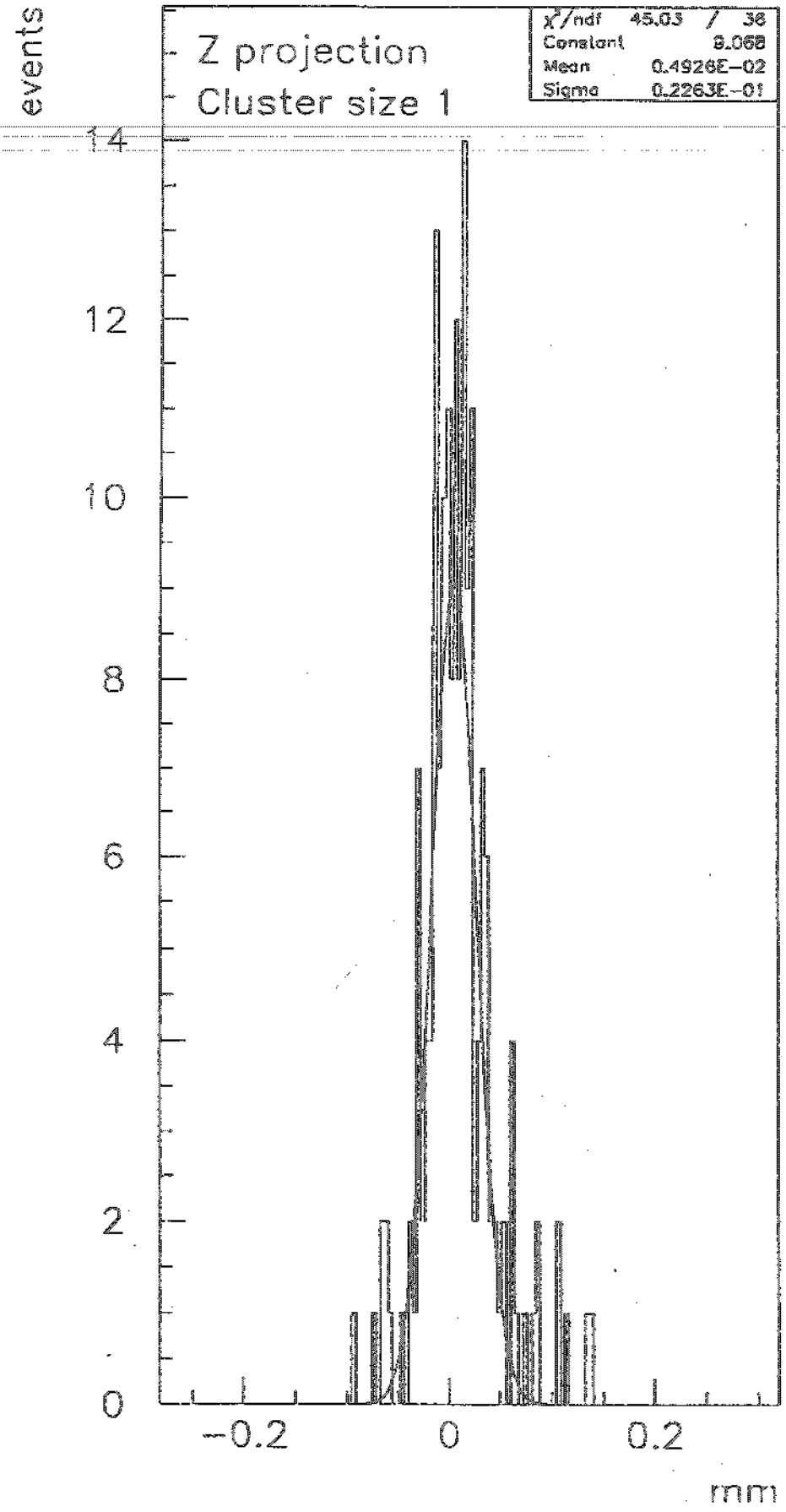

Fig. 35 Distribution in z as in fig. 34 but for selected events with 2 adjacent hits in cells in the same column. The standard deviation is now only 22.6 μm giving a precision of better than 10 μm in the pixel detector.