First-Order SPICE Modeling of Extreme-Temperature 4H-SiC JFET Integrated Circuits

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Abstract

A separate submission to this conference reports that 4H-SiC Junction Field Effect Transistor (JFET) digital and analog Integrated Circuits (ICs) with two levels of metal interconnect have reproducibly demonstrated electrical operation at 500 °C in excess of 1000 hours. While this progress expands the complexity and durability envelope of high temperature ICs, one important area for further technology maturation is the development of reasonably accurate and accessible computer-aided modeling and simulation tools for circuit design of these ICs. Towards this end, we report on development and verification of 25 °C to 500 °C SPICE simulation models of first-order accuracy for this extreme-temperature durable 4H-SiC JFET IC technology. For maximum availability, the JFET IC modeling is implemented using the baseline-version SPICE NMOS LEVEL 1 model that is common to other variations of SPICE software and importantly includes the body-bias effect. The first-order accuracy of these device models is verified by direct comparison with measured experimental device characteristics.

Keywords: SiC, JFET, Integrated Circuit, SPICE

I. Introduction

A separate submission to this conference reports fabrication and testing of 500 °C 1000+ hour durable SiC JFET ICs with two levels of metal interconnect [1]. This advance to multi-level interconnect for 500 °C durable ICs facilitates more rapid up-scaling to higher levels of complex electronic functionality in order to better meet the needs of various aerospace, automotive, energy production, and industrial systems [2,3]. For further development and application adoption of such extreme temperature durable ICs, the realization of readily accessible and usable IC design and simulation tools is clearly important. Towards this end, this paper reports on the development and experimental verification of first-order accuracy SPICE models for design and simulation of this IC technology over the ambient temperature (T) range of 25 °C to 500 °C.

II. Technology Overview

Given that prolonged and stable IC functionality is crictical for most applications, the JFET IC technology emphasizes extreme temperature durablity and stability over other semiconductor device performance metrics. *The 500 °C durable ICs are comprised of 4H-SiC n-channel JFETs and 4H-SiC n-channel resistor primitive devices connected by two levels of conductive metal interconnect* [1,4-6]. A simplified cross-sectional diagram of this approach is illustrated below in Figure 1. A SiC JFET on the left is integrated with a SiC resistor on the right, so that this cross-section forms a simple inverting amplifier sub-circuit. The JFETs are "normally-on" (or "depletion mode") at zero gate bias V_G and turn off with application of sufficiently negative gate voltage.

Because the resistor channels and JFET channels are both implemented in n-type 4H-SiC, these devices exhibit very similar temperature dependence [7,8]. This fact enables simplified design of circuits that successfully function over extremely

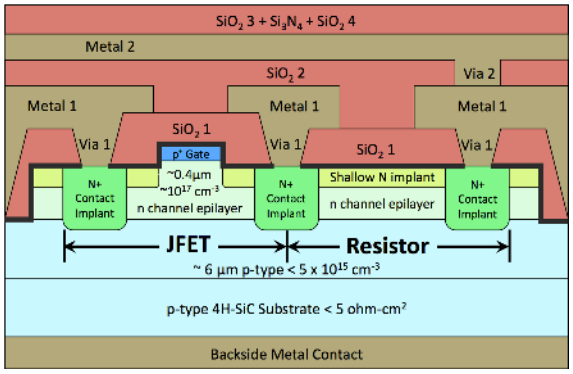

Figure 1. Simplified schematic cross-section of SiC JFET and resistor device structure with two-levels of interconnect used to realize 500 °C durable ICs.

broad temperature ranges. As shown in Figure 1, all 4H-SiC devices reside on top of an electrically biased p-type 4H-SiC substrate, so their electrical properties are therefore somewhat dependent on substrate bias voltage V_S via the substrate body bias effect [9].

A major circuit biasing constraint for JFETs is that significant forward bias (i.e., beyond about 1 V that would draw significant forward current interfering with desired signals in the n-channels) must be avoided for all pn junctions in the structure. To avoid drawing current through the (lower) substrate-channel pn junction, the substrate/chip backside contact is always (reverse) biased at the negative power supply voltage $-V_{SS}$.

Since depletion mode n-channel JFETs require negative gate voltage V_G to turn-off source-to-drain current flow I_D, negative signal input and output voltages are used for digital and analog circuit implementation. The basic logic gate circuit used in this work, which operates with output high voltage V_{OH} ~ 0 V and output low voltage V_{OL}~ $-V_{SS}/2$, has been well-described elsewhere [7,8,10]. *This circuit approach vitally (1) avoids forward biasing the gate-to-channel pn junction (Fig. 1), and (2) relies on relative layout ratios of transistor and resistor dimensions, rather than absolute values of device parameters.* Most circuits require $+V_{DD}$, GND (ground), and $-V_{SS}$ power supply inputs.

Hierarchical cell-based device and circuit layout is accomplished starting from primitive cells with 6 µm minimum feature size and 3 µm alignment tolerance layout rules. The designed gate length L_G of all JFETs is 6 µm, while the designed gate width W_G is always a multiple of 12 µm. *Therefore, all JFETs consist of one or more paralleled W_G=12 µm/L_G=6 µm "standard JFET unit cells" arrayed in single-gate-finger or multiple-gate-finger layout configurations.* The JFET unit cell includes source and drain mesa and contact regions with the necessary high-dose n^+ contact implants, ohmic contact vias and contact metalization that are depicted in cross-section in Figure 1. Similarly, all n-type SiC resistors were designed with 6 µm n-type mesa width and identical contact implant/via/metal end regions.

III. SPICE Modeling Approach

Circuit modeling is implemented using baseline-version SPICE with features and models common to other variations of SPICE software [11,12]. This approach offers the broadest accessibility to potential users, and its first-order accuracy is sufficient in light of electrical parameter variations documented in the following sections of this paper. While baseline-version SPICE implements basic JFET and semiconductor resistor devices, neither of these basic SPICE models account for the substrate body bias effect. *Therefore, the baseline SPICE NMOS LEVEL 1 model, which importantly includes body bias effect, is instead chosen for first-order modeling of these wafer-integrated devices [9,13]. It is important to note that this NMOS modeling approach is only valid so long as JFET gate and substrate pn junctions do not become forward biased,* which is the case for the circuits implemented in this work. Also, the baseline-version SPICE software NMOS model crashes when the SPICE TEMP (temperature) simulation parameter exceeds ~300 °C. Therefore, SPICE temperature dependence is handled by calculating different NMOS models that each represent device behavior at a desired simulation temperature, but are all run with TEMP=27.

The remainder of this paper is dedicated to extraction and verification of relevant NMOS LEVEL 1 parameters that model experimentally observed device and circuit behavior to first order accuracy across the wafers from 25 °C to 500 °C.

IV. Experimental Extraction of SPICE Models

Experimental measurements from two successively processed JFET IC wafer runs were used for SPICE model development/verification: 76 mm diameter epitaxial "Wafer 8.1" (procured in 2008) was processed first [4,5,14], followed by 76 mm diameter epitaxial "Wafer 9.2" (procured in 2014) [1,6,14]. While the same photolithography masks were used for both wafers, Reference [6] describes all the significant differences in processing between the two wafers. Most relevant to this report was the difference in source/drain 4H-SiC ohmic contact processing: Wafer 8.1 used titanium (Ti) metal to contact the high-dose nitrogen implant,

while Wafer 9.2 used hafnium (Hf) metal to contact the high-dose phosphorous implant.

At the conclusion of fabrication prior to dicing, all devices and circuits on both wafers were electrically characterized on a probing system using computer-controlled test instruments that enabled complete-wafer maps of electrical parameters at 25 °C. Following dicing, a few chips selected from each wafer were bonded into custom ceramic packages [15] and wired for computer-automated prolonged high temperature testing in separate ovens.

A. Electrical Parameters vs. Wafer Position

In mature IC wafer manufacturing technologies, device/circuit electrical parameters exhibit negligible dependence on position across large wafers. As described in this section, such uniform electrical behavior is clearly *not presently* the case for this newly demonstrated 500 °C durable IC process technology.

1. JFET Behavior vs. Wafer Position

Both Wafers 8.1 and 9.2 exhibit significant dependence of device electrical behavior on radial device distance ***r*** from the center of each wafer. The four measured JFET drain current vs. drain voltage (I_D vs. V_D) characteristics (with gate voltage V_G steps shown) of Figure 2 are representative of this dependence. Specifically, Figure 2 compares 25 °C 12 µm/6 µm JFET I_D vs. V_D characteristics from both wafers measured at ***r*** = 0.3 cm (near wafer center) and ***r*** = 3 cm (near wafer edge). As seen in Figure 2 characteristics, JFETs near the wafer edge exhibit substantially more negative threshold voltage V_T, which results in larger on-state currents. I_D vs. V_G sweeps (shown elsewhere [1,6]) demonstrated complete JFET channel turn-off to less than 1/1000th of on-state current.

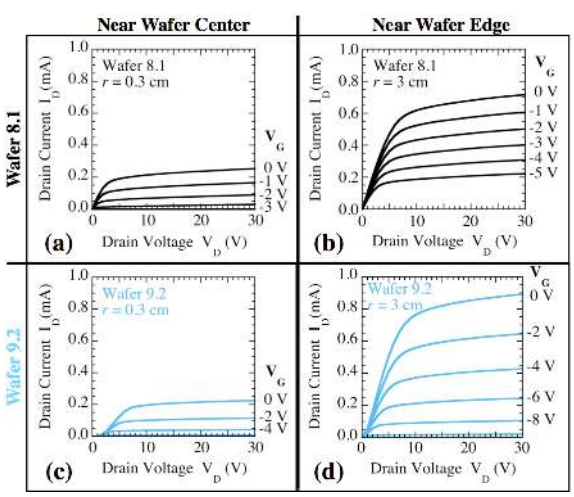

Figure 2. Drain characteristics of 12µm/6µm JFETs at V_S = -15V from Wafer 8.1 (top, black) and Wafer 9.2 (bottom, blue), near the wafer center (***r*** = 0.3 cm, left) and near the wafer edge (***r*** = 3 cm, right), all plotted on the same current scale.

Most JFET on-state channel conduction parameters depend on threshold voltage V_T [16,17]. Figure 3 plots the 25 °C V_{TO} (i.e., Zero-Bias Threshold Voltage = SPICE VTO parameter = V_T at V_S = 0) of both experimental wafers as a function of device radial distance ***r*** from the wafer center. Both wafers demonstrate the similar trend of substantially more negative V_T with increasing radial distance ***r*** from the wafer center. As there is no implant residing directly beneath the JFET p+ gate (Fig. 1), *the threshold voltage V_T of all JFETs is governed by the doping and thickness of the as-received commercially-grown epilayers.* A secondary ion mass spectroscopy (SIMS) study conducted on Wafer 8.1 [9] revealed that n-channel thickness variation is primarily responsible for V_T positional dependence, and that physical thickness of the JFET n-channel epilayer can be extracted from measured V_T data. This study also documented/verified behavior and modeling of JFET body effect parameter γ (SPICE NMOS model parameter GAMMA).

Figure 4 quantifies the large (~ 4-fold) increase in measured JFET saturation current I_{DSS} with ***r*** that primarily arises from the V_T ***r*** position dependence. The larger I_{DSS} scatter for Wafer 9.2 is attributed to contact effects described in the next section. In contrast to V_T and I_{DSS}, channel-length modulation parameter λ (SPICE LAMBDA) exhibited almost no dependence on ***r***, with $\lambda \simeq 0.006\ V^{-1}$ for both wafers.

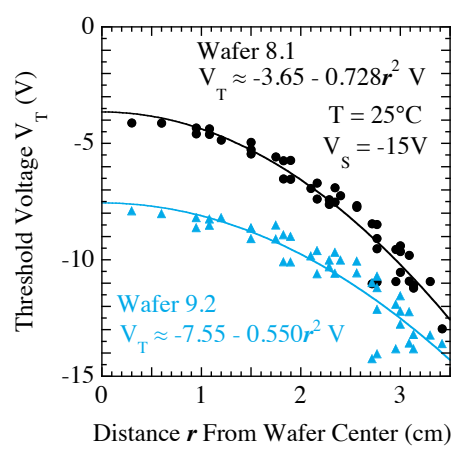

Figure 3. Measured JFET threshold voltage V_T as a function of radial device distance ***r*** from the center of the wafer.

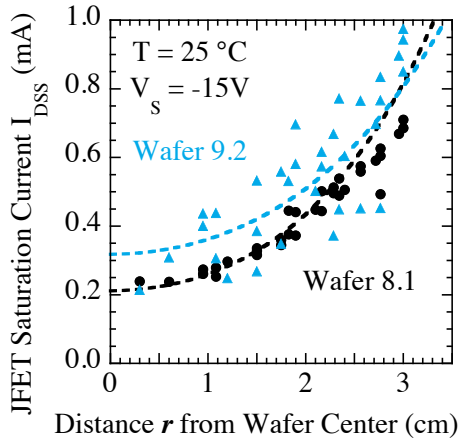

Figure 4. 12µm/6µm JFET drain saturation current I_{DSS} as a function of radial distance ***r*** from the wafer center. Symbols are experimentally measured data, dashed lines are software-generated SPICE parameter modeling results.

2. Resistor Behavior vs. Wafer Position

The other notable behavior for the JFETs of Figure 2 is the non-linear shape of the Figure 2c Wafer 9.2 I_D vs V_D characteristic for $V_D < 5$ V that indicates inferior ohmic contact properties at 25 °C. Comparing the degree of non-linearity seen in Figure 2c to Figure 2d, contacts near the center of Wafer 9.2 appear further from ideal than contacts near the outer edge of this wafer. This contact behavior trend was confirmed by independent 25 °C measurements of n-type SiC linear transmission line method (TLM) resistor devices [18]. Figure 5 shows the positional ***r*** dependence of (a) n-type sheet resistance (R_{SheetN}) and (b) specific n-type contact resistivity ($R_{Spec.N}$) extracted from 25 °C wafer map measurements of n-type SiC TLM resistor devices. Resistances at each TLM contact spacing were calculated from the slope of linear regressions of the measured current vs. voltage (I-V) data from 0 V to 2V applied bias, even for somewhat non-linear I-Vs observed for central regions of Wafer 9.2. Data regression fit equations and lines are also shown in Figure 5.

For both wafers, R_{SheetN} in Figure 5a exhibits miniscule dependence on ***r***. This miniscule change with ***r*** suggests that shallow n-type implant doping (Figure 1, with uniform dose across the wafer) dominates R_{SheetN} over the (non-uniform thickness) as-grown n-type epilayer conductivity.

In contrast to relatively constant R_{SheetN} behavior, there is such a large difference in extracted $R_{Spec.N}$ data that a logarithmic y-axis scale is needed for Figure 5b. Wafer 8.1 $R_{Spec.N}$ (shown in black) is nearly independent of ***r*** and with relatively little scatter from the emperical best fit line. On the other

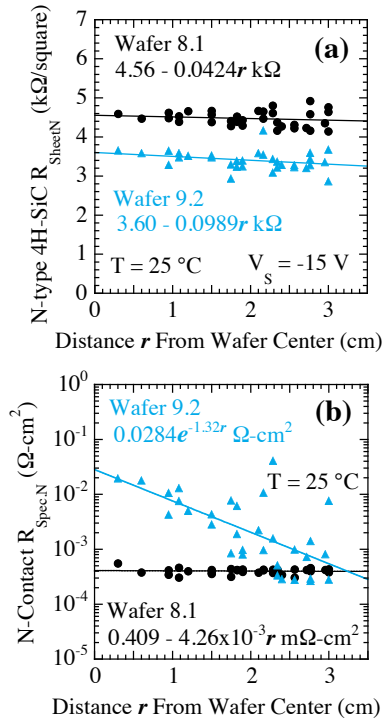

Figure 5. Wafer 8.1 (black) and Wafer 9.2 (blue) (a) n-type sheet resistivity R_{SheetN} and (b) specific n-contact resistivity $R_{Spec.N}$ as a function of radial distance ***r*** from wafer center, extracted from 25 °C wafer map I-V measurements of linear TLM devices.

hand, Wafer 9.2 $R_{Spec.N}$ (shown in blue) exponentially decreases with ***r*** with order of magnitude larger scatter. The larger Wafer 9.2 contact behavior scatter in turn affected many JFET on-state (i.e., higher-current) extractions for Wafer 9.2, such as the larger I_{DSS} scatter seen in Figure 4 for Wafer 9.2 (blue) compared to Wafer 8.1 data (black). The physical process reasons for the anomalous 25 °C Wafer 9.2 Hf contact behavior vs. ***r*** are presently under further investigation, but there is preliminary evidence (including near-wafer-edge electrical data of Figure 2d and Figure 5b) that improved and more uniform Hf contact performance is attainable with process revisions.

In spite of this non-ideal Hf contact behavior at 25 °C, it is imporant to note that Wafer 9.2 ICs nevertheless exhibited excellent 80%-95% integrated circuit 25 °C wafer probe yields [1,6], substantially superior to Wafer 8.1 probe yields [4,5] for corresponding circuits. Almost all SiC integrated circuit resistors were intentionally designed with sufficient length/width ratios (i.e., number of squares) so that SiC conduction properties would dominate total resistance over ohmic contact (end) resistance. As seen in Figure 2c, JFET layouts were more susceptible to contact resistance effects.

B. Electrical Parameters vs. Temperature

As only a few devices have been custom-packaged and oven-tested to date, the measured dataset for verifying T-dependence is limited. Despite the fact that prolonged 500 °C electrical device stability has been a major accomplishment of these ICs, there are nevertheless parameter changes (i.e., "burn-in") related to contacts, interconnect, and dielectrics that occur during the first ~100 hours of 500 °C operation [1,6,19]. However, device characteristics dominated by SiC transport physics, such as V_T and R_{SheetN}, are free of such aging effects due to the inherent physical stability of SiC. Except where otherwise noted, T-dependent properties reported in this section were measured during initial temperature ramps from 25 °C to 500 °C of packaged devices.

Figure 6 summarizes measurement results of n-type SiC (TLM) resistor devices as a function of temperature. Figure 6a plots the n-type sheet resistance (R_{SheetN}) while Figure 6b plots specific n-type contact resistivity ($R_{Spec.N}$). The increase in R_{SheetN} of the shallow nitrogen-implanted 4H-SiC epilayer (Figure 1) of both wafers with T is generally consistent with prior studies of the temperature dependence of 4H-SiC n-channel JFETs and n-layer carrier transport [20,21].

Current conduction through metal-semiconductor contacts is known to be governed by thermally activated transport of majority carriers through the metal-semiconductor junction potential barrier [18]. Therefore, the large observed drop in specific contact resistance $R_{Spec.N}$ shown in Figure 6b with increasing T is (at least qualitatively) somewhat expected. At 500 °C, all contacts (including Wafer 9.2 Hf contacts) exhibited linearly ohmic I-V characteristics. However, the dropoff in $R_{Spec.N}$ with T between the two wafers is different. Wafer 8.1 Ti specific contact resistances dropoff linearly with T until they become unmeasurably small before 300 °C, whereas Wafer 9.2 Hf contacts exhibit a slower yet exponential rate of decline. Given the experimental limitations of this study (e.g., 25 °C wafer position dependence and T-dependent data for only a few packaged devices), the quantitative $R_{Spec.N}$ data extracted in this work should be viewed as preliminary and process-specific.

As decreasing contact resistances exert decreasing parasitic influence on JFET I-V characteristics with increasing T, intrinsic 4H-SiC transistor conduction properties increasingly dominate electrical device peformance by the time T approaches 500 °C. Figure 7 plots measured I_{DSS} from oven-tested JFETs as a function of T. As expected, Figure 7 I_{DSS} drops substantially with T,

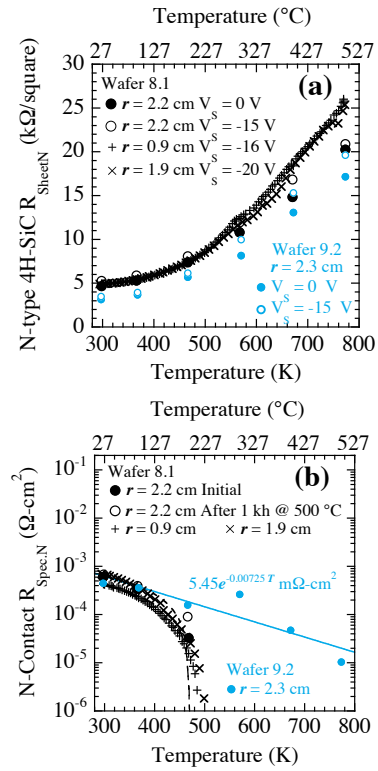

Figure 6. Wafer 8.1 (black) and Wafer 9.2 (blue) (a) n-type sheet resistivity R_{SheetN} and (b) specific n-contact resistivity $R_{Spec.N}$ as a function of temperature, extracted from measurements of linear TLM devices on oven-tested packaged chips. The solid blue line with equation in (b) is the exponential fit to Wafer 9.2 $R_{Spec.N}$ data.

generally consistent with prior physical understanding of 4H-SiC transport physics (wherein increased thermal phonon scattering reduces electron channel mobilities) [20,21]. While not plotted, the channel modulation parameter λ exhibits negligible T-dependence. Therefore, $\lambda = 0.006\ V^{-1}$ independent of T was used for all SPICE modeling. The theoretical and experimental T-dependence of this technology's JFET V_T and body effect parameter γ have been previously reported [9].

V. SPICE Circuit Design & Modeling

From the preceding experimental data, it is clear that device properties not only vary significantly as a function of temperature, but also depend strongly upon position on the wafer. However, since these electrical parameter dependences are systematic, circuits can be designed based on the fact that adjacent devices will exhibit similar temperature and ***r***-position behaviors. In particular, circuits are designed to operate based on

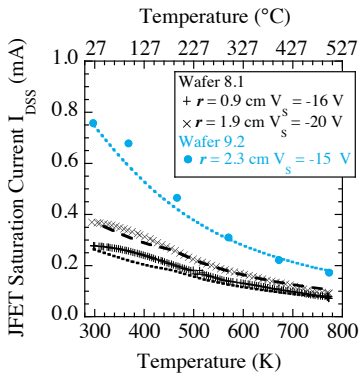

Figure 7. 12µm/6µm JFET I_{DSS} for three oven-tested packaged devices. Symbols are experimentally measured data, dashed lines are software-generated SPICE parameter modeling results.

electrical parameter ratios that can be readily controlled using device layout geometry ratios [7,8,10]. Experimental demonstrations of the ability of this approach to provide desired circuit functionality over unprecedented temperature ranges (from -124 °C to +727 °C) are described in References [7,8]. In these and other prior work [20], both 6H-SiC and 4H-SiC JFET and resistor bias currents peak within 50 °C of room temperature, and then systematically decline with either increasing or decreasing T away from room temperature.

It should be noted that power supply voltages $+V_{DD}$ and $-V_{SS}$ are usually adjusted somewhat as a function of ***r*** to compensate for V_T ***r***-dependence (Figure 3). For most Wafer 9.2 circuit mapping at 25 °C, power supply magnitudes were changed from ~ 25 V near the wafer center to ~ 30 V closer to the wafer edge. Circuits with reasonable ohmic contacts typically maintained desired functionality at supply voltages within ± 2 V of "nominal" values and adjusment of V_{SS} and V_{DD} as a function of temperature is typically *not* required.

A. JFET SPICE Models

The depencence of 4H-SiC JFET electrical properties on wafer position and temperatue dictates that SPICE models also depend on wafer position and temperature. Towards this end, we have implemented LabVIEW-based software tools to expediently generate first-order accuracy SPICE models for given wafer position and temperature (as well as bias and process information) as inputs. While details of the specific model calculations will be presented in a future publication, the software employs a combination of 1-dimensional 4H-SiC JFET device physics equations and fitting of experimentally measured data.

For devices with linearly ohmic source/drain contacts, the software-generated SPICE models have yielded reasonable approximations to experimentally measured data. Examples of SPICE simulations conducted with software-generated SPICE JFET (NMOS Level 1) parameters are plotted as dashed lines against corresponding experimentally measured data in Figure 4 and Figure 7. Figure 8 compares SPICE-modeled (circles) with measured (lines) drain I-V characteristics of the oven-tested Wafer 9.2 12µm/6µm packaged JFET at (a) 25 °C and (b) 500 °C. The NMOS Level 1 SPICE model text and device instance text used for the two simulation examples are also shown.

For design and simulation of ratio-based circuit designs, a "boundaries + middle value" design methodology has been adopted. Device models near the extremes and middle of temperature and wafer position limits are simulated as test cases for providing insight/verfication into circuit operation across the range of expected electrical parameters. Combining minimum (***r*** = 0 cm), mid-range (***r*** = 1.5 cm), and near-outer (***r*** = 3.0 cm) radial position cases with analagous 25 °C, 300 °C, 500 °C temperature cases result in the nine specific simulation model cases shown in Table I. The SPICE syntax model text in this table can be selected and copied from this PDF manuscript and pasted into plain text SPICE files.

Table I. 4H-SiC JFET SPICE Models

T (°C)	***r*** (cm)	JFET SPICE Model Text
25	0	.MODEL sicnjfet NMOS LEVEL=1 VTO=-8.85 KP=1.08E-5 GAMMA=0.897 LAMBDA=0.006 CJ=6.86E-5 PB=2.87 PHI=1.435 RD=3175 RS=3175
25	1.5	.MODEL sicnjfet NMOS LEVEL=1 VTO=-10.27 KP=1.03E-5 GAMMA=0.953 LAMBDA=0.006 CJ=6.86E-5 PB=2.87 PHI=1.435 RD=3175 RS=3175
25	3	.MODEL sicnjfet NMOS LEVEL=1 VTO=-15.03 KP=9.34E-6 GAMMA=1.12 LAMBDA=0.006 CJ=6.86E-5 PB=2.87 PHI=1.435 RD=3175 RS=3175
300	0	.MODEL sicnjfet NMOS LEVEL=1 VTO=-9.23 KP=3.62E-6 GAMMA=0.897 LAMBDA=0.006 CJ=7.53E-5 PB=2.378 PHI=1.189 RD=4291 RS=4291
300	1.5	.MODEL sicnjfet NMOS LEVEL=1 VTO=-10.67 KP=3.49E-6 GAMMA=0.953 LAMBDA=0.006 CJ=7.53E-5 PB=2.378 PHI=1.189 RD=4291 RS=4291
300	3	.MODEL sicnjfet NMOS LEVEL=1 VTO=-15.45 KP=3.14E-6 GAMMA=1.12 LAMBDA=0.006 CJ=7.53E-5 PB=2.378 PHI=1.189 RD=4291 RS=4291
500	0	.MODEL sicnjfet NMOS LEVEL=1 VTO=-9.55 KP=2.00E-6 GAMMA=0.897 LAMBDA=0.006 CJ=8.22E-5 PB=1.997 PHI=0.998 RD=6203 RS=6203
500	1.5	.MODEL sicnjfet NMOS LEVEL=1 VTO=-11.00 KP=1.92E-6 GAMMA=0.953 LAMBDA=0.006 CJ=8.22E-5 PB=1.997 PHI=0.998 RD=6203 RS=6203
500	3	.MODEL sicnjfet NMOS LEVEL=1 VTO=-15.80 KP=1.73E-6 GAMMA=1.12 LAMBDA=0.006 CJ=8.22E-5 PB=1.997 PHI=0.998 RD=6203 RS=6203

As first mentioned in Section III, the SiC JFETs are simulated using baseline SPICE NMOS LEVEL 1 model and device instances [11,12,13]. These models are based on Wafer 9.2 threshold voltage fit equation of Figure 3, which is considered more representative of presently available 4H-SiC JFET epi-wafers than Wafer 8.1. These models also presume that ***r***-independent ohmic contact behavior will be obtained in future process runs with T-dependent $R_{Spec.N}$ shown in Figure 5b for Wafer 9.2. For SPICE NMOS parameters not listed in Table I, SPICE default parameters can be assumed.

The models shown in Table I are based on the W_G = 12µm/L_G = 6µm "unit cell" JFET layout, which is the smallest possible JFET in the present 500 °C durable IC process. *To realize larger JFETs with larger gate widths (and correspondingly larger on-state current and transconductance) the SPICE device instance M parameter should be increased, wherein M is the number of 12µm/6µm unit cells to be paralleled in the larger JFET.* Changing SPICE device instance L and W parameters instead of M will result in inaccurate SPICE simulation of parasitic resistances and capacitances.

A suggestion to facilitate rapid swapping of the above models into SPICE is to have SiC JFET device cells load the .MODEL from a common .INCLUDE file location. A simple program (such as we implemented in LabVIEW) can provide the user with a simple point and click model selection interface that places the desired T and ***r*** .MODEL case into the .INCLUDE file to be read by SPICE as the schematics or netlists are loaded and simulated.

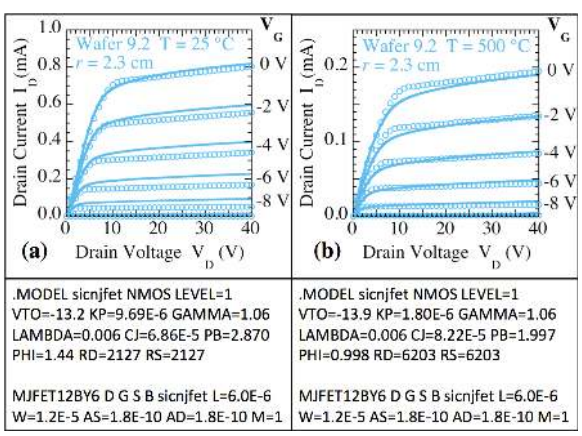

Figure 8. Measured (lines) vs. SPICE (circles) JFET I-V characteristics at (a) 25 °C and (b) 500 °C for oven-tested 12µm/6µm packaged JFET. The software-generated NMOS parameters used for the SPICE I-V simulations are below each plot, along with the SPICE device instance lines.

B. Resistor SPICE Models

The most straightforward way to simulate 4H-SiC n-type resistors is using the baseline SPICE semiconductor resistor model. This model relies on RSH parameter directly corresponding to data plotted in Figures 5a and 6a. By neglecting the minimal dependence of R_{SheetN} on position ***r*** (Figure 5a), contact resistance, and the substrate body bias effect, the semiconductor resistor simulation model cases can be simplifed down to the three temperature models shown in Table II.

Table II. 4H-SiC IC Resistor Models

T (°C)	Resistor SPICE Model Text
25	.MODEL sicnres R RSH=4000
300	.MODEL sicnres R RSH=10000
500	.MODEL sicnres R RSH=20000

Figure 9 compares resistor I-Vs simulated in SPICE using these models (dashed lines) with I-Vs measured (solid lines) on a 480 µm long by 6 µm wide resistor from an oven-tested packaged Wafer 9.2 chip. The SPICE I-Vs sufficiently approximate the measured I-Vs for first-order accuracy circuit modeling that was employed to design the Wafer 8.1 and 9.2 integrated circuits.

However, some trends in Figure 9 are worth noting towards realizing even more accurate SPICE resistor modeling. The slightly non-linear I-V near the origin of the 25 °C measurement is attributed to the non-ideal Hf ohmic contact properties at 25 °C. As contact conduction improves with increasing T (e.g., Figure 6b), excellent modeled vs. measured agreement is obtained for low voltages. At increasingly higher voltages, the measured I-Vs deviate further from the linear models due to the

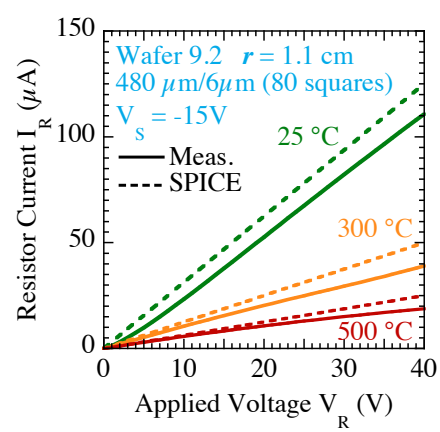

Figure 9. Measured (solid) vs. SPICE (dashed) resistor I-V characteristics.

substrate body bias effect not being accounted for in baseline-version SPICE resistor models. The resistor body effect is the manifestation of the fact that increasing positive applied bias increasingly depletes the n-channel side of the substrate-channel pn junction (i.e., lower pn junction of Figure 1) near the positive end of the resistor. As was the case for JFETs in Reference [9], improved circuit simulation accuracy is expected upon future inclusion of the body bias effect into SPICE resistor modeling.

VI. Conclusion

Using the information presented in the preceding sections and references therein, *integrated circuits implemented using the NASA Glenn 500 °C durable JFET IC process can be designed and modeled in SPICE.* Application-specific analog and digital circuits comprised of interconnected combinations of up to 200 JFETs, 400 resistors, with 32 or less input/output/power pins can presently be fabricated on a single 3 mm x 3 mm SiC chip. NASA Glenn is open to prototype fabrication of compatible third-party custom IC designs during future 500 °C durable IC developmental wafer fabrication runs [22]. The primary aim of these future wafer fabrication runs is to further improve IC capability in terms of electrical functionality, performance and high temperature durability, and also simplify the fabrication process needed to realize this unique capability.

Future reports will detail the physics and software-generation of SPICE parameters, the addition of body bias effect to the IC resistor modeling, and SPICE modeling results of circuits compared to measured circuit performance. Logical next steps in the further maturation of this uniquely enabling IC technology include implementation of a complete process development kit (PDK) and shrinkage of the minimum feature size to facilitate 500 °C durable ICs of 1000+ transistors on a single chip.

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