Hindawi Publishing Corporation
VLSI Design
Volume 2007, Article ID 45269, 13 pages
doi:10.1155/2007/45269

Research Article

Flexible Architecture of Ultra-Low-Power Current-Mode Interleaved Successive Approximation Analog-to-Digital Converter for Wireless Sensor Networks

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Received 31 October 2006; Accepted 21 April 2007

Recommended by Wieslaw Kuzmicz

A novel 8-bit current mode interleaved successive approximation (SAR) analog-digital converter (ADC) has been proposed. The proposed converter architecture is very flexible. Using two control DC voltages and one reference current, the converter can be tuned to work with different sampling rates, number of bits of resolution, and power consumption levels. Due to its very low-power consumption and flexibility, the converter is particularly suitable for application in wireless sensor networks. Compared to other solutions presented in the literature, the proposed converter achieves very high figure of merit (FOM) value due to numerous low-power circuit innovations utilized in its design. The circuit has been implemented in CMOS 0.18 μm technology. Minimum energy consumption has been found to be in a 25–250 kS/s range (for clock sampling frequency in a 200 kHz–2 MHz range) for a single SAR section with the corresponding power dissipation varying from 220 nW to 560 nW for 0.55 V power supply.

1. INTRODUCTION

Advantages of wireless sensor networks (WSNs) lie in the development of a low-cost, scalable, and flexible network architectures. WSNs create invisible interconnections with the physical world for the measurement, monitoring, and management of data from multiple sensors and probes with little constraint on their location. These networks provide distributed processing, data storage, wireless communication, and dedicated application software with high reliability, inherent redundancy, failure-tolerant security, and possibly encrypted privacy. The effectiveness of WSNs requires sensor information to be conveyed to the user at low-data rates with very low-power consumption. In a typical wireless sensor network, application sensors can communicate with a base station or directly between themselves in a peer-to-peer fashion. A typical wireless sensor node consists of a RF front end (for wireless communication), an analog to digital converter (ADC), an optional microprocessor to process the collected data, and a power supply block [1].

The ultimate focus of the WSN development is to be able to integrate ultra-low-power nodes that require only a one-time battery charge or have an ability to scavenge energy from the external environment. In terms of hardware characterization, different components that make up the wireless sensor node dissipate different levels of power depending upon their mode of operation (sleep, wake-up, data acquisition). It has been observed that one of the largest sources of power dissipation in most cases is RF front end and analog to digital conversion (ADC).

The goal of this paper is to propose a novel ADC architecture that is suitable for WSN applications. The paper is organized as follows. First, various ADCs are compared in Section 2 in terms of their power and input data conversion rate. One of the important conclusions from that comparison is that successive approximation (SAR) converters are the most suitable candidates for ultra-low-power operation. Consequently, reported SAR implementations are discussed in Section 3. Circuit solutions that can be used to obtain a very low-power ADC operation are discussed in Section 4 for a single block SAR operation and extended to an interleaved solution in Section 5. CMOS implementation of the proposed circuitry is shown in Section 6 [2]. Finally, conclusions are given in Section 7.

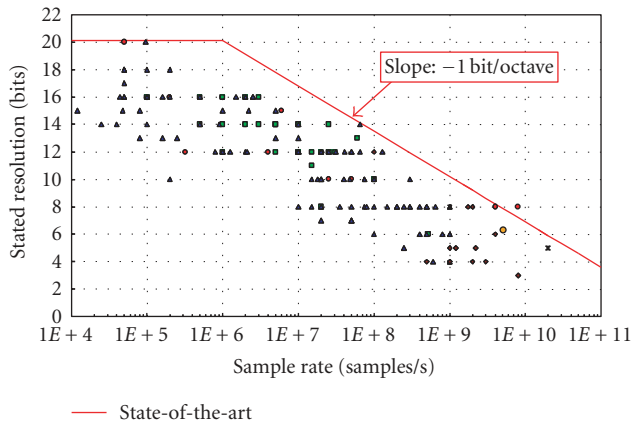


FIGURE 1: Performance characteristics of published ADC converters in the last 10 years.

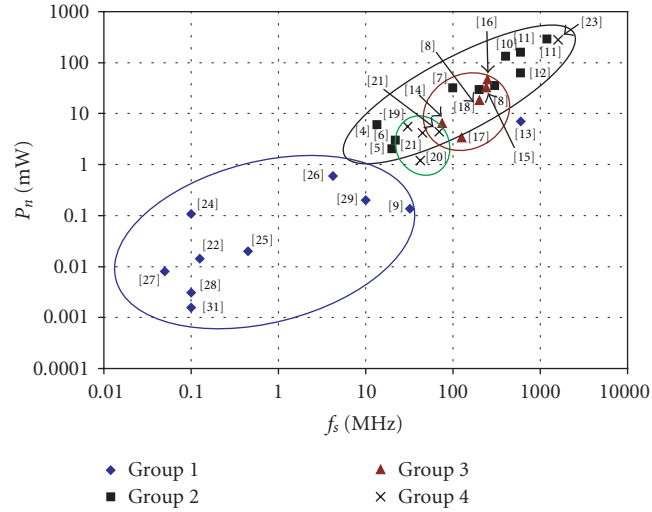


FIGURE 2: Performance (power normalized and 8 bits of resolution versus sampling frequency) comparison between four groups of ADCs: group 1: algorithmic and SAR, group 2: flash, group 3: pipelined, group 4: folding and interpolating. Normalized power with respect to $V_{DD} = 1$ V.

2. ANALOG TO DIGITAL CONVERTERS (ADCs) FOR WIRELESS SENSOR NETWORKS

In order to select the right type of the desired converter, a careful analysis of various classes of converters has been conducted. In practical terms, ADCs can be divided into nyquist-rate and sigma-delta converters. Sigma-delta ADCs are preferred for the highest levels of bit resolution and demand very fast over-sampling clocks making them inherently low-speed converters. Their clock generator has to be very clean as the clock jitter has direct influence on the obtained signal-to-noise ratio (SNR). This demanding clock requirement makes sigma-delta ADCs not suitable for WSN applications as WSN should have simple structure and operate at very low-power levels. For these reasons, we have eliminated sigma-delta from the presented comparison.

Broadly speaking, nyquist-rate ADC converters can be classified into the following four groups [3]:

(i) flash,
(ii) pipeline,
(iii) folding-interpolating,
(iv) algorithmic-SAR.

Flash ADCs, where signal conversion is performed in one sampling stage, are used for high-frequency applications where dissipated power is of secondary importance. Pipeline, folding, and interpolating ADCs are used when higher resolution, than that of flash, is required at the cost of lower speed. Finally, successive approximation (SAR) and algorithmic converters are expected to exhibit the lowest dissipated power levels at the cost of the slowest sampling rate available.

To gain some insights into power dissipation versus sampling frequency tradeoffs, various Nyquist-rate ADC converters that present a wide spectrum of available resolution bits and speed/sampling rates were collected and shown in Figure 1. There have been more than 500 converters that have been published over the last 10 years, however, only selected 100 points are presented in Figure 1 for clarity. As expected, the larger the sampling frequency the smaller the maximum resolution. The state-of-the-art devices can achieve 14-bit resolution at 10 MHz and 6-bit resolution at 10 GHz sampling rate.

While interesting on its own, the performance characteristics shown in Figure 1 do not take power dissipation levels into account. Clearly, taking power dissipation into consideration is of paramount importance for WSN applications. In order to make the power analysis manageable, only converters with resolution of 6 to 8 bits, as typically required by WSN applications, have been selected for further analysis [4–29] and shown in Figure 2. For meaningful comparison, the reported power numbers have been normalised with respect to V_{DD}^2, where V_{DD} is the power supply level. As can be observed, the dissipated power correlates well with the sampling frequency as expected. Each group of converters is clustered in one area of the plot. Clearly, for WSN application, the first group of converters, that encompasses algorithmic and successive approximation (SAR) is the best candidate for CMOS implementation.

3. SUCCESSIVE APPROXIMATION (SAR) AND ALGORITHMIC ADCs: A REVIEW

In our analysis of the existing ADCs, we have focused on five examples of algorithmic ADCs that consume the least amount of power due to requirements of the intended application in WSNs. In general converter space voltage mode, ADCs are used more commonly, most of the converters selected in the comparison shown in Section 2 belong to that class [4–29]. However, in the case of low-power and low-frequency circuits, current mode circuits are gaining popularity as indicated by 3 out 5 examples of converters analyzed in this section [22, 25, 29].

Converter no.1 [22]: 6-bit algorithmic ADC

In [22], the current mode 6-bit algorithmic ADC implemented in 0.18 μm is presented. The particular ADC stages consist of current-mode sample and hold (S&H) elements and integrating current-mode comparators. Each stage in this ADC produces residue current for the subsequent stage. This residue current is then multiplied by two and compared to the current, which is a sum of the reference current and bias current. The biasing circuit needs additional bias voltages. The authors indicate a necessity for good matching between transistors in current mirrors in order to preserve linearity. They use the same reference current copied via different current mirrors to all stages. If there is a mismatch between the transistors in the current mirrors (in different stages), the residue currents produced will be compared to different reference currents in the following stages. This limits the linearity of the circuit. However, this structure has important advantages such as Nyquist rate A/D conversion, which results from the use of pipeline structure. Very low-power consumption of 6 μW is also valuable.

Converter no.2 [25]: 8-bit current mode cyclic ADC

A low-power (450 μW at a supply voltage of 5 V) current-mode cyclic ADC is presented in [25]. This ADC was designed in CMOS 3 μm technology more than 10 years ago. Nevertheless, it still compares well with the state-of-the-art recent converters, like the one presented in [24] exhibiting good performance parameters. This converter needs only $N/2$ clock cycles for N bit conversion. The speed is higher than in typical SAR ADC, but number of analog components is doubled. The essential crux behind this ADC is similar to the ADC reported in [22]. The input voltage signal is stored in one of the voltage-mode S&H elements and is converted to a current. This current is then compared with a reference current that results from the conversion of a reference voltage. As a result of this comparison, the reference current is subtracted from the input current, producing a residue current for the second stage. After the second stage, the residue current is converted to a voltage and stored in the second voltage-mode S&H element. This voltage is then copied to the first S&H element. In one clock cycle, two bits are obtained in two pipelined stages. Thus, four clock cycles are required for an 8-bit conversion. The advantage of this solution is in that no S&H elements are used between two pipeline stages. However, the solution requires many V-I and I-V conversion operations, which introduces additional errors. The ADC also suffers from a similar problem of transistor matching, as was observed in the current mirrors in [22]. Another disadvantage of this ADC is the necessity of using active elements in voltage-mode S&H components and in voltage-to-current converters. This requirement causes an increase in the required power consumption.

Converter no.3 [24]: 8-bit cyclic voltage-mode ADC

Unlike the two current mode converters described above, this voltage mode ADCs need active elements at every stage of conversion. This causes their power consumption to be potentially higher as compared to the current mode circuits. This disadvantage is visible in [24], where simple 8-bit (designed in CMOS 0.6 μm technology) cyclic ADCs consume about 1 mW of power, as compared to the 450 μW consumption reported in [25] for a similar current mode converter. Using voltage-mode S&H elements creates a possibility of higher precision data acquisition. This is important when higher accuracy is required. One of the drawbacks of this ADC is a low-voltage swing (0.5 V for $V_{DD} = 3$ V) and a slightly more complicated architecture of the clock generator that controls the S&H elements.

Converter no.4 [27]: 8-bit voltage-mode ADC

Another voltage-mode ADC is presented in [27] implemented in CMOS 2 μm technology and consumes 200 μW from a 5 V voltage supply, enabling a sampling frequency of 50 kHz. The circuit operates with three reference voltages in each conversion stage. Two of them define the conversion range for input data and correspond to the minimum and maximum values of the analog input signal. The third voltage is calculated to be the median of this range. The input signal is compared with this median. If the input signal is higher than the median reference voltage, the minimum voltage will be set to the previous median voltage and a new median is calculated. Theoretically, the new value should be equal to 3/4th of the previous maximum range voltage. If the input signal is lower than the median reference voltage, the maximum range voltage will be set to the previous median voltage and a new median is calculated. Theoretically, this new value should be equal to 1/4th of the previous maximum reference voltage. This algorithm is repeated for all bits between (and inclusive of) MSB and LSB, defining in each step new values for these three references voltages. This ADC has a very simple structure in general, but suffers from some disadvantages. The first disadvantage is that in each stage it is necessary to calculate new reference voltages, which requires two additional clock phases. Reference voltages are stored in capacitors. Calculation of their new values requires charging or discharging of these capacitors: a time consuming process leading to unnecessary power dissipation loss. The timing of this process limits the maximum sampling frequency. Another disadvantage lies in the calculation of new reference voltages on the basis of previous values. Each step introduces an error due to the finite operational amplifier gain and charge injection. This causes an increase in the cumulative error in each step that can be especially visible for LSBs.

Converter no.5 [28]: 7-bit voltage-mode SAR converter

An ultra-low-power voltage-mode SAR ADC is presented in [28]. This circuit was designed in CMOS 0.25 μm technology and operates with a sampling frequency of 100 kS/s, dissipating only 3.1 μW from 1 V voltage supply. In principle, this is a typical SAR ADC, where the reference voltage converges to the input data as a result of the digital circuitry operation. The disadvantage of this circuit is somewhat similar

Table 1: Comparison of low-power SAR and algorithmic ADCs.

Ref.	Process	Res.	f_s [kHz]	Power dissip.	Power norm.	Area [mm^2]	Mode	V_{DD} [V]	FOM$_P$ [MHz/μW]	FOM$_A$ [mm^2/NOB]
[31]	CMOS 0.18 μm	8, 12	200, 100	25 μW	1.56 μW	0.63	V-mode	1	32.82	1.62
[24]	CMOS 0.6 μm	8	100	980 μW	110 μW	0.6	V-mode	3	0.23	0.21
[27]	CMOS 2 μm	8	50	200 μW	10 μW	0.068	V-mode	5	1.28	0.002
[28]	CMOS 0.25 μm	8	100	3.1 μW	3.1 μW	0.053	V-mode	1	8.26	0.06
[25]	CMOS 3 μm	8	450	500 μW	20 μW	NA	I-mode	5	5.76	NA
[22]	CMOS 0.18 μm	6	125	6 μW	10 μW	0.0475	I-mode	0.65	0.8	0.24
[32]	CMOS 0.18 μm	10	1	15 μW	3.75 μW	1.2	U-mode	1	0.27	3.7
This work SAR	CMOS 0.18 μm	1–8	2000	560 nW	1.85 μW	0.0092	I-mode	0.55	276.76	0.035
This work interleaved	CMOS 0.18 μm	1–8	2000	3.5 μW	11.6 μW	0.1	I-mode	0.55	353.10	0.048

to the ADC described in [27], wherein the settling time of the voltage in the capacitors limits the maximum conversion speed. Charging and discharging of the capacitors via nonideal switches introduces errors that limit the accuracy [3]. Another source of speed limitation is the comparator, in which the voltage-mode circuits are realized as active elements. This causes a trade-off between speed and power consumption. The advantage of this ADC is rail-to-rail input voltage swing.

The basic parameters of the compared ADCs are listed in Table 1. For a given sampling frequency power dissipation is the most important parameter for application in WSNs. However, it is difficult to make a direct comparison of power consumption values in these ADCs, due to the different technologies and different supply voltages used. To facilitate comparison, besides comparison of absolute power also consumption of power normalized to $V_{DD} = 1$ V is presented. In case, when resolution of ADCs collected in Table 1 was higher than 8, the power was normalized to 8 bits. A figure of merit (FOM$_P$) for normalized power versus frequency comparison of ADCs has been defined as a ratio of sampling frequency f_s to dissipated power and normalized by converter resolution, where NOB is number of resolution bits [30]:

$$\text{FOM}_P = f_s \cdot 2^{\text{NOB}}/\text{Power\_normalized}. \quad (1)$$

A proposed new SAR ADCs, described later in Sections 4 and 5, are also presented in Table 1 for completeness. figure of merit (FOM$_A$) for chip area has been defined as a ratio of a converter A normalized to 1 μm and number of bits (NOB) in the converter and L_X is the minimal transistor length in a given CMOS technology. In case of the interleaved ADC, the chip area is additionally divided by 8 (parameter $d = 8$) due to the parallel connection of 8 the same SAR sections, each of them having NOB equal to 8. In case of other ADCs parameter d is equal to one,

$$\text{FOM}_A = \frac{A}{L_X^2 \cdot \text{NOB} \cdot d}. \quad (2)$$

In summary, it can be stated that current mode circuits are good solutions for low-power and low-speed ADCs. Based on the analysis of the above chosen ADCs, it was observed that voltage-mode ADCs already operate at maximum potential and further improvements are difficult due to the limitations of the active elements. In case of current-mode ADCs a potential possibility to improve the parameters by introducing new circuit solutions seems to exist. Thus, a current-mode ADC was chosen as the selected architecture for meeting the low-power requirement.

In Section 4, we are presenting a uniquely flexible architecture for the current mode SAR of 8-bit current-mode algorithmic ADC. The presented circuitry is very flexible by enabling operating in a wide range of input frequencies and required output resolution (from 1 to 8 bits).

The interleaved SAR converter described in Section 5 consists of eight single SAR blocks, where each of them is sampled with 2 MHz clock to obtain 8-bit output resolution at 250 kS/s of output data, dissipating power equal to about 560 nW. Parallel operation of eight blocks in the interleaved mode enables 8x increase of the data conversion rate while maintaining 2 MHz sampling frequency.

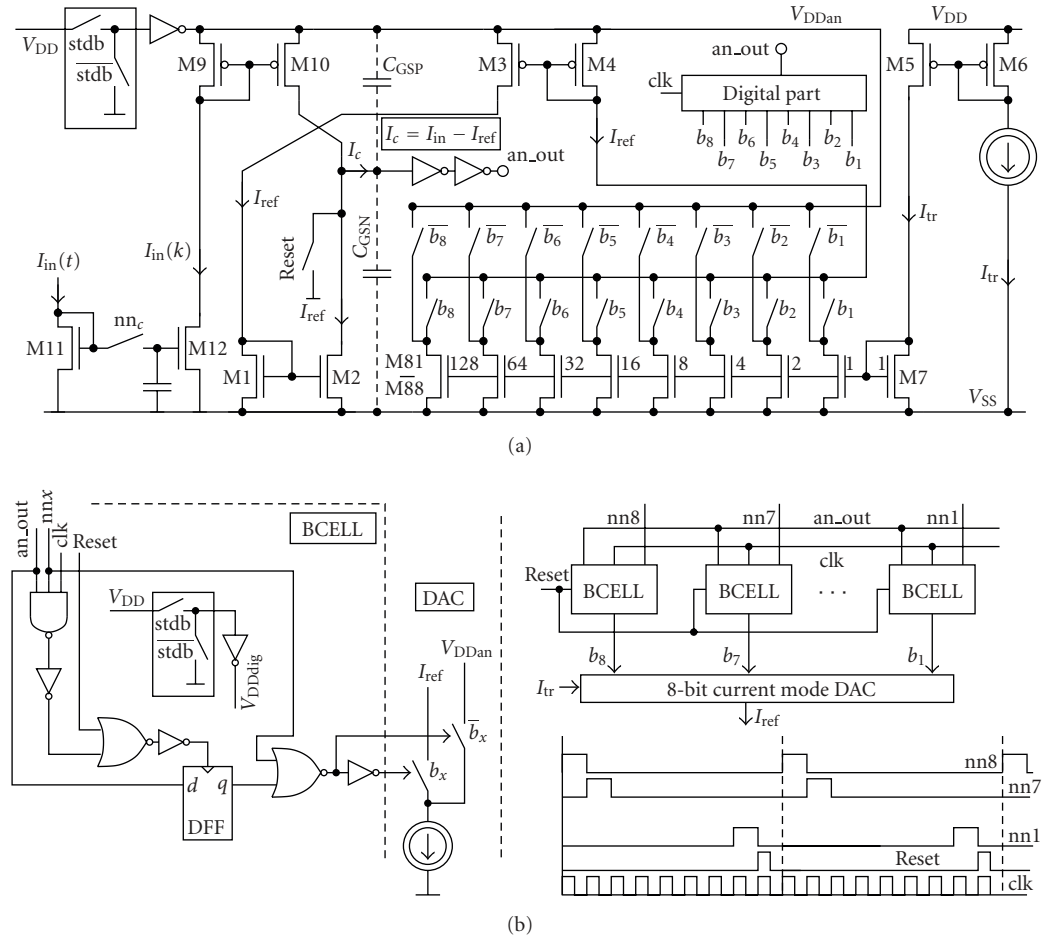


Figure 3: Block diagram of the proposed current mode algorithmic ADC with implemented standby mode: (a) analog part and (b) digital part.

The operational flexibility in both cases is accomplished by turning off unused portions of the circuitry when required, resulting in good matching of dissipated power to realized tasks. Such a performance is obtained by use of only two DC control voltages. One voltage controls the number of used sections (from 0 to 8) while the second one controls the number of resolution bits (from 1 to 8). When all eight sections are nonactive (standby mode), which is a desired functionality when the WSN node is in a sleep mode, the entire ADC consumes 130 nW.

4. SAR ADC ARCHITECTURE

A single conversion block used in the proposed interleaved ADC is shown in Figure 3. It consists of the analog circuitry responsible for signal conversion and the digital control circuitry. Both analog and digital parts are powered from separate power supplies to enable various power-down modes and to decrease influence of digital noise on the analog part.

The proposed SAR converter is based on a current mode principle. It derives its essence from the integrating current comparator reported in [33, 34]. This circuit converts an input current I_{in}, which is obtained by using a current-mode sample and hold (S&H) element [22]. The input current is compared in each SAR stage with a reference current I_{ref}, which is obtained as an output of the current mode DAC and can be expressed as

$$I_{ref} = (b_8 \cdot 2^7 + b_7 \cdot 2^6 + \cdots + b_2 \cdot 2 + b_1) \cdot I_{tr}. \quad (3)$$

Taking the difference current between I_{in} and I_{ref} establishes a differential current I_c ($I_c = I_{in} - I_{ref}$) that charges the input gate-to-source capacitances of the first inverter (integrating comparator). The digital output signal (V_{an_out}) and clock (clk) control the digital circuitry that sets bits $b_1 - b_8$, using successive approximation algorithm.

SAR ADC functionality is illustrated in Figure 4 for operation at 1 MHz sampling frequency. The waveform at the top depicts V_c voltage at the input of the first NOT gate of the comparator during SAR operation. Waveforms at the bottom depict the output signals corresponding to calculated bits $b_1 - b_8$. Transistor's dimensions of the first NOT gate (comparator) were chosen as minimal as possible to minimize gate-to-source capacitance (C_{GS}) in order to obtain the highest possible speed of this circuit. Speed of this element

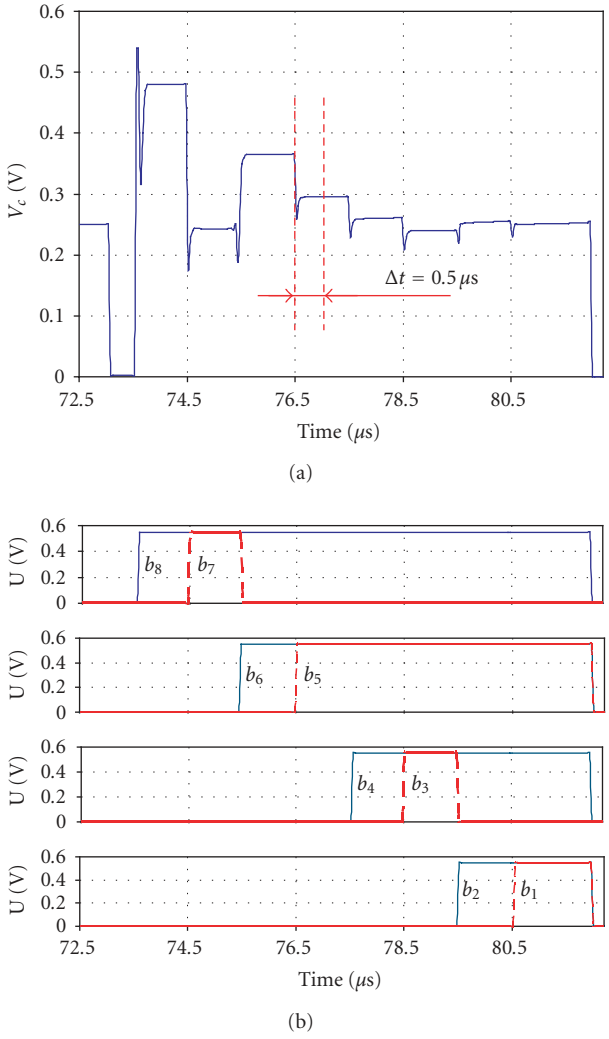


FIGURE 4: Successive calculation of the output bits for input current $I_{in} = 211$ nA sampled with $f_s = 1$ MHz, and for $I_{tr} = 1$ nA: voltage of the current comparator (top) and calculated bits (bottom). For each step of the algorithm signal becomes stable in period shorter than 0.5 μs, showing that operation at 2 MHz is possible.

is critical and determines the speed of the entire ADC. In CMOS 0.18 μm technology, operation with clock frequency about 2 MHz is possible, because the settling time at each algorithmic stage is below 0.5 μs, as visible in Figure 4. Simulations illustrated in Figure 4 were performed for I_{tr} current equal to 1 nA.

The difference current I_c is a difference between the input current that can vary in a wide range and the reference current I_{ref} for which values are quantized. As a result, the difference current I_c can vary in a wide range as well. If I_c is below 1 nA, the settling time will be longer 0.5 μs, meaning that in these cases, one clock cycle might not be sufficient to resolve the given bit. However, this characteristic is not a problem as the resulting error is smaller than 1 bit.

One of the advantages of the proposed ADC is that good matching between transistors in pairs M1-M2, M3-M4, M5-M6, M7 and M81-M88, M9-M10, M11-M12 is not critical because any mismatch in these pairs can be easily compensated by adjusting I_{tr} current during device calibration. However, a sufficiently good matching between transistors M81-M88 is important, as it can substantially affect the linearity of the ADC. Residual mismatch, encountered in pipelined ADCs for example, is not a serious problem here, as widths of the channels of transistors M81-M88 increase when traversed from the LSB to MSB. Matching in the MSB's transistors is better as compared to the LSB's transistors resulting in the better linearity than in ADC reported in [22], where matching between transistors affects all bits to the same degree. In [22], this property is due to the fact that residue currents—after subtraction of the reference current—are copied (with a factor of two) many times in the subsequent stages.

Another advantage of proposed current-mode ADC it that it is not necessary to use many samples and hold (S&H) elements between ADC stages as in [22]. These S&H elements introduce additional error to each stage's residue current. In the presented solution, the same input current is compared with a reference current I_{ref} in all algorithm stages, and reference current depends only on the value of bits $b_1 - b_8$, and the initial matching of transistors M81-M88.

We have implemented two sets of switches in DAC subcircuit (transistors M7 and M81-M88). Switches controlled by bits $b_1 - b_8$ connect current sources to gates of the M3-M4 transistors and switches driven by $b_1 - b_8$ signal of the opposite polarity connect unused current sources to V_{DD}. Tying unused currents to V_{DD} is necessary; otherwise gate potentials at M3-M4 would be affected by unused current sources due to transistor leakage.

Simulated input-output characteristics are shown in Figure 5. As shown, the slope changes by 16% in a -40°C to $+100^\circ$C temperature range, but the characteristics remain linear, which is an important feature. The corresponding slope can be easily calibrated by adjusting I_{tr}.

The converter has been implemented in an 8-bit resolution configuration. However, preliminary data indicate that the resolution can be extended to 10–12 bits if required. This SAR ADC implementation currently operates at a reference level I_{tr} of 1 nA. However, lowering I_{tr} down to 0.1 nA is also possible as indicated by simulation results.

The proposed SAR ADC has a very interesting advantage in that a simple adjustment of the I_{tr} current can effect the power consumption as well as the speed of the ADC. Figure 6 illustrates power consumption values for analog and digital portions of the ADC versus input sampling frequency (for 8-bit resolution). The digital part consumes only small fraction of the total dissipation power.

Figure 7 displays energy per 8-bit output data sample versus input sampling frequency. As can be observed, the optimal region of operation is in the low data range of 100 to 250 kS/s. The results presented in Figures 6 and 7 depict the worst-case scenarios for calculating the MSB. Here, the input current is slightly below the threshold value of the first bit, and reference current I_{ref} from DAC changes from zero to the threshold value of the first bit causing switching over the inverter. This threshold is equal to the median between

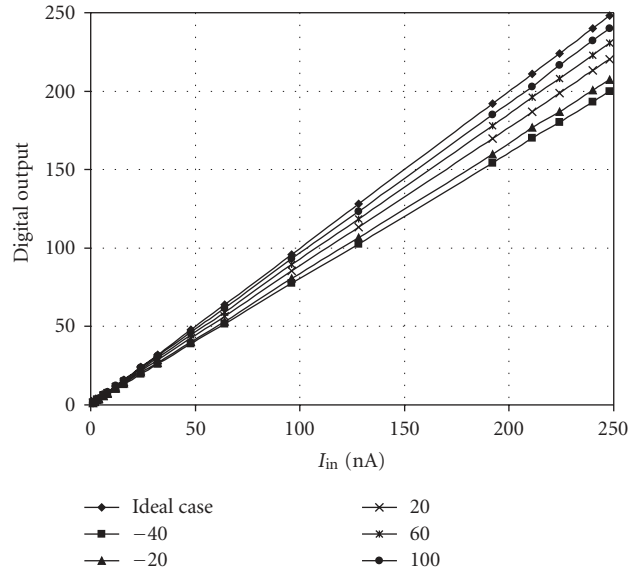


Figure 5: Input/output characteristics for the proposed 8-bit current mode SAR ADC for $I_{tr} = 1$ nA in a temperature range from −40°C to +100°C.

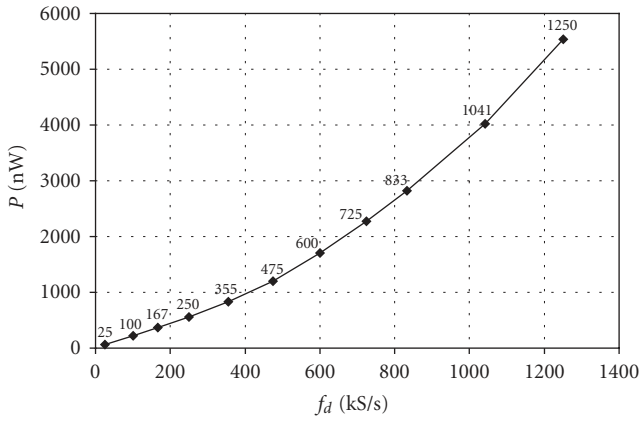


Figure 6: Power consumption versus 8-bit output data rate in the proposed single section current-mode SAR ADC.

the maximum and minimum values of the input current. In this case, the difference current I_c is very low (equal to I_{tr}), causing the longest possible charging period of the gate-to-source capacitances (C_{GS}) in transistors of the first inverter. For transistor dimensions $W = 0.6\,\mu$m and $L = 0.18\,\mu$m value of C_{GS} is equal to about 1 fF. For maximum value of the difference voltage at the inverter's input $\Delta V = 0.25$ V, and $I_c = 1$ nA, the time required to charge this capacitance is about 0.5 μs, which means that the maximum sampling frequency is equal to about 2 MHz, a value confirmed in the postlayout SPICE simulations.

The standby mode is realized by use of the NOT gate and switches controlled by stdb signal (see Figure 3). Transistor widths in this inverter are large, resulting that when ADC is working, the resistance between V_{DD} and $V_{DD\,an}$ (or $V_{DD\,dig}$ for digital part) is about 100 Ω. The maximum current (for maximum input current) that flows through this resistance is about 1 μA for $I_{tr} = 1$ nA. In result, the difference between V_{DD} and $V_{DD\,an}$ is about 100 μV, that is, less than 0.02% of V_{DD}. Influence of this error on ADC's performance can be neglected. In case of digital part, this error is much smaller and is of no importance.

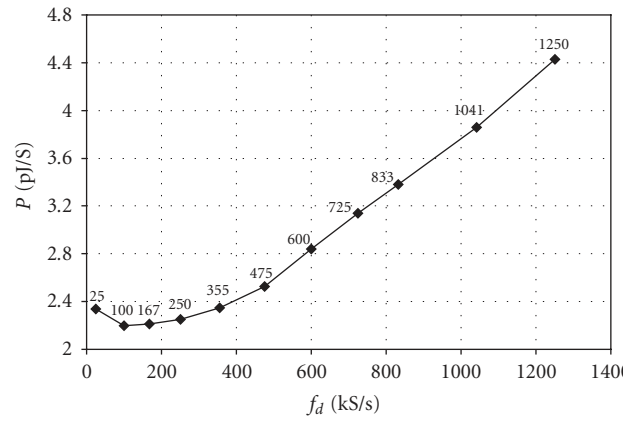


Figure 7: Energy per sample (8 bits) versus output 8-bit data rate.

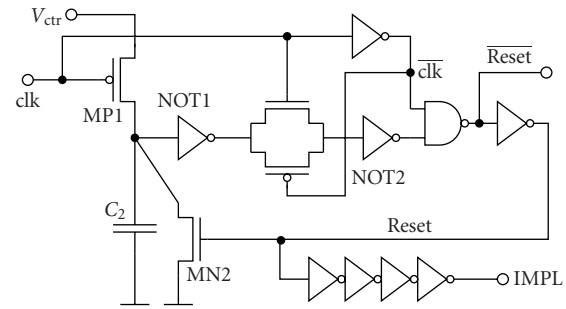


Figure 8: Voltage controlled pulse generator.

5. PROPOSED INTERLEAVED SAR ADC

The proposed interleaved SAR ADC contains eight SAR blocks described in the previous section and the additional circuitry used to control performance of the entire ADC. The core controlling subcircuits are shown in Figures 8 and 9. A novel pulse generator, that operates as an analog counter, is shown in Figure 8. This circuit counts during the algorithmic operation clock (clk) pulses that control voltage increases across C_2. It also generates pulse IMPL after the threshold voltage of NOT1 gate has been reached. Signal IMPL is then shifted in one bit NOT-based delay line shown in Figure 9, generating clock phases nn8 to nn1, that control ADC.

The presented clock generator has very important advantages. Using only NOT gates instead of typically used D-flip flops, we greatly simplify the circuit structure. Pulse generator generates logical "1," which is then propagated along the delay line, meaning that "1" is only in one place in a given time moment, resulting that only one NOT gate changes its

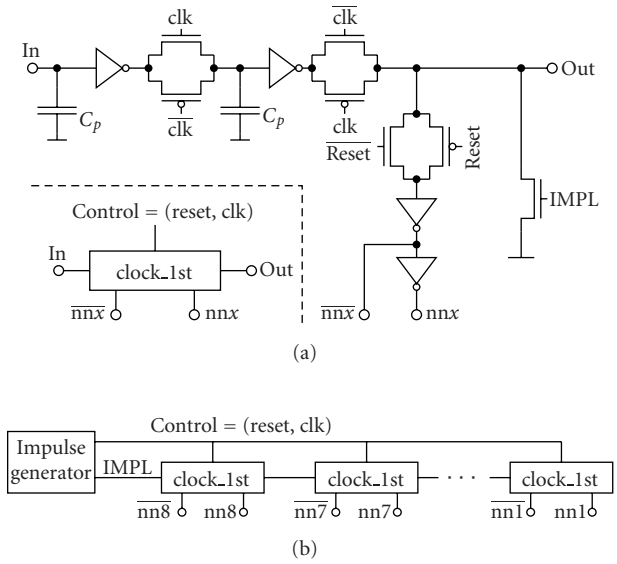


Figure 9: Digital 1-bit delay line: (a) single clock stage, (b) clock diagram.

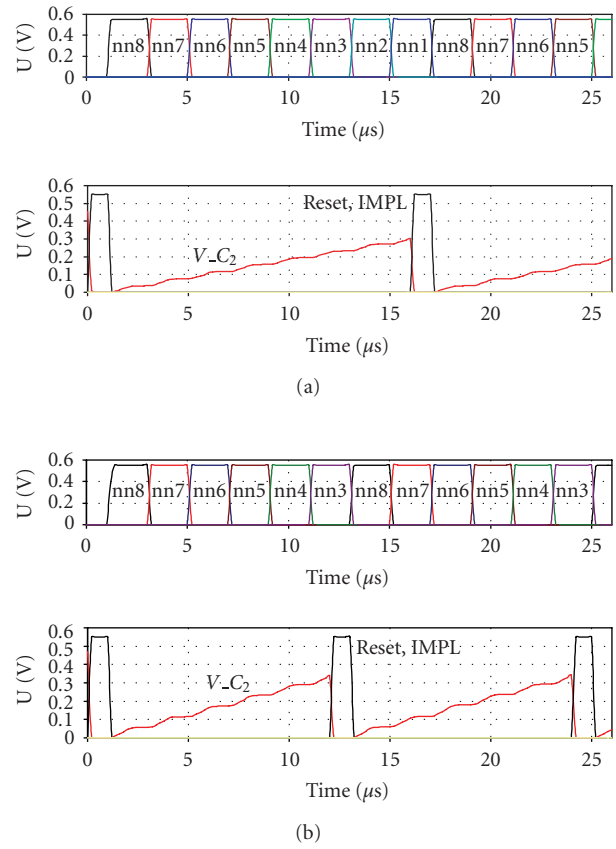


Figure 10: Clock phases nn8-nn1 from the multiphase clock generator for different values of controlling voltage V_{ctr}: (a) 8 phases (nn8-nn1), (b) 6 phases (nn8-nn3).

logical state in each clock (clk) phase. As a result power consumption of entire delay line is independent on the number of delay elements and is always equal approximately to power consumption of only one NOT gate where very small transistor dimensions can be used.

Simulated power consumption of this clock generator is about 100 nW and most of the power is consumed by the pulse generator. The pulse generator in turn is controlled by the DC voltage V_{ctr} and by width of the clk pulses. For higher values of V_{ctr}, C_2 capacitor charges faster and IMPL signal occurs more frequently and reset of the delay line occurs before all SAR sections are waken up from the standby mode. As a result using V_{ctr}, we control number of sections used for data processing. Operation principles for both the pulse generator and the delay line are illustrated in Figure 10 for two cases, when ADC resolution is set to be 8 and 6 bits, respectively.

Both the pulse generator and the delay line are used in top-level central circuit that controls entire interleaved ADC. The ADC is activated when the central IMPL pulse occurs. This signal is then shifted in central delay line activating (waking up) particular SAR ADC sections by switching on individual power supplies $V_{DD\,an}$ and $V_{DD\,dig}$, and resetting digital memory and the current comparator. Signals nn8-nn1, from central digital delay line, become a local IMPL signals (for given SAR sections). These signals after starting up particular SAR sections are then shifted in their individual delay lines, creating individual (separated for each of SAR sections) sets of clock signals nn8-nn1, that directly control SAR algorithm. As a result, each SAR ADC block works with clock shifted in time by one pulse, thus creating interleaved nature of proposed ADC.

Each of SAR sections has additionally its own pulse generator, similar to central pulse generator, used for another purpose. These individual pulse generators generate IMPL signals that put particular SAR sections into a standby mode after a given number of clk pulses controlled by the second constant voltage. As a result, using this voltage, we control the frequency of these IMPL signals and number of calculated bits in each of SAR sections. Thus, using only two DC voltages we are able to control both the number of SAR sections used in data processing (as a result the power dissipation of entire interleaved ADC) and precision (number of calculated bits) of the ADC.

One of the original problems with pulse generators used in ADC is that frequency of IMPL pulses depends on temperature due to resistance variation of MP1 PMOS transistors (see Figure 8). To solve this problem, the special compensation circuit, shown in Figure 11, was designed to eliminate this disadvantage. Output from this circuit is the clocking signal (clk), that is connected to the input of the pulse generator, controlling its performance. This circuit works on similar principle like pulse generator, charging the capacitor C_1 trough PMOS transistor. As a result, resistances of PMOS transistors' channels in both circuits change proportionally. In this way, compensation circuit controls the width of the clk pulses, which in turn stabilizes frequency of the IMPL pulses. When, for example, the resistance of MP1 in pulse

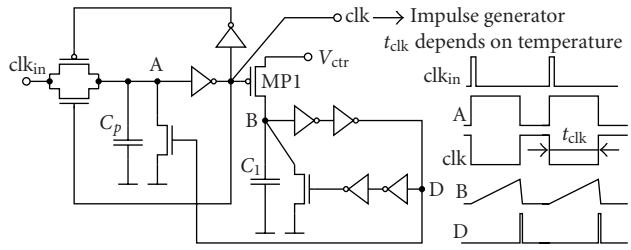


Figure 11: Temperature compensation circuit, which stabilizes frequency of the IMPL signal in the pulse generator.

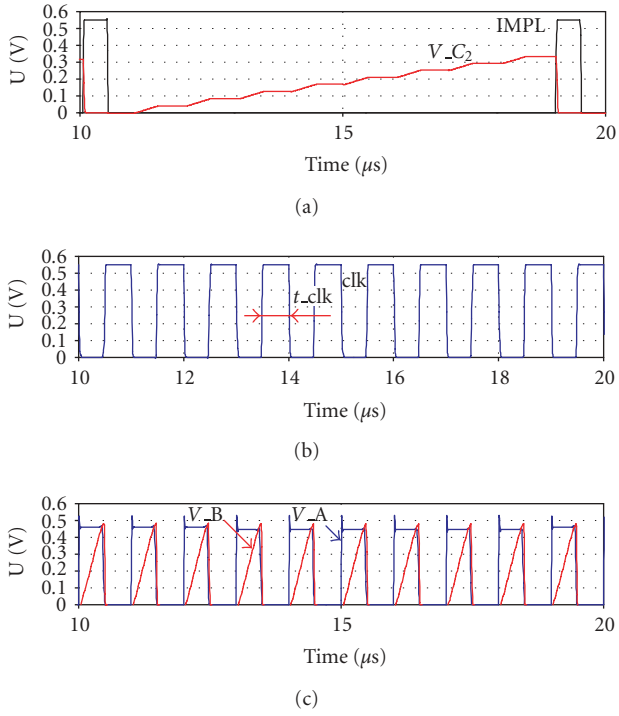


Figure 12: Operation of the pulse generator in connection with the compensation circuit for temperature 0°C.

generator increases, then frequency of IMPL signal decreases due to lower current charging the C_2 capacitor. At the same time, the width of clk pulses coming from the compensation circuit also increases, due to smaller current charging C_1.

Illustrative simulation results are shown in Figures 12 and 13 for 0 and 100°C, respectively. In both cases, frequency of IMPL pulses is the same, and both the number of calculated bits and the number of working SAR sections remain constant for given controlling constant voltages V_{ctr}.

Single SAR sections contain additional logic circuits that control the output multiplexer. After calculation of all 8 bits in a given SAR section or when this SAR section is going to the standby mode, the calculated bits are earlier rewritten to the output memory (multiplexer) and then to the output of the interleaved SAR.

Illustrative simulation results showing the interleaved SAR performance are presented in Figures 14 and 15 for 8

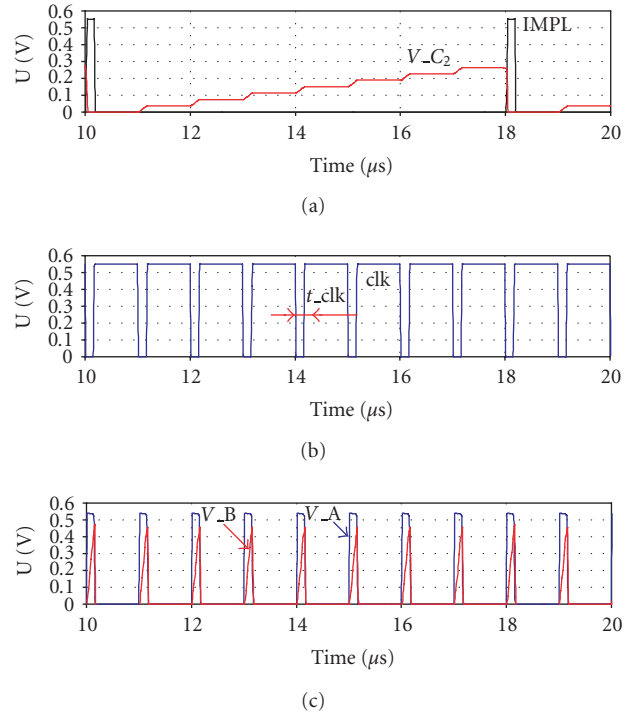


Figure 13: Operation of the pulse generator in connection with the compensation circuit for temperature 100°C.

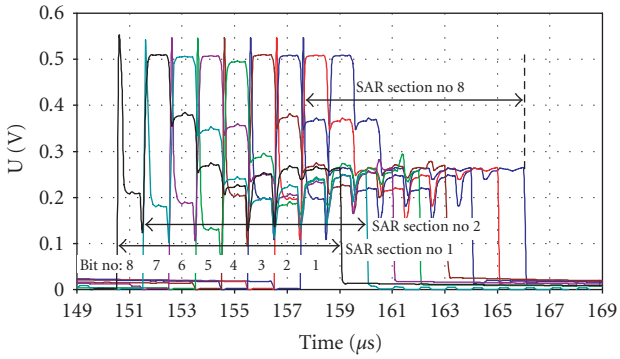
and 6 calculated bits. As shown, current consumption starts increasing when the first ADC section wakes up. Maximum current is reached when all eight sections are on, and then decreases as the subsequent section completes signal evaluation and goes into a power down mode.

6. CMOS IMPLEMENTATION

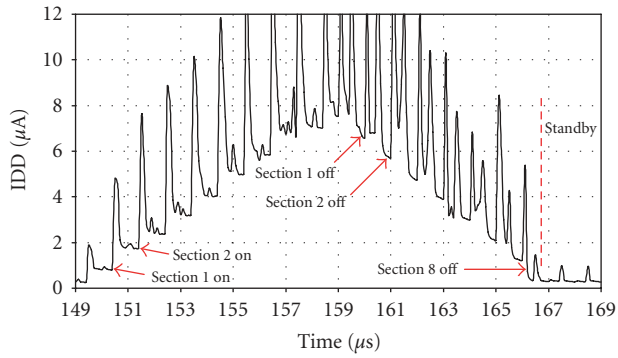
The proposed eight-block interleaved SAR ADC converter has been implemented in a 0.18 μm CMOS process. Layout of a single SAR ADC block is presented in Figure 16 with indication of main circuit blocks. Analog portion of the circuitry and the DAC converter (section C) use only small part of the overall area. The main area is consumed by digital circuitry indicated as sections B and D.

The microphotograph of the interleaved SAR ADC realized in TMSC CMOS 0.18 μm technology is shown in Figure 17. The chip occupies 0.1 mm^2 area and dissipates 3.5 μW from 0.55 V power supply, at the sampling rate of 2 MHz. In a standby mode, when all SAR sections are turned off, average power dissipation is 130 nW, most of which comes from the central pulse generator. Further reduction in the standby power reduction is possible by turning off the pulse generator.

The current design has been implemented for a nominal 8 bits of resolution but extensions up to 12 bits are possible. Increasing the converter resolution will increase area of the digital part linearly with a number of bits by adding additional delay elements. Each additional bit requires an additional transistor in the DAC, and channel width of this



(a)



(b)

Figure 14: Voltage and current waveforms illustrating interleaving action of eight SAR sections sequentially turning on and off during algorithmic operation for calculation of 8 bits.

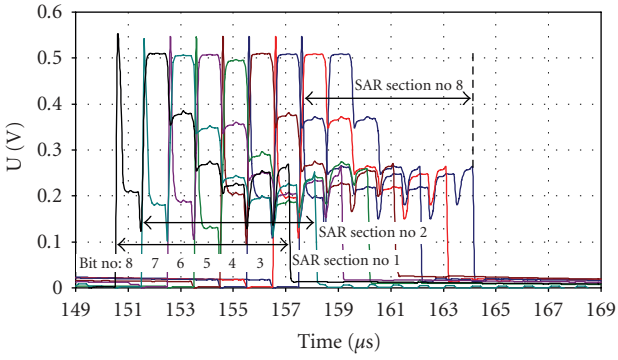


Figure 15: Voltage waveforms illustrating interleaving action of eight SAR blocks for calculation of 6 bits.

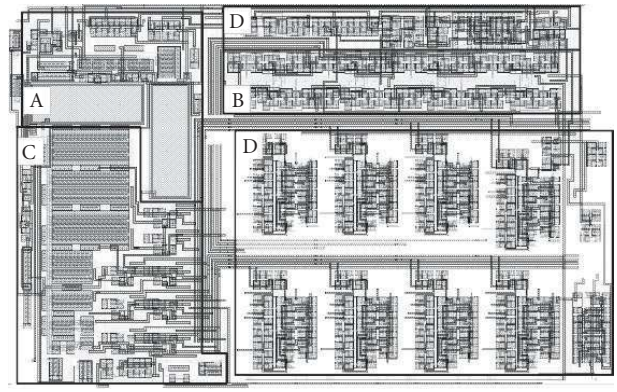


Figure 16: Layout of the successive approximation ADC depicting: (A) pulse generator that controls number of calculated bits through sending power down pulse, (B) one bit digital delay line, that generates clock pulses for 8-stage SAR algorithm, (C) analog core—DAC converter, comparator, and controlling switches, (D) additional digital control circuitry that is used to put ADC section into power down mode and to communicate with the interleaved output memory and multiplexer.

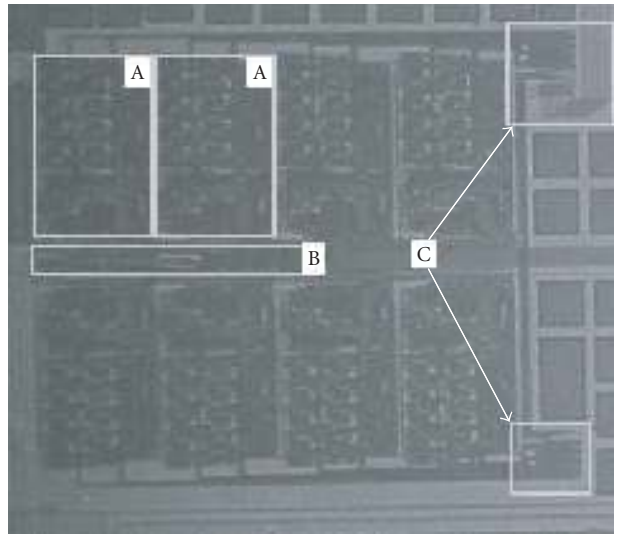


Figure 17: Microphotograph of the proposed current mode interleaved SAR ADC chip realized in CMOS 0.18 μm process: (A) particular SAR ADC sections; (B) central control circuit—pulse generator and delay line; (C) output multiplexer with memory.

element must be two times larger than in the previous DAC stage. This means that the area of the DAC will increase faster than linearly, but this affects the entire chip area only to a small degree. We have estimated that a 12-bit converter will occupy less than double the area of the currently implemented 8-bit ADC.

The proposed architecture has many important advantages, when compared to other low-power SAR and algorithmic ADCs described in Section 3. It is less sensitive to analog impairments compared to existing solutions. As shown in Section 4, transistor matching in most current mirrors is not critical as any device mismatch can be calibrated out by simple reference current (I_{tr}) adjustments. The only mismatch sensitivity resides in the DAC circuitry, but even there it only matters for least significant bits where transistor sizes are the smallest.

The second advantage of the proposed architecture is its sampling rate and power dissipation flexibility, a critical feature in WSN applications. For the reference current I_{tr} of 1 nA, the converter operates correctly with a sampling rate

Table 2: Summary: parameters of the proposed single SAR and interleaved SAR analog-to-digital converters.

Parameter	Single SAR ADC	Interleaved SAR ADC
Resolution	1-8 bits	1-8 bits
Maximum sampling rate (f_s) for I_{tr} = 1 nA	2 MHz	2 MHz
Conversion rate for 8-bit output data	250 kS/s	2 MS/s
Input current range	0-250 nA	0-250 nA
Reference current I_{tr}	1 nA	1 nA
INL	< 1 LSB	< 1 LSB
DNL	< 1 LSB	< 1 LSB
Minimum voltage supply	0.55 V	0.55 V
Power consumption during normal operation	560 nW for f_s = 2 MHz	3.5 μW for f_s = 2 MHz
Power consumption in a standby mode	4 nW	130 nW (all sections switched off)
Technology	CMOS 0.18 μm	CMOS 0.18 μm
Die area	80 μm × 115 μm	0.09 mm^2

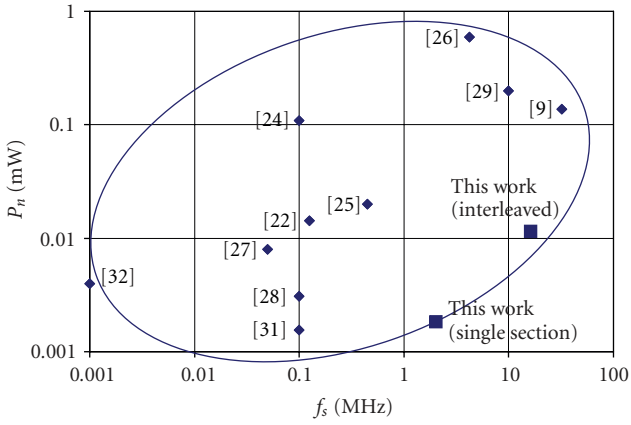


Figure 18: Comparison of various SAR and algorithmic ADCs including the proposed converters in this work. Normalized power dissipation P_n is plotted versus sampling frequency f_S.

of 2 MHz and enables data conversion with 250 kS/s (for an 8-bit resolution) while for I_{tr} of 10 nA it operates as fast as 1 MS/s. This feature offers a direct trade-off between dissipated power and data throughput. For example, when a WSN node is energy starved it can continue ADC processing at slower data rate. The maximum to minimum sampling rate ratio is above 100, such a high value is possible only in current mode implementations.

The third advantage of the proposed architecture is a special control system. The core circuitry is controlled only by DC voltages that enable adjustment of both the number of resolution bits and the number of sections that are used for the SAR operation. In addition, carefully designed temperature compensation circuitry ensures that the control section is stable within the wide temperature range. Digital control circuitry on the other hand has a very simple structure, resulting in both reduced overall circuit complexity and very lower-power dissipation.

Interleaving operation offers some advantages compared to a simple parallel operation that would equally increase data throughput at the expense of higher-power dissipation. Number of sections working in interleaved ADC in a given time moment can be controlled independently resulting in maximum flexibility. For example, if required, only 1 section can be processing the data while the remaining 7 sections are in a standby mode.

Clocking has been designed to be efficient and robust. The clocking circuitry presented in Section 5 is built only from inverters and switches. At any given moment in the entire delay line, which is an important part of this clock generator, only one inverter is active. As a result, the power dissipated by the clocking tree is only 100 nW almost independently on number of clock phases required. In addition, due to its inherent clock simplicity, the resulting silicon area is very small as compared to other solutions presented in the literature.

7. CONCLUSIONS

The analysis presented in this paper shows that for wireless sensor network applications having power dissipation constraints, successive approximation (SAR) ADCs offer the best possible solution. An example of a novel current mode power flexible SAR has been presented. The proposed converter is built using a unique architecture that offers tremendous flexibility in regulating sampling rate, bit resolution, and dissipated power. These characteristics make it particularly suitable for application in wireless sensor networks where flexibility in energy control is of paramount importance. The main parameters of designed single section of SAR ADC and interleaved SAR ADC are shown in Table 2. The proposed ADCs compare very well against reported low-power algorithmic and SAR converters as illustrated in Figure 18.

The proposed ADC can easily be adjusted to operate with different sampling frequencies. The optimum input sampling frequency range for a single SAR block is in a range of 100 kHz to 250 kHz (when operating in an 8-bit resolution mode), but at frequency as high as 1.25 MHz, the circuit still operates well. In this optimum energy range, power dissipation ranges from 220 nW to 550 nW for a 0.55 V power supply. For low values of sampling frequency f_s, below 100 kHz, the energy per bit increases. The existence of the minimum on that range is due to the fact that power consumption of the clock generator does not scale down with the same factor as the core ADC circuitry. At high frequencies, above 250 kHz, the energy per bit increases linearly with the sampling frequency. At the frequency of 1.2 MHz, the energy per bit is two times higher than the optimum. This data point indicates that fast ADC operation is significantly less energy efficient. Other components of the WSN hardware node, like RF transceiver, might however benefit from fast operation, so

careful system level power optimization is required to decide on a sampling frequency selection.

The proposed interleaved SAR ADC consists of eight single SAR ADC blocks. Due to parallel signal processing capability, the circuit is able to increase data throughput 8 times while maintaining 2 MHz clock generator. One of the advantages of the proposed circuitry is its flexibility in controlling its mode of operation. Only two DC control voltages are required to select nominal bit resolution from 1-bit operation up to 8 bits. While the first silicon prototype implemented these two voltages as analog control signals, we have found that this implementation is prone to disturbances caused by noise sources. In a revised design, two configuration DACs will be added in order to have a clean, digital control over the modes of operation for the SAR ADC.

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