FLEXIBLE HIGH SPEED CODEC*

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ABSTRACT

HARRIS, under contract with NASA Lewis, has developed a hard decision BCH (Bose-Chaudhuri-Hocquenghem (ref. 1)) triple error correcting block CODEC ASIC, that can be used in either a bursted or continuous mode. The ASIC contains both encoder and decoder functions, programmable lock thresholds, and PSK related functions. The CODEC provides up to 4 dB of coding gain for data rates up to 300 Mbps. The overhead is selectable from 7/8 to 15/16 resulting in minimal band spreading, for a given BER. Many of the internal calculations are brought out enabling the CODEC to be incorporated in more complex designs. The ASIC has been tested in BPSK, QPSK and 16-ary PSK link simulators and found to perform to with in 0.1 dB of theory. for BER's of 10^{-2} to 10^{-9}. The ASIC itself, being a hard decision CODEC, is not limited to PSK modulation formats. Unlike most hard decision CODEC's, the HARRIS CODEC doesn't degrade BER performance significantly at high BER's but rather becomes transparent.

INTRODUCTION

This paper details the development of the BCH ASIC and its features. Control of the ASIC through a single control line (Block Mark) is discussed. Operation in both bursted and continuous modes of synchronization are detailed. Many of the special features, enabling use of the ASIC in more complex coding schemes, is discussed. In particular an architecture enabling use of the CODEC as a soft decision CODEC is detailed and performance is evaluated. Theoretical performance is predicted, through simulation, and compared to the performance data taken using a digital noise test set and a commercially available bit error rate test set. Details of the test set are presented and programming is discussed. The test set developed under this program is interesting in that any modulation format between 2-ary and 16-ary can be evaluated.

The NASA contract that funded the development of the ASIC also funded the development of the soft decision architecture, discussed in this paper, and the digital noise test set. Ten of the CODEC's were manufactured and supplied to NASA. A preliminary data sheet has been generated for the CODEC and is available.

The ASIC

The ASIC is a high speed low power CMOS design. It was developed using VLSI design tools and was fully simulated. It is packaged in a 132 pin PGA and consumes 1.5 Watts of power when clocked at 45 Mhz. The ASIC contains both the encoder and decoder functions, input/output formatting functions, block mark generation circuits, lock detection circuits and PSK carrier phase ambiguity circuits. As a hard decision CODEC operating in the continuous mode the ASIC can provide all the functions necessary for stand alone operation.

The CODEC can provide up to 4 dB of hard decision coding gain at 10^{-8} BER for bit rates to 300 Mbps (see Fig 1.). The ASIC supports interface widths of 1, 2, 4 or 8 bits. This interface will operate up to a rate of 43 Mhz providing a 38 Mbps, 75 Mbps, 150 Mbps or 300 Mbps data rate for the specified interface width. The data format can be either continuous or bursted.

In the continuous mode the ASIC generates all dynamic control signals internally. Static control signals, such as interface width and lock threshold, must still be supplied. In this mode the ASIC generates a gated clock for clocking data to and from the user. Coded data out of the encoder and into the decoder is continuous. Code words are formed by appending 32 parity bits to every 256 bits of data, resulting in a code rate of $(256)/(32+256)$ or 7/8. The resulting gated clock, supplied to the user, is therefore on for 224 bit times and off for 32. The decoder is self synchronizing in this mode. Circuits within the decoder search for the code word boundaries and a lock detect signal indicates when the decoder has locked. One of the special features of this ASIC is it can resolve carrier phase ambiguities for BPSK, QPSK and 16-ary PSK modulation formats. Static control signals are used to set the modulation mode when this feature is enabled. Note: the acquisition time increases when this mode is enabled.

Hard Decision Performance of a (256, 224) Code
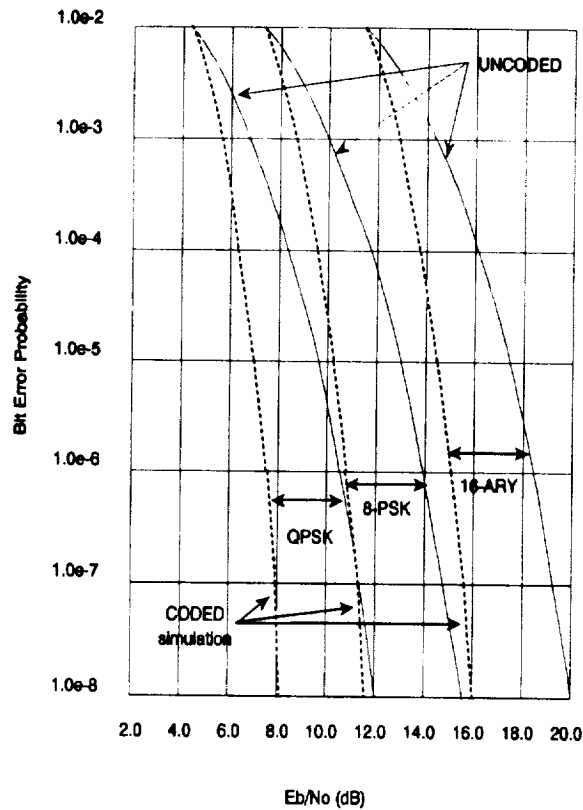
Hard Decision Coding Gain (in dB)			Hard Decision Coding Gain (in dB)			
(256, 224) Code			(512, 480) Code			
BER	QPSK	8-PSK	16-PSK	BER	QPSK	8-PSK	16-PSK
10^{-4}	2.0	2.2	2.4	10^{-4}	1.8	2.0	2.2
10^{-6}	3.0	3.2	3.4	10^{-6}	2.8	3.0	3.2
10^{-8}	3.8	3.9	4.0	10^{-8}	3.6	3.7	3.8

Fig. 1 Hard Decision Coding Gains

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The parity bits appended to the data are made up of two parts. The first 28 bits are true code word parity. The last 4 bits are not important to the decoder operation and are therefore supplied to the user (i.e. USER BITS). It is important to note the bits are not protected by the coding process. The decoder removes these bits and supplies them to the user on the receive side. These bits can be used to support network protocol or order wire functions.

Operation of the CODEC in the bursted mode is very similar to the continuous mode. The exception is the user supplies the code word boundaries to both the encoder and the decoder. These boundaries are determined by the control signal Block Mark. This control signal is a TTL level signal which is high for 224 - 480 bit times and low for 32 bit times. The one constraint is once a burst begins transitions in Block Mark must occur on 16 bit boundaries. Bursts longer than 480 bits are formed by concatenating blocks (see Fig 2). This allows very long bursts to be formed. If a the Block Mark signal is left low for more than 32 bit times then the encoder and decoder assume a new burst and a reset is initiated, for the next burst. Note the code rate in the bursted mode is determined by the code word boundaries supplied by the USER and can be as high as (480/(32+480)) 15/16. The coding gain for this over head is only 0.2 dB less than that of the shortest code word. As in the continuous mode the four USER BITS at the end of every code word are made available to the user.
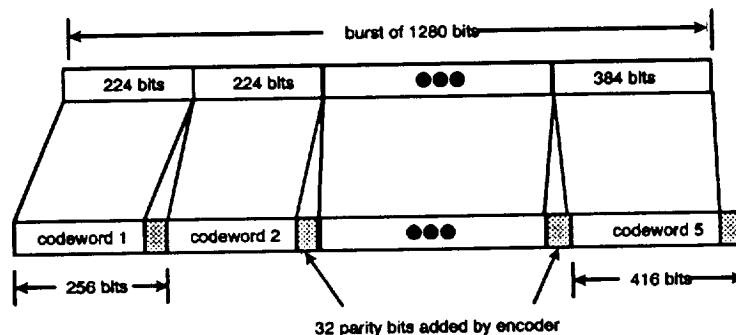

Fig. 2 Concatenated blocks

In addition to providing the decoded data to the user, the decoder can tell the user which bits within a code word were changed by the decoder. This feature was incorporated to enable the ASIC to take advantage of soft decisions when they are available. The application, considered in the NASA funded program, incorporates a Chase Algorithm. (ref. 2) to increase coding gain.This approach is referred to as the FHSC CODEC.

FHSC CODEC

In the FHSC CODEC the decoding function incorporates fourBCH Decoder ASIC's to perform the decoding (fig. 3). The soft decisions are used to generate four code words, one to each of the four decoders. A likelihood term for each of the four code words is also generated. The four code words generated differ in only three bit locations. The bit locations changed are determined by the soft decisions and are the bits with the poorest statistics. Strictly speaking the approach would require 8 decoders to consider all possible combinations of the three bit locations. But, by taking into account the code word parity and the fact that the decoder can only decode code words with 3 errors or less the number of decoders can be reduced to four. The four decoders perform theirdecoding and output the decoded data. The Chase Post Processor circuits read the changed bit locations from each of the 4 decoders. The soft decisions for each of the changed bit locations and the pre-likelihood's calculated previously are then used to calculate a final likelihood for each of the four decoders. The most likely decoder is finally selected and it's decoded output is chosen as the decoded data for that received code word.

Simulations of the FHSC CODEC indicate this technique can provide as much as 1.5 dB additional coding gain (fig 4). Paper designs were generated that preserved all of the features of the ASIC. These designs

were ECL circuits which handled interface widths of 3 or 4 bits. With these widths the FHSC can handle 2-ary, 4-ary, 8-ary and 16-ary modulation formats. The design was a four card design using 300K ECL and FCT logic.
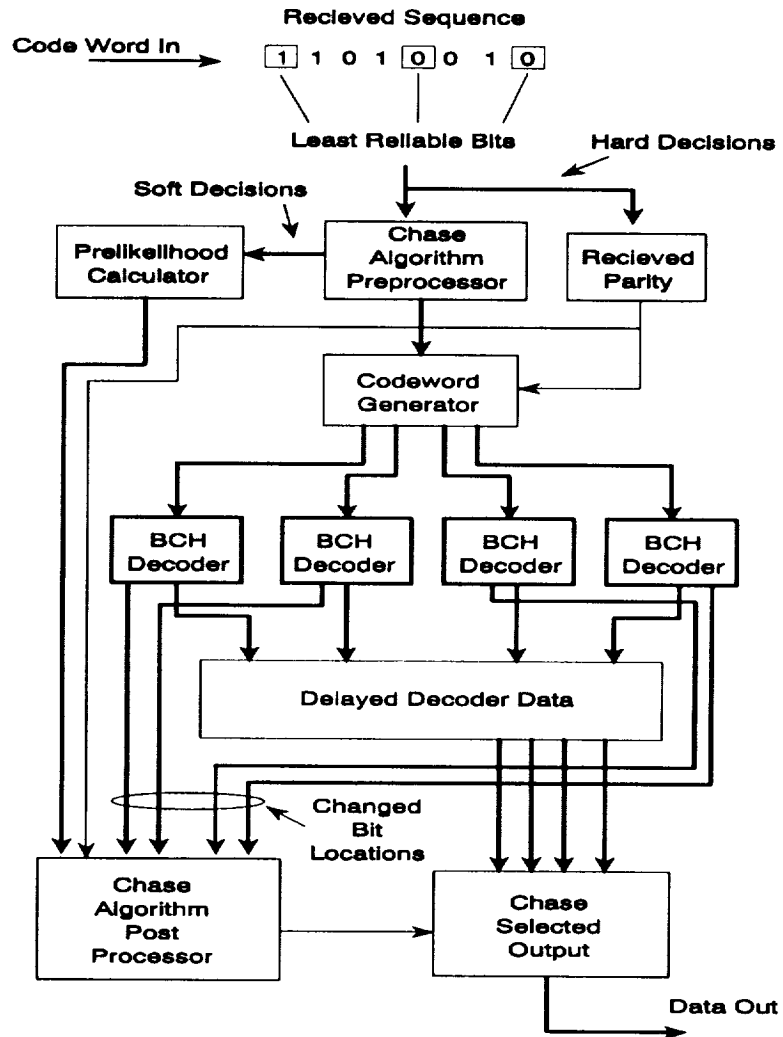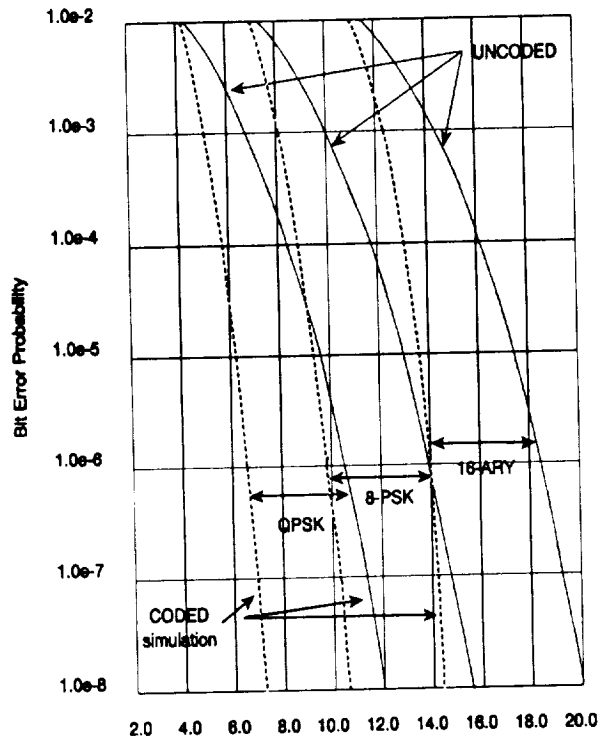

Fig. 3 The Chase Appliqué

Soft Decision Performance of a (256, 224) Code

Fig. 4 Soft Decision Coding Gains

Soft Decision Coding Gain (in dB) (256, 244) Code				Soft Decision Coding Gain (in dB) (512, 480) Code			
BER	QPSK	8-PSK	16-PSK	BER	QPSK	8-PSK	16-PSK
10^{-4}	2.7	2.9	3.1	10^{-4}	2.5	2.7	2.9
10^{-6}	4.0	4.3	4.5	10^{-6}	3.8	4.1	4.3
10^{-8}	4.9	5.2	5.4	10^{-8}	4.7	5.0	5.2

ASIC testing was done using test and development equipment (TDE) developed under the NASA contract and a commercially available BERT. The TDE equipment generated all of the control signals needed for control of the ASIC in both the bursted and continuous modes and provides a digital link simulator for BER testing. Testing was performed for BPSK, QPSK and 16-ary PSK signals, at Eb/No's ranging from 0 dB to + 20 dB. In all cases the BCH CODEC performed to within 0.1 dB of theory. Calibration of the TDE equipment was accomplished by turning the CODEC off and measuring the resulting BER. The coding gain was then measured by turning the CODEC back on and measuring the BER. After compensating for the appropriate band spreading the gain was then determined.

Although the link simulator supports data rates up to 250 Mbps, signals within the TDE equipment indicate the ASIC did support encoder/decoder functions to 300 Mbps. This includes the lock indicator signal of the ASIC.

The digital link simulator is interesting in that it is completely under PC control. In order to handle all the modulation modes it generates quantized I and Q samples based on the modulation mode and the desired Eb/No (fig. 5.). These samples are then mapped into the desired hard decision bits biased on the modulation mode. The modes tested were all PSK signals but there is nothing stopping the RAM memory from being loaded with QAM profiles or FSK profiles. The one limit is that only 2-ary, 4-ary, 8-ary and 16-ary signals can be tested. The TDE equipment was designed to handle both the ASIC and the FHSC. It therefore can also generate the soft decisions needed for the FHSC CODEC designed but never built.
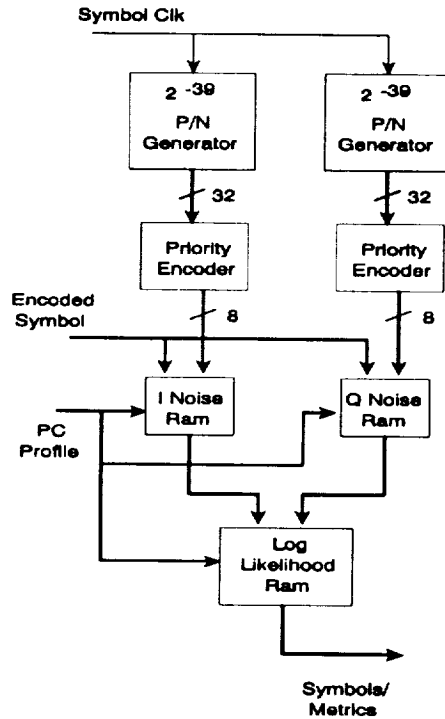

Fig. 5 Noise Generator / Log Likelihood

POTENTIAL APPLICATIONS

The BCH CODEC was developed to deal with the problems of satellite communication systems, in particularly the poor signal quality typically associated with satellites. Many of the video bandwidth compression algorithms require BER' s better than can be maintained on satellites. The BCH CODEC can support the high data rates needed for video signals while providing considerable improvement to the signal quality for a very small overhead. The networking of computers and machines over long distances or to remote locations also may be best served by satellites. Once again the BCH CODEC can provide the coding gain needed to guarantee link integrity. The ability to resolve carrier phase ambiguities, in PSK systems, is an attractive alternative to differential encoding. The self synchronization feature minimizes the circuitry needed to integrate the ASIC into a continuous link.

Though the ASIC's design was tailored to the parameters of a satellite link the basic BCH encoder/decoder can provide coding gain to any link. Cellular phones could pick up considerable coding gain to combat the problems of fading and multi-path associated with travel around a city. High speed digital transcontinental links like those being developed for the phone system could benefit. Digital audio links, such as those being developed for the Cable TV industries, where as many as 30 digital audio channels are multiplexed together forming a high speed digital link, could also use the CODEC.

Considerable interest has already been generated by the chip's development. For many the low overhead rate of the code coupled with magnitude of the coding gain is the most desirable feature. Speed is not an issue. The primary concern of these users is the power consumption and cost. The power consumption of the BCH

CODEC ASIC, as with all CMOS designs, is a function of the clock speed. For clock speeds less than 100 Khz the power consumed is essentially the DC power of the chip and is less than 50 mWatts (Fig. 6).
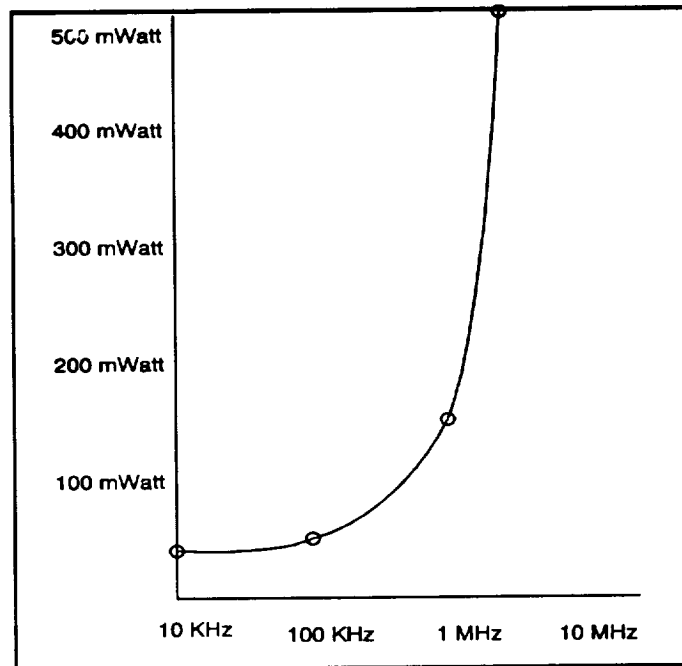

Fig. 6 Power Consumption vs Speed

Cost and Availability

Currently the only chips in existence are those belonging to NASA. Harris is currently evaluating the market. If a market can be identified, several things could be done to drive the costs down. Currently the ASIC's die size is unnecessarily large, due to the large package size needed to accommodate the pin count needed to support all the features of the ASIC. Elimination of the carrier phase ROM's, the bit location circuitry and optimization of the lock detection circuits would result in a sizable reduction in the die size. In addition, the die size could be further reduced by implementing the resulting design in the smaller gate technologies now available. The smaller die would result in an increase in yield and a reduction in cost. The resulting die could be packaged in a 64 pin PLCC rather than the 132 pin PGA, further reducing the price.

CONCLUSIONS

A high speed, high rate CODEC suitable for both burst and continuous modes of operation has been developed by NASA and Harris. It can operate as a single chip hard decision CODEC or, with a decoding appliqué, it can utilize soft decision information in the decoding process. Coding gains up to 4 dB are obtained by the BCH CODEC ASIC, increasing to up to 5.5 dB with soft decisions.

Error correction coding has long been considered a good means to lower the required EIRP in communication systems having unlimited bandwidth. However, high-rate codes such as the one described are also well suited for bandwidth efficient systems. The CODEC rate and interface are matched to the larger signaling alphabets used for constrained bandwidth communications. Performance data indicates that coding gain improves slightly with increasing modulation alphabet size and is a weak function of code word length. Even with the overhead required to insert parity bits, the net result is less power required to communicate a given data rate over a fixed bandwidth channel.

Performance testing indicates the BCH CODEC performs very close to the theory. Using the TDE equipment, coding gains for many other modulation formats can be evaluated. The approach is extremely flexible

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by design. The BCH CODEC supports several different modulation formats and interface modes, at data rates up to 300 Mbps/s.

It is believed that the approach and hardware resulting from this project will prove useful to a variety systems. Tailoring the design to a specific application would reduce the size cost and power consumption of the CODEC, required by many potential applications.

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