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Flexible Multi-Channel Analog-Frontend for Ultra-Low Power Environmental Sensing

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ABSTRACT The trend towards ubiquitous electronics drives the development of autonomous hardware components with longer operating times. This work presents a novel ultra-low power analog sensor frontend (AFE) for environmental sensing applications. Relevant operation parameters like resolution (6 to 13 bit), sample rate (1 to 7.5 kS/s), voltage gain (−6 to 12 dB), transimpedance (1.5 to 12 MΩ), and moving average (1 to 128 taps) are real-time programmable. Four input channels are separately configurable to process voltage, current and potentiometric signals of external or internal sources. The flexible channel-wise configuration enables processing of various signal types and therefore offers a versatile solution for sensors from the Internet-of-Things (IoT) market segment. The AFE integrates switched-capacitor amplifiers, 13 bit, 10 kS/s successive approximation analog-to-digital converter (SAR ADC), bias references, oscillator, digital signal pre-processing and communication in a system-on-chip. A novel sensor power regime supports the flexible read-out of commercial IoT sensors, resulting in excellent power consumption. Fabricated samples in 180 nm technology show an ultra-low power consumption of 8.8 µW. The SAR ADC achieves 10.6 effective bits while consuming 1.8 µW, resulting in a Figure-of-Merit of 116.0 fJ/conv.-step. Measurements with commercial sensors prove the AFE's suitability for an energy-harvester-powered IoT environmental sensor node.

INDEX TERMS Analog to digital converters, low power/low voltage circuits, SAR ADC, sensor/actuator interface circuits, switched-capacitor circuits.

I. INTRODUCTION

LOWERING maintenance costs and increasing the lifetime of autonomous sensor nodes (SNs) fuels the striving for ultra-low power (ULP) integrated circuits (ICs). While wearables and autonomous bio-signal acquisition ICs find already massive usage [1], the trend has not yet reached wide-spread in automation and control, where environmental sensors are processed. Applications like urban air quality monitoring rely on periodical measurements of environmental parameters, e.g., weather (ambient light, humidity, temperature), particles and gases (CO, CO_2, NO_x). Here, the SN form factor still allows large batteries, which delays investment in pricey hardware with higher energy efficiency. With the advent of Internet of Things (IoT) devices to the number of Billions, the demands change [2]: highly-integrated, spatial distributed SNs must be supplied with energy over several years in remote locations. Due to problematic rare-earth materials and increasingly impracticable replacement, batteries become unpopular. Autonomous zero-power SNs, operated fully by energy harvesters, may emerge to the dominant type [3].

Researchers pursue closing the persistent gap between energy harvester output levels and the supply demands of SNs. Recent publications suggest that 1 cm^3 solar and vibration energy harvesters can produce tens of microwatts of output power [4], [5]. On the load side, analog frontends (AFEs),

integrated in complete system-on-chips (SoCs) and operating at very low supply levels below 1 V with power consumption in the range of several nanowatts, have been reported for dedicated (proprietary) biomedical sensors [6], [7]. In order to operate available sensor devices, environmental sensing applications demand typically higher voltage levels and wider frequency ranges, which results ultimately in a power demand towards several microwatts [8], [9], [10]. An environmental sensing AFE targeting ULP consumption of maximum 10 µW is therefore one challenging key part for the implementation of a harvester-powered autonomous long-life SN.

This paper presents a novel four channel integrated sensor AFE in 180 nm CMOS with an outstanding degree of real-time configurability for adjusting the trade-off between application-specific functionality, commercial sensor usage and ULP consumption. It specifically aims for environmental sensing applications with sensors available on the market. Moreover, in a sparse sensing scenario unnecessary power consumption is potentially introduced from idle on-board sensors. Therefore, a novel sensor power regime (SPR) is introduced, effectively removing this problem. The proposed flexible channel configuration supports readout of a variety of IoT-compatible sensors, which enables possible adaption to a wide range of applications, which is demonstrated with an environmental monitoring setup including commercial ambient light, gas and temperature sensors. The AFE provides voltage, current, and potentiometric measurement with channel-wise programmable gain, sample rate, resolution, digital offset correction (DOC) and moving averaging.

System-level considerations and SPR are reviewed in Section II. The architecture of the analog part with numerous innovations is presented in Section III, whereas Section IV deals with the digital part. In Section V, testchip measurement results are presented and discussed. Conclusions are drawn in Section VI.

II. SYSTEM DESIGN

Key specification parameters of the AFE are derived after surveying commercial IoT-compatible environmental sensors. Part of this survey is listed in Table 1. The majority of low-power sensors (current consumption below 300 µA) show signal levels in the range of volts and bandwidths up to several thousand hertz. This implies challenging specifications for the AFE: Sample rates of at least 1 kS/s and an input voltage range of more than 1.4 V must be realized. Most practical applications require an ADC accuracy of more than 10 bit. The classical approach to achieve ULP consumption, which is lowering operation voltage, accuracy and speed, cannot be followed.

A. FRONTEND ARCHITECTURE

The architecture of the proposed AFE is shown in Figure 1. It operates with analog and digital supply voltages of 1.8 V. The four differential analog inputs $IN_P[3:0]$, $IN_N[3:0]$ are multiplexed by a four-to-one analog multiplexer with

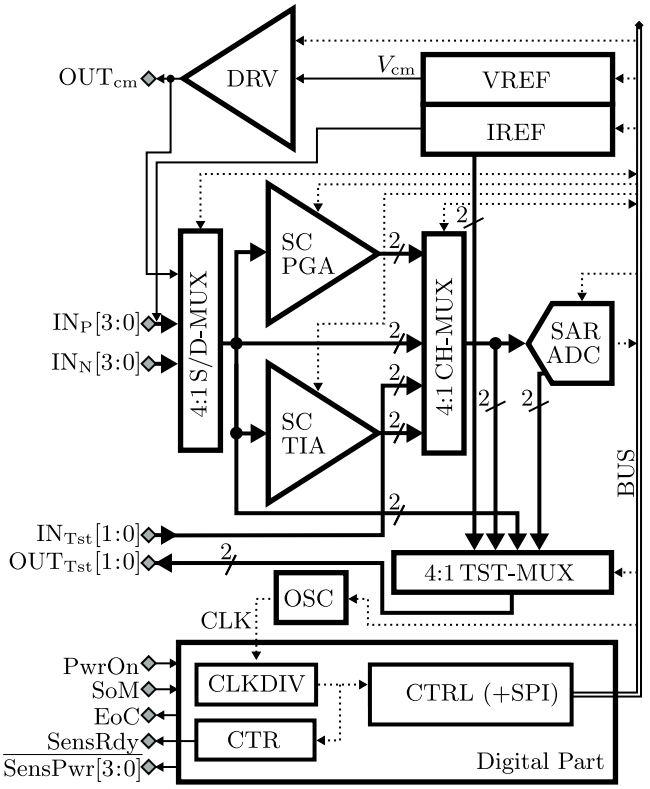

FIGURE 1. AFE block diagram.

differential and single-ended (pseudo-differential) mode (S/D-MUX). With $\{0.9 \pm 0.85\}$ V, the input voltage signal range is close to rail-to-rail over a usable signal band of 0 Hz to 3.75 kHz. The output signal is split up and transferred via amplifiers, or directly, to the channel multiplexer (CH-MUX), which chooses between voltage, current or direct channel, or test input $IN_{Tst}[1:0]$.

The programmable gain of the voltage channel is realized with a SC PGA. In the current channel, current signals are converted to voltages with a programmable impedance, which is realized by a SC TIA. All channels are capable of single-ended to differential conversion, with help of the internal reference voltage OUT_{cm}, which can be applied to the negative input inside the S/D-MUX [11]. All paths can be gain-adjusted, in order to deliver the same differential voltages close to rail-to-rail, fitting to the input of the following programmable SAR ADC. A third test multiplexer (TST-MUX) serves for needs of production test and debugging.

The digital outputs of the ADC are transferred via an on-chip parallel bus (BUS) to the digital part. The BUS delivers as well configuration and clock signals to the analog blocks. A SPI interface handles data exchange with the chip periphery, and a custom digital controller (CTRL) provides timing signals, configuration data and signal pre-processing functionalities, including DOC and SPR. An on-chip oscillator (OSC) produces a digital clock signal, which can be divided by the programmable clock divider (CLKDIV) in order to

TABLE 1. Survey of commercially available, IoT-compatible sensors with current consumption below 300 µA.

No.	Class	Manufacturer	Name	Measuring Range	Output Signal	Bandwidth	Current Cons.
1	**Temperature**	MAXIM	MAX6607[1]	-20 °C to +85 °C	Voltage: 0.2 V to 1.4 V	below 1 Hz	8 µA to 15 µA
2	**Ambient Light**	Renesas	ISL1902[1]	0.3 lux to 10 klux	Voltage: 0.02 V to Supply	below 5 kHz	0.65 µA to 15 µA
3	**CO Gas**	Spec Sensors	3SP_CO[1]	0 ppm to 1000 ppm	Potentiometric Current: 0 A to 26 µA	below 1 Hz	10 µW to 50 µW
4	**Accoustic**	PUI Audio	PMM3738	more than 100 Hz	Voltage: 0 V to Supply	more than 100 Hz	5 µA to 85 µA
5	**Acceleration**	Analog Devices	ADXL316	±16 g to ±19 g	Voltage: 0.1 V to 75% Supply	below 1.6 kHz	250 µA to 400,µA
6	**Humidity**	Honeywell	HIH5030	0 %RH to 100 %RH	Voltage: 0.5 V to Supply	below 5 kHz	200 µA to 500 µA

[1] selected for multi-sensor demonstration case

adjust sample rate. Alternatively, a more accurate external clock source can be used. A counter (CTR) produces the long-time delayed signals for SPR.

All necessary bias voltages and currents are generated by PTAT/CTAT current reference (IREF) and voltage reference (VREF). The trimming of IREF is possible by monitoring current copies via the TST-MUX. The output of VREF is buffered by an analog driver amplifier (DRV), in order to regulate loading in potentiometric mode and S/D mode.

Selecting a supply voltage V_{DD} of 1.8 V is a compromise between the necessary input voltage range and requirements of the instrumentation and on-board interfacing. An important benefit of choosing a standard supply voltage is the possible usage of standard components, without the need for additional power-demanding level-shifters on SN level.

B. MEASUREMENT MODES

The AFE is capable of converting signals originating from different sensor types and applications. In order to give an idea of the offered flexibility, an overview of the AFE measurement modes is shown in Figure 2a–f. Differential voltage signals are sampled and amplified by the SC PGA and transferred to the ADC (Figure 2a). Single-ended voltages are S/D-converted with an external reference voltage V_{ext}, applied to the pin $IN_N[i]$, which defines the zero offset of the transfer curve (Figure 2b). The internal reference $OUT_{0.9}$ can be used, too (Figure 2c). Note that the signal, which is transferred to the ADC is always a differential voltage, V_{diff}.

Single-ended and differential currents can be measured accordingly with the arrangement in Figure 2d. With the circuit of Figure 2e, three-and four-terminal potentiometric sensors, such as sensor 3 from Table 1, can be biased and measured [12]. The depicted circuit maintains a sensor bias voltage V_{bias} of 0 V, which is recommended for sensor 3 from Table 1. Other potentiometric sensors parts may require a different bias, which can be produced with a combinations of Figure 2b and 2e.

The cascade of internal IREF, which produces a CTAT current, TIA and ADC, reflects a temperature monitor, shown in Figure 2f. It can be used for temperature drift calibration.

The ADC can be driven directly from sensors, too. This mode is recommended for sensors, which come with high driving capability and a fitting voltage level, and enables low-power measurement without the need for additional references and amplifiers.

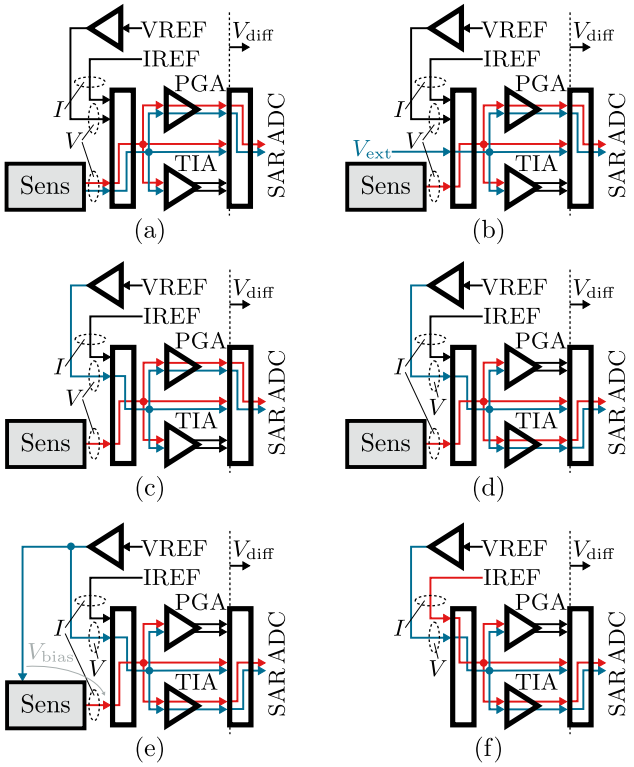

FIGURE 2. AFE measurement modes: differential voltage (a), single-ended voltage with external reference (b), single-ended voltage with internal reference (c), single-ended current with internal reference (d), potentiometric current with internal reference (e), temperature monitoring (f).

C. SENSOR POWER REGIME

According to Table 1, the targeted AFE power consumption of 10 µW is exceeded by some sensors. In a SN scenario with sparse measurements, shown in Figure 3a, the AFE is started only once a minute, hour or day, as soon as a wake up event is indicated by an on-board wake-up transceiver (Rx/Tx). In order to reduce the on-time of sensors and therefore minimize their idle power consumption, we propose an AFE-driven sensor power regime (SPR), which is a generalization of the concept of [13], and is depicted in Figure 3b.

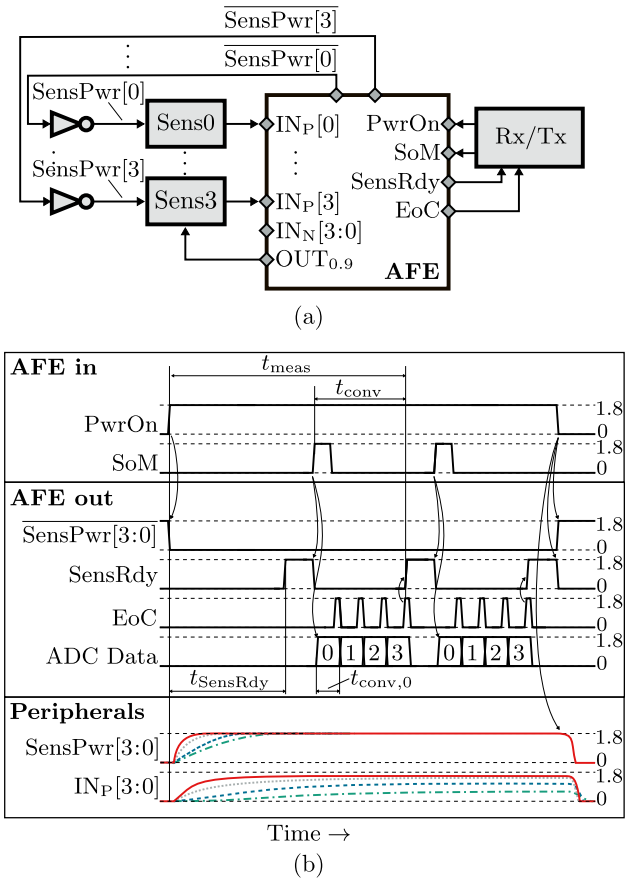

FIGURE 3. Concept diagram of SPR (a) and measurement cycle with four sensors (b). Off-chip support circuitry is grey-colored. Logic high value is 1.8 V, logic low value is 0 V.

As soon as the AFE is started with PwrOn (power on), the signals $\overline{\text{SensPwr}[3:0]}$ (sensor power) turn logic low, which powers the sensors via off-chip inverters with high driving capability. The number of measured sensors is configurable within the AFE. As indicated by the slow charging of SensPwr[3 : 0], the sensor's start-up can take some micro- to hundreds of milliseconds. The CTR block delays the flag SensRdy (sensors ready) by a programmable time delay t_{SensRdy}. When SensRdy shows a rising edge, the measurement is started by SoM (start of measurement). This turns SensRdy to logic low, following a handshake protocol, and starts processing of the pre-programmed channel numbers, starting with number zero.

Internally, the ADC performs between 1 and 128 averaged conversions, before the data is stored in a register. A new release of data is indicated by a pulse of EoC (end of conversion). If all four channels are processed, EoC will pulse four times. The pre-processed data is transmitted via Rx/Tx, and the complete SN goes back to sleep mode, until the next wake-up event is indicated. Here, the SPR shows its full capacity of reducing the SN average power P_{sn}:

$$P_{\text{sn}} \approx \frac{t_{\text{meas}}}{t_{\text{wu}}}(P_{\text{Sens}} + P_{\text{inv}}) + \frac{t_{\text{conv}}}{t_{\text{wu}}}P_{\text{conv}} + P_{\text{RxTx}} \qquad (1)$$

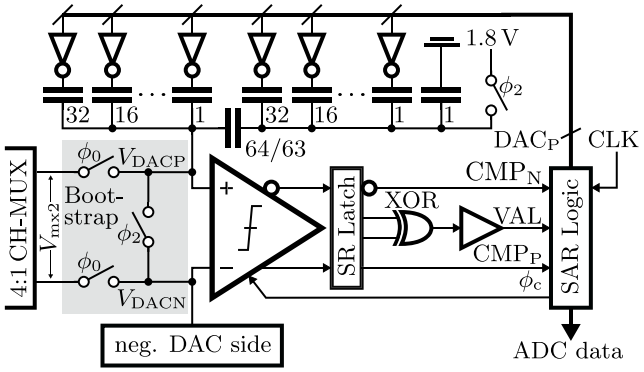

FIGURE 4. Schematic diagram of programmable charge-redistribution SAR ADC.

where t_{wu} is the wake-up period of one minute, P_{Sens} is the average power consumed by the sensor components 1, 2 and 3 from Table 1, P_{inv} is the leakage power of the inverters of about 1 µW, P_{conv} is the power while conversion of 10 µW, and P_{RxTx} is the transceiver power of about 100 µW. The CTR power during t_{SensRdy} is neglected. With $t_{\text{meas}} = 1$ s and $t_{\text{conv}} = 50$ ms, the SN's average power consumption with SPR can be calculated to 101.8 µW, compared to 205 µW with always-on sensors. The saving introduced by SPR in this example is therefore about 50 %. Note, since the transceiver power has a critical impact on this relationship, lowering $P_{\text{Rx/Tx}}$ will result in more savings.

III. FRONTEND IMPLEMENTATION

The AFE of Figure 1 is implemented in a low-cost 180 nm silicon-on-insulator (SOI) technology with high-voltage option. Ultra-low power applications benefit less from high computational power offered by smaller nodes. Instead, the design flow demands high process stability and model accuracy and low silicon cost for IoT market acceptance. Therefore the 180 nm node is an optimal compromise. The high-voltage option enables future integration of power regulators and sensors operating in the range of 5 to 12 V (not listed in Table 1). Furthermore, because of their inherently duty-cycled behavior, ultra-low power circuits benefit from the SOI technology feature, which effectively isolates highly dynamic circuit parts.

A. CHARGE-REDISTRIBUTION SAR ADC

The key part of the AFE is the programmable charge-redistribution SAR ADC shown in Figure 4. This topology shows one of the best energy efficiencies and is a natural choice for low-speed, medium-resolution ADCs [8]. The resolution n and sample rate are programmable in the range of 6 to 13 bit and 1.25 to 10 kS/s.

The timing diagram of one conversion is shown in Figure 5. The internal clock signal CLK serves as time base for the binary search algorithm. One conversion begins with phase ϕ_0, where bootstrapped switches (Figure 6a) sample the differential voltage V_{mx2} at the CH-MUX output on the top-plates of negative and positive 12 bit binary capacitive

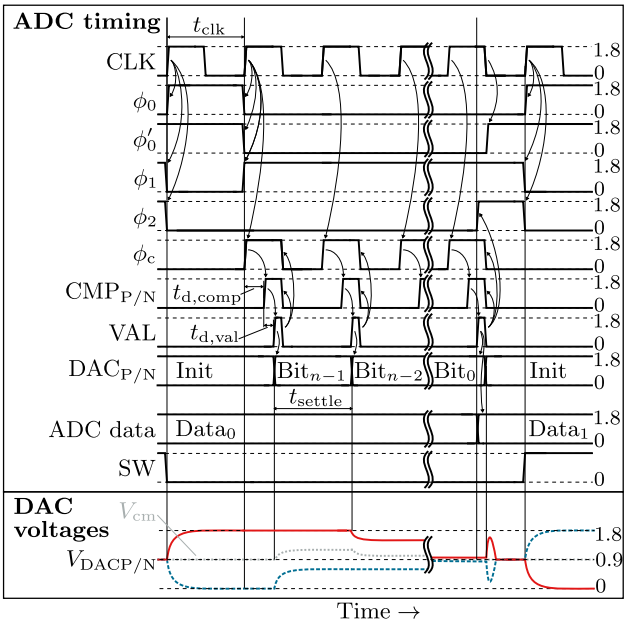

FIGURE 5. Internal waveforms of SAR ADC conversion with AFE-specific timing signals ϕ_0–ϕ_2, SW and DAC voltages generated by inverse switchback switching scheme.

digital-to-analog converters (CDACs). The common-mode voltage $V_{cm} = (V_{DACP} + V_{DACN})/2$ is defined by the input signal common mode, i. e., 0.9 V introduced by the preamplifiers. During bit conversion phase ($\phi_0 = 0$), the two-stage dynamic comparator (Figure 6b), is clocked with synchronous signal ϕ_c and generates decision signals $CMP_{P/N}$ after time delay $t_{d,comp}$. A valid decision is sensed by a XOR gate, whose output signal VAL is delayed by $t_{d,val}$, in order to fulfill setup-and-hold requirements. Triggered by VAL and based on the comparator decision, the SAR logic generates one by one all bits of the 12 bit CDAC input words $DAC_{P/N}$. Since the clock speed is low compared to $t_{d,comp}$ and $t_{d,val}$, this self-timed strategy maximizes CDAC settling time t_{settle}, and minimizes the time in which the comparator is powered on (neglecting digital gate delay):

$$t_{settle} = t_{clk} - t_{d,comp} - t_{d,valid} \approx t_{clk} \tag{2}$$

The proposed SAR ADC employs a modified bufferless switching scheme. Power-demanding reference voltage buffers are omitted by employing the 1.8 V analog supply voltage and ground as references, therefore achieving a differential full-scale range V_{FS} of almost rail-to-rail [14]. Moreover, the use of the supplies as references combined with the relatively low clock speed minimizes settling errors and dismisses CDAC redundancy. The proposed architecture requires a minimum number of comparator decisions and therefore low power consumption.

The CDAC switching scheme is a modification (inversion) of the switchback scheme, which shows improved power efficiency and reduced V_{cm}-variation compared to classical monotonic switching [15], [16], but relatively low complexity. The phase and switching diagram of a $n = 4$

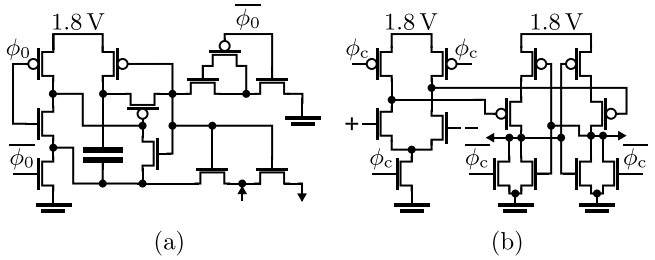

FIGURE 6. Schematic diagrams of bootstrapped switch (a) based on [16] and two-stage dynamic comparator (b) based on [14].

binary scaled SAR ADC is shown in Figure 7, illustrating the cycling through ADC reset phase ($\phi_2 = 1$), sampling phase ($\phi_0 = 1$) and bit resolving phase ($\phi_1 = 1$). Common-mode voltage V_{cm} is increased after the comparator's MSB decision by $V_{FS}/4 = V_{DD}/2$, and is decreased successively in the following $n - 2$ steps by $V_{FS}/8$, $V_{FS}/16$, and so on, approaching 0.9 V±1 LSB during LSB decision. Inversion of the scheme from [15] is achieved by inverting the initial value of $DAC_{P/N}$. The dummy capacitor is left connected to ground, which does not disturb the capacitive divider [14]. Two major advantages compared to [15] are obtained: first, the rising V_{cm} enables the use of a NMOS dynamic comparator, which shows improved speed compared to the PMOS type. Second, CDAC charging happens only during the MSB phase and the reset phase, whereas during the rest of the bit resolving the CDAC is discharged. Therefore, heavy loading of the supply occurs mostly in the uncritical reset phase, which results in reduced *IR* drop during bit resolving and improved ADC reliability and linearity. These advantages come at no expense, since the sum of overall switching and reset energy is not increased by the inverted scheme, as shown in Figure 7.

The required 12 bit resolution of the CDAC is achieved with a split-capacitor topology, which reduces the number of unit capacitances to 128 per DAC [17]. Compared to a binary-scaled CDAC with 4096 unit capacitors, the power consumption is drastically reduced. The unit capacitor is sized to 76 fF using simulation tools to fulfill the 12 bit matching requirement. For the 180 nm node with less digital performance it is advantageous to omit a mismatch calibration strategy, which would require a calibration sequence and more logic power. In return, the total ADC input capacitance adds up to around 5 pF, which illustrates a trade-off between reducing logic power and increasing analog power.

B. PROGRAMMABLE GAIN AND TRANSIMPEDANCE AMPLIFIERS

The voltage and current amplifier stages change the signal from continuous to discrete time and are therefore realized as switched capacitor (SC) circuits. SC amplifiers outperform continuous time amplifiers in low-power applications because they can be realized very efficiently with switched operational amplifiers (SOA) [18]. High on-chip resistances resulting in high noise and area contributions can be omitted.

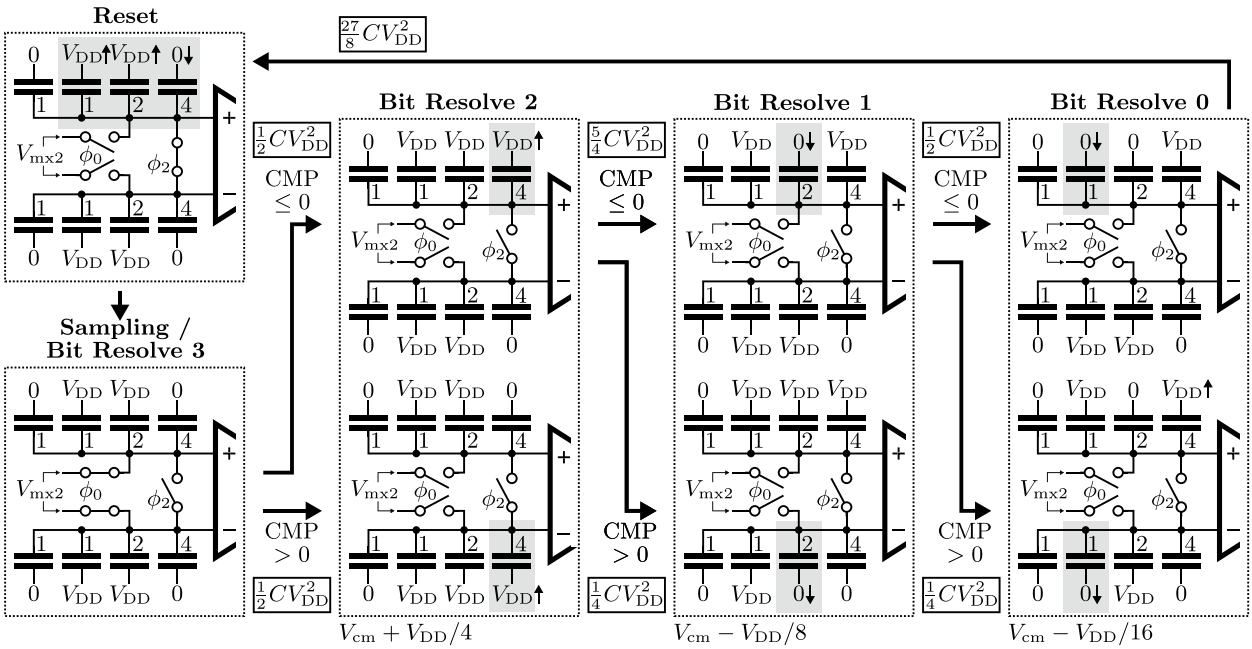

FIGURE 7. Phase diagram of exemplary binary SAR ADC ($n = 4$ bit) with inverse switchback switching scheme.

This enables the TIA, which is realized as SC integrator [19], to handle very low input current levels efficiently.

The SC PGA and SC TIA circuits are shown in Figure 8a–b. Both include a SOA in two feedback configurations, utilizing different combinations of CMOS switches, fixed capacitors, fixed resistors, and programmable capacitor matrices of unit elements C_u. Binary-to-thermometer decoders (B2T) convert the static vectors P[1 : 0] and T[2 : 0] to their thermometer-coded representations $P_{t3\text{-}0}$ and $T_{t7\text{-}0}$, which control the total capacitance of binary-weighted capacitor array (BWCA) and unary-weighted capacitor array (UWCA).

The operation of the SC PGA (Figure 8a) is as follows: as shown previously in Figure 5, the non-overlapping clock signals $\{\phi_0', \phi_0, \phi_1\}$ control the amplifiers in synchronization with the ADC sampling and bit resolving phases [20]. In phase ϕ_1, the SOA is powered-off, while the SAR ADC is performing bit resolving. Input voltage signal V_{mx1} is sampled and charges track-and-hold capacitor C_{th}, which is realized as BWCA. Phase ϕ_0' starts shortly (half period) before ϕ_0 and powers the SOA in order to fulfill internal settling times. In phase ϕ_0, the saved charge is transferred to the output via fixed feedback capacitor $C_{fb} = 2\,C_u$. A voltage gain A_V is realized:

$$A_V = \frac{V_{out}}{V_{mx1}} = \frac{C_{th}}{C_{fb}} = 2^{\sum_{i=0}^{1} P[i]2^i - 1} \tag{3}$$

The configuration in Figure 8a achieves the four discrete gain steps {0.5, 1, 2, 4} with only eight capacitors controlled by P[1 : 0]. The gain steps were primarily chosen to match sensors from Table 1 to the ADC input, but can be potentially extended. During ϕ_0, the CDACs are capacitive loads of the SOA, and the differential output voltage V_{out} is sampled via the CH-MUX. Eventually, the cycle begins again with phase ϕ_1. Rail-to-rail level of V_{out} is achieved for a variety of input signal levels with the programmable gain setting. The average amplifier power consumption is duty-cycled by factor $1/n$, compared to always-on amplifiers, while no additional buffers have been inserted into the signal path.

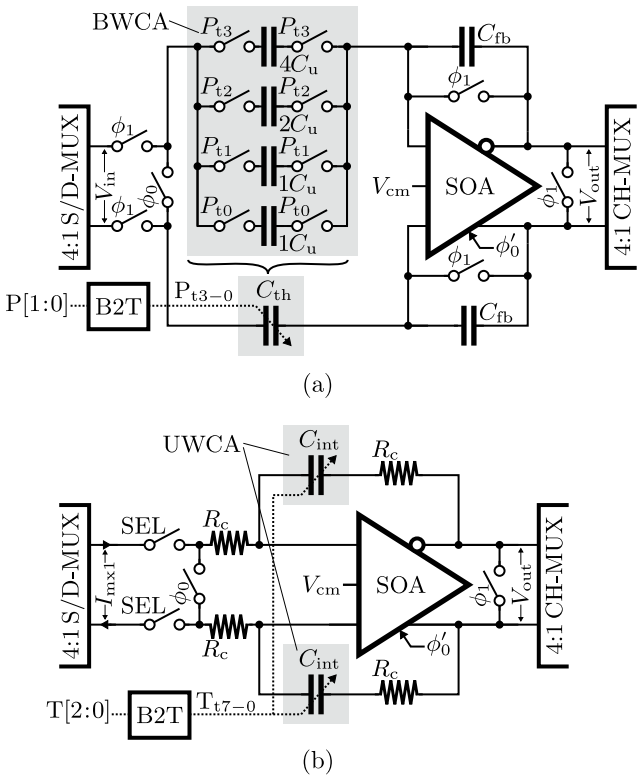

FIGURE 8. Schematic diagrams of SC voltage amplifier (a) and current amplifier (b).

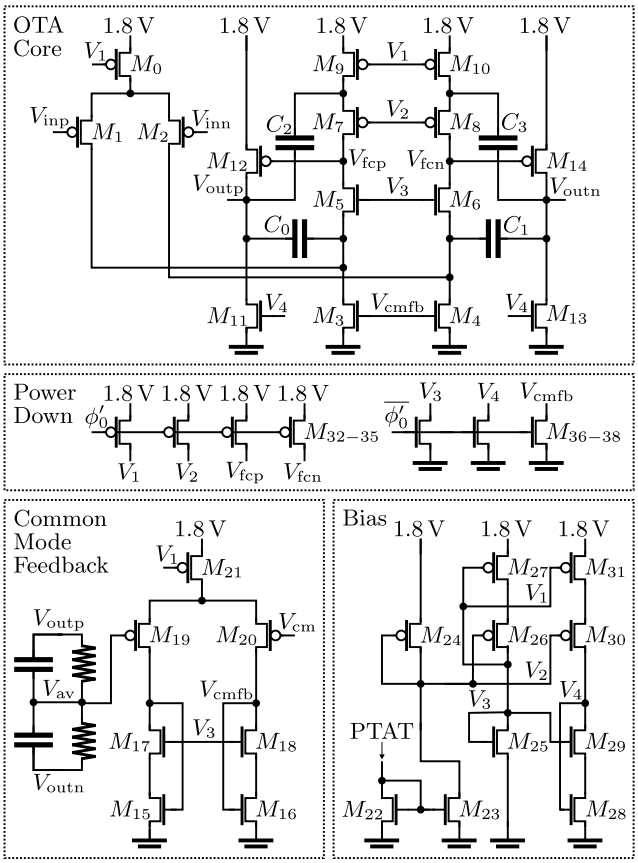

FIGURE 9. Schematic diagram of SOA [20].

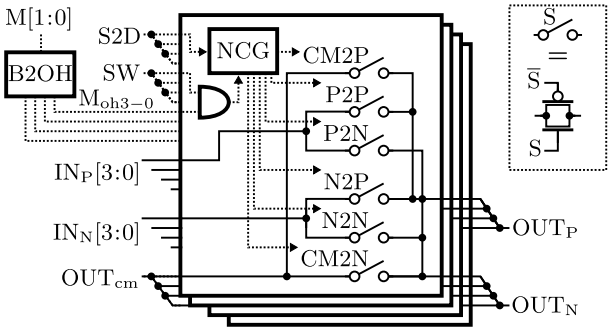

FIGURE 10. Schematic diagram of analog multiplexer with differential and single-ended mode (S/D-MUX).

The operation of the TIA (Figure 8b) is likewise [19]. During ϕ_1, the current signal I_{mx1} is steered towards the negative terminal, which is connected to a current sink, while the SOA is powered-off. The static current flow enables measurement of very low currents in reasonable speed. Note that additional SEL switches are inserted in signal path in order to avoid undesired shorting of the terminals. In ϕ_0' the SOA is powered-on and phase ϕ_0 is the TIA integration phase. I_{mx1} charges the integration capacitor C_{int}, realized as UWCA, for the fixed time amount of one clock period. A transimpedance Z_I is realized and controlled by T[2 : 0] in eight steps between 1.5 MΩ and 12 MΩ:

$$Z_I = \frac{V_{\mathrm{out}}}{I_{\mathrm{mx1}}} = \frac{t_{\mathrm{clk}}}{C_{\mathrm{int}}} = \frac{t_{\mathrm{clk}}}{\sum_{i=0}^{7} \mathrm{T}[i] C_{\mathrm{u}}} \tag{4}$$

Compensation resistors R_{c} are inserted in the loop for stability. Since their contribution is in the ranges of Ohms, they are neglected in (4).

The SOA, which is the main block of both PGA and TIA circuits, is shown in Figure 9. It is based on a two-stage topology [21] implemented by a fully-differential folded-cascoded operational transconductance amplifier (devices M_{0-10}) followed by a common-source amplifier (transistors M_{11-14}). The first stage delivers high gain bandwidth, while the second stage increases the voltage range of $V_{\mathrm{outp,n}}$ to quasi rail-to-rail fulfilling the required trade-off of low power consumption.

Miller compensation is chosen instead of increasing the output transconductances $g_{\mathrm{m12,14}}$, in order to save power. Nevertheless, this pole splitting technique also introduces a positives zero. This new feedforward current through the compensation path adds another -90∘ phase shift. One way to get rid of it, is using a cascode to block it. Thus, the compensation capacitances C_{0-3} are split between the cascode devices of the first stage instead of connecting them between the output and input of the second stage [21]. Sizing these compensation capacitors requires a special trade-off with the above-mentioned compensation resistors R_{c} in the TIA circuit to guarantee the stability and symmetry of the whole chain including multiplexers and sample switches. Moreover, since all these components sum up at the amplifier output nodes increasing their loads and thus slowing down the action of the power-down devices in Figure 9, a trade-off between power-up speed, output voltage range, current consumption and area of the output stage puts additional constrains to the design. The resulting SOA achieves open-loop gain of 94 dB, gain-bandwidth of 1.4 MHz and phase margin of 92.6 ° at a 6 pF load.

C. ANALOG MULTIPLEXER AND OFFSET CORRECTION

The schematic diagram of the 4:1 analog S/D-MUX is shown in Figure 10. CH-MUX and TST-MUX are reduced versions of this circuit, since they do not include additional S/D switches and logic.

The two bit vector M[1 : 0] controls the multiplexing of differential output $\mathrm{OUT_{P/N}}$ among the four differential inputs $\mathrm{IN_{P/N}}$[3 : 0]. A binary-to-one-hot decoder (B2OH) activates one single line $m \in \{0, 1, 2, 3\}$ of one-hot-coded vector $\mathrm{M_{oh3\text{-}0}}$, which selects one out of four unit cells. Each unit cell is composed of six analog switches realized as transmission gates and a non-overlapping clock generator (NCG) [13]. They are placed in separate isolated P-wells for lowering channel crosstalk. Table 2 shows the truth table of control signals SW (swap), S2D (single-ended-to-differential) and the switch-on signals. With DOC enabled, SW will toggle with each new conversion (Figure 5) and by

TABLE 2. Truth table of S/D-MUX control signals.

S2D	SW	P2P	P2N	N2N	N2P	CM2P	CM2N
0	**0**	1	0	1	0	0	0
0	**1**	0	1	0	1	0	0
1	**0**	1	0	0	0	0	1
1	**1**	0	1	0	0	1	0

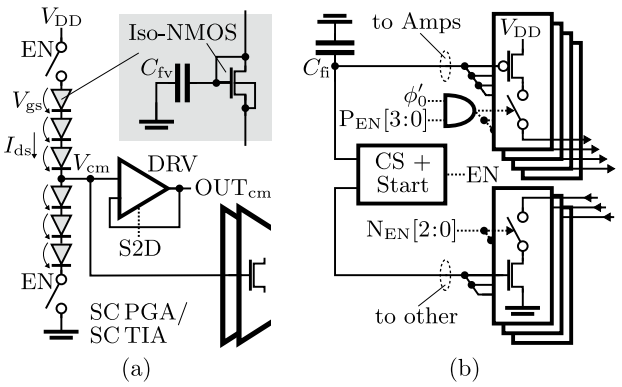

FIGURE 11. Schematic diagrams of voltage reference source (a) and current reference source (b).

applying digital averaging to several samples, channel offset is effectively corrected.

Finally, static signal S2D sets the MUX in single-ended mode. Instead of the negative terminals, the internal common-mode reference OUT_{cm} is connected to $IN_N[i]$. OUT_{cm} is further transferred to the amplifiers, which perform the single-ended to differential conversion. The distortion of these components must therefore satisfy the ADC accuracy. Since the amplitude of a single-ended signal is half of the amplitude of a differential signal, the total resolution of the AFE is reduced by one bit in this mode.

Linearity, distortion, crosstalk, mismatch and noise considerations require careful sizing of the transmission gate switches [22]. The proposed S/D-MUX configuration of Figure 10 manages S/D and DOC functionalities by using only one serial transmission gate in the signal path, therefore effectively reducing introduced non-ideal effects.

D. REFERENCE SOURCES

The AFE's main components require several bias currents for the amplifier blocks (Section III-B) and specific measurement modes (Section II-B), as well as a 0.9 V (half-supply) common mode voltage. The on-chip reference generation is an typical analog task and adds subsequent static power consumption to the overall SoC.

Figure 11a shows a schematic diagram of VREF implemented as uncompensated voltage divider of six stacked diode-connected NMOS transistors. This architecture is inherently energy-efficient since the voltage drop V_{gs} across each diode is around 300 mV, biasing them in subthreshold region and realizing a high drain-source resistance r_{ds} [23].

Only a small shunt current I_{ds} of about 100 nA is allowed to flow. One major drawback of diode dividers is the inaccurate divider factor introduced by the body effect and bulk leakage currents. The proposed architecture takes advantage of the SOI technology and uses NMOS in isolated P-wells. The bulk terminal is connected to the source terminal compensating the body effect. The division factor is only dependent on device matching and can be optimized by sizing and statistical simulations.

The unregulated output V_{cm} is attached to the high-ohmic common-mode terminals of the SC amplifier blocks. In order to suppress ripples on V_{cm}, which are introduced by the switched operation of SC PGA and SC TIA, filter capacitors C_{fv} are placed on the cathodes. C_{fv} is realized as metal capacitor (in total around 35 pF) and placed above the active structure, therefore not increasing area. The regulated terminal OUT_{cm} is used for S2D operation. A driver circuit (DRV) realized as single-ended opamp in voltage buffer configuration delivers subsequent driver strength. Note that V_{cm} and OUT_{cm} intentionally follow half-supply. The signal common-mode is conveniently centered in the middle of the SAR ADC full-scale range.

A simplified block diagram of IREF is depicted in Figure 11b. In total, seven bias currents are required in the system and produced by a current source block including start-up circuitry (CS+Start). The bias currents are set to 100 nA, but not all seven currents are enabled at the same time in order to minimize the impact on overall AFE power consumption. Any unwanted shunt currents are avoided with the help of vectors $N_{EN}[2:0]$ (N enable) and $P_{EN}[2:0]$ (P enable), which control current switches [18]. They are connected to control signals $M_{oh3\text{-}0}$ from CH-MUX and S/D-MUX and from the digital part. While the lower currents controlled by $N_{EN}[2:0]$ are enabled or disabled, the upper currents controlled by $P_{EN}[2:0]$ are designated for the SC amplifiers and AND-gated with the signal ϕ_0'. They will therefore only flow in ϕ_0'-phase, following the ADC-driven duty-cycling. Ripple suppressing C_{fi} of around 20 pF are inserted here, too.

IV. DIGITAL CONTROLLER

A digital subsystem (CTRL) is used for communication with the surrounding external environment as well as for controlling all internal processes. As shown in Figure 12, this comprises an SPI-based external interface (SPI subsystem), the signal pre-processing (SPP) and various configuration registers (Cfg Regs) in addition to the actual control unit (main controller). The provided SPI interface allows operation with commercially available microcontrollers with minimal effort for on-board communication. Based on the actual 8 bit data transfer layer (Phy), a register protocol is implemented to provide an abstraction of the various functional units.

The Main Controller implements the following functions:

- Configuration of SPR delay $t_{SensRdy}$ and generation of SPR power and ready signals ($\overline{SensPwr[3:0]}$, SensRdy).
- Channel selection and configuration.

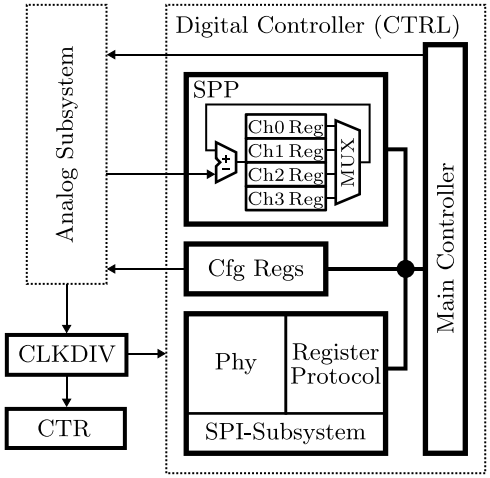

FIGURE 12. Detailed block diagram of digital controller.

- Generation of channel clocks signals ϕ_0–ϕ_2 depending on selected sample rate and resolution.
- Configuration of digital signal processing.

A. SIGNAL PRE-PROCESSING

The digital SPP contains accumulator registers for each channel which can be accessed from outside via SPI. Therefore, it does not only reduce data transfer, but allows further reduction of memory and computational power in a processing unit, e.g., an external microcontroller.

Using the accumulator registers, the SPP is able to perform the digital offset correction (DOC) of the actual ADC data. Two operating modes are supported.

1) Moving Average: To increase the signal-to-noise ratio [24], the incoming ADC values are summarized and averaged with a hardware-efficient programmable moving average filter. AVG $\in \{1, 8, 32, 128\}$ is the number of values (taps) to be summed up and averaged and is determined by a configuration register. AVG $= 1$ means no averaging.

$$\text{Data}_{\text{av}} = \frac{1}{\text{AVG}} \sum_{i=0}^{\text{AVG}} \text{Data}_i. \tag{5}$$

2) Digital Offset Correction: If DOC is activated, the summation is done with alternating sign. This also requires mirroring the swapped (SW logic high) and thus negative ADC values before summing them up. Note, that mirroring also depends on the selected accuracy.

$$\text{Data}_{\text{av,DOC}} = \frac{1}{\text{AVG}} \sum_{i=0}^{\text{AVG}-1} \begin{cases} \text{Data}_i, & i \text{ even} \\ 2^{13} - \text{Data}_i, & i \text{ odd} \end{cases}. \tag{6}$$

B. CLOCK DIVISION

The SAR ADC sample rate can be adjusted in four steps between 10 kS/s and 1.25 kS/s with CLKDIV. The final sample rate of the AFE is reduced by additional clock cycles, which are inserted in between the ADC conversions, in order to determine the next state of the CTRL. Therefore, a total sample rate of 1 to 7.5 kS/s is achievable per channel. With moving averaging, the sample rate drops accordingly. The manipulation of sample rate and number of averaged samples in fact shapes the frequency response of moving averaging filter, which must be considered when processing the incoming data.

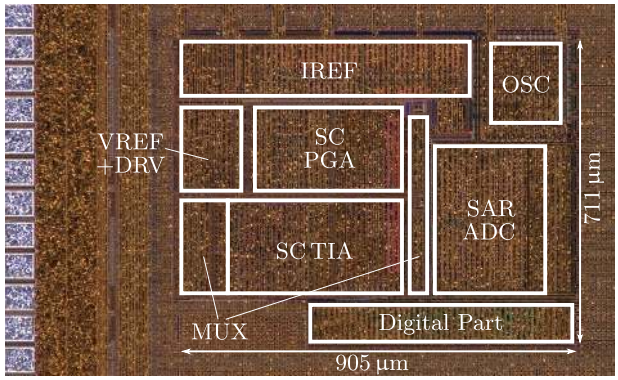

FIGURE 13. Chip micrograph of 180 nm AFE testchip.

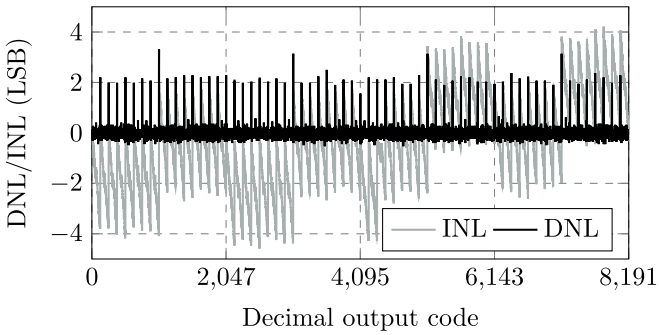

FIGURE 14. Measured differential and integral non-linearity of stand-alone SAR ADC output data, obtained at full 13 bit resolution.

V. MEASUREMENT RESULTS

Thirty chip samples were fabricated in 180 nm SOI technology and characterized within laboratory environment. A micrograph of the AFE core is shown in Figure 13. The total active area occupies 0.64 mm^2, where SAR ADC (14.9%), PGA (23.8%), TIA (14.9%) and current reference (15.6%) are the main contributors. With 0.06 mm^2, the digital part requires only 9% of the active area. Due to the high number of test access pads, the layout is placed in a 3.6 mm^2 pad area.

Static and dynamic errors of the stand-alone SAR ADC are extracted. The differential non-lineratiy (DNL) and integral non-linearity (INL) are shown in Figure 14 for 13 bit resolution setting and do not exceed $\{-0.5, 3.3\}$ LSB and $\{-4.6, 4.2\}$ LSB, respectively. The result indicates inaccuracies between measured and post-layout extracted parasitic elements associated with the split capacitor. The ADC linearity can be further optimized by calibration or iterative tweaking of the split capacitor in a future ADC version. A

TABLE 3. Performance of the proposed AFE in comparison to state-of-the-art AFEs and SAR ADCs.

	This Work, 2021	[9], 2021	[10], 2020	[13], 2019	[6], 2019	[8], 2018	[17], 2017	[7], 2017
General								
Analog Supply (V)	1.8	1.8	2	0.6	1	0.6	1.2	0.3
Tech. (nm)	180	180	130	65	180	40	65	65
Application	IoT	IoT	Bio	IoT	Bio	Bio	Bio	Bio
Total Sample Rate (kS/s)	1 to 7.5	0.1	1	10 to 100	N/A	20 to 400	0.4	1.0
Total Bandwidth (kHz)	0.01 to 3.8	0.0001 to 0.05	0.04 to to 0.32	N/A	N/A	0.001 to 128	N/A	0.02 to 0.42
Area (mm^2)	0.64	1.81	0.6	0.08	0.23	1	0.13[2]	0.22
Average Power (µW)	1.8[2] / 8.8	160.5[2] / 425 to 500	1.3[2] / 6.3	0.0003 to 0.6	2[2] / 5.4	0.24[2] / 3.8	0.1[2]	0.0038
Support commerical IoT sensors? (e. g. Table I)	Yes	Yes[3]	No[4]	No[4]	No[4]	No[4]	No[4]	No[4]
ADC								
ADC Sample rate (kS/s)	1.25 to 10	N/A	1	10 to 100	N/A	20 to 400	0.4	1.0
Resolution (bit)	6 to 13	SAR: 8 to 12	8	10	N/A	13	10	8
ENOB (bit)	10.6	8.5 to 12.9	7.9	N/A	7	9.7	9.6	7
FoM_{ADC} (fJ/st.)	116.0	N/A	5.2e3	31 to 150	14.4	322.0	15.6	34.8
Preamplifier								
Prog. Gain?	Yes	No	Yes	No	Yes	Yes	N/A	No
Gain (dB)	-6 to 12	N/A	43 to 55	N/A	N/A	20 to 30	N/A	40
Preamp Power (µW)	3.9	28.6 to 107.8	1.6	N/A	N/A	N/A	N/A	0.0009

[2] stand-alone ADC excluding preamplifier

[3] electrochemical sensors and chemo-resistive sensors

[4] Table I bandwidth and/or voltage range not achieved

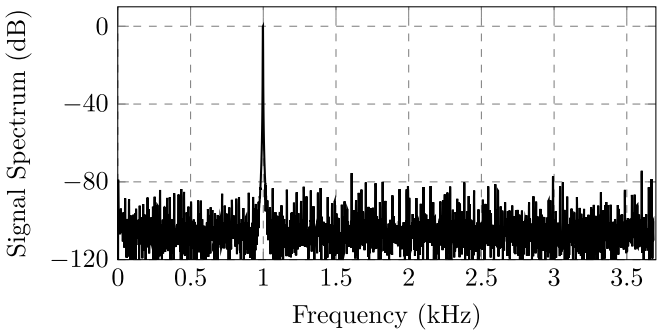

FIGURE 15. Measured FFT output spectrum of stand-alone SAR ADC, obtained at full 13 bit resolution setting, with input sinusoidal frequency of 1 kHz.

gain error of 4.33 % is achieved, which is introduced by the parasitic capacitive divider between CDAC and comparator (refer to Figure 4). The DOC effectively reduces the offset below the measurement resolution of 100 µV. Dynamic measurements are carried out with a sinusoidial signal source with full-scale amplitude at various frequencies. Since the jitter of the on-chip oscillator can reduce the AFE's accuracy significantly, the measurement is carried out with an external clock source. The output spectrum is obtained with FFT, which is shown in Figure 15 for an 1 kHz input. The peak differential ENOB is calculated from spectral signal-to-noise and distortion ratio to 10.6 bit, at maximum ADC resolution setting (9.6 bit single-ended).

The measured power consumption of the AFE in voltage measurement mode stays well below 8.8 µW. SAR ADC and PGA consume 1.8 µW and 3.9 µW, respectively. The value of the ADC includes here as well the complex digital controller. Without the ADC-driven duty-cycling, the PGA power-consumption is 50.9 µW. The duty-cycling shows therefore an effective power reduction by 92%. The power consumption in power-down mode is 61 nW, enabling extraordinary long sensor node lifetime in sleep mode.

Multi-channel measurements with the AFE are performed within an example environmental monitoring setup including single-ended sensors 1, 2 and 3 of Table 1. The setup resembles an environmental multi-sensor node gathering data from ambient temperature, light and carbon monoxide gas sensors (similar to [20]). Channel mismatch and crosstalk showed sufficiently low in the measurements. In standard configuration, i. e. no SPR, always-on sensor components result in a steady power consumption of 73 µW and 45.8 µW for a wake-up period t_{wu} of 1 s and 5 s, respectively. With proposed SPR, the power consumption drops by 20% to 59 µW, at $t_{wu} = 1$ s. At $t_{wu} = 5$ s, the saving is 73%. To illustrate that, Figure 16 shows a measured waveform of the SPR with one sensor. Configuration via SPI, wake up, measurement start after a delay $t_{SensRdy} = 4$ ms, averaging, data read via SPI, and sleep mode can be observed.

Table 3 lists various published AFEs from the biomedical and the IoT field and single SAR ADCs in comparison to the proposed AFE. Competitive results in terms of power consumption, sample rate, ENOB and bandwidth are achieved. While partially showing better FoM_{ADC} than the proposed work, most concurrent designs of Table 3 do not allow read-out of commercial IoT sensors as listed e. g. in Table 1,

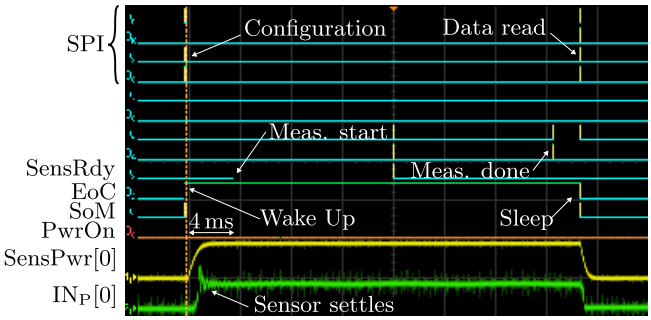

FIGURE 16. Measured waveforms of SPR with one sensor (x-axis: 500 ms/div, y-axis: 1 V/div).

either due to their low supply voltages of 1.2 V and below, or due their limited bandwidths below 1 kHz. For example, [6] and [7] are AFEs optimized only for dedicated biomedical (partially proprietary) sensor hardware, explaining their better efficiency. Other than that, [10] and [13] show versatile solutions which could potentially handle sensors from Table 1, but the adaption of voltage and sample rate would require substantial design changes, trade-offs and potentially higher power consumption. The AFE from [9] offers a comparable level of functionality and sensor adaptability, but shows almost fifty times higher power consumption than the proposed AFE.

VI. CONCLUSION

This work introduces a novel analog frontend for ultra-low power environmental sensing applications, with two major challenges. First, the AFE is aimed for different possible IoT-applications. It must support a broad variety of sensor hardware and signal types, voltage levels, etc, and deliver extraordinary flexibility. Second, the AFE must achieve ultra-low power consumption, while maintaining other state-of-the-art performances. Based on a survey of commercially available IoT sensor hardware, specifications are derived and a viable solution is developed, implemented, measured and the results are discussed.

A total AFE power consumption of only 8.8 µW is achieved by optimizing the effciency on multiple design levels, starting from system considerations, block level design and transistor sizing methods. The combination of SAR ADC with modified switching scheme, SC amplifiers, low-power references, digital signal pre-processing and duty-cycling methods, achieves good performance in comparison to other published AFEs. The support of different sensor in a complete SN is improved by a novel sensor power regime technique. The channel-wise configurable signal processing offers a flexible solution for fast adaption to different sensors and reuse in various applications. This ensures market acceptance by reducing costly IC redesign and benefits price reduction and dissemination of long-life electronic hardware.

The proposed AFE is suitable to operate in a long-life autonomous environmental sensor node, which is currently under development. Results are expected in 2021.

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