Hindawi Publishing Corporation VLSI Design Volume 2012, Article ID 549768, 2 pages doi:10.1155/2012/549768

Editorial

Flexible Radio Design: Trends and Challenges in Digital Baseband Implementation

Guido Masera, 1 Amer Baghdadi, 2 Frank Kienle, 3 and Christophe Moy4

- ¹ Department of Electronics and Telecommunications, Politecnico di Torino, 10129 Torino, Italy
- ² Telecom Bretagne/Lab-STICC, Technopôle Brest-Iroise, CS 83818, 29238 Brest, France
- ³ Microelectronics System Design, Technical University of Kaiserslautern, Postfach 3049, 67653 Kaiserslautern, Germany
- ⁴ Supélec/IETR, Campus de Rennes, Avenue de la Boulaie, CS 47601, 35576 Cesson-Sévigné Cedex, France

Correspondence should be addressed to Guido Masera, guido.masera@polito.it

Received 1 August 2012; Accepted 1 August 2012

Copyright © 2012 Guido Masera et al. This is an open access article distributed under the Creative Commons Attribution License, which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

Fourth-generation communications systems call for a high amount of computational power due to multiantenna and multimode features. The level of flexibility required is growing rapidly with the number of modes to be supported for a single protocol and the number of protocols to be supported by a single receiver. Such high level of flexibility becomes a key feature of new and legacy radio applications in many domains (military radio, broadcast systems, aeronautic communications, etc.), which call for adopting a software-defined radio (SDR) approach, or even for incorporating additional adaptive capabilities, such as suggested by cognitive radio (CR) research.

In general, the design of flexible base-band platforms raises several critical problems, including the high level of required performance, the dissipated power, and the reconfiguration process itself. Several alternatives have been partially explored to implement flexible base-band building blocks and a lot of research is still required to bring efficiency into programmable platforms.

The design of flexible channel decoders for low density parity check codes is addressed in two papers. M. Awais and C. Condo provide a rich overview of state-of-the-art decoders able to deal with multiple LDPC codes adopted in communication standards such as DVB-S2, IEEE 802.11n (WiFi), IEEE 802.3an (10GBASE-T), and IEEE 802.16e (WiMAX). Similarly, P. Schläfer et al. presents a systematic investigation of the design space for flexible multigigabit LDPC applications, such as ultrawideband communications (WiMedia), wireless personal area networks (IEEE

802.15.3c), and gigabit wireless local area networks (IEEE 802.11ad). Both papers give extensive comparisons among already available results and also introduce new implementation examples proposed by the authors. Interestingly, from the reading of the two papers, it can be understood that incorporation of flexibility in LDPC decoding architectures introduces different constraints in medium throughput and multigigabit throughput applications.

The use of two popular soft-input soft-output detectors for multiple-input multiple-output (MIMO) communications is analysed by C. Gimmler-Dumont et al. in the context of both open- and closed-loop architectures. A depth-first sphere detector and a breadth-first fixed effort detector are deeply studied and compared in terms of communications performance and implementation complexity. The work shows that the fixed effort detector is advantageous in a throughput centric scenario, where very high-processing speed has to be ensured at moderate communications performance. On the contrary, the sphere detector offers much higher efficiency in a communication centric scenario, where very low-error rate is required.

Two further papers of this selection deal with the digital and analog front-ends, respectively. In particular, K. Grati et al. propose efficient implementations for FIR decimation filters to be used in multistandard receiver designs. Polyphase decomposition has been shown to provide a relevant reduction in the dissipated dynamic power with respect to the direct form implementation and this advantage is obtained at the cost of an increased static power consumption.

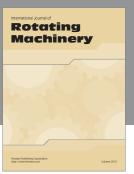
2 VLSI Design

Finally, an overview of the key technology challenges in the development of RF front-end, and analog-to-digital and digital-to-analog interfaces for cognitive radio system is presented by V. T. Nguyen et al.

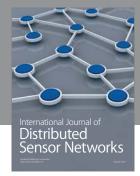
Guido Masera Amer Baghdadi Frank Kienle Christophe Moy

















Submit your manuscripts at http://www.hindawi.com





