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Flexible Zinc-Tin Oxide Thin Film Transistors Operating at 1 kV for Integrated Switching of Dielectric Elastomer Actuators Arrays

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Abstract:

Flexible high-voltage thin-film transistors (HVTFTs) operating at more than 1 kV are integrated with compliant dielectric elastomer actuators (DEA) to create a flexible array of 16 independent actuators. To allow for high-voltage operation, the HVTFT implements a zinc tin oxide channel, a thick dielectric stack, and an offset gate. At a source-drain bias of 1 kV, the HVTFT has a 20 µA on-current at a gate voltage bias of 30V. Their electrical characteristics enable the switching of DEAs which require drive voltages of over one kilovolt, making control of an array simpler in comparison to the use of external high-voltage switching. These HVTFTs were integrated in a flexible haptic display consisting of a 4x4 matrix of DEAs and HVTFTs. Using a single 1.4 kV supply, each DEA is independently switched by its associated HVTFT, requiring only a 30 V gate voltage for full DEA deflection. The 4x4 display operates well even when bent to a 5 mm radius of curvature. By enabling DEA switching at low voltages, flexible metal-oxide HVTFTs enable complex flexible systems with dozens to hundreds of independent DEAs for applications in haptics, Braille displays, and soft robotics.

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Main text:

Soft robotic systems offer many advantages over more conventional systems made of rigid elements: they can mechanically conform to a great variety of configurations, adapt to different scenarios, are intrinsically safe to handle for humans, and enable extremely large degree of freedom operation. Systems based on soft actuators can be used in a broad range of applications across different length scales, including compliant grippers[1–4] and soft locomotion,[1,5] Braille displays,[5,6] biomedical applications,[7,8] and flexible optics.[9]

To realize their full potential, soft systems require numerous independent actuators. For instance, a gripper needs several fingers, a swimming robot needs many actuators for fine control of propulsion, and a large Braille display needs to switch thousands of pins. A great diversity of soft actuators for soft robotics have been demonstrated.[10] Integrated actuators are essential to avoid need of external, bulky motors or pneumatic sources. Among soft actuators, dielectric elastomer actuators,[11] (DEAs) consisting of an elastomer membrane sandwiched between compliant electrodes, possess many appealing properties: they can generate extremely high strain (over 400% in-plane strain has been reported),[12] they are fast (< 1 ms),[9] consume negligible power when holding any fixed position, and can be scaled down to the µm scale.[13] DEAs have been demonstrated as the key building blocks for numerous applications including grippers,[1–3] haptic displays,[6] deformable bio-reactors,[14] tunable optics[9,15] as reviewed in[13,16].

DEAs are electrostatic devices that with actuation voltages generally greater than 1 kV, which implies bulky external control circuits. This makes it difficult – if not impossible – to develop complex soft machines driven by DEAs for applications that require a large number of independent actuators, such as Braille or haptic display, as one would need. Indeed, if DEAs enable a compact and efficient design, the driving electronics would be bulky and cost-prohibitive.

In this paper, we demonstrate the integration of 16 flexible 1 kV transistors to individually control a matrix of 16 DEAs using only one single high voltage power supply. The novelty of our method lies in the fabrication and integration of 1 kV metal-oxide thin-film transistors (TFTs), switching at 30 V gate voltage, each driving one DEA in a 4x4 array. The addressing of the matrix of 1 kV DEAs is then done using only 30 V signals. The integration of flexible high-voltage TFT (HVTFT) with DEAs in a flexible system solves the problem of compact control driving electronics. The HVTFTs can be directly processed on the frame holding the DEA, replacing bulky external switches, thus enabling very compact integration.

A TFT is a field effect transistor with a thin-film semiconducting channel.[17] The key advantage of TFTs over silicon MOS technology is that they can be fabricated on insulating substrates, including flexible polymer substrates. The insulating substrate eliminates substrate current leakage, a critical aspect needed for high-voltage operation.

Fabricating a flexible kV thin-film transistor that can switch with sub 50 V gate voltage is far from trivial given the numerous high-voltage specific challenges affecting the dielectric and the semiconductor channel. The gate dielectric must be flexible and withstand high voltages. The choice of the semiconductor material is critical because high electric fields usually degrade the conduction properties of organic and polycrystalline semiconductors. This issue has limited the drain-source voltage of both those two technologies to below 400 V.[18,19] For drain-source voltages greater than 100 V, organic HVTFTs exhibit very high parasitic space charge limiting current and channel length modulation, degrading transistor operation.[19] Polysilicon HVTFTs high voltage operation is very sensitive to grain boundaries: the polycrystalline channel self-heats under a high electric field, leading to destructive kink effects at high-voltage.[18,20] Amorphous silicon semiconductor technologies are promising for high voltage operation,[21–23] and have been demonstrated up to 800 V,[24] but are limited by low on-currents in the µA range, thus limiting switching speed when they are used to control capacitive loads, such as DEAs.

We report here HVTFTs based on amorphous metal-oxide (MOx) semiconductor technology, namely zinc tin oxide (ZTO), a novel approach for TFTs operating with drain-source voltage higher than 500 V. To date, MOx TFTs have been reported for low-voltage applications (< 5 V) such as flexible transparent displays, optoelectronics, biosensors and biomedical implants.[25–28] Our method enables metal oxide TFTs operation at over 1 kV. Unlike polysilicon, the amorphous phase prevents grain-boundary effects, and MOx TFTs are not sensitive to space-charge limited currents as organic TFTs are.[25,29] The electronic transport properties of amorphous MOx TFTs, such as mobility and resistivity, are a strong function of the cation stoichiometry of the amorphous thin-film.[25] MOx semiconductor properties are thus far more tunable than amorphous silicon.[30–32] Many MOx TFTs use indium-based compounds such as IGZO. Indium is however expensive, rare, and toxic.[33]With the longer-term aim of printing HVTFTs on the DEA's flexible frame, we selected a solution processed zinc-tin oxide (ZTO) as the HVTFT semiconductor. ZTO is composed of only 2 metallic cations. Varying the stoichiometry can be used to tune the electronic properties.[32,34–36]

To illustrate how HVTFTs the benefit of using HVTFTs for addressing large matrices of independent DEAs, we fabricated a haptic display consisting of a matrix of 4x4 out-of-plane DEAs[37] operating at 1 kV, each driven by an integrated HVTFT controlled by a 30 V gate signal, and operating as 1 kV switch (**Figure 1)**. The entire matrix is biased by a single high-voltage supply. This demonstration of low-voltage control of a matrix of kV actuators paves the way for DEAs to be used in applications where many degrees of freedom are needed such as in soft robotics, haptic displays and flexible Braille displays. The haptic display operation is shown in the **video S1**.

The circuit architecture is an N-type inverter consisting of the HVTFT, a pull-up resistor and the DEA at the output node (**figure 1f)**. The use of a passive bias resistor avoids referencing a control signal to the high-voltage signal line as would be the case if using a p-type TFT in a complementary circuit architecture. When the HVTFT is off (gate voltage of 0 V), charges

accumulate on the DEA electrodes, and the DEA actuates, deflecting out-of-plane. When the HVTFT is on (gate voltage of 30 V), the charges are drained across the TFT channel, and the DEA goes back to its initial unpowered position. DEAs and TFTs are interconnected using a flexible PCB. A cross-section of the TFT is given **figure 1e**. To limit effects of the high-electric field on the HVTFT, we used a channel 500 µm length for a 5 mm width (W/L = 10). High-field effects are similar to short-channel effects and can be decreased by increasing the channel length.[38] The substrate was coated with 20 nm Al_2O_3 for back-side passivation and for synthesizing the semiconductor on an insulating metal-oxide layer rather than on the polymer substrate. The zinc-tin oxide thin-film was spin-coated and synthesized using a 450 °C sol-gel process as described in[39] on heat-resistant polyimide. The sol-gel process provides a 45 nm porous ZTO thin-film (**TEM cross-section figure S2**) with high resistivity (45 Ω.m), which is critical to ensure low off-state current at kV operation.

To avoid dielectric breakdown at 1 kV, we used a bilayer dielectric consisting of 100 nm atomic-layer deposited Al_2O_3 (E_{bd} = 700 V/µm) and of 1 µm flexible Parylene-C (E_{bd} = 300 V/µm). We used an offset gate geometry, as this geometry has been shown to increase the maximum operation voltage of TFTs by several hundreds of volts.[18,19,21–24] The gate electrode was offset from the drain by 150 µm. With the implementation of these two material and geometrical modifications, the HVTFT breakdown voltage reached 1.1 kV, the highest breakdown voltage reported for a TFT up to date. The HVTFT uses a top-gate configuration, which makes for easier alignment of the offset gate than a bottom-gate one. Furthermore, with a top-gate configuration, we can deposit the Parylene after the 450 °C ZTO sol-gel process.

The TFT output and transfer characteristics, plotted in **figure 2a,** demonstrate successful operation at 1 kV. The gate-source voltage of the transfer characteristics was swept forwards and backwards from 0 to 100 V. The on-off current ratio for a 1 kV drain-source voltage is 50, with an on-current of 100 µA at V_g = 100 V. The saturation mobility of the device is 0.3 cm^2/Vs. Unlike lower voltage TFTs, the HVTFT has an almost linear dependence between the saturation

current and the gate bias. This is evidence of the saturation of the carrier velocity, which is a trigger for high electric field effects. For V_g > 30 Volts, the HVTFT's current–drain voltage dependency becomes quadratic in the pre-saturation region. This quadratic behavior can be attributed to space-charge limited current.[40] However, in the saturation regime, the drain current does not show any evidence of space-charge-limited current. As for amorphous silicon and organic HVTFTs, we can assume that the space charge-limited current occurs in the offset region until channel pinch-off[19,22]. The HVTFT has a drain-source onset voltage shift of 150 V. This shift is a function of the maximum applied drain and gate voltage; a similar effect has been reported for poly-silicon, a-silicon and organic HVTFT technologies.[18,19,22]. The drain-voltage shift appears only when the applied drain voltage exceeds 500 V. One hypothesis is that the shift is due to fringing fields between the edges of the gate electrode and the channel at the offset position.[19,22] These fringing fields damage the semiconductor, creating traps at the interface with the dielectric. There may be an increase of the contact resistance due to the non-gated offset region. The drain-source onset voltage shifts the minimal voltage at the DEA node in the N-type invertor circuit from 150 V to 400 V at V_g = 30 V (In the output characteristics, this corresponds to the transition between the linear and the saturation region of the curve). The effect of this shift is demonstrated on the inverted characteristics in **figure 2d.** The transfer characteristics shows no hysteretic behavior indicating the absence of charge trapping despite the high-voltage bias. However, the off-current is high, between 2 µA and 3 µA. A likely explanation is the intrinsic conduction in the zinc-tin oxide thin-film, which is not negligible at 1 kV. Another hypothesis is the formation of a back-channel leading to higher off-current.[42]

For the haptic display, we designed a DEA operating at 1 kV that could move out of plane by at least 250 µm, a displacement consistent with haptic applications.[43] Each DEA consists of a 4 mm diameter circular membrane, 17 µm thick, with compliant electrodes on each side. To determine the DEA parameters and backpressure, we used a numerical model based on the DEA

strain-voltage relation (see **figure S3)**.[37,41] The swing reaches a maximum 1.5 µm/V before DEA breakdown with direct high-voltage source control.

Using the HVTFT to drive the DEA with the N-type inverter structure presented **figure 1f**, for constant 1.4 kV bias voltage we characterized the DEA deflection as a function of TFT gate voltage curve. The bias resistance's value is 200 MΩ. We swept the gate bias voltage from 0 V and 50 V and measured the DEA out-of-plane deflection. At 0 V gate voltage, the DEA reaches 320 µm deflection **(figure 2d)**. In the 0-30 V interval, the actuation varies showing a swing of 15 µm/V, 10 times higher than the deflection swing with direct HV-source control as shown in **figure S3**. The time response of the system is 50 ms. It is limited by the RC constant of the bias resistor and the DEA. The system can sustain a drain bias stress of 1 kV with a gate voltage of 0 V over 10,000 seconds after which the current starts to shift.

The maximum DEA strain depends on the potential division between the bias resistor and the HVTFT. For a high DEA voltage, we aim at a low HVTFT off-current. The DEA minimum strain is determined by the voltage at the transition between the linear and the saturation region (400 V at 30 V gate voltage) in the on-state. To obtain the smallest minimum strain we have to target a high on current to avoid voltage division, a steep slope in the saturation region, and limit the onset shift seen in **figure 2a**. A high on-current means that the TFT has to have a high transconductance and a steep slope means a low channel on-resistance. However, a major challenge when increasing the operating voltage of a HVTFT is the trade-off between the operation voltage and the TFT trans- and on-conductance. To quantify this, we compared our HVTFT with a low-voltage TFT (LVTFT) made using a similar process flow. The LVTFT is identical to the HVTFT except that a) it does not have Parylene-C layer and b) has a fully overlapping gate (**See figure S4**). We compared it with a HVTFT with the 1 µm Parylene layer, and offset the gate from 0 to 150 µm with a 50 µm increment. We extracted the breakdown voltage from the output characteristics (**figure 3a**). To quantify the impact of the offset gate geometry and the dielectric material on the transconductance, we plotted the product between

the saturation mobility and the dielectric capacitance per unit of area (**figure 3b)**. The channel on-resistance was extracted from the linear region of the output characteristics (**figure 3c**). The addition of a 1 µm Parylene results in a 400 V increase of the breakdown voltage, as well as a decrease by one order of magnitude of the transconductance and on-state conductance. The 150 µm offset gate increases the breakdown voltage by 700 V, while increasing by 5 times the on-resistance and decreasing by almost 3 times the transconductance. However, the decrease of transconductance with increasing offset gate is much stronger for an offset gate length > 100 µm.

Finally, we characterized the effect of static bending on the display **(figure 4a-d)**. The samples were bent in directions parallel and perpendicular to the channel, with similar results obtained for both directions. The HVTFT output and transfer characteristics for the perpendicular case are plotted in **figure 4c and 4d** for 3 different radii of curvature. The TFT can be bent to a radius of curvature of 2.5 mm. The TFT is not affected by bending at high drain voltage as shown on the transfer characteristics (**figure 4d)**. Stability under bending at high-voltage had been observed on organic technologies and was attributed to the high-bias voltage assisting charge release from the traps generated by bending.[19] For bending radii lower than 2 mm, our device fails. The HVTFT is thus suitable for operations down to a 2.5 mm bending radius, which is amply sufficient for nearly all flexible DEA applications.

To reach the 2.34 mm pitch of a Braille display, the HVTFT and the DEA both need to be scaled down, which raises fundamental and processing challenges. Reducing the HVTFT channel width and length worsens high electric field effects. Simply decreasing the DEA diameter leads to reduced force and vertical displacement, and needs to be compensated for instance by using multi-layer DEAs.

In summary, we designed, fabricated, and integrated the first ZTO HVTFTs operating at 1 kV, and used them to drive DEAs, allowing switching DEAs with only 30 V gate voltage. The HVTFTs exhibit an unprecedented breakdown voltage of 1.1 kV and are robust, operating reliably down to a radius of curvature of 2.5 mm. Stretchable and soft systems with many DEAs

were previously unthinkable, as they would have required one dedicated HV supply or one dedicated HV switch for each DEA. Our successful integration of DEAs and flexible HVTFTs paves the way towards complex soft and compliant systems where full advantage can be taken of the excellent properties of DEAs for application where a large number of independent actuators are needed, such as Braille displays, microfluidic circuits, soft robotics, and artificial skins.

Experimental section

Fabrication of the HVTFT: The fabrication of the HVTFTs is described in **figure S5**. The semiconductor precursor solution is composed of 0.2 M of a solute mix of zinc chloride (99 % purity, Sigma-Aldrich) and tin chloride (99 % purity, Sigma-Aldrich) to achieve a 2:1 ZTO thin-film, mixed in acetonitrile (35 % volume, Sigma-Aldrich) and ethylene glycol (65 % volume, Sigma-Aldrich) for 24 h in air at room temperature. We used a 10 cm wide heat-resistant polyimide (Goodfellow Upilex 50 µm) wafer as substrate. We coated it with a 20 nm thick layer of Al_2O_3 using atomic layer deposition (200 °C, TMA and H_2O as the precursor, Beneq TFS200). We spin-coated the semiconductor chloride precursors on the foil at 2000 rpm. The thin-film was then dried at 120 °C for 1 hour in air. The oxide was synthesized by curing at 450 °C for 1 hour in air. TEM and EDS spectra validate the formation a 45 nm chloride-free zinc-tin oxide thin-film (**see figure S2**). To define the source and drain electrodes, we evaporated a 200 nm thick aluminum film through a steel shadow masks defining 4x4 TFTs arrays on the foil (e-beam evaporator Alliance Concept EVA 760). We then coated the semiconductor with a 100 nm conformal layer of Al_2O_3 (200 °C, TMA and H_2O as the precursor, Beneq TFS200) for passivation and optimal dielectric-semiconductor interface. On top, we deposited 1 µm thick Parylene-C by chemical vapor deposition (COMELEC C-30-S). To define the gate, we evaporated 200 nm thick aluminum electrodes with a 5 nm chromium adhesion layer through an aligned shadow mask (e-beam evaporator Alliance Concept EVA 760). Ultimately, the device was cured for 1 hour at 150 °C in air to activate the channel.[44] In order

to open the source and drain contacts, we engraved the Parylene and the alumina layer using a CO_2 laser (Trotec speedy 300). The TFTs were then diced in 35 mm x 35 mm squares resulting in a 4x4 TFT array with a CO_2 laser (Trotec speedy 300).

Fabrication of the DEA: The fabrication of the DEAs with cross-sectional view is described in **figure S6**. It follows the protocol described in[45]. The DEA membrane was made of PDMS (Silicone Dow Corning Sylgard 186, 10:1 (monomer:crosslinker). We diluted the solute (35% mass) in OS-2 (Dow Corning). The uncured PDMS was casted with a film applicator coater (Zehntner ZAA2300) on a polyethylene terephthalate (PET) foil coated with a sacrificial polyacrylic acide (PAA) layer to obtain a 17 µm thick membrane. The film was annealed at 80 °C for 1 hour in air to crosslink. The PET substrate was removed by dissolving the PAA sacrificial layer in hot deionized water. The 4x4 DEA electrodes top layer were transfer printed on both sides of the membrane using a pad-printer and annealed for 1 hour at 80 °C to cross-link. Holes aligned to the position of the source, drain, gate of the TFT and back DEA electrodes were machined with a CO_2 laser (Trotec speedy 300) in the DEA membrane.

Assembly: An exploded view of the assembly is shown in **figure S7**. The TFT was attached to a 50 µm polyimide foil coated with a dry adhesive film (Adhesive Research AR-clear 8932EE). A stencil mask from a dry adhesive film (Adhesive Research AR-clear 8932EE), patterned with a CO_2 laser (Trotec speedy 300) was laminated on it. Conductive silver glue (Henkel-CE3103WLV) was stenciled through the dry adhesive mask to define source, drain, gate and backside DEA electrode contacts. 5mm diameter holes were laser drilled between each TFT with an 8 mm pitch to suspend the actuators. The DEAs were then aligned and stuck on the TFTs layer. The assembly was cured for 3 hours at 80 °C. An ultimate stencil mask was made in dry adhesive to make via, that connect the source, drain, gate of the TFT, the top and back electrodes of the DEA. The connection was done thanks to a flexible PCB made in polyimide. Silver glue (Henkel-CE3103WLV) was stenciled to make the contact. The PCB was aligned and laminated on the assembly. The whole device was annealed at 80 °C for 3 hours under air.

The bias resistors and the connectors were ultimately soldered on the PCB providing the display shown **figure 1**. In the future, the bias resistor could be integrated directly in the flexible TFT fabrication process for higher integration, for instance by using the ZTO as the resistive material between aluminum electrodes. For safe use as a haptic display, a user must be protected from the high-voltage. In addition to ensuring that the DEA electrode facing the user is grounded, an additional flexible passivation layer to ensure sufficient electrical insulation between the DEA and the finger such as in[3] could to be added, or hydrostatic coupling could be implemented as in [46].

DEA measurements: The assembly was mounted on a 3d-printed flexible chamber to provide a 50 mbar back-pressure for out-of-plane expansion. The deflection of the DEA was measured using a laser-displacement sensor (Keyence, LK-HD 500) pointed on the highest point of the DEA bubble.

TFT characteristics measurement: The TFT output and transfer characteristics were measured by probing the TFT three terminals on a characterization setup controlled with a controlled 0-2 kV (drain) and a 0-200 V (gate) voltage supplies (respectively EMCO-CA20P and EMCO-CA02P). In the case of the transfer characteristic, the gate voltage was ramped up and down. The measurements of the TFT under static bending were achieved by probing the devices on cylinders with radii of curvature from 5 mm to 1 mm.

DEA-TFT characteristics measurements: Mounted together, the deflection of the DEA was measured using a laser-displacement sensor pointed on the highest point of the DEA bubble, while the driving voltage was applied with the 0-2 kV regulated power supply. Then, the voltage of the gate was ramped using the 0-200V high-voltage unit.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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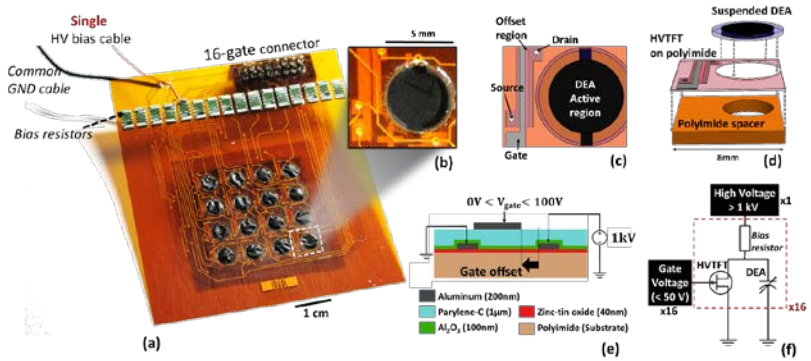

Figure 1. (a) Flexible haptic display consisting of a matrix of 4x4 out-of-plane DEAs driven by a matrix of 4x4 High-Voltage Thin Film Transistors (HVTFTs), driven by a single 1.4 kV supply. Each DEA is operated by applying 0V or 30V to the gate of the corresponding HVTFT. (b) One cell of the display showing the DEA connected to HVTFT using the flexible PCB. (c) Top view of a single the cell showing the 4 mm diameter DEA and the HVTFT. (d) Stack integrating DEA and HVTFT. The flex-PCB (not shown) is bonded on this stack for interconnections. (e) Cross-section of one HVTFT, in a top-gate configuration. To increase the drain-gate breakdown voltage to over 1 kV, we use a thick dielectric bilayer of Al_2O_3 and Parylene-C, and implement an asymmetric geometry with an offset gate. (f) Electrical circuit for a single cell. An N-type inverter circuit topology with a pull-up bias resistor is used, so that the HVTFT controls the charge on the DEA. This architecture enables a large number of DEAs to be individually addressed using only a single high-voltage power cable. A movie showing the device in operation can be found in **video S1**.

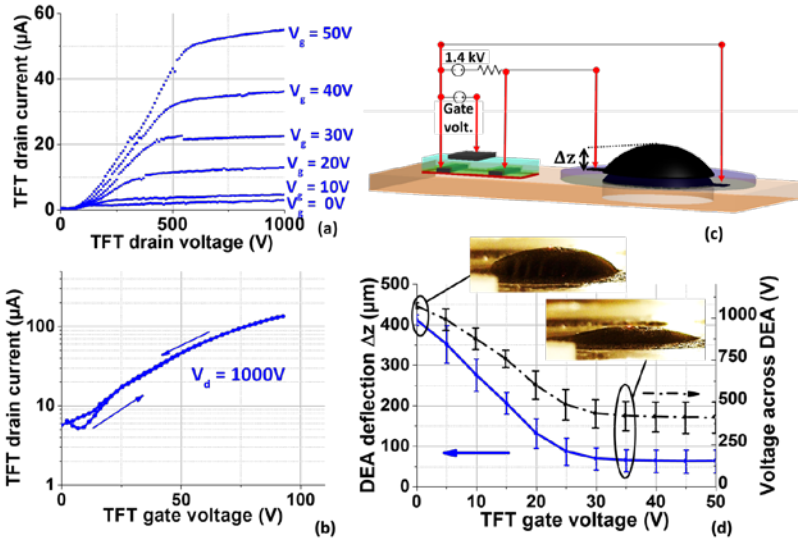

Figure 2. (a) and (b) HVTFT output (I_d vs. V_d) and transfer characteristics (I_d vs V_g) at 1 kV source-drain voltage. (c) Schematic diagram of a DEA controlled by a HVTFT. At a constant 1.4 kV bias voltage, the out-of-plane deflection Δz of the DEA is controlled by setting the TFT gate voltage. (d) DEA out-of-plane deflection and voltage across the DEAvs. HVTFT gate voltage with a constant 1.4 kV bias voltage. This plot demonstrates control of 1 kV applied on the DEA using only a 30 V gate signal. The DEA deflects by 15 μm per 1 V of gate voltage, which is 10 times higher than under direct high-voltage source control. The 0 μm deflection point is referenced when the DEA is under 0 V direct bias as shown in figure S3.

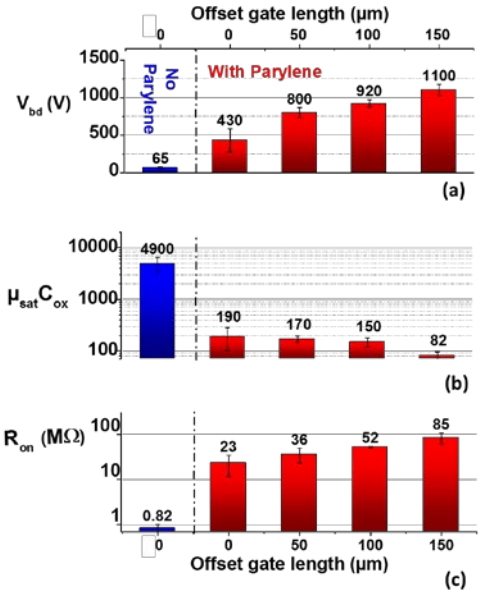

Figure 3. (a) Breakdown voltage of the HVTFT vs. offset gate length without (blue bars) and with (red bars) Parylene in the dielectric stack. (b) Transconductance constant $K_n = \mu_{sat}C_{ox}$ in (pF/V.s) vs. offset gate length. (c) Channel resistance measured at V_g = 30 V vs offset gate length. The trends between the three bar charts highlight a trade-off between achieving high breakdown voltage, and obtaining high trans- and on-conductance.

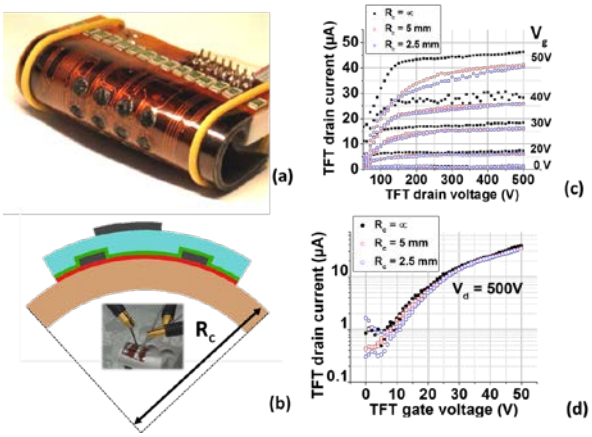

Figure 4. Photograph of the 4x4 haptic display under bending. Operation of the device bent to a 5 mm radius of curvature is shown in the video in **S1**. (b) Geometry and picture of the HVTFT at a radius of curvature R_c. (c) Output characteristics of HVTFT when flat ($R_c = \infty$) and under static bending ($R_c = 5$ mm) and ($R_c = 2.5$ mm). (d) Transfer characteristics of HVTFT when flat ($R_c = \infty$) and under static bending, ($R_c = 5$ mm) and ($R_c = 2.5$ mm).

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Supporting Information

Flexible Zinc-Tin Oxide Thin Film Transistors Operating at 1 kV for Integrated Switching of Dielectric Elastomer Actuators Arrays

*Alexis Marette, Alexandre Poulin, Nadine Besse, Samuel Rosset, Danick Briand, and Herbert Shea**

Video S1 – Video showing operation of the 4x4 display, key fabrication steps, and operation when bent to a 5 mm radius of curvature

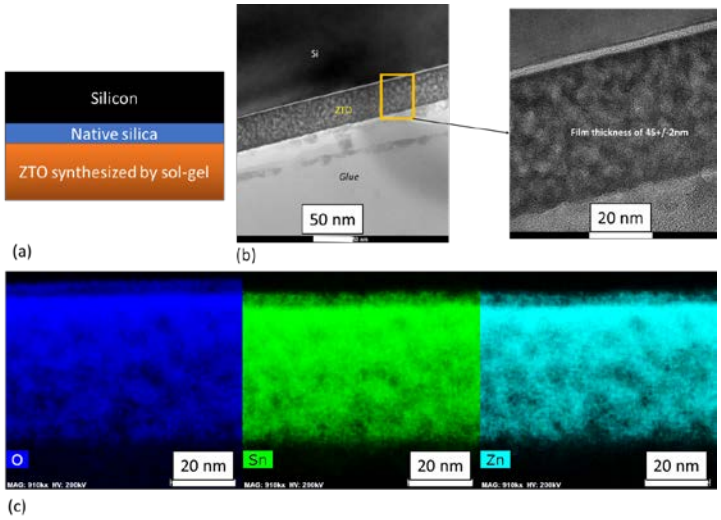

Figure S2. TEM cross-section and EDS spectra of the zinc-tin oxide thin-film (a) Cross-section of the zinc-tin oxide thin-film synthesized on the native silica layer of a silicon wafer. The oxide thin-film was deposited by spin-coating its precursors at 2000 rpm. The ZTO thin-film was synthesized at 450 °C following the recipe described in the experimental section. (b) Transmission electron microscopy (TEM) cross-section picture of the ZTO thin-film. The contrast within the thin-film is caused by porosity due to the reaction of the chloride precursors forming HCl vapors during the sol-gel process. (c) Energy dispersive x-ray spectroscopy (EDS) pictures of the semiconducting thin-film for (left) oxygen, (middle) tin, (right) zinc intensity spectra, demonstrating effective formation of the metal-oxide thin-film after the sol-gel process.

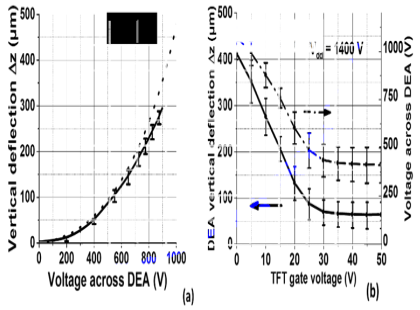

Figure S3. Vertical displacement of DEA: model prediction and experimental results
Plot of vertical deflection and membrane thickness vs. voltage applied across the DEA when directly driven by a high-voltage power supply. The dashed curves correspond to the model prediction and the data points fitted with the solid line, to the experimental measurements on the DEAs. The DEAs have a 4 mm diameter circular active region, a membrane thickness of 17 μm and with a 50 mbars applied pressure and no initial prestretch. The mechanical effect of the compliant electrode has been neglected in the model. The deflection swing is < 1.5μm/V. For the model, a 1.05 MPa Young's modulus a Poisson's ratio of 0.5 and a permittivity constant of 2.7 were considered for the DEA membrane.

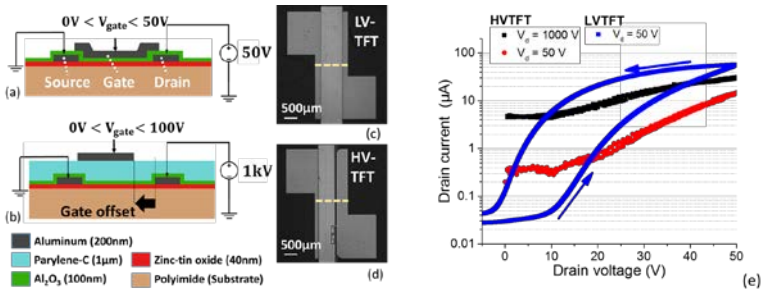

Figure S4. HVTFT vs. low-voltage TFT. Cross-section of a top-gate TFT designed for low voltage operation (a) and a HVTFT (b). Micrograph top-view of a TFT with fully overlapping gate (c) and of a TFT with an offset gate. (e) HVTFT and LVTFT transfer characteristics. The LVTFT has a strong hysteretic behavior showing charge trapping at the interface between the dielectric and the semiconductor. The LVTFT dielectric capacitance is higher leading to higher on-current and lower subthreshold swing than the HVTFT.

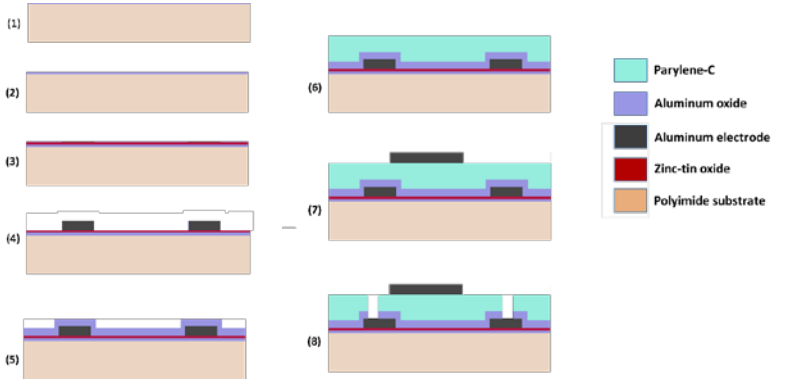

Figure S5. Process flow for the HVTFT fabrication
(1) Start with a Polyimide substrate (50 μm thick)
(2) Coat the polyimide substrate with an Al_2O_3 passivation layer by Atomic layer deposition (200°C, TMA and H_2O as the precursors).
(3) Spincoat zinc chloride + tin chloride precursors mixed in acetonitrile and ethyleneglycol at 2000 rpm. Dry by curing at 120 °C for 1 hour in air. Cure at 450 °C for 1 hour in air to trigger the sol-gel reaction to obtain ZTO.
(4) Deposit the aluminum source and drain electrodes (200 nm) by e-beam evaporation through a shadow mask.
(5) Coat a 100 nm thick Al_2O_3 gate dielectric layer by atomic layer deposition (200°C, TMA and H_2O as the precursors).
(6) Coat a 1 μm thick parylene-C gate dielectric layer by chemical vapor deposition.
(7) Deposit the aluminum gate electrode (200 nm) with a 5 nm chromium adhesion layer by e-beam evaporation through a shadow mask. Cure at 150 °C for 1 hour in air.
(8) Open with laser engraving contacts for the source and the drain through the gate dielectric.

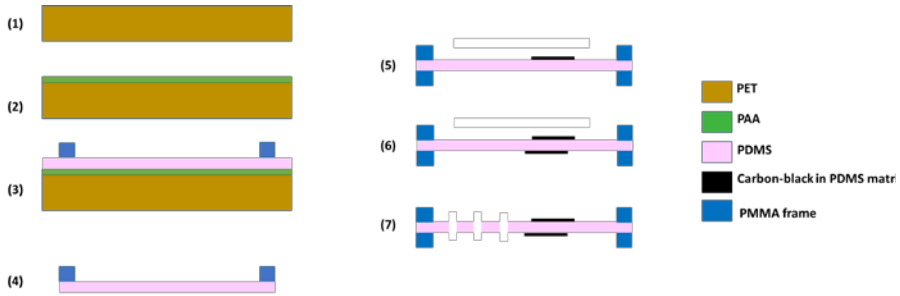

Figure S6 – Process flow for the DEA fabrication
(1) Start with a PET sheet (125 µm thick)
(2) Coat the PET substrate with a Poly (Acrylic acid) sacrificial layer diluted in isopropanol (5%)
(3) Cast the PDMS membrane on the PET substrate's sacrificial layer. Anneal for 1 hour at 80 °C for cross-linking. Select and cut a region by applying a PMMA circular frame (50 mm diameter) coated with dry adhesive.
(4) Release the membrane by putting the sheet in boiling water. PAA dissolves separating the membrane and the PET substrate.
(5) Mix carbon-black in a PDMS matrix to get a conductive stretchable ink. Stamp the top electrode of the DEA with the ink. Anneal at 80 °C.
(6) Stamp the bottom electrode of the DEA. Anneal at 80 °C.
(7) Laser cut via positions for source, drain and gate for the HVTFT assembly.

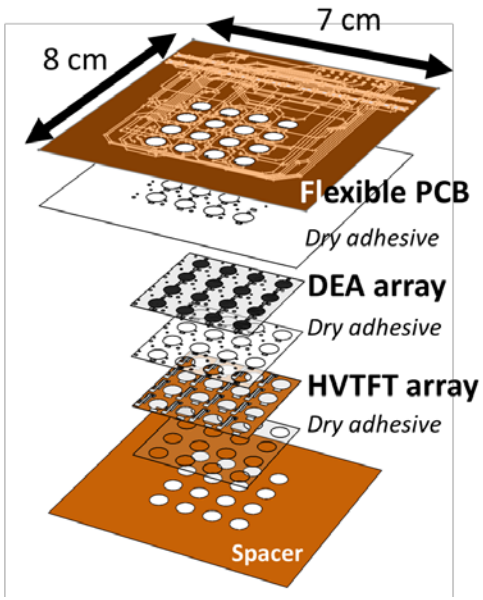

Figure S7 – Exploded view of 4x4 Haptic Display. Exploded view of the entire DEA-TFT assembly: Layers are attached using a dry adhesive, which is also used as a solder-mask. Through the solder-mask, we cast conductive glue at the position of the DEA topside and backside electrode, the HVTFT source, drain and gate electrode. By attaching the flexible PCB to the DEA and the TFT layer the conductive glue creates an electrical contact between the DEAs and the TFTs.