Flicker Noise Upconversion and Reduction Mechanisms in RF/Millimeter-Wave Oscillators for 5G Communications

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by

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To my lovely parents

"Simplicity is the hidden complexity."

Contents

Abstract

The fifth generation (5G) cellular communications in millimeter-wave (mmW) bands (e.g. 28 GHz) place very tough requirements on phase noise (PN) of local oscillators (LO). However, in the advanced CMOS technology (e.g., 28nm, 16nm, 7nm, ...), the intrinsic $1/f$ current noise of MOS transistor is increasingly worsening. It could adversely affect the PN of the LO significantly, especially the flicker PN, leading to a very high $1/f^3$ PN corner (usually exceeding 1 MHz), which is difficult to be attenuated by a mmW PLL. On the other hand, the current literature is full of conflicts and confusing theories about the flicker noise upconversion, with a large number of ambiguities in the RF range, let alone in the mmW range. Thus, lowering the $1/f^3$ PN and figuring out its actual mechanisms are highly desired for 5G mmW communications.

In this thesis, we demonstrate, for the first time ever, a 30 GHz oscillator with a record $1/f^3$ PN corner of ∼100 kHz, which is an order-of-magnitude better than all previous mmW oscillators. Thanks to the special considerations in the common-mode (CM) return path, 2nd harmonic resonance is accurately implemented in this 30 GHz oscillator. Firstly, we numerically verify and illustrate how the 2nd harmonic resonance could reduce the $1/f^3$ PN, featuring the proposed simulation techniques of the $1/f$ noise modulation function (NMF) (i.e., $I_{1/f,\mathrm{rms}}(t)$) and impulse sensitivity function (ISF) (i.e., $h_{\mathrm{DS}}(t)$) (based on a periodic transfer function (PXF)). To physically explain the complex process of flicker noise modulation, a new $1/f$ model is introduced, considering both a carrier number fluctuation (CNF) and a correlated mobility fluctuation (CMF).

Further, we identify and numerically verify a new flicker noise reduction mechanism based on narrowing of a conduction angle, which has been presented in the literature but

never properly explained. Through narrowing of the conduction angle, we demonstrate a wide-tuning range low $1/f^3$ PN corner oscillator for 5G sub-6 GHz applications (i.e., Internet-of-Everything (IoE)).

Chapter

1

Introduction

1.1 What is 5G Communications?

Wireless communications have started with a transmission of voice and messaging with limited data traffic, which were called 1st- and 2nd-generation networks (1G & 2G), as shown in Fig. 1.1(a). With the introduction of 3rd-generation networks (3G), consumers got the real taste of being able to access the Internet, surf the Web, engage in social media, and stream music, all while being mobile. Naturally, the desire for faster data rate suddenly surged, which was further boosted by the advent of the fourth generation networks (4G) in 2010. The 4G communications has been witnessing the explosive growth of mobile Internet, featuring extremely rapid updates of all kinds of smart-phones or other mobile devices.

The fifth generation of wireless communications (5G) [1–7] is branching into two frequency bands: sub-6 GHz and near-millimeter wave (e.g., 28 GHz), shown in Fig. 1.1(b). The former, called Internet-of-Everything (IoE), is embracing all the existing technologies, including consumer applications (e.g., smart home, wearable technology,...), commercial applications (e.g., smart transportation, internet of health things,...), infrastructure applications (e.g.,

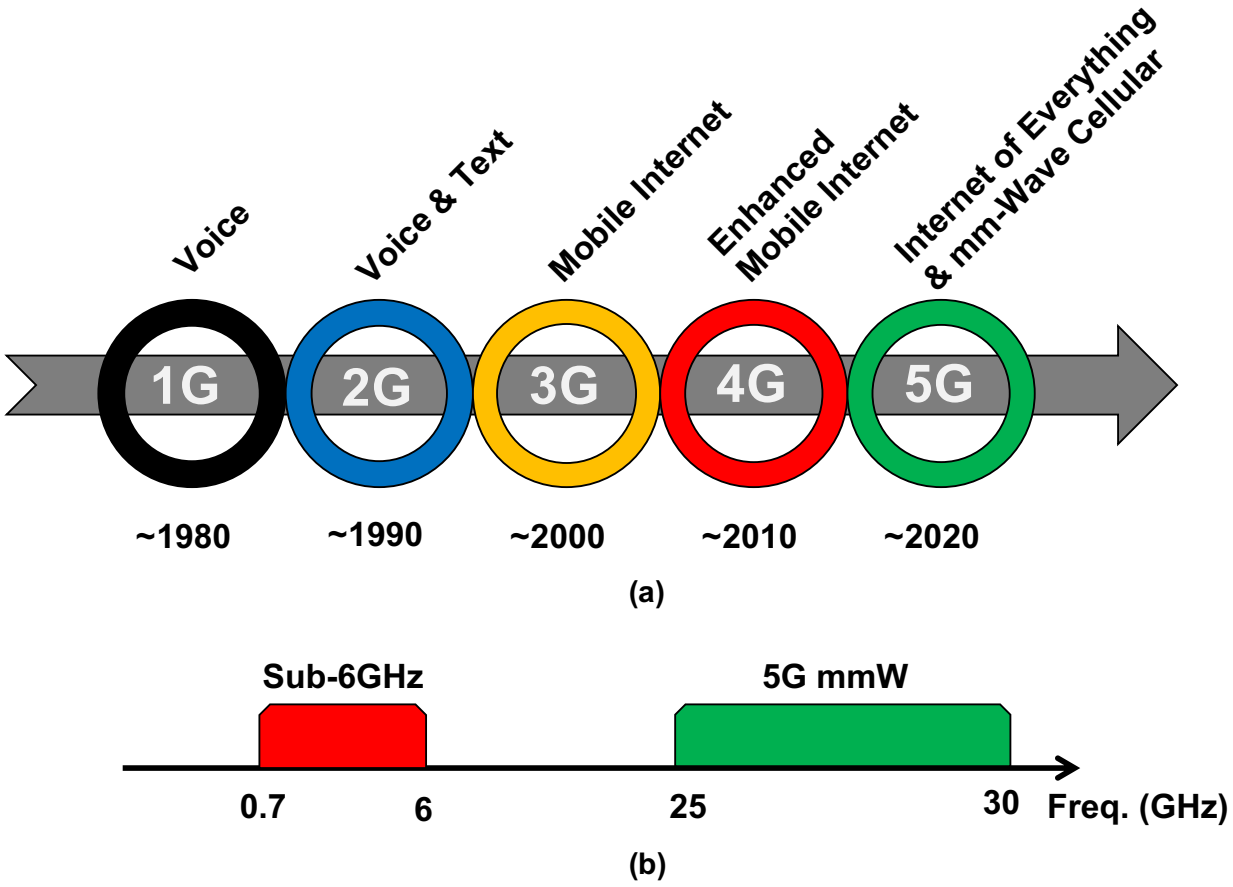

Figure 1.1: (a) Evolution of wireless communications (1G: voice, 2G: voice & text, 3G: mobile Internet, 4G: enhanced mobile Internet, 5G: Internet-of-Everything (IoE) & millimeter-wave (mmW) cellular). (b) Crowded sub-6 GHz frequency band range and brand-new mmW band range for 5G communications.

smart city, environmental monitoring,...), and industrial of Internet-of-Things (see Fig. 1.2). However, due to the physical limitations and other existing radio standards, the increasingly crowded sub-6GHz bands find it difficult to meet the requirement of the data rate growth. In particular, high-definition (HD) mobile video, virtual reality (VR), and augmented reality (AR) are becoming the main drivers of 5G cellular communications, significantly increasing the requirement of data rate [1].

1.2 Why 28GHz Frequency Bands?

As shown in Fig. 1.3, the mobile video traffic is forecast to account for 75% of all the data traffic in 2023 [1]. Its estimated compound annual growth rate (CAGR) would be up at

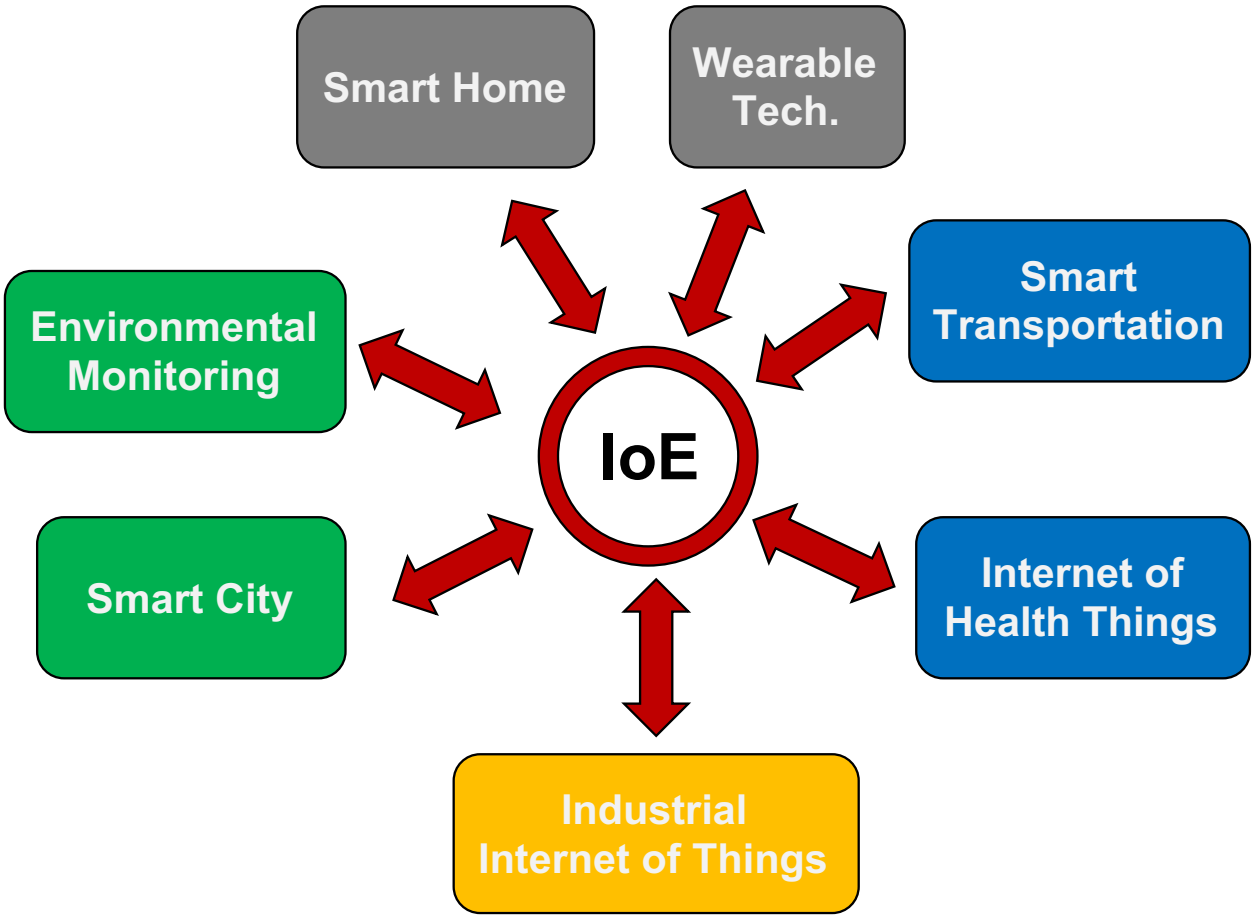

Figure 1.2: Some of the trends of 5G communications: Internet-of-Everything (IoE), embracing all existing radio techniques at sub-6GHz frequency bands.

almost 50% from 2017 to 2023. The data rate requirement of HD mobile video, virtual reality (VR), and augmented reality (AR) could be up to 10Gb/s, which forces the 5G cellular to explore brand-new near-mmW bands.

Obviously, the mmW cellular networks will be the most prominent feature of 5G communications. This makes it physically different from previous generations of wireless communications. However, this also poses a main concern of atmospheric absorption of mmW frequencies. Fig. 1.4 shows the atmospheric absorption properties of sub-terahertz radio spectra. The frequency bands with extremely high-attenuation properties (i.e., 60, 120, 183, 325, and 380 GHz) are allocated for short-range applications, such as wireless personal area network (WPAN) and imaging, while the 28, 77, and 240GHz frequency bands with relatively low space attenuation would be suitable for long-range applications, such as cellular, backhaul, and vehicular radar [3]. Especially, among all the mmW bands, the 28GHz band enjoys

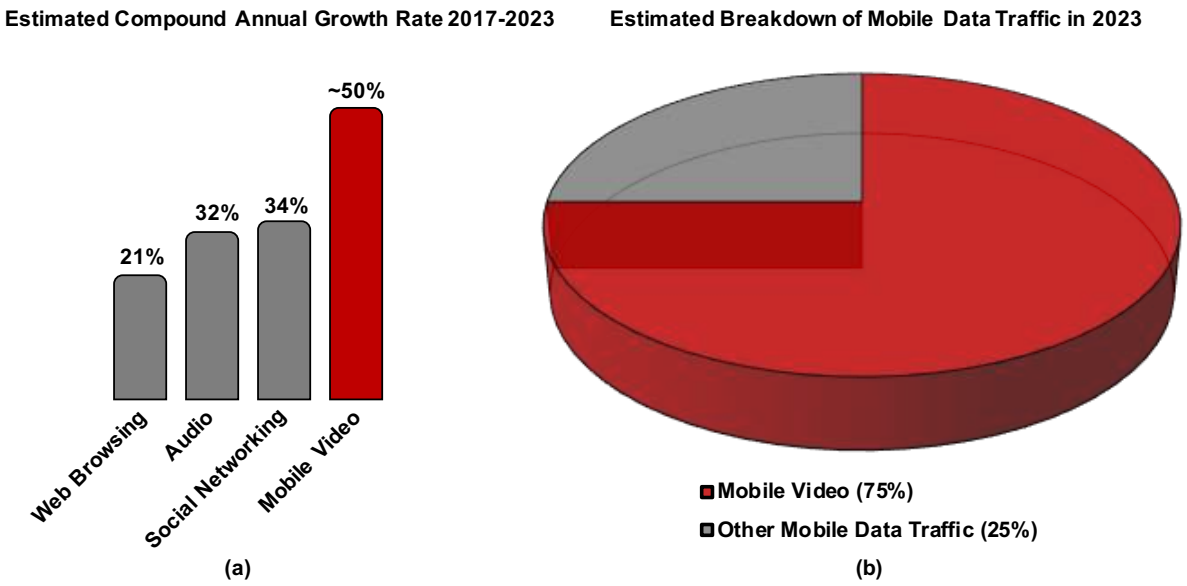

Figure 1.3: (a) Estimated compound annual growth rate (CAGR) of mobile traffic by application from 2017 to 2023, in which the CAGR of mobile video will be up to 50% [1]. (b) Mobile video traffic is expected to account for 75% of all mobile-data traffic in 2023.

the lowest attenuation, thus placing it among the best candidates for 5G mmW cellular communications [4].

1.3 Why Antenna Array, Beamforming, and CMOS Technology?

The adoption of 28 GHz can enable a high-gain and small-size of antenna array, which could be fabricated on a printed circuits board (PCB) [8–10] or even on-chip [7] for cellular networks due to its wavelength being an order of magnitude smaller than that of the sub-6 GHz systems. Benefiting from the miniaturized antenna array, a beamforming technique was introduced in 5G mmW cellular for creating electronically-controlled directional links [8–13]. It promotes energy efficiency, massive MIMO (multiple-input and multiple-output), and delivers enough output power, further mitigating the space attenuation of 28 GHz frequency bands. Three possible architectures have been under intensive research in recent years, including RF beamforming [8–11], LO beamforming [13], and digital beamforming [12]. An RF beamformer can be directly added to an existing receiver/transmitter architecture, supporting wide-band signals (using variable true-time-delay (TTD) where applicable) or narrow-band signal (using variable phase shifter). However, since the low-loss, linear, and compact RF variable delay is difficult to be implemented in integrated circuits (ICs), RF phase-shifters [8–11] are the

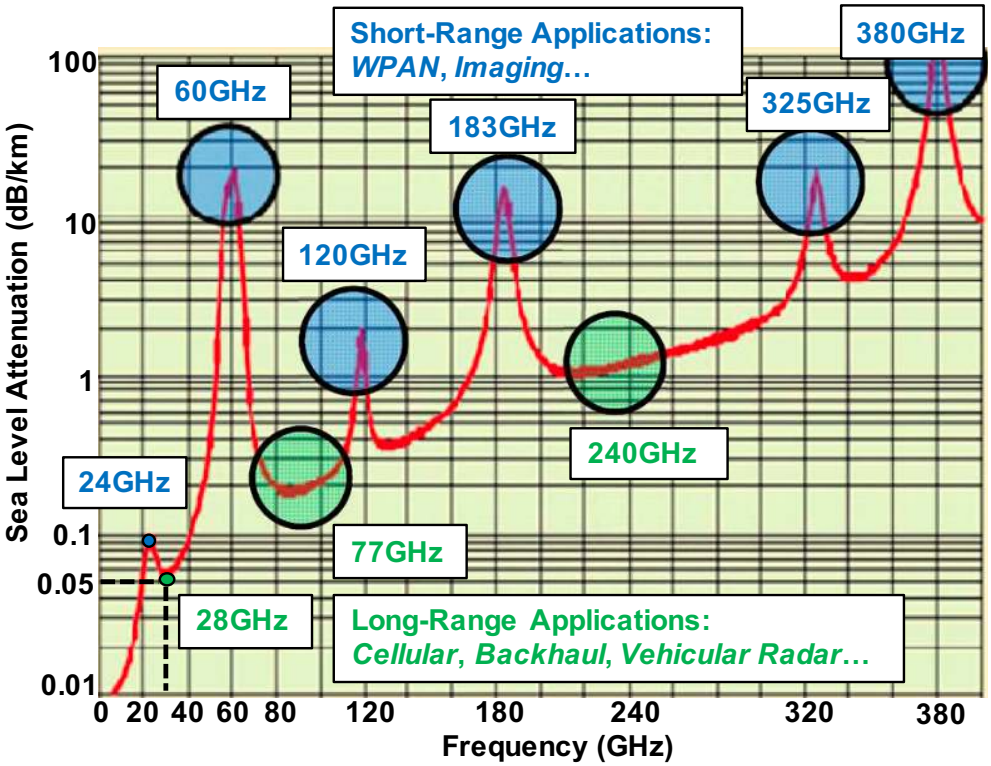

Figure 1.4: Atmospheric absorption across mmW frequencies in dB/km. The frequency bands of 28GHz shows the smallest space attenuation of all mmW bands, a best candidate for mmW cellular communications (Modification of Fig. 2 in [3]).

mainstream, thus limiting the signal bandwidth. Instead of shifting the phase of an RF transmitting/receiving signal, it would be easier to shift the phase of the LO [13]. But, LO phase shifting is still an inherently narrow-band approach, and it is also challenging to do LO routing for large arrays. Digital beamforming [12] has the highest capacity and flexibility, but has to handle a large number of digital I/Os, thus consuming large power.

The beamforming technique with an antenna array (power combining of the transmitted signal can be performed in space) can relax the requirement of a single power amplifier (PA) in the array. Thus, the 28 GHz CMOS PAs [14–16] (or CMOS RF/mm-Wave-DACs [17, 18]) are becoming increasingly popular, which has been traditionally hampered by its limited breakdown voltage and poor capability for current handling. On the other hand, the technique of beamforming will benefit from the high-integration of CMOS technology, which enables all kinds of digital calibration algorithms. Fig. 1.5 shows a compact 28 GHz phased-array transceiver scheme [9], in which a miniaturized antenna array and a CMOS RFIC are built on two sides of a chip-scale package, respectively.

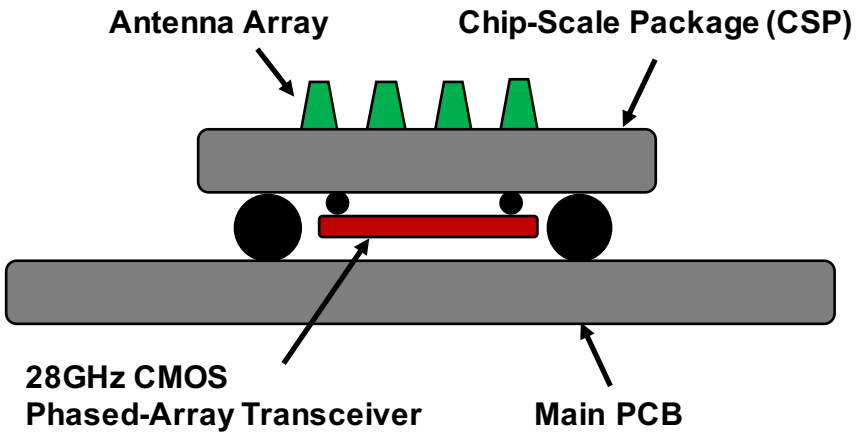

Figure 1.5: A compact 28 GHz phased-array transceiver scheme: an antenna array is built on one-side of a chip-scale package, while the 28 GHz CMOS phased-array transceiver is packaged as a flip-chip on the other side [9].

1.4 Flicker Phase Noise in CMOS Technology

No matter what architectures of beamforming will be employed in the CMOS phase-array transceiver, the quality of their 28 GHz local oscillators could be a bottleneck limiting further improvements in the data rate. As a result, the 5G mmW cellular will place very tough requirements on phase noise (PN) of local oscillators due to the complex modulation scheme [51].

The quality factor (Q) of capacitor banks will significantly decrease when the resonating frequency of oscillators is above 20 GHz [25], worsening the thermal PN region of mmW oscillators. Several techniques have been proposed to improve the situation: 1) multi-core oscillators [19, 20, 22], 2) harmonic-extraction based on 2nd [21, 22] or 3rd [23] harmonic, and 3) mmW oscillators injection-locked by RF oscillators [24–28]. For multi-core oscillators, the thermal PN will be improved in theory by $10 \cdot \log_{10} N$ dB when N cores are inter-connected at the cost of $N\times$ power and area. Operating at a lower frequency (e.g., $<$ 20GHz) and extracting its own higher harmonics, the harmonic-extraction oscillators could have good thermal PN due to the high-Q tank at the low frequency. Unfortunately, the additional harmonic extractors may burn more power than the oscillators themselves. Replacing the harmonic extractor (burning high power) with a high-frequency oscillator (low power), then injecting a low frequency signal (good thermal PN) into the high frequency oscillator, the injection locking technique is able to achieve low thermal PN and low power at the same

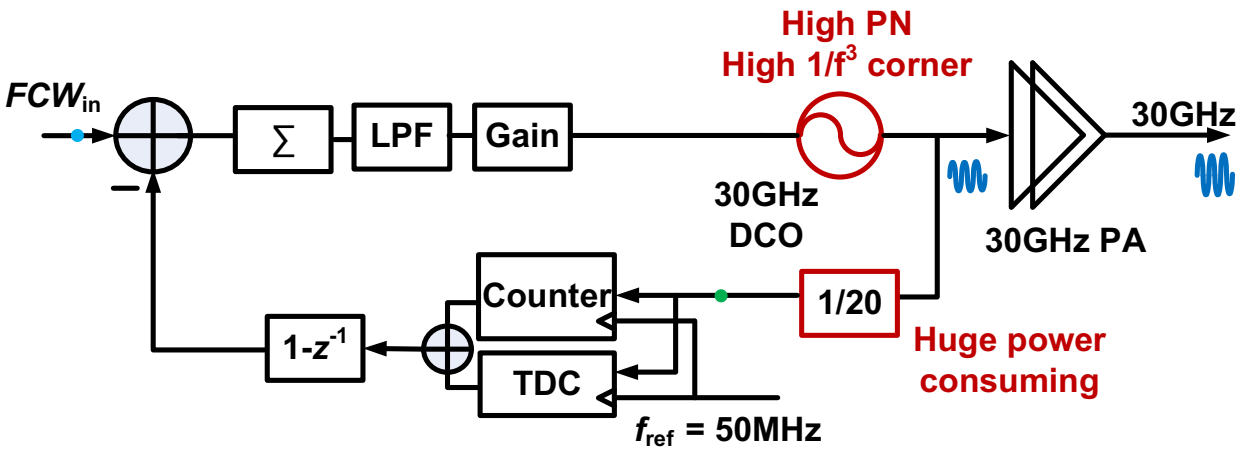

Figure 1.6: Challenges of a conventional 30GHz ADPLL architecture for 5G communicaitons.

time. However, the PVT (process, voltage, temperature) robustness and locking range are challenging for this technique [29–31].

Despite these $1/f^2$ PN improvements in mmW oscillators, their $1/f^3$ PN corner seems to always exceed 1 MHz per survey in [51] (see Chapter 2). Furthermore, the intrinsic $1/f$ current noise of MOS transistor is worsening with the CMOS technology advancements [32]. Both the carrier number fluctuation (CNF) and correlated mobility fluctuation (CMF) mechanisms of $1/f$ noise show largely adverse effects in shorter channel-length devices [33]. The increasingly worse $1/f$ current noise could up-convert to $1/f^3$ PN, leading to a further increase in the $1/f^3$ PN corner.

Fig. 1.6 shows a possible conventional architecture of an all-digital phase locked loop (ADPLL) for 5G mmW communications. The bandwidth (BW) of this ADPLL should be maintained quite narrow to prevent reference noise and time-to-digital converter (TDC) noise from dominating its integrated jitter especially amplified by the large frequency ratio N (e.g., 30GHz/50MHz = 600) at mmW. The limited BW of mmW PLLs would fail to effectively attenuate the flicker PN of the mmW oscillator, worsening the total integrated jitter. Thus, the techniques to reduce the $1/f$ noise upconversion are highly desired for 5G mmW communications.

1.5 Evolution of Theories on Flicker Noise Upconversion

1.5.1 Phase Noise Model: ISF, Phasor Analysis, PPV, and Matrix

To be able to significantly reduce the $1/f^3$ PN, a deep understanding of the flicker noise upconversion mechanism is necessary. However, the flicker PN theory was not effectively developed [34] until an impulse sensitivity function (ISF) was first introduced by Hajimiri and Lee [35] in 1999. The ISF theory suggests that a symmetric effective ISF (eISF) would suppress the flicker noise upconversion, which could be realized by forcing symmetries in the oscillating waveform. However, the theory was silent on how to achieve that symmetric oscillation waveform. In fact, we will demonstrate in this thesis that, even for asymmetric waveforms (i.e., lack of 2nd harominc resonance), narrowing of conduction angle or adding additional drain-gate phase-shift with consideration of 2nd harmonic termination can also suppress the flicker noise upconversion.

In addition to the ISF theory, other well-known PN theories are listed as follows:

1) Phasor-based analysis [36]. It has been demonstrated to be equal to the ISF theory in the thermal PN range, but the flicker PN analysis is still missing there.

2) Perturbation projection vector (PPV) [37]. The PPV analysis could be seen as an extended (or more rigorous) version of ISF, considering the time-shift of ISF itself when noise is injected into a LC tank [38, 39], which enables the ISF to predict the injection locking phenomenon [39–41]. However, for thermal PN analysis using PPV shows almost the same results as with ISF [38]. Also, there is no discussion in [37] on the flicker noise upconversion.

3) Matrix analysis [42]. Both thermal and flicker PN analyses are discussed in [42]. However, the method neglects the consideration of even-harmonic waveform and common-mode (CM) tank, which are seen as the main contributors to the flicker PN [51]. An interesting point was proposed in which the non-resistive path of 3rd harmonic (any higher odd-order) current will not introduce any flicker noise upconversion.

In summary, the ISF theory could be the most promising method to explain both qualitatively and quantitatively the flicker noise upconversion and reduction mechanisms as long as we can accurately understand and simulate it [51, 86].

1.5.2 Flicker Noise Upconversion Analysis in Voltage-Biased Oscillators

Two groundbreaking architectures of the 2nd harmonic resonance (i.e., tail-filtering) [45,46] and class-C operation (i.e., narrowing of conduction angle) [47] have shown quite good thermal and flicker PN performance. In recent years, the technique of 2nd harmonic resonance started to employ an implicit parallel-LC common-mode (CM) tank [44, 49–53] or series-LC CM tank [54] (only improving the flicker PN) to save area, while the technique of class-C mode of operation attempted to add two "controlled switches" (e.g., NMOS-based [55], PMOS-based RC coupling [56], and PMOS-based transformer coupling [58]) under the cross-coupled pair to decrease the conduction angle.

As the supply voltage decreases in the advanced CMOS technology, the tail-current source in an LC-tank oscillator would partially enter the triode region, causing only a small amount of flicker noise of the tail-current source to upconvert to flicker PN [43, 44]. In recent years, directly replacing the tail-current source with switched tail-resistors (or no tail-resistor at all) has become increasingly popular due to the elimination of one of the most dominant sources of $1/f$ noise upconversion as well as suitability for low supply operation. These types of oscillators are called voltage-biased oscillators. Consequently, the study of flicker noise upconversion then focuses mainly on the $1/f$ noise from the cross-coupled pair. The pioneering works of [32, 64, 65] have tried to demonstrate that the non-zero dc value of the effective ISF comes from the 3rd harmonic current entering the capacitive path. Nevertheless, the theory totally neglects the effects of 2nd harmonic current, which has already manifested its significant effects on the flicker noise upconversion [45, 46]. Shahmohammadi *et al.* claims that the asymmetry between rising and falling portions of the oscillation waveform results in $1/f$ noise upconversion, which is a consequence of the 2nd harmonic current entering a non-resistive path while the 3rd harmonic current is shown as benign. However, this claim lacks a rigorous numerical verification, and also it cannot explain the good $1/f^3$ PN corner in oscillators with the narrowed conduction angle but with no special considerations of the 2nd harmonic resonance [47, 55–58, 61–63].

The current literature on the theory of flicker noise upconversion suffers from the following drawbacks: 1) Some of the authors merely mention various qualitative aspects [34, 45, 46, 49, 55, 56, 58–60], but rigorous quantitative analysis is missing. 2) Some pioneering quantitative research is conducted in [32, 43, 44, 64, 65], but they neglect the importance of implicit CM

tank and further they employ oversimplified ISF and flicker noise modulation function (NMF), which might damage the credibility of their theories to some extent. Therefore, a unified theory of flicker noise up-conversion and reduction is highly desired, which can perform rigorous numerical verification (e.g., numerical verification of PN@ 10kHz between calculation and simulation) and intuitively explain all the flicker noise reduction mechanisms, such as the 2nd harmonic resonance and narrowing of conduction angle.

1.6 Thesis Objectives and Outline

In this thesis, we claim the first-ever demonstration of a 30 GHz oscillator with an ultra-low flicker noise corner (∼100 kHz) featuring a special consideration of the CM current return path, which up to now has been neglected by RF/mmW designers. Based on the proposed simulation techniques of ISF (derived from positive sidebands of periodic transfer function (PXF)) and flicker NMF, we first rigorously verify in a numerical manner the flicker noise upconversion and reduction mechanisms against the advanced TSMC 28 nm LP CMOS technology. We identify that the 2nd harmonic current entering a non-resistive path (i.e., causing asymmetries in rising and falling edges of the oscillation waveform) is the main contributor to the $1/f$ noise upconversion, while the 2nd harmonic resonance (i.e., making symmetric the rising and falling parts of the oscillating waveform) and the narrowing of conduction angle but with no consideration to the 2nd harmonic resonance (i.e., decreasing modulated $1/f$ noise *exposure* to asymmetric rising and falling waveform) are the two effective ways to lower the $1/f^3$ PN. To intuitively and physically understand the complex behavior of flicker noise modulation in oscillators, the carrier number fluctuation (CNF) and correlated mobility fluctuation (CMF) mechanisms are introduced in analyzing the flicker noise upconversion. Based on the newly identified $1/f^3$ PN reduction mechanism of narrowing of conduction angle, a 2.4 GHz transformer-based digitally controlled oscillator (DCO) is proposed, achieving around 100 kHz $1/f^3$ PN corner across the whole wide tuning range (TR) up to 35%, while its intrinsic start-up problem of narrowing the conduction angle is mitigated by the passive gain of a 2:3 transformer.

The rest of thesis is organized as follows: Chapter 2 shows an analysis and design of the low-flicker-noise 30 GHz class-F_{23} oscillator in 28-nm CMOS using implicit resonance and explicit common-mode return path. The newly identified flicker noise reduction mechanism

of narrowing the conduction angle is revealed in Chapter 3. It also proposes a comprehensive analysis method of flicker noise upconversion and reduction based on simulated flicker NMF and ISF. Based on the narrowing of conduction angle technique, a 0.3 V, 35% TR, 60 kHz $1/f^3$ PN corner DCO with vertically integrated switched capacitor banks is demonstrated in Chapter 4. Chapter 5 concludes the thesis and gives future research suggestions.

Chapter

2

A Low-Flicker-Noise 30-GHz Class-F_{23} Oscillator in 28-nm CMOS using Implicit Resonance and Explicit Common-Mode Return Path

This chapter presents a mm-Wave frequency generation stage aimed at minimizing phase noise (PN) via waveform shaping and harmonic extraction while suppressing flicker noise upconversion via proper harmonic terminations. A second-harmonic resonance is assisted by a proposed embedded decoupling capacitor inside a transformer for the explicit common-mode current return path. Class-F operation with third-harmonic boosting and extraction techniques allow maintaining the high quality factor of a 10 GHz tank at the 30 GHz frequency generation. We further propose a comprehensive quantitative analysis method of flicker noise upconversion mechanism exploiting latest insights into the flicker noise mechanisms in nanoscale short-channel transistors, and it is numerically verified against foundry models. The proposed 27.3–31.2 GHz oscillator is implemented in TSMC 28 nm CMOS. It achieves PN of -106 dBc/Hz at 1 MHz offset and FoM of -184 dBc/Hz at 27.3 GHz. Its flicker PN ($1/f^3$) corner of 120 kHz is an order-of-magnitude better than currently achievable at mmW.

2.1 Introduction

Traditional cellular bands, i.e., $< 6\,\text{GHz}$, suffer from severe bandwidth (BW) congestion and can barely cope with the increasing demands for data. Consequently, the fifth generation (5G) of cellular communications starts to utilize a lower range of millimeter-wave (mmW) frequency bands, e.g., 28 GHz [1]. To support higher data rates, more complex modulation schemes are being introduced, thus placing challenging requirements on phase noise (PN) of local oscillators. It is well known that for mmW oscillators, the quality (Q) factor degradation of a tuning varactor or a switched-capacitor (sw-cap) tuning network leads to worse PN in the thermal ($1/f^2$) noise region. To mitigate such degradation, the following solutions have been devised: the oscillator's resonant frequency gets lowered but then increases via a frequency multiplier, such as a doubler/quadrupler in [21] and [22], multi-core oscillators [22], sub-harmonic injection locking [25, 66], and transformer-based class-F oscillator with a tuned power amplifier (PA) to extract its 3rd harmonic [23].

Yet, despite those PN improvements in the $1/f^2$ region, the flicker PN ($1/f^3$) corner of $>10\,\text{GHz}$ oscillators appears to always exceed $\sim$1 MHz, as surveyed in Fig. 2.1. Moreover, the underlying cause, i.e., the flicker ($1/f$) noise of MOS transistors, tends to worsen as CMOS scales, which will further degrade the integrated PN, thus limiting the achievable data rates in mmW transceivers. Considering an example of a mmW type-II all-digital PLL (ADPLL) shown in Fig. 2.2, the loop BW needs to be limited to $< 400\,\text{kHz}$ to suppress the typical 10 ps quantization noise of its time-to-digital converter (TDC), according to the system simulations in Fig. 2.3 (a). Even with the TDC resolution as fine as 1 ps [see Fig. 2.3 (b)], the loop BW must still be maintained quite narrow in order to prevent the reference noise from dominating the ADPLL's PN. This is due to the high multiplication ratio N of mmW PLLs (e.g., $N = 600$ for a 30 GHz oscillator locked to a typical $f_{\text{ref}} = 50\,\text{MHz}$ reference). Even the best realistic attempts at reducing the remaining ADPLL PN contributors will unfortunately leave the oscillator's $1/f^3$ PN as the limiting factor preventing from breaking through the 520 fs and 410 fs integrated jitter limits for the TDC resolution of 10 ps (typical state-of-the-art) and 1 ps (yet to be achieved), respectively. Consequently, techniques to lower the $1/f^3$ PN are highly desired for mmW generation.

Recent studies [44, 49, 65] deal with the flicker noise reduction in voltage-biased RF oscillators, i.e., in which the conventional mechanism of $1/f$-noise upconversion via the

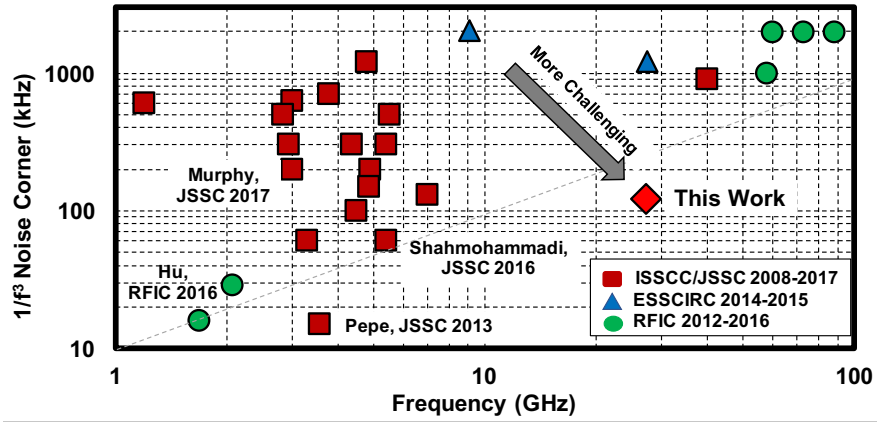

Figure 2.1: Survey of $1/f^3$ corner of state-of-the-art RF and mmW oscillators.

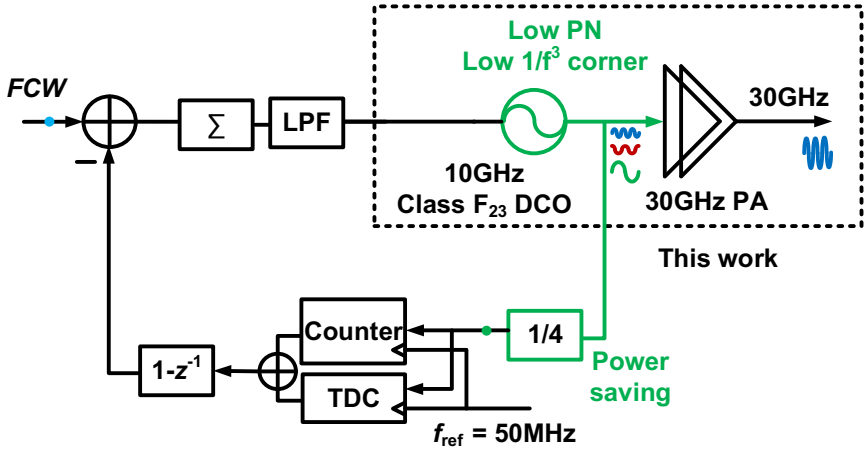

Figure 2.2: An intended architecture of a 30 GHz ADPLL focused on its low-power and high-performance aspects.

tail current source does not appear anymore [43]. In [64, 65], it is suggested that the non-zero dc value of the effective impulse sensitivity function (ISF) is mainly caused by a 3rd harmonic current entering a capacitive path, resulting in the $1/f^3$ PN degradation. However, the effect of 2nd harmonic current is entirely neglected. Shahmohammadi *et al.* [44] explains that the $1/f$ noise up-conversion is due to an asymmetry between rising and falling edges of the tank's voltage waveform, which is a consequence of a 2nd harmonic current (I_{H2}) entering the capacitive path. The effects of the 3rd harmonic current are shown as benign. That was further experimentally supported in [49], but the rigorous quantitative analysis of flicker noise upconversion is still missing in [44, 49]. It appears that the lack of a complete numerical verification and the over-simplification of the flicker noise model employed cause some contradictions and ambiguities in the currently available theory of

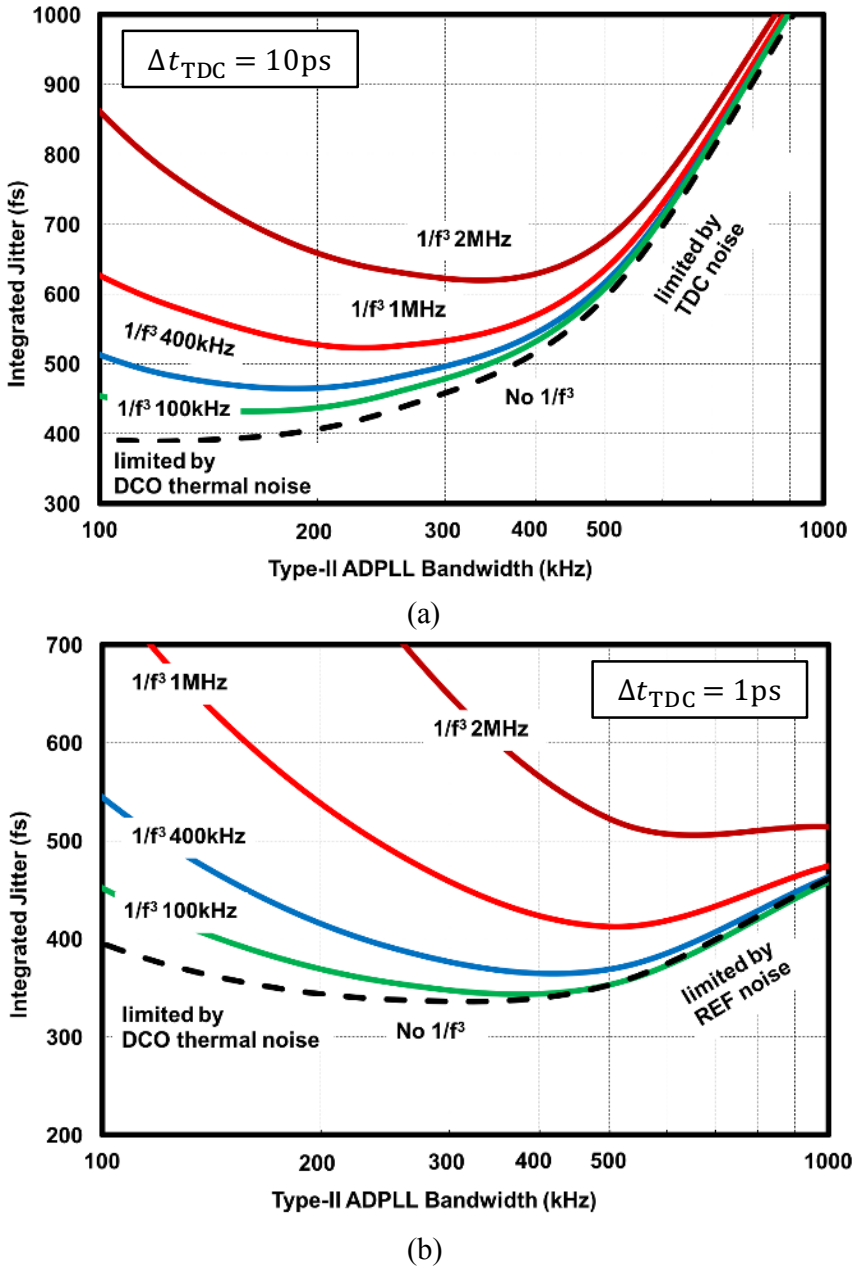

Figure 2.3: Simulated integrated phase noise (translated to jitter) across loop bandwidth of a type-II 30 GHz ADPLL for various $1/f^3$ noise corners of the oscillator. Conditions: PN_{DCO} @10 MHz = -120dBc/Hz, f_{ref} = 50MHz, σ_{ref} = 1ps. TDC resolution: (a) 10 ps, and (b) 1 ps.

flicker noise upconversion and reduction mechanism. Moreover, a direct translation of the above techniques [44, 49, 65] into mmW does not appear so straightforward. For example, employing a high-frequency oscillator with a one-turn inductor [67] or a conventional 1:2 transformer [44, 48] could suffer from high $1/f^3$ PN corner due to the uncontrolled 2nd

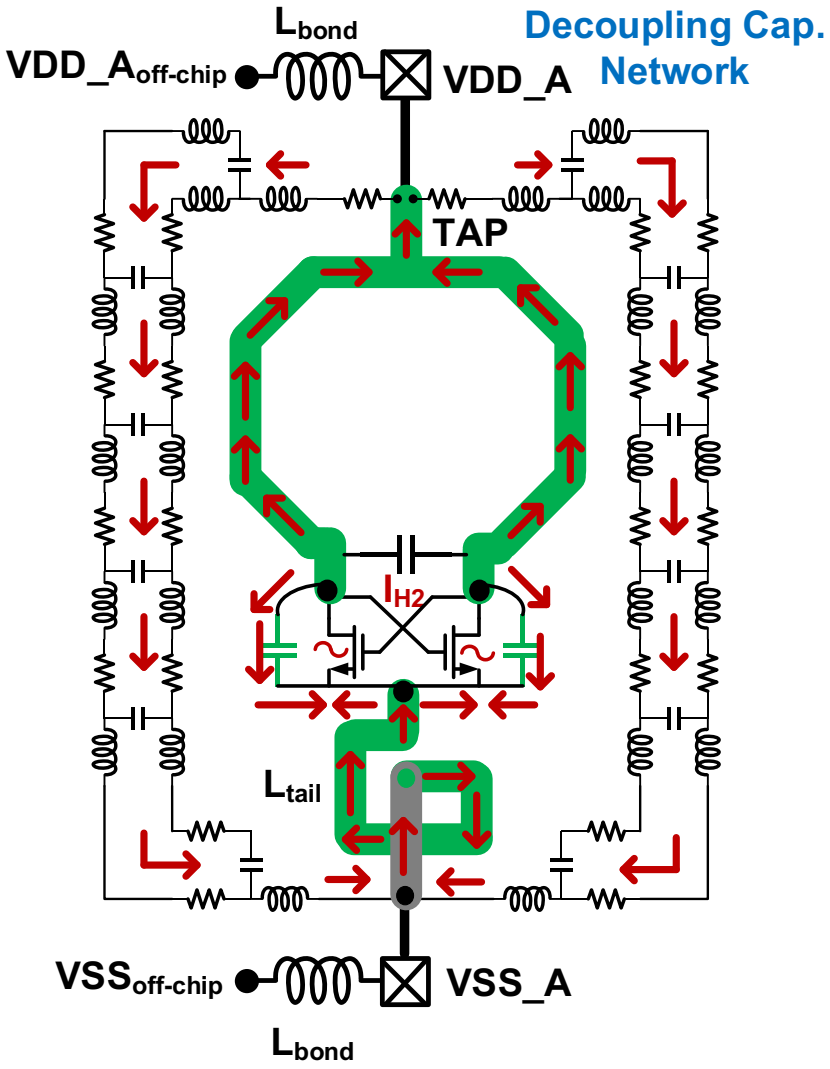

Figure 2.4: Diagram of a conventional voltage-biased mmW oscillator with a tail inductor further showing its parasitic common-mode return path.

harmonic current return path of the decoupling capacitor, as shown in Figs. 2.4 and 2.5(a), thus shifting the expected common-mode (CM) resonant frequency.

This thesis proposes a 30 GHz frequency generation scheme shown in Fig. 2.6 using a 3rd harmonic extraction from a class-F_{23} oscillator operating at 10 GHz fundamental. It features a special 1:2 transformer including a proposed embedded decoupling capacitor for the precise control of the CM current return path, as illustrated in Fig. 2.5(b) [50]. Its PN in the $1/f^2$ thermal region is kept low via the 3rd harmonic resonance, and its $1/f^3$ PN corner is greatly improved (by an order-of-magnitude vs. state-of-the-art) via a precise implementation of the 2nd harmonic resonance and the proposed explicit CM return path.

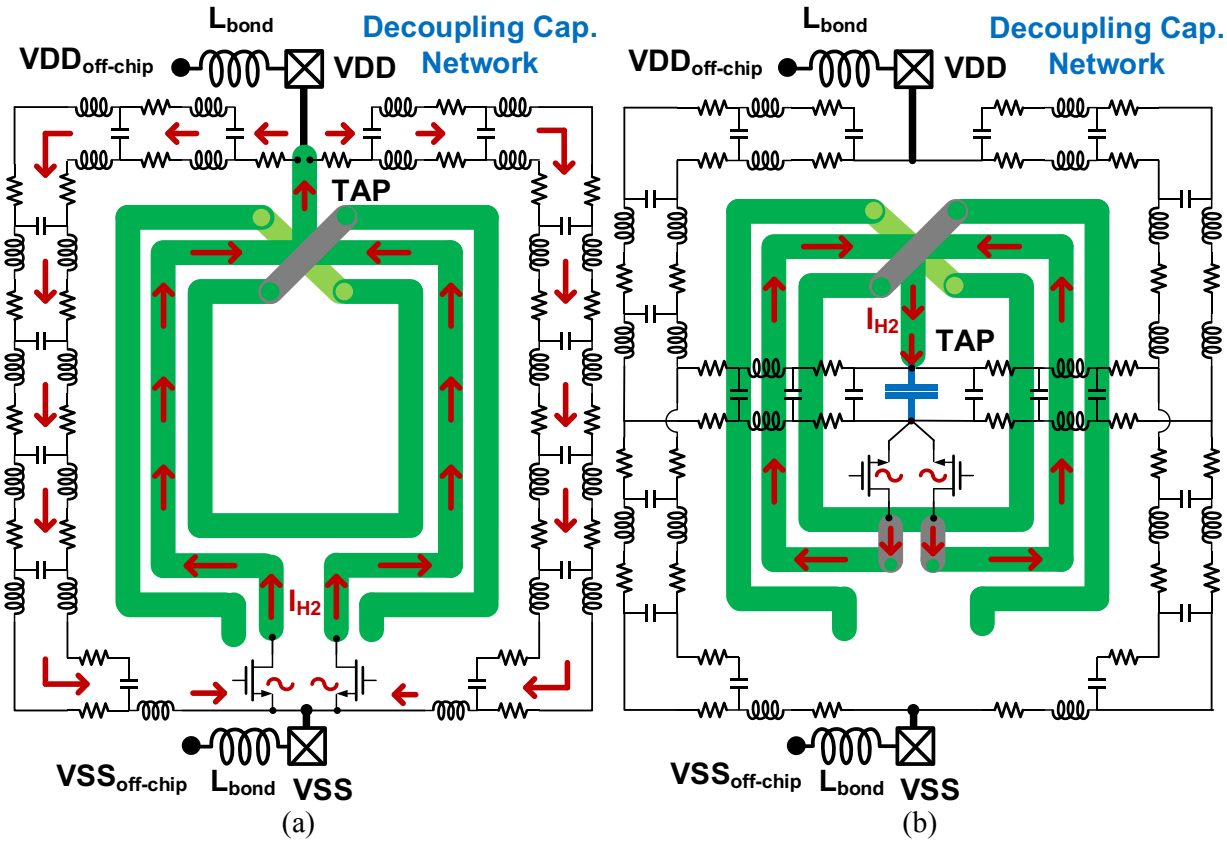

Figure 2.5: (a) Conventional class-F_{23} oscillator w/o the well-controlled CM return path [44, 48]. (b) Proposed structure to control the CM return path in which the 1:2 transformer features an embedded decoupling capacitor (blue capacitor) [50].

In Section 2.2, the $1/f$-noise reduction mechanism based on the 2nd harmonic resonance in mmW voltage-biased oscillators is numerically verified in the 28-nm technology. Details of the proposed 30 GHz frequency generation scheme, focusing on an accurate implementation of the 2nd harmonic resonance, are revealed in Section 2.3. In Section 2.4, the proof-of-concept 30 GHz oscillator demonstrates the lowest $1/f^3$ PN corner of 120 kHz among mmW oscillators.

2.2 Flicker Noise Upconversion and Common-Mode Return Path in mmW Oscillators

2.2.1 Current Return Path in mmW Oscillators

The conventional voltage-biased mmW oscillator with a one-turn inductor [see Fig. 2.4] can be modeled as in Fig. 2.7 (a). The circuit includes a cross-coupled pair (M1, M2, with

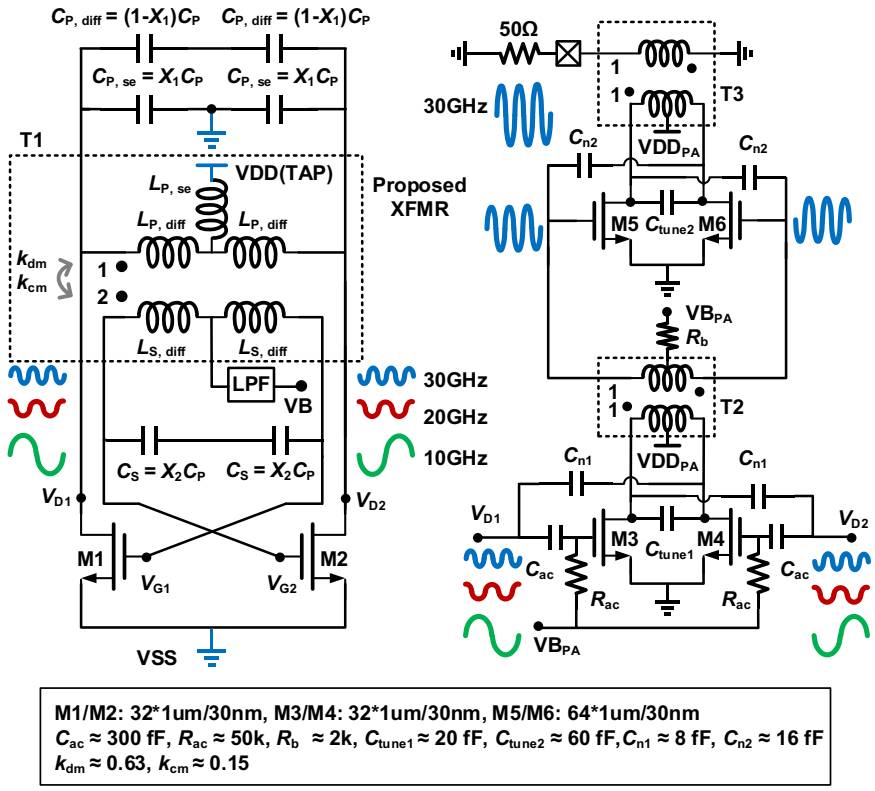

Figure 2.6: Schematic of the proposed 30 GHz class-F_{23} oscillator using second-harmonic resonance and third-harmonic extraction.

their parasitic capacitances C_{se1}), switched-capacitor (sw-cap) bank with its elements shown in Fig. 2.7 (b) (C_{diff} and the switch parasitics C_{se2}), main inductor (L_{diff}, L_{se}), decoupling capacitor network for the supply/ground (C_{decap} and its parasitic inductance L_{decap}), and tail inductor (L_{tail}). Two supplies are used, i.e., "analog" supply (VDD_A/VSS_A) for the oscillator core and "digital" supply (VDD_D/VSS_D) for the sw-cap bank. In addition, L_{bond} is used to model wire-bonding inductors from the external supply ($VDD\_A_{off\text{-}chip}$, $VDD\_D_{off\text{-}chip}$, and $VSS_{off\text{-}chip}$) to the IC wirebonding pad (PAD), while L_{wire} models the interconnecting wire inductances from PAD to the local supplies and grounds. C_{decap_bank} is used to model a local decoupling capacitor for the sw-cap bank, while $C_{decap,\ off\text{-}chip}$ and $L_{decap,\ off\text{-}chip}$ model the off-chip decoupling capacitor and its parasitic inductance, respectively.

In RF, and especially mmW circuits, defining local supply points, i.e., VDD_A or VSS_A, as ac grounds is not so straightforward. To start with, "current return path" should be considered. The differential-mode (DM) return path is for the DM current (e.g., I_{H1}, I_{H3}) from the drain of M1 to the drain of M2, and then from the source of M2 back to source

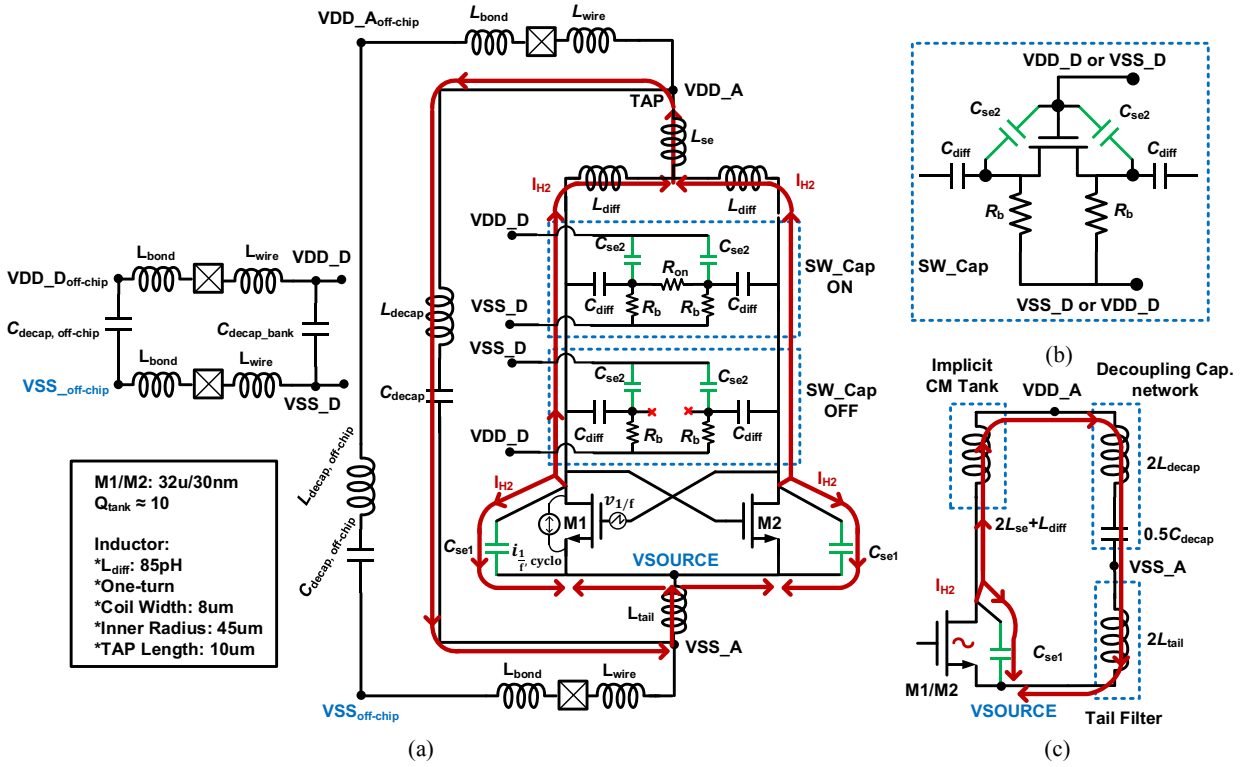

Figure 2.7: (a) Model of a conventional 30 GHz oscillator w/ tail filtering and its CM return path. (b) Conventional switched-capacitor tuning element. (c) Half-circuit of the CM return path.

of M1, and vice versa. Thus, the (half-circuit) tank inductance in DM ($L_{\rm dm}$) is simply $L_{\rm diff}$, while the DM capacitance ($C_{\rm dm}$) is dominated by $C_{\rm diff}$ when sw-cap is on and by the parasitic $C_{\rm se2}$ when sw-cap is off. It was only very recently that the common-mode return path got introduced into the RF oscillator design for the purpose of $1/f^2$ and $1/f^3$ PN reductions [44], [49], and [48]. The path carries the CM current (e.g., $I_{\rm H2}$) from the drain of M1/M2 to the source of M1/M2, and then back around. Hence, it is more appropriate to take the source node of the cross-coupled pair (VSOURCE) as a reference rather than VSS_A for the CM return path analysis. One part of the CM return path includes the implicit CM tank, decoupling capacitor network, and tail filter, while the other part goes directly through the transistor's intrinsic capacitance $C_{\rm se1}$ ($= C_{\rm ds1} + C_{\rm gs2}$ for CM signal), shown in Fig. 2.7(c). Note that the parasitic single-ended capacitance of the sw-cap bank ($C_{\rm se2}$) cannot be readily seen by the CM current, irrespective of whether the switch is on or off, since it is connected to a different supply (i.e., "digital") through a large wirebonding inductance. Therefore, for most properly constructed oscillators, their implicit CM tank would comprise only the CM

inductance of the main inductor. The on-chip decoupling capacitor network (L_{decap}, C_{decap}) needs to be properly constructed to provide a tight local return path for the CM current. However, its parasitic inductance L_{decap} is typically neglected by RF oscillator designers, often leading to detrimental effects on the flicker noise upconversion [48].

This consequence of neglecting the L_{decap} effects is becoming more critical now for mmW oscillator designs. As shown in Fig. 2.8(a), L_{decap} is modeled for different considerations of supply injection points ($\text{VDD}_{\text{inj1,2,3}}$). According to electromagnetic simulations in Fig. 2.8(c), the parasitic inductance could be neglected only when the injection point (VDD_{inj3}) is physically close to VSS. Fig. 2.8(b) offers an intuitive explanation. At very high frequencies, all the C_{unit} capacitors are seen as a short and so the LC network becomes inductive, resulting in VDD_{inj3} having the shortest return path. However, in the conventional mmW oscillator with a one-turn inductor, the supply injection point [VDD_A as shown in Fig. 2.7(a)] is physically far from VSS_A, thus introducing a significant inductance (several hundred pH). Finally, a parallel resonant LC tank can be seen by the CM current, [see Fig. 2.7(c)], in which the total CM inductance L_{cm} can be described as $L_{\text{diff}} + 2L_{\text{se}} + 2L_{\text{decap}} + 2L_{\text{tail}}$, while the total CM capacitance C_{cm} is only C_{se1}. Obviously, both the parasitic L_{decap} and the deliberate L_{tail} have a large influence on the CM resonant frequency (i.e., $1/(2\pi\sqrt{L_{\text{cm}}C_{\text{cm}}})$) in the mmW oscillator.

2.2.2 Flicker Noise Modulation and Upconversion

According to the theory of impulse sensitivity function (ISF) [35], the flicker noise upconversion from $\text{M}_{1/2}$ in Fig. 2.7 to phase noise involves two steps: 1) low-frequency voltage noise at the gate, $v_{1/f}$ at $\Delta\omega$ (e.g., 10 kHz), is modulated to cyclostationary current noise $i_{1/f,\text{cyclo}}$ around different harmonics $k\omega_0 \pm \Delta\omega$ through a noise modulation function (NMF) and 2) the current noise $i_{1/f,\text{cyclo}}$ turns into phase noise through its corresponding ISF.

It is well known that the flicker NMF is modeled by a time-varying transconductance [44]. However, this model only considers the $1/f$ noise mechanism due to the carrier number fluctuation (CNF), which means the carriers will be randomly trapped and released by impurities on the Si/SiO_2 interface. As CMOS technology scales, another $1/f$ noise mechanism, called correlated mobility fluctuation (CMF), is becoming increasingly important since the trapped electrons in a short channel will have a larger influence on Coulomb scattering of

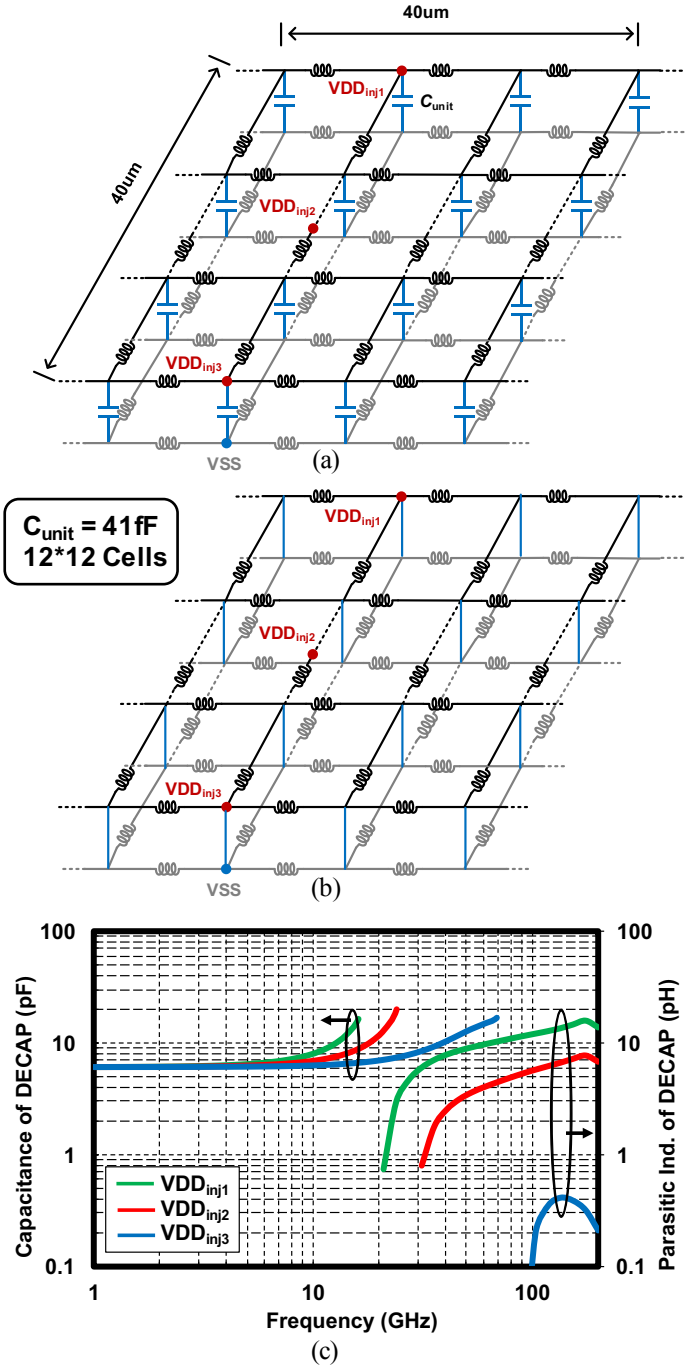

Figure 2.8: (a) Decoupling capacitor network for the proposed mmW oscillator. (b) High-frequency model of the decoupling capacitor network. (c) Effective parasitic inductance at different supply injection points.

neighboring free electrons, thus changing the average electron mobility (see Fig. 2.9). A more accurate $1/f$ noise model for the nanoscale CMOS considering both CNF and CMF was

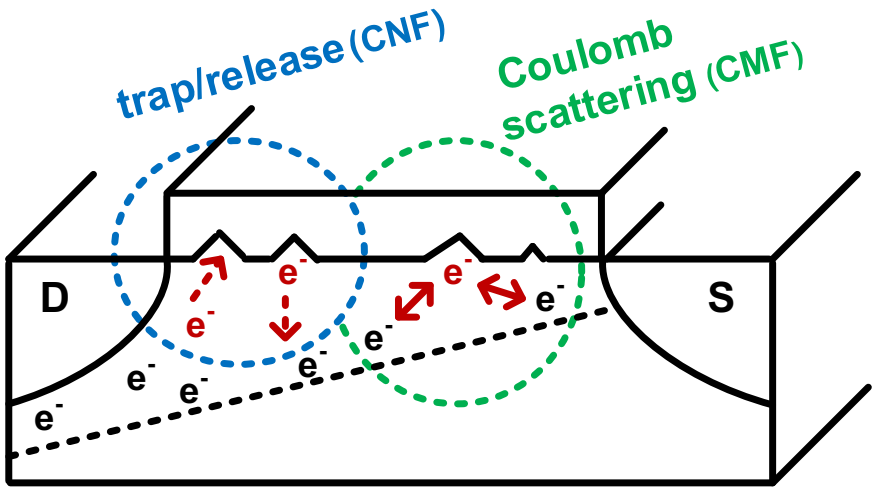

Figure 2.9: Newly discovered flicker noise mechanism in nanoscale CMOS [33].

verified in [33], which is described as:

$$\overline{I_{1/f}^2} = \overline{V_{1/f}^2} \times (g_\mathrm{m} + \Omega I_\mathrm{D})^2 \tag{2.1}$$

where $V_{1/f}^2 = \dfrac{K}{WL\Delta\omega}$ is the power spectral density (PSD) of flat-band voltage, K and Ω (unit: V^{-1}) are process parameters. The first and second terms in parentheses represent CNF and CMF, respectively. Thus, the flicker NMF $m(t)$ in nano-scale CMOS could be modified as periodically modulated transconductance and harmonic current:

$$m(t) = G_\mathrm{m}(t) + \Omega I_\mathrm{D}(t) \tag{2.2}$$

where $G_\mathrm{m}(t)$ and $I_\mathrm{D}(t)$ can be obtained by applying the discrete steady-state waveform point of V_GS, V_DS to dc simulations.

Assume the flicker gate-voltage noise $v_{1/f}$ at $\Delta\omega$ (e.g., 10 kHz) in $\mathrm{M}_{1/2}$ is expressed as

$$v_{1/f}(t) = \sqrt{2} V_{1/f,\mathrm{rms}} \cos(\Delta\omega t + \gamma) \tag{2.3}$$

where $V_{1/f,\mathrm{rms}}$ is rms value of $\overline{V_{1/f}^2}$, and γ is an initial random phase. Thus, the cyclostationary

flicker noise current is as follows:

$$\begin{aligned} i_{1/f,\text{cyclo}}(t) &= v_{1/f}(t) \times m(t) \\ &= \sqrt{2} I_{1/f,\text{rms}}(t) \cos(\Delta\omega t + \gamma) \end{aligned} \tag{2.4}$$

where $I_{1/f,\text{rms}}(t)$ ($\approx V_{1/f,\text{rms}} \times m(t)$) is the periodically modulated rms value of flicker current noise. It can be directly simulated by dc/NOISE simulations using the discrete waveform point of V_{GS} and V_{DS} from periodic steady-state (PSS) simulations, while the introduced model $V_{1/f,\text{rms}} \times m(t)$ is mainly used to intuitively and physically explain the complex behavior of $I_{1/f,\text{rms}}(t)$ in the large-signal operation and advanced CMOS technology.

Further, assume the non-normalized ISF h_{DS} associated with V_{DS} of $\text{M}_{1/2}$ is

$$h_{\text{DS}}(t) = \frac{1}{2} h_0 \cos\theta_{\text{h0}} + \sum_{1}^{N} h_k \cos\left(k\omega_0 t + \theta_{\text{h},k}\right) \tag{2.5}$$

where h_k and $\theta_{\text{h},k}$ are the magnitude and phase of k_{th} harmonic term, respectively. Note that θ_{h0} is either 0 or π depending on the sign of dc term h_{DS}. Thus, the phase noise is

$$\begin{aligned} \phi(t) &= \int_{-\infty}^{t} h_{\text{DS}}(\tau) \cdot i_{1/f,\,\text{cyclo}}(\tau) d\tau \\ &\approx \frac{\sqrt{2} h_{\text{eff,dc}}}{\Delta\omega} \sin\left(\Delta\omega t + \gamma\right) \end{aligned} \tag{2.6}$$

where $\phi(t)$ is mainly dominated by the slow frequency term, and $h_{\text{eff,dc}}$ is the dc value of non-normalized effective ISF $h_{\text{eff}}(t)$ ($= h_{\text{DS}}(t) \times I_{1/f,\text{rms}}(t)$), which is defined as

$$h_{\text{eff,dc}} = \frac{1}{T} \int_0^T h_{\text{DS}}(t) \cdot I_{1/f,\text{rms}}(t) dt \tag{2.7}$$

where $T(= 2\pi/\omega_0)$ is the oscillation period.

The phase noise $\phi(t)$ appears at V_{DS} of $\text{M}_{1/2}$, showing two correlated terms at $\omega_0 \pm \Delta\omega$,

$$\begin{aligned} V_{\text{DS}} \approx\ & V_{\text{H1}} \cos\left(\omega_0 t + \theta + \phi(t)\right) \approx V_{\text{H1}} \cos\left(\omega_0 t + \theta\right) \\ &+ \frac{V_{\text{H1}} \sqrt{2} h_{\text{eff,dc}}}{2\Delta\omega} \cos\left((\omega_0 + \Delta\omega) t + \theta + \gamma\right) \\ &- \frac{V_{\text{H1}} \sqrt{2} h_{\text{eff,dc}}}{2\Delta\omega} \cos\left((\omega_0 - \Delta\omega) t + \theta - \gamma\right) \end{aligned} \tag{2.8}$$

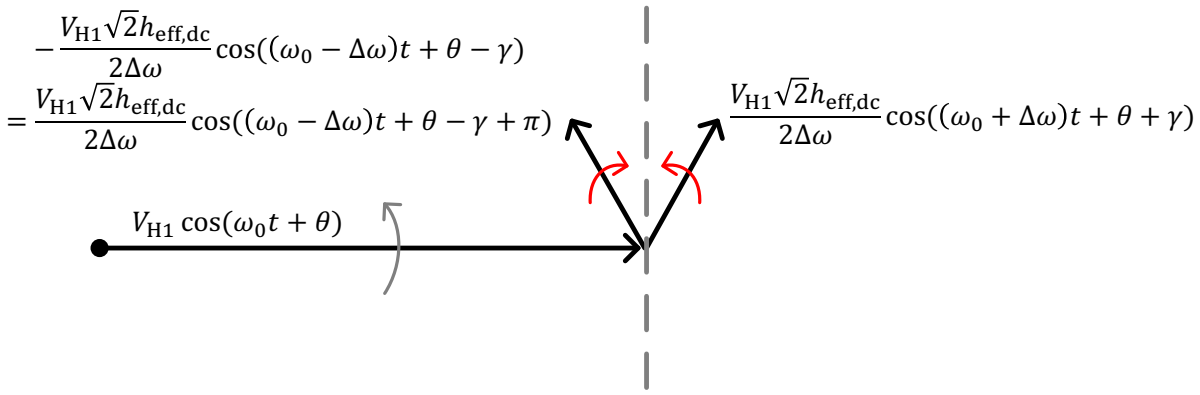

Figure 2.10: Phasor diagram of (2.8).

where V_{H1} and θ are the 1st harmonic amplitude and phase of V_{DS}, respectively. To gain more insight into (2.8), its phasor diagram is illustrated in Fig. 2.10, where it is evident that the two correlated terms (i.e., $\omega_0 \pm \Delta\omega$) can only modulate the phase of V_{DS}. Hence, the single-sideband to carrier ratio (SSCR) can be written as

$$\begin{aligned}\mathcal{L}(\Delta\omega) &= \frac{1}{2}\left(\frac{V_{\mathrm{H1}}\sqrt{2}h_{\mathrm{eff,dc}}}{2\Delta\omega}\right)^2 / \frac{1}{2}V_{\mathrm{H1}}^2 = \left(\frac{\sqrt{2}h_{\mathrm{eff,dc}}}{2\Delta\omega}\right)^2 \\ &= \left(\frac{\sqrt{2}}{2\Delta\omega}\cdot\frac{1}{T}\int_0^T h_{\mathrm{DS}}(t)\cdot I_{1/f,\,\mathrm{rms}}(t)dt\right)^2\end{aligned} \tag{2.9}$$

which is the flicker phase noise at $\omega_0 \pm \Delta\omega$ caused by a single transistor M1 or M2. The final SSCR caused by cross-coupled pair is $2 \times \mathcal{L}$. It is important to address an apparent non-physicality of (2.9): $h_{\mathrm{eff,dc}}^2$ itself is proportional to $1/\Delta\omega$, since $I_{1/f,\mathrm{rms}}^2(t)$ is proportional to $1/\Delta\omega$. Thus, $\mathcal{L}(\Delta\omega)$ is ultimately proportional to $1/\Delta\omega^3$.

2.2.3 Numerical Verification

To verify the proposed expression (2.9), it is necessary to get the periodically modulated rms value of flicker current noise $I_{1/f,\mathrm{rms}}(t)$ and non-normalized ISF $h_{\mathrm{DS}}(t)$. The former is based on the dc/NOISE simulations using the steady-state waveform point of V_{GS} and V_{DS} from PSS simulation (see Chapter 3). For the latter, it can be acquired by Periodic Transfer Function (PXF) simulations [86], which is more accurate and much faster than the conventional transient simulation method [35]. The linking equation between the non-normalized ISF and

positive sidebands of PXF is derived as follows [86]:

$$\begin{aligned} h_{\mathrm{DS}}(t) &= \frac{1}{2}\frac{4\Delta\omega|H(-1)|}{V_{\mathrm{H1}}}\cos[\theta - \angle H(-1)] \\ &+ \sum_{k=1}^{N}\frac{4\Delta\omega|H(k-1)|}{V_{\mathrm{H1}}}\cos\left[k\omega_0 t + \theta - \angle H(k-1)\right] \end{aligned} \tag{2.10}$$

where N is the number of harmonics for consideration, $k-1(=-1,0,1,2,...,N-1)$ is the index of positive sidebands of PXF, $H(k-1)$ represents $H(\omega_0+\Delta\omega+(k-1)\omega_0)$, and $|H(k-1)|$, $\angle H(k-1)$ are the magnitude and phase of periodic transimpedance, respectively. The magnitude V_{H1} and initial phase θ of 1st harmonic V_{DS} can be simulated by PSS with the Harmonic Balance (HB) engine, which solves for the steady-state of cosines rather than sines.

Both qualitative and quantitative analysis of flicker noise upconversion and reduction mechanisms of mmW oscillators are demonstrated in Figs. 2.11 and 2.12. By changing $L_{\mathrm{tail}}+L_{\mathrm{decap}}$ from 0 to 800pH, the 2nd harmonic current I_{H2} will enter the inductive path (e.g., $L_{\mathrm{tail}}+L_{\mathrm{decap}}=0$, I_{H2} mainly entering $2L_{\mathrm{se}}+L_{\mathrm{diff}}$), resistive path (i.e., $L_{\mathrm{tail}}+L_{\mathrm{decap}}=120\,\mathrm{pH}$, 2nd harmonic resonance), and capacitive path (e.g., $L_{\mathrm{tail}}+L_{\mathrm{decap}}=800\,\mathrm{pH}$, I_{H2} mainly entering C_{se1}), successively. As a consequence, it causes less steep falling parts of V_{DS}, symmetric rising/falling parts of V_{DS}, and less steep rising parts of V_{DS}, as illustrated in Figs. 2.11(a), (b), and (c), respectively[1]. Compared with a steeper edge, the flatter edge is vulnerable to noise due to its longer-time exposure to noise. Figs. 2.11(d)–(f) (blue lines) show the corresponding non-normalized ISF $h_{\mathrm{DS}}(t)$ based on PXF[2].

The periodically modulated flicker current noise $I_{1/f,\mathrm{rms}}(t)$ at 10 kHz models the process of flicker noise modulation, as shown in Fig. 2.11(a)-(c) (red lines). The flicker noise peaks in the regions where $M_{1,2}$ operates in saturation, (i.e., $t\approx 10\,\mathrm{ps}$ and 25 ps), while it also keeps relatively high levels in the triode region (i.e., $t\approx 12\,\mathrm{ps}$ to 22 ps). Although a complex BSIM flicker noise model is employed in the process development kit (PDK) of TSMC 28-nm technology, the CNF/CMF model could still be fairly accurate and provide a physical understanding about flicker noise behavior in large-signal operation. As a means of verifying

[1]An intuitive understanding about the waveform-shaping of V_{DS} due to the different terminations of harmonic currents (I_{H2} and I_{H3}) will be presented in the next subsection, which extends the analysis and clarifies the ambiguities in [44].

[2]Note that $h_{\mathrm{DS}}(t)$ is approximately proportional to the derivative of $V_{\mathrm{DS}}(t)$), in which only Fig. 2.11(e) shows a symmetric $h_{\mathrm{DS}}(t)$, due to the symmetric rising and falling portions of V_{DS} (2nd harmonic resonance).

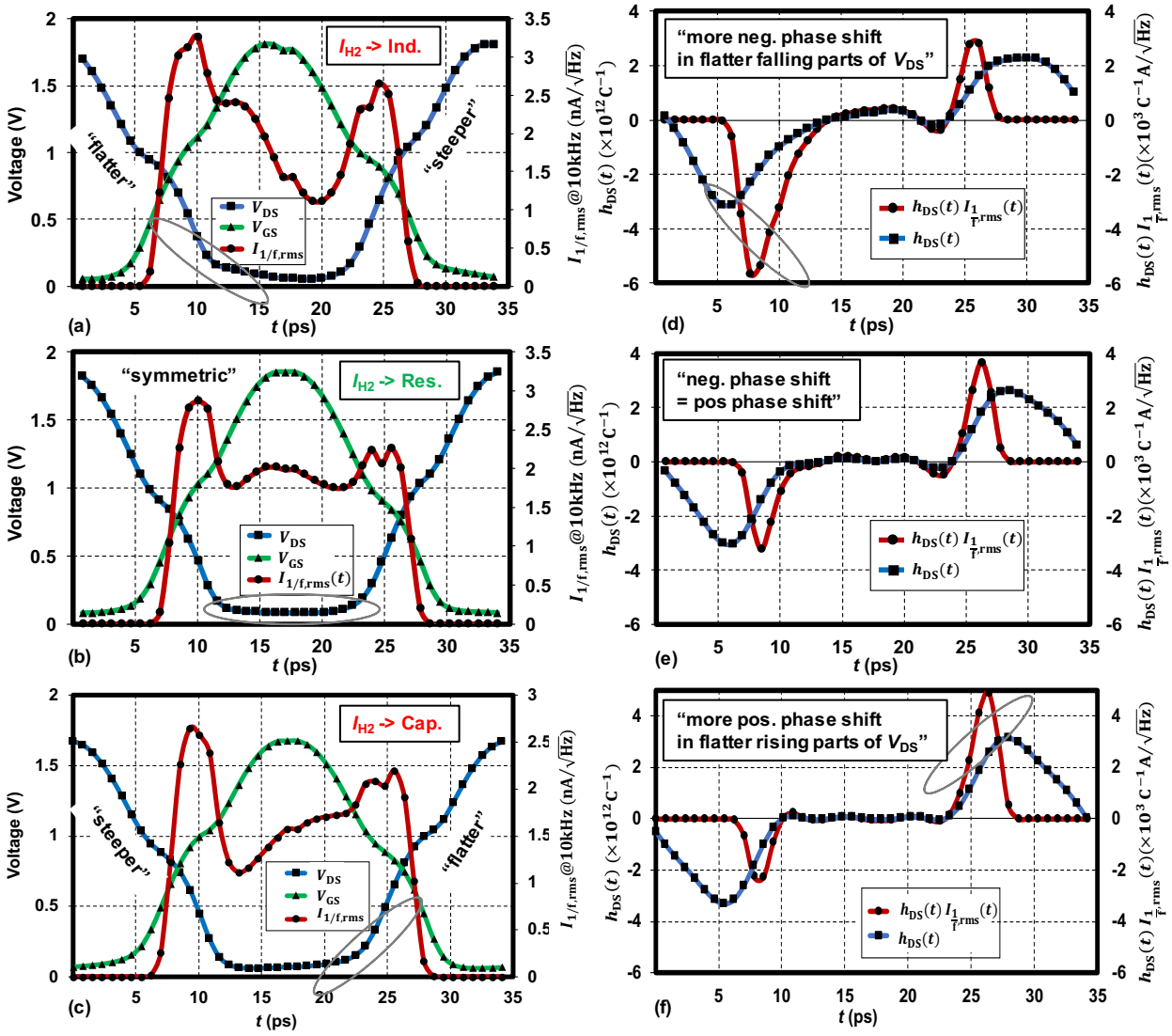

Figure 2.11: Discrete waveform points of $V_{\rm GS}$, $V_{\rm DS}$ in one period based on PSS simulations, and corresponding rms value of flicker current noise $I_{1/f,\rm rms}$ at 10 kHz based on dc/NOISE simulations: (a) $L_{\rm tail}+L_{\rm decap}=0$ pH ($I_{\rm H2}$ mainly entering inductive path (i.e., $2L_{\rm se}+L_{\rm diff}$)), (b) $L_{\rm tail}+L_{\rm decap}=$ 120 pH (2nd harmonic resonance, $I_{\rm H2}$ entering resistive path), (c) $L_{\rm tail}+L_{\rm decap}=800$ pH ($I_{\rm H2}$ entering capacitive path (i.e., $C_{\rm se1}$)) Non-normalized ISF function $h_{\rm DS}(t)$ based on PXF simulations and $h_{\rm DS}(t)\times I_{1/f,\rm rms}(t)$: (d) $L_{\rm tail}+L_{\rm decap}=0$ pH, (e) $L_{\rm tail}+L_{\rm decap}=120$ pH, (f) $L_{\rm tail}+L_{\rm decap}=800$ pH.

the efficacy of the adopted CNF/CMF model in (2.1), let us contrast it with the currently used CNF-only model by examining the flatness of $V_{1/f,\rm rms}(t)$ at $\Delta\omega/2\pi=10$ kHz in both cases. A quick inspection of Fig. 2.12 (a) reveals that $I_{1/f,\rm rms}(t)/(G_{\rm m}(t)+\Omega I_{\rm D}(t))$ is fairly constant. Conversely, $I_{1/f,\rm rms}(t)/G_{\rm m}(t)$ is far from being constant, which means that the presently used CNF model cannot accurately describe the physical flicker noise modulation

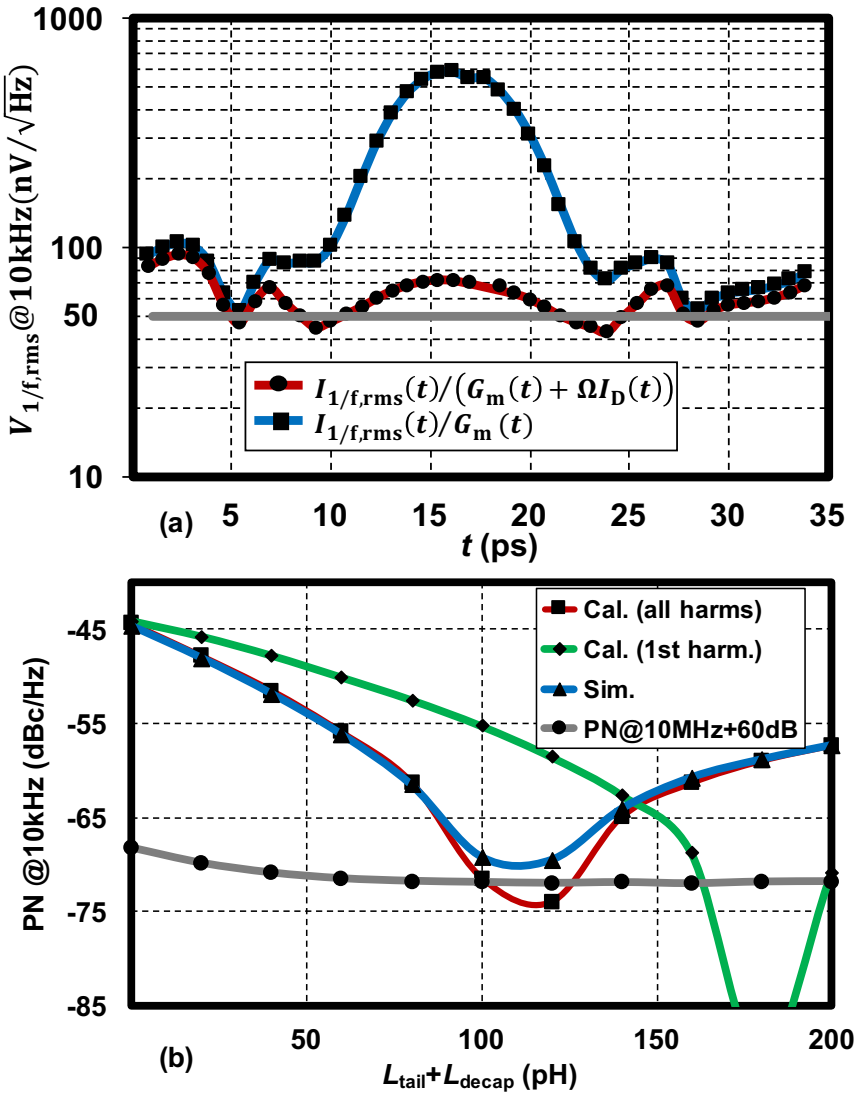

Figure 2.12: (a) Verification of flicker noise model. (b) Numerical verification of PN @10 kHz.

process of oscillators in nanoscale CMOS technology.

The effective non-normalized ISFs $h_{\text{eff}}(t)$ $(= h_{\text{DS}}(t)I_{1/f,\text{rms}}(t))$ are shown in Fig. 2.11(d)-(f) (red lines, the area of $h_{\text{eff}}(t)$ represents phase shift of V_{DS}). It is obvious that the flicker noise mainly affects the phase noise in the two saturation regions, having an opposing influence on the phase change of V_{DS} in each region. As shown in Fig. 2.11(d) (I_{H2} enters the inductive path), phase change in the flatter falling part of V_{DS} (i.e., negative area of $h_{\text{eff}}(t)$, grey circle) is much larger than phase change in the steeper rising part (i.e., positive area of $h_{\text{eff}}(t)$), which means $h_{\text{eff,dc}} \neq 0$, i.e., a flicker noise upconversion. The opposite phenomenon happens when the 2nd harmonic enters the capacitive path, where the positive area of $h_{\text{eff}}(t)$ (i.e., positive

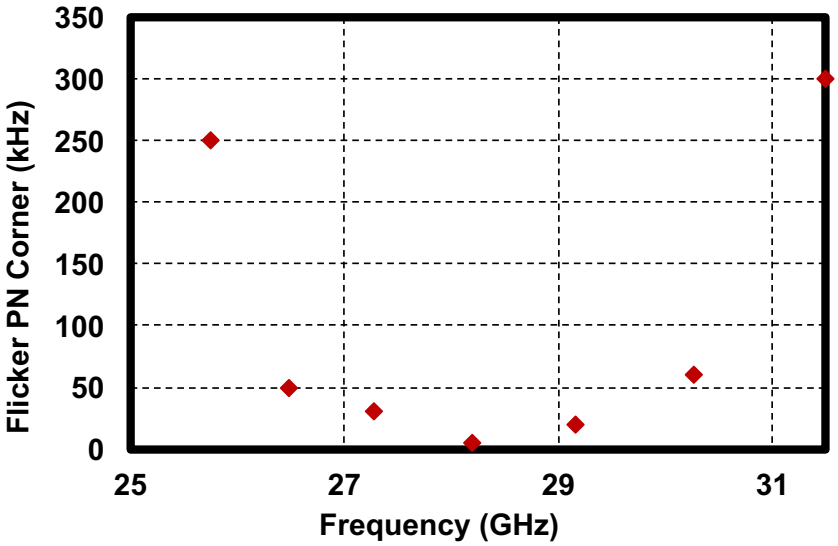

Figure 2.13: Simulated flicker-noise corner across tuning range (TR) in the conventional mmW oscillator ($L_{\text{tail}} + L_{\text{dec}} = 120\text{pH}$). The $1/f^3$ PN corner maintains $\leq$100 kHz within 15% TR, while it significantly worsens when widening the TR.

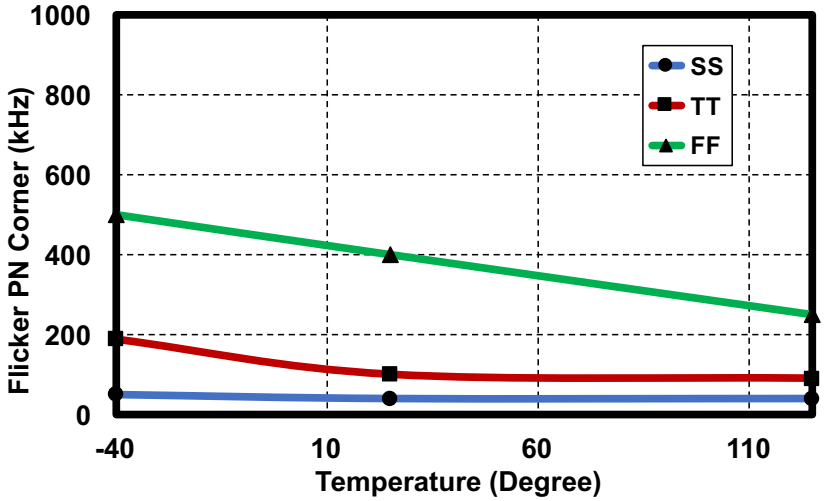

Figure 2.14: Simulated flicker-noise corner versus temperature at different process corners in the conventional mmW oscillator ($L_{\text{tail}} + L_{\text{dec}} = 120\text{pH}$).

phase change) is larger than its negative area (i.e., negative phase change) [see Fig. 2.11(f)], still leading to flicker noise upconversion. However, forcing the 2nd harmonic current to enter the resistive path would make the rising and falling parts of V_{DS} more symmetric (as shown in Fig. 2.11(e)), causing the phase change in the two regions to cancel each other within one period (i.e., $h_{\text{eff,dc}} = 0$).

It is necessary to point out that the other flicker noise reduction mechanisms, i.e., the

introduction of phase shift between $V_{\rm DS}$ and $V_{\rm GS}$ [65] and the narrowing of the conduction angle [75, 86], can also be explained by $h_{\rm DS}(t)$ and $I_{1/f,\rm rms}(t)$. For the former, it is because the positive and negative areas of $h_{\rm eff}(t)$ can be adjusted to be equal by the phase shift between $h_{\rm DS}(t)$ (mainly depending on $V_{\rm DS}$) and $I_{1/f,\rm rms}(t)$ (mainly relying on $V_{\rm GS}$). However, the positive or negative phase shift of $V_{\rm GS}$ (taking $V_{\rm DS}$ as a reference) depends on capacitive or inductive terminations of $I_{\rm H2}$ (see Fig. 2.11), which were not discussed in [65]. An alternative approach would be to use a transformer to introduce a negative phase shift of secondary winding (i.e., $V_{\rm GS}$), compared with its primary winding (i.e., $V_{\rm DS}$), and also force the $I_{\rm H2}$ to enter the inductive path. For the latter, the narrowing conduction angle [75, 86] will decrease the $I_{1/f,\rm rms}(t)$ exposure to the unbalanced $h_{\rm DS}(t)$ (lack of the 2nd harmonic resonance) to suppress the flicker noise upconversion (see Chapter 3).

The resulting phase noise at 10 kHz offset, shown in Fig. 2.12(b), shows an almost perfect agreement between the calculations ($N = 7$, red line) based on (2.9) and simulations ($N = 10$, blue line), thus demonstrating the effectiveness of the proposed theory. Note that merely considering the phase noise contribution from the 1st harmonic ISF (green line) cannot provide the required match to the simulations, except for the single point where $L_{\rm tail} + L_{\rm decap} = 0$ pH (i.e., Van der Pol oscillator [64]). The thermal PN at 10 kHz (represented by "PN @10 MHz + 60 dB") can be suppressed as long as $L_{\rm tail} + L_{\rm decap}$ is large enough, suppressing the "loaded-Q" effect no matter whether the 2nd harmonic resonance happens or not (grey line) (see [22] and [36]). Thus, if the 2nd harmonic resonance is difficult to achieve, a general rule to improve the thermal PN is to increase the CM impedance, including decreasing the CM capacitance (e.g., separating the supplies of sw-caps and the oscillator [51]) and increasing the CM inductance (e.g., adding long-tail inductor [22]).

It is worthwhile to calculate the PN at 10 kHz by replacing the precise simulated value of $I_{1/f,\rm rms}(t)$ with the best-fit CNF/CMF model: $50\,\text{nV}/\sqrt{\text{Hz}} \times [G_{\rm m}(t) + \Omega I_{\rm D}(t)]$ with $\Omega = 3\,\text{V}^{-1}$, as calculated during the non-cut-off region (i.e., from 6ps to 28ps) and indicated as the grey curve in Fig. 2.12 (b). When $L_{\rm tail} + L_{\rm decap} = 0$ pH, the PN @10 kHz based on CNF/CMF model is -43.73 dBc/Hz, while the accurate PDK result is -44.35 dBc/Hz (i.e., using $I_{1/f,\rm rms}(t)$). As mentioned, the CNF/CMF model shows good accuracy for quantitative analysis and also helps designers to understand intuitively the complex behavior of modulated flicker noise. Of course, the most accurate quantitative analysis is still with the simulated $I_{1/f,\rm rms}(t)$, but the demonstrated accuracy of the flicker PN prediction in (2.1) is within 1 dB

of the simulation.

Fig. 2.13 shows the relationship between the simulated flicker noise corner and the tuning range (TR), where $L_{\text{tail}} + L_{\text{decap}} = 120\,\text{pH}$ and the resonance frequency of the implicit CM tank is around $2\times28.5\,\text{GHz}$. Within a 15% TR, the flicker PN corner can be kept lower than 100kHz (especially, no flicker noise upconversion at 28.5 GHz due to 2nd harmonic resonance), then it would significantly worsen. Obviously, the 2nd harmonic resonance suppressing the flicker noise upconversion is a narrow-band technique. As for the PVT robustness of the 2nd harmonic resonance, temperature changes have less effects on the flicker noise corner, while the variation of technology process could shift the flicker noise corner a lot. This is because the resonance frequency of both DM and CM tanks would shift in the same direction due to temperature, while the threshold voltage changes with the process corner would have a large influence on the voltage-biased oscillator. Further, the optimum L_{tail}+L_{decap} for the 2nd harmonic resonance is only $\sim$120 pH, since the inductance in the implicit CM tank $L_{\text{diff}} + 2L_{\text{se}}$ is already dominant. Unfortunately, due to the physical distance between VDD_A and VSS_A in conventional mmW oscillators, the $L_{\text{tail}} + L_{\text{decap}}$ could hardly be made less than 200 pH, which means mmW designers would have difficulties in forcing the 2nd harmonic current to enter the resistive path to suppress the flicker noise. Therefore, for mmW oscillators, the CM return path should be properly constructed for accurate harmonic termination.

2.2.4 Intuitive Understanding of Waveform-Shaping Due to Different Terminations of Harmonic Currents

In the previous subsection, we claimed that the falling part of V_{DS} will be flatter (more vulnerable to noise) than its rising part when I_{H2} enters the inductive path, while its rising part will become flatter when I_{H2} enters the capacitive path. To understand these types of waveform-shaping due to the different terminations of harmonic currents, it is necessary to establish the phase relationship between harmonic currents. Fig. 2.15(a) models the condition that a MOS transistor is operating in the cross-couple pair of a voltage-biased oscillator (i.e., the phase difference between V_{DS} and V_{GS} is π, taking V_{DS} as reference), in which the harmonic currents of a MOS transistor come from its non-linearity. With the input amplitude of the sinusoidal signal (i.e., V_{H1}) increasing, the transistor will work first in

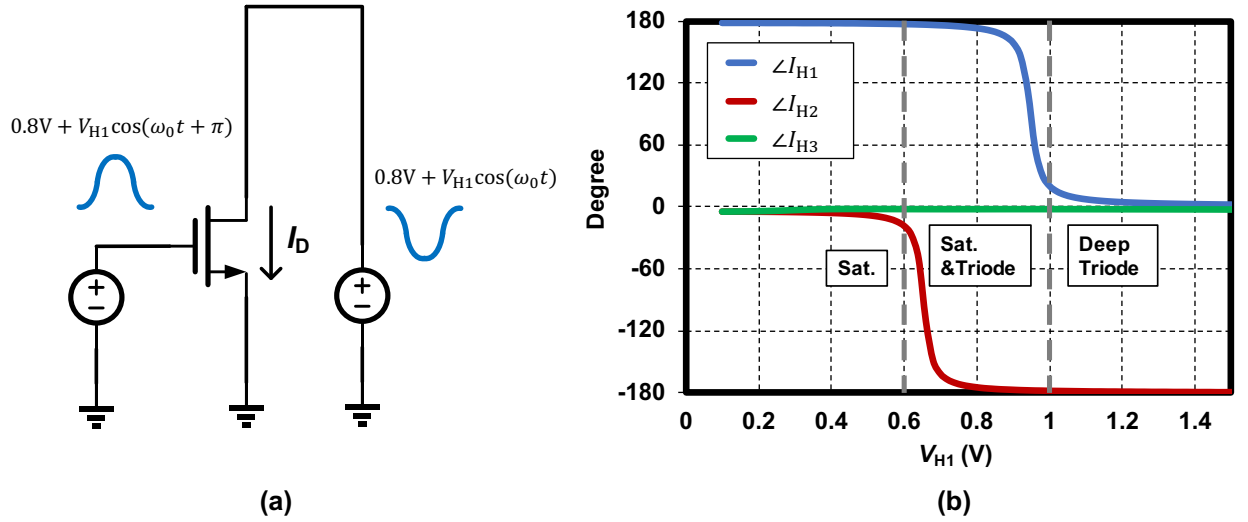

Figure 2.15: (a) Test-bench for studying phase relationship between harmonic currents ($I_{H1,2,3}$) and V_{DS}. (b) PSS simulation results (phase degrees are calculated from cosines).

saturation (i.e., $V_{H1} < 0.6\,V$), then in saturation and triode (i.e., $0.6\,V < V_{H1} < 1\,V$), and finally in the deep triode regions (i.e., $V_{H1} > 1\,V$), respectively [see Fig. 2.15(b)]. Before the transistor enters the deep-triode region (i.e., $V_{H1} < 1V$), I_{H1} is in-phase with V_{GS} (in fact, due to the Groszkowski effect [68], there will still be a small difference between $\angle V_{GS}$ and $\angle I_{H1}$, see [50]), but out-of-phase with V_{DS}, behaving as a "negative resistor" for V_{DS}. However, for $\angle I_{H2}$, it is 0° in saturation, but -180° in the saturation and triode regions, while $\angle I_{H3}$ is always 0°. For the voltage-biased oscillator, the swing of V_{DS} and V_{GS} will be same as the supply voltage (e.g., 0.8 V), forcing the transistor to operate in the saturation and triode regions, thus, the harmonic current is derived as

$$I_D = I_{H0} + I_{H1}\cos(\omega_0 t + \pi) + I_{H2}\cos(2\omega_0 t - \pi) + I_{H3}\cos(3\omega_0 t) \tag{2.11}$$

where the direction of current entering the MOS transistor is assumed as "positive", $I_{H1,2,3}$ represent the magnitude of the 1st, 2nd, and 3rd harmonic voltages, respectively. I_D injects into the DM ($I_{H1,3}$) and CM tanks (I_{H2}); hence the sinusoidal V_{DS} will be affected.

For simplicity, let us study the effects of the 2nd harmonic current first. The harmonic voltage, considering 1st and 2nd harmonic currents (i.e., $V_{DS,H1,2}(= -I_D \times Z_{DM\text{ or }CM})$), is

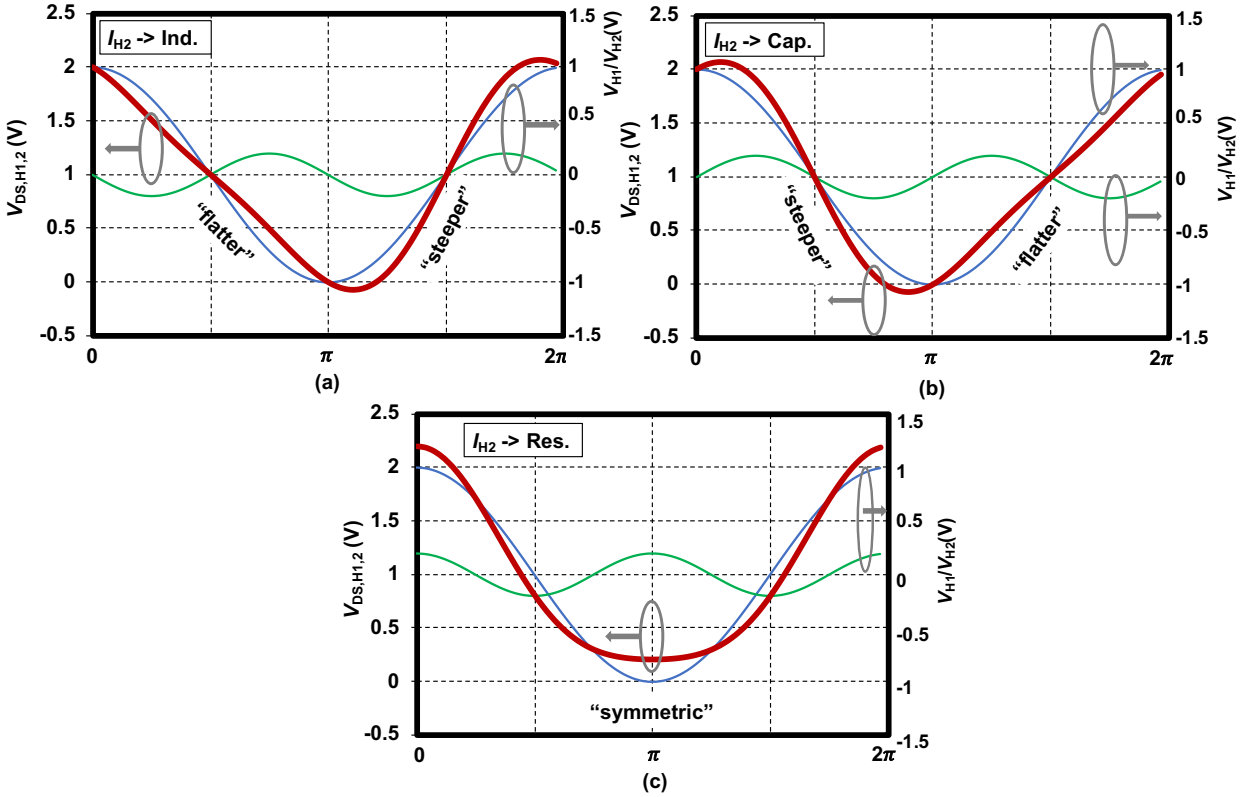

Figure 2.16: Waveform shaping due to different terminations of I_{H2}. (a) Flatter falling part due to inductive termination. (b) Flatter rising part due to capacitive termination. (c) Symmetric rising and falling parts due to resistive termination.

derived as

$$V_{\mathrm{DS,H1,2}} \approx \begin{cases} V_{\mathrm{H0}} + V_{\mathrm{H1}} \cos\omega_0 t + V_{\mathrm{H2}} \cos(2\omega_0 t + \dfrac{\pi}{2}), & I_{\mathrm{H2}} \text{-> Ind.} \\ V_{\mathrm{H0}} + V_{\mathrm{H1}} \cos\omega_0 t + V_{\mathrm{H2}} \cos 2\omega_0 t, & I_{\mathrm{H2}} \text{-> Res.} \\ V_{\mathrm{H0}} + V_{\mathrm{H1}} \cos\omega_0 t + V_{\mathrm{H2}} \cos(2\omega_0 t - \dfrac{\pi}{2}), & I_{\mathrm{H2}} \text{-> Cap.} \end{cases} \tag{2.12}$$

where $V_{\mathrm{H0,1,2}}$ are the magnitude of dc, 1st, and 2nd harmonic voltages. Fig. 2.16 shows the waveform shaping of V_{DS} when I_{H2} enters different terminations, in which we assume $V_{\mathrm{H0}} = 1\mathrm{V}$, $V_{\mathrm{H1}} = 1\mathrm{V}$, and $V_{\mathrm{H2}} = 0.2\mathrm{V}$.[1] Similar as in the simulation results in Figs. 2.11(a)-(c), the falling edge will become flatter when I_{H2} enters the inductive path, while rising edge will become flatter when I_{H2} enters the capacitive path.

The 3rd harmonic current will enter the capacitive path for most inductor-based oscillators,

[1]The phase relationship between V_{H1} and V_{H2} in Figs. 5(a) and 6(a) of Shahmohammadi's work [44] may not be correct.

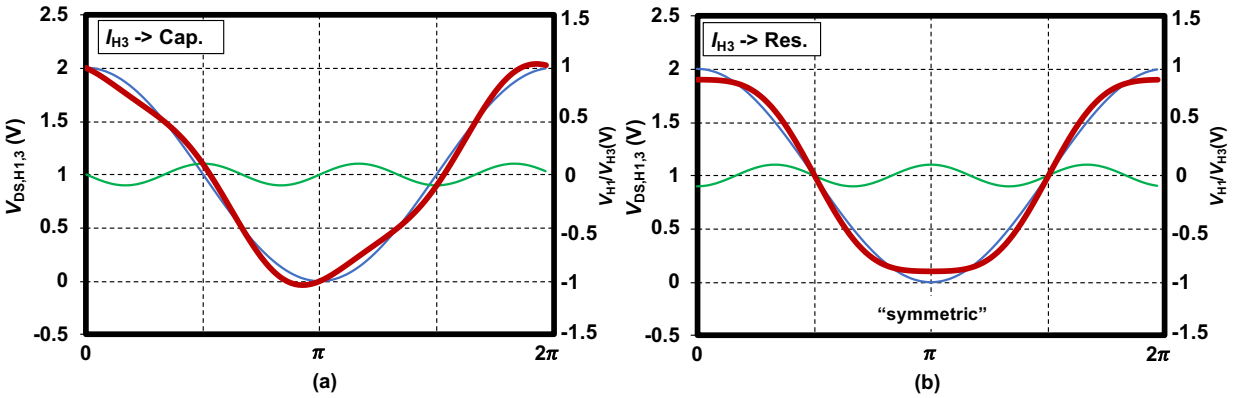

Figure 2.17: Waveform shaping due to different terminations of I_{H3}. (a) Capacitive termination of I_{H3}. (b) Symmetric rising and falling parts due to resistive terminations.

since it sees the same DM tank as I_{H1} (entering resistive path). However, in class-F oscillators [51], it could enter the resistive path. Thus, the harmonic voltage considering the 1st and 3rd harmonic current (i.e., $V_{\mathrm{DS,H1,3}}(=-I_{\mathrm{D}}\times Z_{\mathrm{DM}})$) is as follows,

$$V_{\mathrm{DS,H1,3}} \approx \begin{cases} V_{\mathrm{H0}} + V_{\mathrm{H1}}\cos\omega_0 t + V_{\mathrm{H3}}\cos(3\omega_0 t + \pi), & I_{\mathrm{H3}}\text{ -> Res.} \\ V_{\mathrm{H0}} + V_{\mathrm{H1}}\cos\omega_0 t + V_{\mathrm{H3}}\cos(3\omega_0 t + \dfrac{\pi}{2}), & I_{\mathrm{H3}}\text{ -> Cap..} \end{cases} \tag{2.13}$$

The waveform shaping due to the capacitive and resistive terminations of I_{H3} is shown in Figs. 2.17(a) and (b), respectively, where we assume $V_{\mathrm{H3}} = 0.1\mathrm{V}$. Compared with the I_{H2} entering capacitive path (see Fig. 2.16(b)), the capacitive termination of I_{H3} will have much less effects on the symmetries between the rising and falling edges of V_{DS}, since it is the peak and bottom (*slow* change) of V_{H3} (green line) (rather than "transition" edge (*fast* change) like V_{H2}) appearing at the falling and rising edges of V_{H1}. Recently, Pepe *et al.* [42] have theoretically demonstrated that the non-resistive termination of I_{H3} has nothing to do with the flicker noise upconversion.

2.3 Circuit Description

In [23], a class-F oscillator (first introduced in [70]) with a 3rd harmonic extraction has demonstrated low $1/f^2$ PN at mmW frequencies. However, the $1/f^3$ PN corner still exceeds to 1 MHz. In [44], a class-F_{23} oscillator has achieved both low $1/f^2$ PN and low $1/f^3$ PN corner at carrier frequencies below 7 GHz. Unfortunately, direct application of those techniques

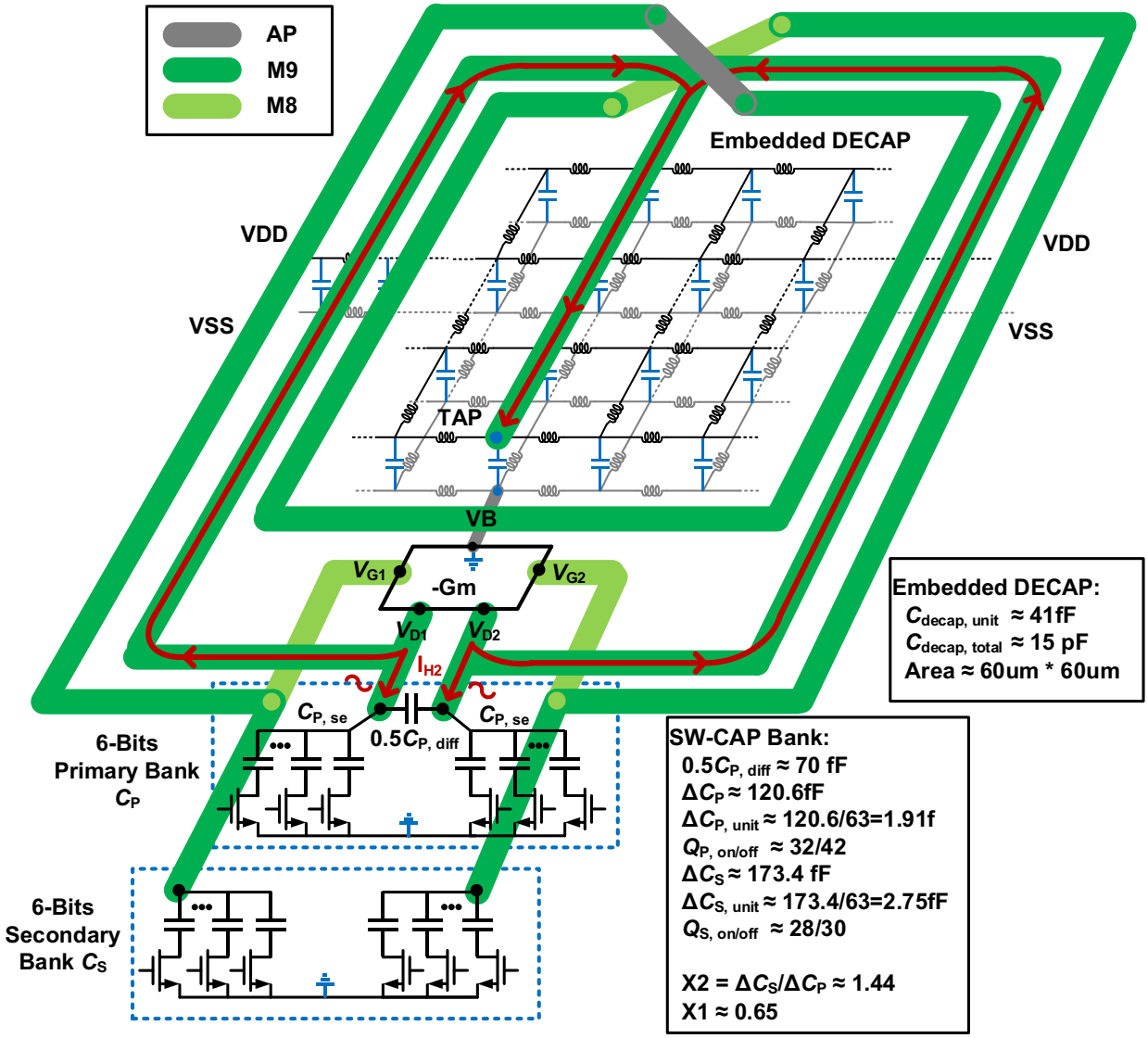

Figure 2.18: Proposed layout of class-F_{23} oscillator with embedded decoupling capacitor and the design switched-capacitor banks.

at mmW frequencies may not deliver the same level of $1/f^3$ performance. In this section, we demonstrate the proposed class-F_{23} oscillator with the 3rd harmonic extraction, which achieves both the best-in-class $1/f^2$ PN and record low $1/f^3$ PN corner at mmW frequencies. As discussed in Section II, the uncontrolled return path of the 1:2 transformer could shift the desired CM resonance which will lead to the degradation of the $1/f^3$ corner. To solve the above issue, the proposed class-F_{23} oscillator employs a transformer with an explicit CM return path using an embedded decoupling capacitor [50]. The detailed circuit operation of the oscillator as well as details of the transformer with embedded decoupling capacitor and

the capacitor bank design will be discussed below.

2.3.1 Operational Principle of Class-F_{23} Oscillator

Fig. 2.6 showed the circuit schematic of the proposed class-F_{23} oscillator, while the proposed layout is presented in Fig. 2.18. The oscillator exploits the 3rd harmonic resonance in the DM tank (class-F_3 operation), and the 2nd harmonic resonance in the CM tank (class-F_2 operation). The former deals with the DM tank, including the primary DM inductance $L_{\mathrm{P,\,dm}}$ ($= L_{\mathrm{P,\,diff}}$), secondary DM inductance $L_{\mathrm{S,\,dm}}$ ($= L_{\mathrm{S,\,diff}}$), DM magnetic coupling factor k_{dm}, primary DM capacitance $C_{\mathrm{P,\,dm}}$ ($= C_{\mathrm{P}}$), and secondary DM capacitance $C_{\mathrm{S,\,dm}}$ ($= C_{\mathrm{S}}$). According to [70], the fundamental frequency ω_0 can be approximately derived as: $\omega_0 = 1/\sqrt{L_{\mathrm{P,\,diff}}C_{\mathrm{P}} + L_{\mathrm{S,\,diff}}C_{\mathrm{S}}}$, while the ratio betwen two DM resonance frequencies ω_3/ω_0 is determined by

$$\frac{\omega_3}{\omega_0} = \sqrt{\frac{1 + X + \sqrt{1 + X^2 + X(4k_{\mathrm{dm}}^2 - 2)}}{1 + X - \sqrt{1 + X^2 + X(4k_{\mathrm{dm}}^2 - 2)}}} \tag{2.14}$$

where $X = (L_{\mathrm{S,diff}}C_{\mathrm{S}})/(L_{\mathrm{P,diff}}C_{\mathrm{P}})$. Thus, for the assumed 1:2 turns-ratio transformer (given $L_{\mathrm{S,diff}}/L_{\mathrm{P,diff}}$), through tuning of the secondary-to-primary capacitor ratio X_2 ($= C_{\mathrm{S}}/C_{\mathrm{P}}$), the $\omega_3/\omega_0 = 3$ condition can be achieved for the class-F operation. Note that k_{dm} is generally chosen around 0.61 to get a strong 3rd harmonic [23]. Due to the low CM coupling factor k_{cm}, only the primary CM tank is considered [44], which includes the primary CM inductance $L_{\mathrm{P,cm}}$ ($= L_{\mathrm{P,\,diff}} + 2L_{\mathrm{P,\,se}}$) and the primary CM capacitance $C_{\mathrm{P,\,cm}}$ ($= C_{\mathrm{P,\,se}}$). Thus, the CM resonance frequency ω_2 is $1/\sqrt{(L_{\mathrm{P,\,diff}} + 2L_{\mathrm{P,\,se}})C_{\mathrm{P,se}}}$. The ratio between ω_2 and ω_0 is derived as follows:

$$\frac{\omega_2}{\omega_0} = \sqrt{\frac{L_{\mathrm{P,\,diff}}C_{\mathrm{P}} + L_{\mathrm{S,\,diff}}C_{\mathrm{S}}}{(L_{\mathrm{P,\,diff}} + 2L_{\mathrm{P,\,se}})C_{\mathrm{P,se}}}} = \sqrt{\frac{L_{\mathrm{P,\,diff}} + L_{\mathrm{S,\,diff}}X_2}{(L_{\mathrm{P,\,diff}} + 2L_{\mathrm{P,\,se}})X_1}} \tag{2.15}$$

where X_1 ($= C_{\mathrm{P,se}}/C_{\mathrm{P}}$) is the ratio of CM capacitance in the primary tank. Through tuning of X_1 to the $\omega_2/\omega_0 = 2$ condition, class-F_2 operation can be achieved. Thus, the secondary-to-primary capacitor ratio (X_2) helps in achieving class-F_3 operation, forcing the 3rd harmonic current to enter the resistive path, thus boosting the 3rd harmonic voltage. On the other hand, the primary CM capacitance ratio (X_1) enables the class-F_2 operation, forcing the 2nd harmonic current to enter the resisitive path, thus maintaining the symmetry between the rising and falling parts of the output waveform, and ultimately helping to reduce the flicker noise upconversion.

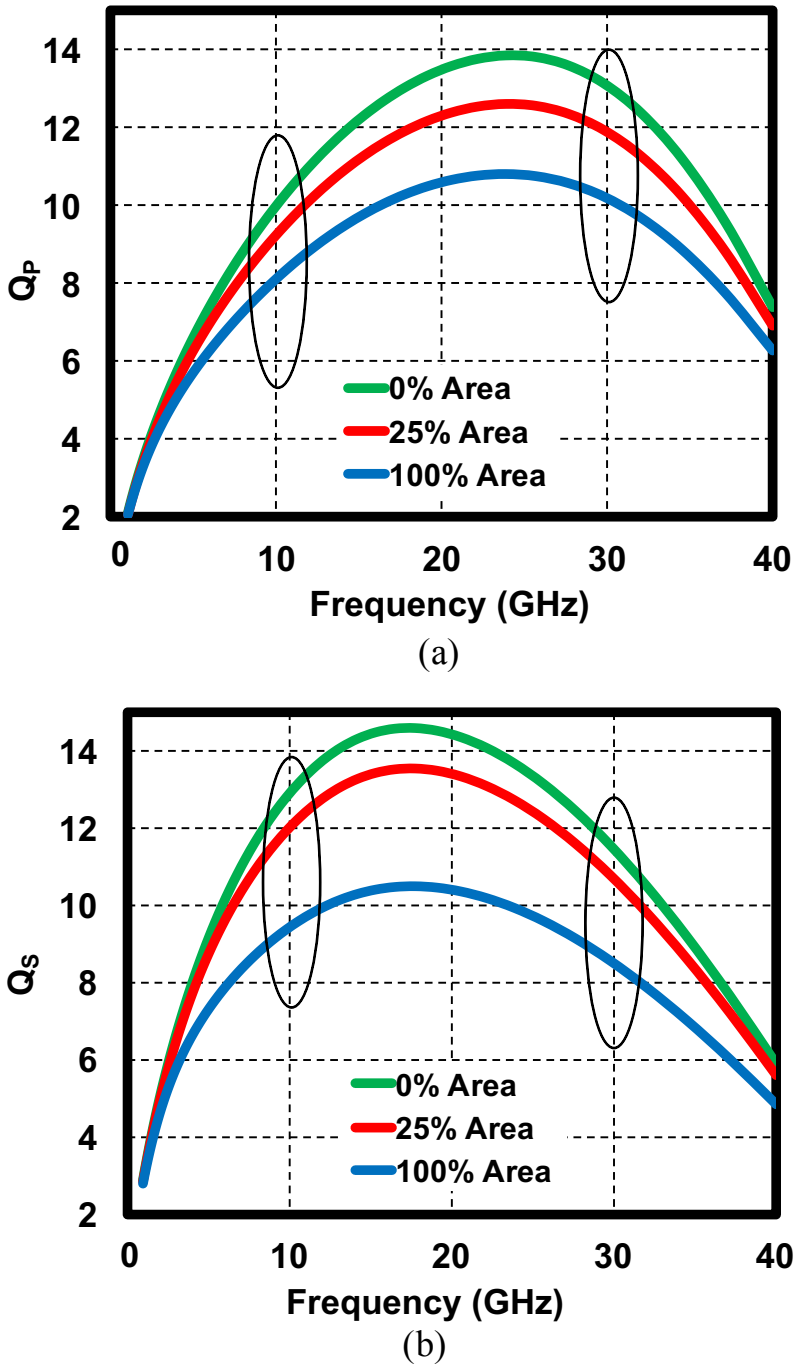

Figure 2.19: Trade-offs between the area of embedded decoupling capacitor and (a) quality factor of the primary coil, and (b) quality factor of the secondary coil.

2.3.2 Proposed Transformer with Embedded Decoupling Capacitor for Explicit CM Return Path

To explicitly define the CM return path, the proposed 1:2 transformer with the embedded decoupling capacitor is shown in Fig. 2.18. By bringing the tap of primary coil as close as

practically possible to the source node of the MOS transistors, the shortest return path for the CM current can be achieved. According to the study shown in Fig. 2.8, the parasitic inductance of the embedded decoupling capacitor network can be safely neglected, thus allowing for the CM inductance L_{cm} to be modeled accurately. The size of the 1:2 transformer is optimized for the intended operating frequency to achieve a high Q-factor but without too much coupling to the substrate. In this work, the self-resonant frequency (where DM coupling factor k_{dm} reaches 0) is about 5× of the operating frequency. Thus, the outer diameter of the transformer is chosen as 220 μm (see Fig. 2.20), with the self-resonance at ∼50 GHz. The coil width is set at 10 μm with consideration of skin effect, while the coil space is 7 μm to make k_{dm} about 0.63. It is well recognized that placing the embedded decoupling capacitor inside the coil may degrade the Q-factor. From the EM simulation (see Fig. 2.19), if the decoupling capacitor area is less than 25% of the coil's internal area, the degradation would be about 1 without affecting the inductance or coupling factor. On the other hand, the embedded decoupling capacitor should still be large enough to provide the short path for the CM current, which is 15 pF in this case. According to simulations using the circuit model in Fig. 2.6, X_2 is about 1.44 to get the 3rd harmonic resonance. It means that

$$\frac{C_{\mathrm{S,\,min}}}{C_{\mathrm{P,\,min}}} = \frac{C_{\mathrm{S,\,max}}}{C_{\mathrm{P,\,max}}} = \frac{\Delta C_{\mathrm{S}}}{\Delta C_{\mathrm{P}}} = X_2. \tag{2.16}$$

Two 6-bit single-ended capacitor banks $C_{\mathrm{P,\,se}}$ and $C_{\mathrm{S,\,se}}$ are designed for the primary and secondary banks (shown in Fig. 2.18), in which $\Delta C_{\mathrm{P}} = 120.6$ fF and $\Delta C_{\mathrm{S}} = 173.4$ fF. The quality factor of the capacitor banks is about 30 at 10 GHz, thus facilitating the overall high Q-factor of the tank. A fixed differential capacitor of $0.5C_{\mathrm{P,\,diff}}$ (=70 fF) is placed in the primary tank, to enable the 2nd harmonic resonance when the sw-cap control word is in the middle (= 32 for the 6-bit code), which makes X_1 about 0.65. For a more accurate control of the CM resonance, the fixed differential capacitor can be replaced with several bits of the differential capacitor bank [49].

2.3.3 Third Harmonic Extraction Using Two-Stage 30-GHz PA(Buffer)

As shown in Fig. 2.6, a two-stage 30 GHz PA (buffer) is used to boost the 3rd harmonic signal and to suppress the fundamental and 2nd harmonics [23, 73].The passive ac-coupling circuit (R_{ac} and C_{ac}) is inserted between the oscillator and PA. C_{ac} is chosen ∼10× of the

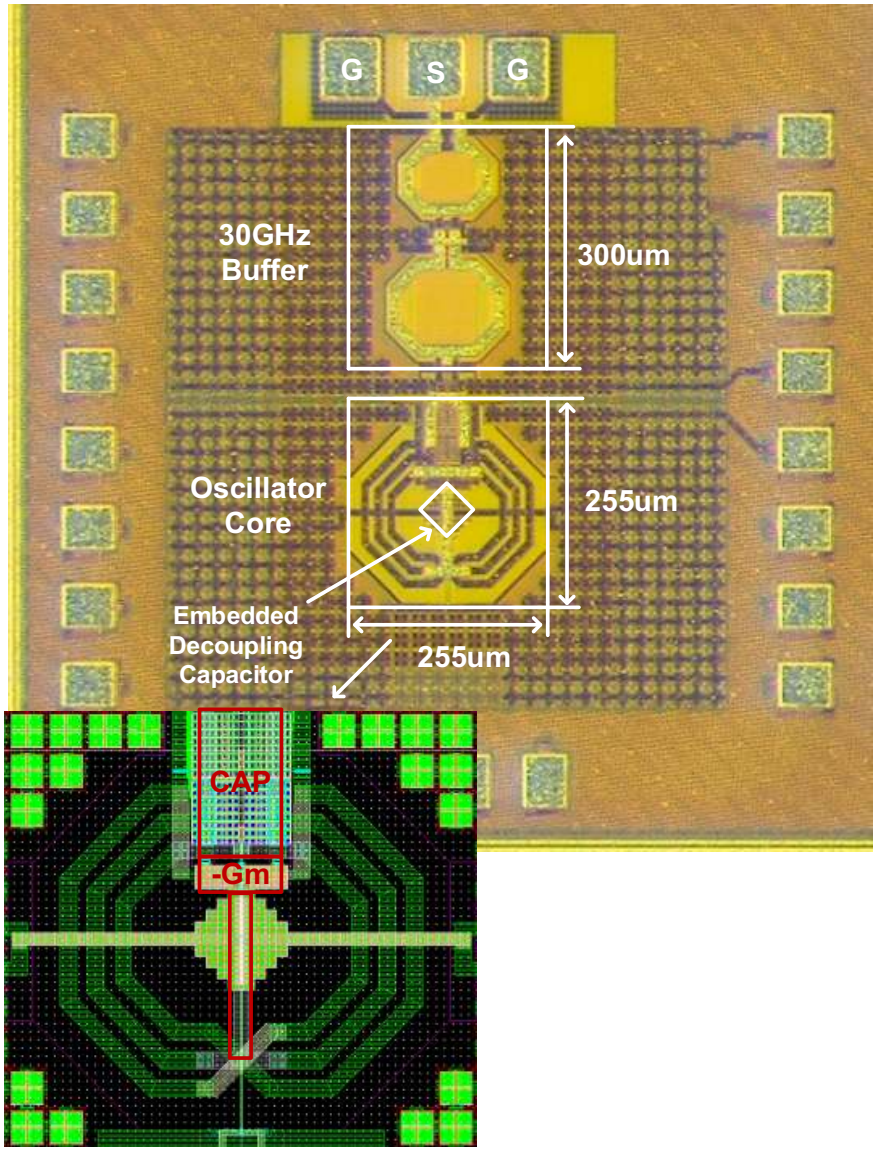

Figure 2.20: Chip micrograph and zoomed-in layout area of the embedded decoupling capacitor network.

input capacitance of 1st stage PA, and R_{ac} ($= 50\,\text{k}\Omega$) is chosen large enough to make the corner frequency much lower than the oscillator output frequency to ensure low coupling losses. Two 1:1 transformers (T2 and T3) vertically stack two one-turn inductors (M9 for the primary coil, and AP for the secondary coil). They are used for coupling between the 1st and 2nd stages, and also to the GSG (ground-signal-ground) PAD (see Fig. 2.20). To decrease the insertion loss in each transformer for the given frequency (i.e., 30 GHz), the diameter of the transformer's coils is optimized for high Q-factor. With the help of EM simulations, the diameters of T2 and T3 are chosen around $120\,\mu$m. Two tuning capacitors ($C_{\text{tune1}} =$

Table 2.1: Performance comparison with state-of-the-art RF and mmW oscillators.

		JSSC'17 [44]	JSSC'13 [60]	JSSC'16 [39]	JSSC'13 [65]	ESSCIRC'15 [66]	ESSCIRC'15 [64]	JSSC'16 [20]	A-SSCC'15 [62]	**This Work**	
Feature		Implicit Resonan.	Drain Resistances	Implicit Resonan.	Class-F	Class-B	Tail Resonance	Class-F	Tail Resonance	Implicit Resonance in Class F_{23} and Explicit Common-Mode Return Path	
Technology (nm)		28	65	40	65	28	65	65	28	**28**	
V_{DD} (V)		0.9	1.2	1.0	1.25	0.9	1.0	0.7/1.0	0.9	**1.0**	
Tuning Range (%)		27	18	25	25	32	10	25	17	14	
Core Area (mm^2)		0.19	0.08	0.13	0.13	0.13	0.2	0.13	N/A	0.15	
Freq. (GHz)		3.3	3.3	7	7.4	12.7	27.5	57.8	23.5	27.3	31.2
Power (mW)		6.8	0.72	10	15	8.3	23*	24*	7.2	12/22*	13/23*
Phase Noise (dBc/Hz)	100k	-106	-94	-102	-98	-80	-72	-72	-74	-83	-80
	1M	-130	-114	-124	-125	-107	-100	-100	-102	-106	-104
	10M	-150	-134	-144	-147	-132	-126	-122	-127	-126	-125
FoM** (dBc/Hz)	100k	-188	-186	-189	-184	-172	-167*	-173*	-172	**-181/-178***	**-179/-177***
	1M	-192	-186	-191	-191	-179	-177*	-181.5*	-180	-184/-181*	-183/-180*
	10M	-192	-186	-191	-193	-184	-181*	-183.7*	-186	-184/-181*	-184/-181*
$1/f^3$ Corner (kHz)		200	20	130	700	4000	1200	1000	3000	**120**	**210**
Freq. Pushing (MHz/V)		N/A	15@1.2V	23@1V	50@1.25V	N/A	N/A	N/A	N/A	37@1V	

*Including power consumption from frequency multiplier/first-stage buffer, **FoM = PN -20log(f_{osc}/f_{offset})+10log(P_{DC}/1mW)

20 fF and $C_{\text{tune2}} = 60$ fF) are used to make the resonant frequency of the 1st and 2nd tank stages equal and around 30 GHz in order to boost the 3rd harmonic oscillator output and to suppress its fundamental. On the other hand, R_{b} is used further to suppress the 2nd harmonic within the PA. The C_{n1} (= 8 fF) and C_{n2} (= 16 fF) are the neutralization capacitors to cancel the Miller effect at the input stage, improving the PA's stability.

2.4 Experimental Results

The prototype of the proposed 30 GHz frequency generation stage comprising the 10 GHz class-F_{23} oscillator and the two-stage 30 GHz PA is fabricated in TSMC 28-nm LP CMOS. The chip micrograph is shown in Fig. 2.20 and it occupies a core area of 0.15mm^2. While the power supply line is fed into the embedded decoupling on the left and right hand sides, the CM inductance is fed directly right near the source of the cross-coupled pair, as shown in the zoom-in layout of the proposed transformer. Thus, the CM return path is well defined.

To verify the proposed technique, phase noise (PN) is evaluated using an Agilent E5052B signal source analyzer (SSA) and a 11970A harmonic mixer. The measured tuning range is from 27.3 GHz to 31.2 GHz (14%) and Fig. 2.21 (a) shows the measured PN at 27.3 GHz and 31.2 GHz. At the 27.3 GHz carrier, drawing 12 mW from 1 V supply of the main oscillator,

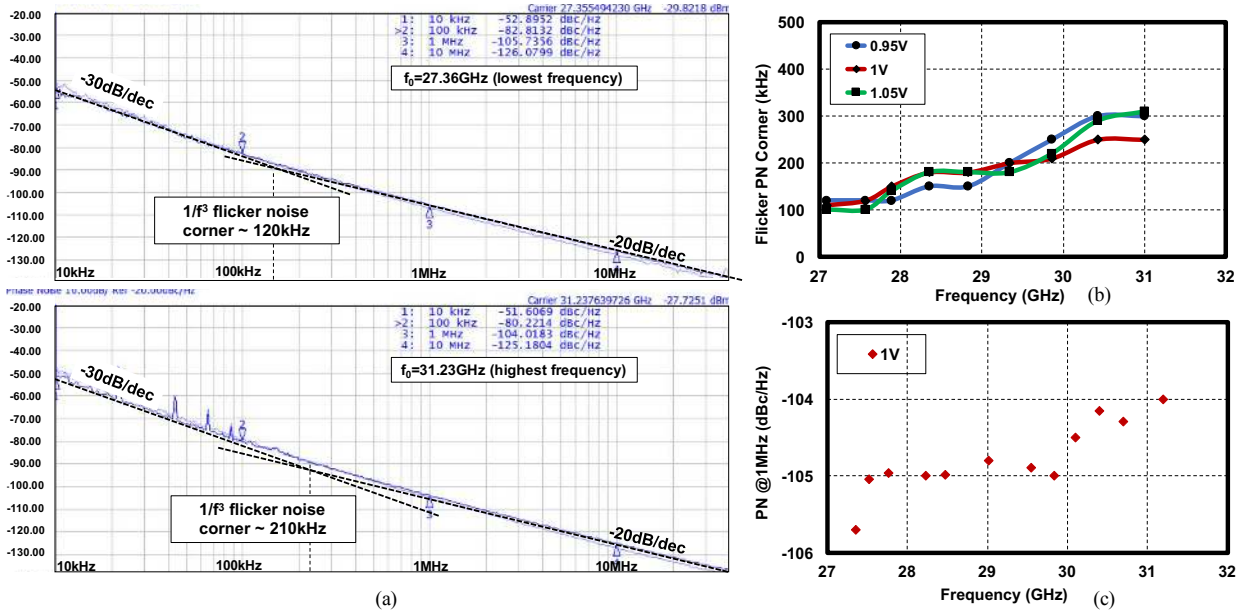

Figure 2.21: (a) Measured phase noise plots at 27.36 GHz and 31.23 GHz. (b) Measured flicker PN corner over tuning range (c) Measured PN @1MHz over tuning range

it achieves -82.8 dBc/Hz and -126 dBc/Hz at 100 kHz and 10 MHz offsets, respectively. The supply pushing is only 37 MHz/V (by sweeping V_{DD} from 0.95 V to 1.05 V) which is in line with recently published best-in-class reports. Fig. 2.21 (b) shows measured flicker noise corner across the TR and at three supply levels: 0.95, 1.0 and 1.05 V. It increases almost monotonically from 100 kHz to 300 kHz across the TR and is quite stable over voltage changes. The measured PN at 1MHz offset is shown in Fig. 2.21 (c). Table I compares this work with other flicker-noise aware designs (albeit at single GHz) as well as mmW CMOS oscillators. The techniques using tail filtering improve PN performance in the the far-out $1/f^2$ region [67, 69], but fail to maintain the same PN FoM at 1 MHz offset which can deteriorate the system data rate. The 3rd harmonic peak-to-peak output swing of the 1st stage buffer in the proposed circuit is ∼2 V, consuming ∼10 mW. Additional stage of buffers can help further suppress the fundamental frequency, and deliver enough power to the load [23]. The proposed oscillator achieves 120 kHz and 220 kHz flicker noise corners at 27.3 GHz and 31.2 GHz carriers, respectively, which confirms the validity of the proposed approach. This is the lowest $1/f^3$ corner reached among the >10 GHz oscillators, which usually report >1MHz, and comparable to those oscillators with flicker-noise-aware designs but at much lower frequencies [44, 49]. To the best of the authors' knowledge, the proposed oscillator achieves the best PN FoM at

100 kHz offset while maintaining competitive FoM at 1 MHz across its tuning range when compared with >10 GHz oscillators.

2.5 Conclusion

A 30 GHz frequency generation stage using a 3rd harmonic extraction and a 2nd/3rd harmonic tuning is proposed. A new 2nd harmonic resonance technique with careful consideration and control of parasitics in the CM current return path results in state-of-the-art performance with an order-of-magnitude reduction in flicker noise among >10 GHz oscillators. The proposed simulation method of periodically modulated rms flicker current noise $I_{1/f,\mathrm{rms}}(t)$ and effective non-normalized ISF for flicker noise $h_{\mathrm{eff}}(t)$ $[= h_{\mathrm{DS}}(t) \times I_{1/\mathrm{f,rms}}(t)]$ are instrumental in the first-ever numerical verification of the flicker noise reduction mechanism using 2nd harmonic resonance. This further provides a powerful tool to study quantitatively other low-flicker noise oscillator topologies.

Chapter

3

Intuitive Understanding of Flicker Noise Reduction via Narrowing of Conduction Angle in Voltage-Biased Oscillators

This chapter aims to explain intuitively and verify numerically the observed phenomenon of flicker noise reduction in oscillators due to reduced conduction angle (i.e., in class-C), which has been presented in the literature but never properly explained. The flicker phase noise in a voltage-biased oscillator capable of operating in class-B and class-C is compared and numerically verified using a commercial simulation model of TSMC 28-nm CMOS. We illustrate how narrowing the conduction angle can suppress the $1/f$ noise up-conversion by decreasing $1/f$ noise exposure to the *asymmetric* rising and falling edges of oscillation waveform. The effects of implicit common-mode (CM) tank in the class-C operation are also discussed. We further clarify ambiguities among several simulation methods of impulse sensitivity function (ISF) based on periodic small-signal analysis (PAC or PXF), which is a key tool in understanding the flicker noise up-conversion. A clearer ISF simulation method based on positive sidebands of PXF is proposed.

3.1 Introduction

The flicker noise up-conversion mechanism in voltage-biased oscillators [42, 44, 51, 64, 65] (i.e., where the tail current source is eliminated [43]) has received a great amount of attention in recent years. It is recognized that asymmetry between the rising and falling portions of the oscillation waveform results in $1/f$ noise up-conversion, which is a consequence of a 2nd harmonic current entering a non-resistive termination. This conclusion was first proposed in [44], numerically verified in [51], and further experimentally supported by [49]. Moreover, Shahmohammadi *et al.* [44] claimed that the non-resistive termination of 3rd (or any higher odd-order) harmonic current does not introduce the $1/f$ noise up-conversion [64], which was then theoretically demonstrated in [42].

Several $1/f^3$ phase noise (PN) reduction mechanisms have been identified [44,51,65]. Pepe *et al.* [65] demonstrated that introducing an additional phase shift between the drain and gate of the cross-coupled pair can suppress the $1/f$ noise up-conversion. In addition, an accurate implementation of the 2nd harmonic "parallel LC resonance" in voltage-biased oscillators has proved to be an effective method in reducing the $1/f^3$ PN in class-B [49], class-D [44], and class-F oscillators [44, 51, 52], which all cover single-GHz RF [44, 49] and mmW bands [51, 52], as surveyed in Fig. 3.1. It makes the phase of the 2nd harmonic voltage component well-behaved, eventually causing symmetric rising and falling portions of oscillation waveform [51], thus reducing the $1/f$ noise upconversion. The high CM impedance due to the 2nd harmonic parallel-LC resonance also helps to improve thermal PN by suppressing the $4kTg_{\mathrm{ds}}$ current noise (i.e., "loaded-Q" effects). Recently announced, a 2nd harmonic "series-LC resonance" technique [54] aims to make the waveform symmetric by minimizing the magnitude of the 2nd harmonic voltage (its phase is also well-behaved), which effectively suppresses the flicker noise upconversion. However, it cannot suppress the $4kTg_{\mathrm{ds}}$ current noise and improve the thermal PN due to the extremely low CM impedance.

Interestingly, Fig. 3.1 also suggests that class-C operation can achieve similarly good $1/f^3$ PN performance as the aforementioned techniques in both its current-biased [47, 61, 62] and voltage-biased [63] versions. As a variant of the class-C oscillator, the "pulse-tail-feedback" topology [55] recently reported a record-low $1/f^3$ corner of 700 Hz. It adds controlled tail-switches to decrease the current conduction angle of cross-coupled pair significantly, making it much smaller than π. The effect of the reduced conduction angle improving the $1/f^3$ PN is

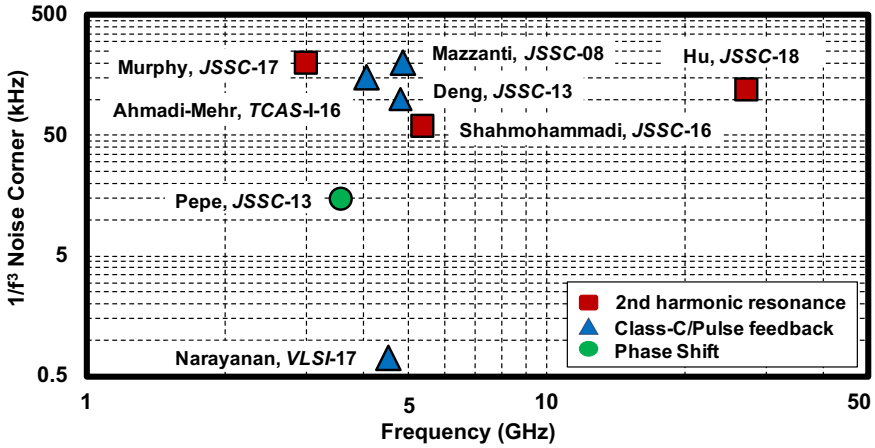

Figure 3.1: Survey of state-of-the-art oscillators with low measured $1/f^3$ corner ($< 300\,\text{kHz}$).

also seen in the measurements of [56–58]. Two PMOS transistors are added under the cross-coupled pairs to decrease the conduction angle, through the coupling of an RC-filter [56] or transformer [57,58]. However, the literature still lacks a detailed explanation on why reducing the current conduction angle would improve the $1/f^3$ PN performance [47,55–57,61–63].

To study the $1/f$ noise up-conversion in oscillators, the impulse sensitivity function (ISF) [35] plays an important role [51]. Unfortunately, its conventional extraction method based on transient simulations (TRAN) is rather time-consuming and not accurate. Kim *et al.* [76] associated the ISF with periodic small-signal analysis, especially, periodic AC (PAC) analysis. It was not until recently that a periodic transfer function (PXF) was recognized as a more convenient simulation method to obtain the ISF [72,77,78]. A single-run PXF simulation can acquire N harmonic terms of ISF, which is much more convenient than running PAC simulations N times. However, several confusing issues still persist: 1) It is not straightforward to understand a derivation linking ISF to PXF in which a small-signal voltage at $\omega_0 + \Delta\omega$ is observed in response to a small input test current at $k\omega_0 - \Delta\omega$ [72,78]. 2) All the derived equations linking ISF to PXF require negative sidebands of PXF (i.e., negative frequency), while the default settings in PXF does not support negative frequencies [79]. 3) The concept of index of PXF sidebands is missing.

This brief extends our previous work [51], offering a clear derivation associating the ISF with positive sidebands of PXF, and clarifies the ambiguities existing in its negative sidebands. It numerically verifies the $1/f^3$ PN reduction mechanism in a class-C oscillator, featuring the proposed simulation method of ISF. The rest of this brief is organized as follows: Section 3.2

presents the derivation from PXF to ISF based on positive sidebands of PXF and explains the confusing parts in the PXF negative sidebands. The flicker noise reduction mechanism in class-C oscillators is shown in Section 3.3.

3.2 Non-Normalized ISF Extraction from PXF

3.2.1 Transimpedance in LTI System and Periodic Transimpedance in LPTV System

For a linear time-invariant (LTI) system, its transimpedance transfer function [of magnitude $|H(\omega_0 + \Delta\omega)|$ and phase $\angle H(\omega_0 + \Delta\omega)$] at a specific frequency $(\omega_0 + \Delta\omega)$ can be calculated by observing a response of an output voltage signal v_t at $\omega_0 + \Delta\omega$ to an input test current signal i_t at $\omega_0 + \Delta\omega$, as shown in Fig. 3.2(a). Note that the observed v_t at $\omega_0 + \Delta\omega$ can only be caused by the input test current signal i_t at exactly the same frequency. However, for a linear periodically time-variant (LPTV) system with a period of $2\pi/\omega_0$ (e.g., an oscillator), the observed small output voltage v_t at $\omega_0 + \Delta\omega$ could result not only from the input current i_t at the same frequency $\omega_0 + \Delta\omega$, but also from other positive harmonics of the current at $\omega_0 + \Delta\omega + (k-1)\omega_0$ (i.e., $\Delta\omega + k\omega_0$) or from negative harmonics at $\omega_0 + \Delta\omega - (k+1)\omega_0$ (i.e., $\Delta\omega - k\omega_0$), where $k = 0, 1, 2, ..., N$. A periodic transfer function (PXF), e.g., periodic transimpedance, was introduced to describe this type of LPTV system [79], as illustrated at the top of Fig. 3.2(b). The $(k-1)$ and $-(k+1)$ (rather than k and $-k$) are the indices of positive and negative PXF sidebands, respectively, since the output at frequency $\omega_0 + \Delta\omega$ (rather than at $\Delta\omega$) is observed in the case of oscillator.

3.2.2 ISF Extraction from Positive Sidebands of PXF

The link between ISF and positive sidebands of PXF will be built based on a voltage-biased oscillator shown in Fig. 3.4. Assume a small test signal current source across the drain-source of $\mathrm{M}_{1/2}$ at $\omega_0 + \Delta\omega + (k-1)\omega_0$ (i.e., $\Delta\omega + k\omega_0$),

$$i_\mathrm{t}(t) = I_\mathrm{t} \cos[(\omega_0 + \Delta\omega)t + \gamma_k + (k-1)\omega_0 t] \tag{3.1}$$

where $k-1$ $(= -1, 0, ..., N-1)$ is the chosen index of positive sidebands, N is the number of harmonics for consideration, and I_t, γ_k are the amplitude and initial phase, respectively.

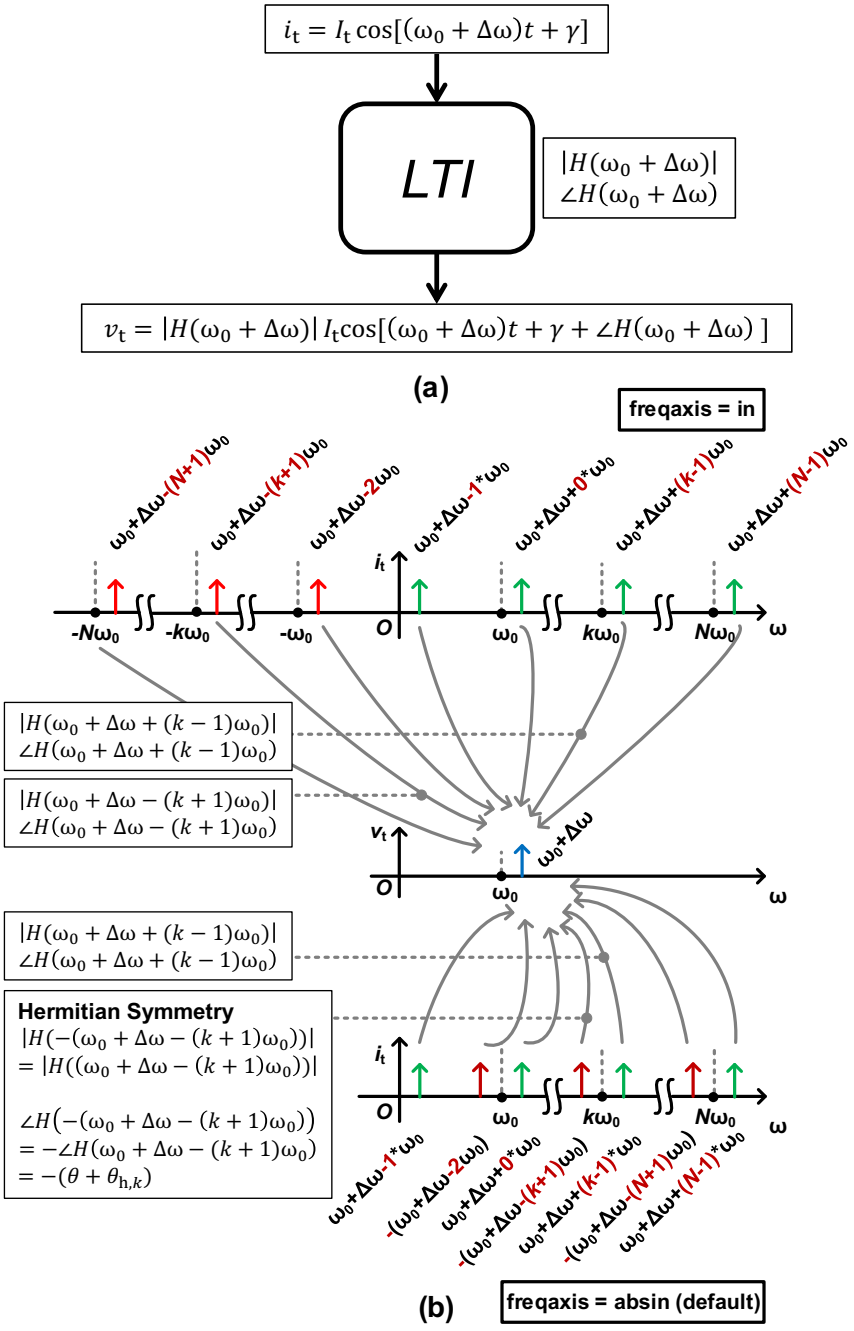

Figure 3.2: (a) Transimpedance in a linear time-invariant (LTI) system. (b) Periodic transimpedance in a linear periodically time-variant (LPTV) system with a period of $2\pi/\omega_0$, *supporting* negative frequencies (top, PXF option: "freqaxis = in"), and *not* (bottom, PXF option (default): "freqaxis = absin").

Further, assume a non-normalized ISF, h_{DS}, associated with V_{DS} of $\mathrm{M}_{1/2}$,

$$h_{\mathrm{DS}}(t) = \frac{1}{2} h_0 \cos\theta_{\mathrm{h0}} + \sum_{m=1}^{N} h_m \cos\left(m\omega_0 t + \theta_{\mathrm{h},m}\right) \tag{3.2}$$

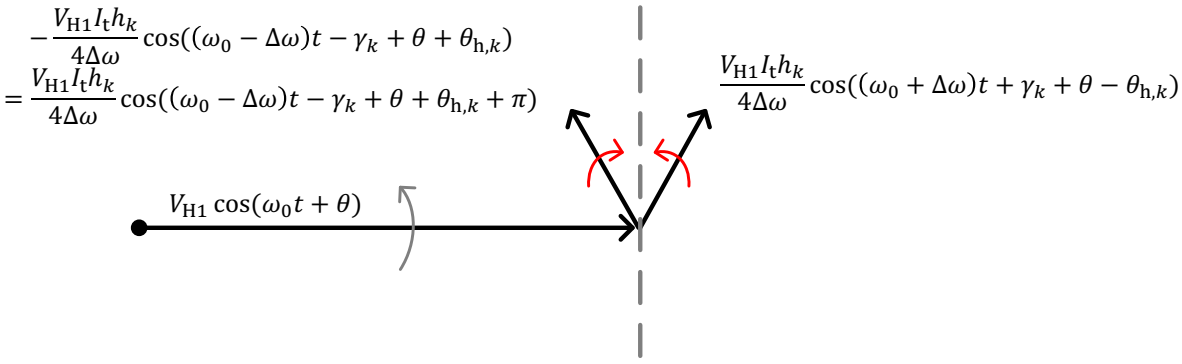

Figure 3.3: Phasor diagram of (3.4).

where h_m and $\theta_{\mathrm{h},m}$ are the magnitude and phase of mth harmonic term, respectively.

As per the physical meaning of ISF, the phase perturbation $\phi(t)$ at V_{DS} is derived as

$$\begin{aligned}\phi(t) &= \int_{-\infty}^{t} h_{\mathrm{DS}}(\tau) i_{\mathrm{t}}(\tau) d\tau \\ &\approx \frac{I_{\mathrm{t}} h_k}{2\Delta\omega} \sin\left(\Delta\omega t + \gamma_k - \theta_{\mathrm{h},k}\right)\end{aligned} \tag{3.3}$$

in which only the slow frequency term (i.e., $\Delta\omega$) dominates when $m = k$. Then, $\phi(t)$ will appear at V_{DS} as

$$\begin{aligned}V_{\mathrm{DS}} &\approx V_{\mathrm{H1}} \cos\left(\omega_0 t + \theta + \phi(t)\right) \approx V_{\mathrm{H1}} \cos\left(\omega_0 t + \theta\right) \\ &+ \frac{V_{\mathrm{H1}} I_{\mathrm{t}} h_k}{4\Delta\omega} \cos\left[(\omega_0 + \Delta\omega)t + \gamma_k + \theta - \theta_{\mathrm{h},k}\right] \\ &- \frac{V_{\mathrm{H1}} I_{\mathrm{t}} h_k}{4\Delta\omega} \cos\left[(\omega_0 - \Delta\omega)t - \gamma_k + \theta + \theta_{\mathrm{h},k}\right]\end{aligned} \tag{3.4}$$

where V_{H1} and θ are the 1st harmonic amplitude and phase of V_{DS}, respectively. The phasor diagram of (3.4) is shown in Fig. 3.3, where the correlated upper (i.e., at $\omega_0 + \Delta\omega$) and lower (i.e., at $\omega_0 - \Delta\omega$) sidebands could only modulate the phase of V_{DS}. From i_{t} in (3.1) to the upper sideband of V_{DS} in (3.4), the periodic transimpedance from the small current i_{t} at the $(k-1)$th sideband to the small output voltage of V_{DS} at $\omega_0 + \Delta\omega$ can be written as

$$|H(k-1)| = \frac{V_{\mathrm{H1}} h_k}{4\Delta\omega} \tag{3.5}$$

$$\angle H(k-1) = \theta - \theta_{\mathrm{h},k} \tag{3.6}$$

where $H(k-1)$ represents $H(\omega_0+\Delta\omega+(k-1)\omega_0)$. $|H(k-1)|$ and $\angle H(k-1)$ are the magnitude and phase of periodic transimpedance, which can be simulated directly by PXF. The magnitude $V_{\rm H1}$ and initial phase θ of 1st harmonic of $V_{\rm DS}$ can be simulated by PSS with Harmonic Balance (HB) engine, which solves for the steady-state of cosines rather than sines [51]. As per (3.2), (3.5), (3.6), we can link ISF with positive sidebands of PXF as,

$$\begin{aligned} h_{\rm DS}(t) &= \frac{1}{2}\frac{4\Delta\omega|H(-1)|}{V_{\rm H1}}\cos[\theta-\angle H(-1)] \\ &+\sum_{k=1}^{N}\frac{4\Delta\omega|H(k-1)|}{V_{\rm H1}}\cos\left[k\omega_0 t+\theta-\angle H(k-1)\right]. \end{aligned} \tag{3.7}$$

3.2.3 ISF Extraction from Negative Sidebands of PXF

Following the similar derivation steps as above, we can also derive the periodic transimpedance from a small-signal test current source at $(\omega_0+\Delta\omega)-(k+1)\omega_0$ to a resultant small output voltage of $V_{\rm DS}$ at $\omega_0+\Delta\omega$ as follows:

Assume a small test current source at $(\omega_0+\Delta\omega)-(k+1)\omega_0$ (i.e., $-(k\omega_0-\Delta\omega)$),

$$i_{\rm t}(t)=I_{\rm t}\cos[(\omega_0+\Delta\omega)t+\gamma_k-(k+1)\omega_0 t] \tag{3.8}$$

where $-(k+1)(=-2,-3,...,-(N+1))$ is the index of negative sidebands of PXF. Similarly, we can derive the output voltage $V_{\rm DS}$ as

$$\begin{aligned} \phi(t) &= \int_{-\infty}^{t} h(\tau)i_{\rm t}(\tau)d\tau \\ &\approx \frac{i_{\rm t}h_k}{2\Delta\omega}\sin\left(\Delta\omega t-\gamma_k+\theta_{{\rm h},k}\right). \end{aligned} \tag{3.9}$$

Then, $\phi(t)$ will still appear at $V_{\rm DS}$ as

$$\begin{aligned} V_{\rm DS} &\approx V_{\rm H1}\cos\left(\omega_0 t+\theta+\phi(t)\right)\approx V_{\rm H1}\cos\left(\omega_0 t+\theta\right) \\ &+\frac{V_{\rm H1}I_{\rm t}h_k}{4\Delta\omega}\cos\left[(\omega_0+\Delta\omega)t+\gamma_k+\theta+\theta_{{\rm h},k}\right] \\ &-\frac{V_{\rm H1}I_{\rm t}h_k}{4\Delta\omega}\cos\left[(\omega_0-\Delta\omega)t-\gamma_k+\theta-\theta_{{\rm h},k}\right]. \end{aligned} \tag{3.10}$$

From $i_{\rm t}$ in (3.8) to the upper sideband of $V_{\rm DS}$ in (3.10), the periodic transimpedance from the small current $i_{\rm t}$ at $-(k+1)$th sideband to the small ouput voltage at $\omega_0+\Delta\omega$ can be

written as

$$|H(-(k+1))|= \frac{V_{\mathrm{H1}} h_k}{4\Delta\omega} \tag{3.11}$$

$$\angle H(-(k+1)) = \theta + \theta_{\mathrm{h},k} \tag{3.12}$$

where $H(-(k+1))$ represents $H(\omega_0 + \Delta\omega - (k+1)\omega_0)$. $|H(-(k+1))|$ and $\angle H(-(k+1))$ are magnitude and phase of the periodic transimpedance, respectively. The linking equations (3.11) and (3.12) between ISF and negative sidebands of PXF are exactly the same as the counterparts in [72, 78]. In other words, they are actually the periodic transimpedance based on current at $(\omega_0 + \Delta\omega) - (k+1)\omega_0$ (i.e., $-(k\omega_0 - \Delta\omega)$) rather than the current at $k\omega_0 - \Delta\omega$, which was a rather confusing assumption in [72, 78].

However, the negative frequency is not supported in PXF at the default settings [79], in which the input frequency axis is only available for absolute frequency (i.e., PXF options: freqaxis = absin). To get the correct results of $|H(-(k+1))|$ and $\angle H(-(k+1))$, it should enable negative frequency in PXF by setting the option "freqaxis = in". Otherwise, PXF will give the periodic transimpedance of $H(-(\omega_0 + \Delta\omega - (k+1)\omega_0))$ rather than $H(\omega_0 + \Delta\omega - (k+1)\omega_0)$ (with a shorthand notation of $H(-(k+1))$), when the negative sidebands of $-(k+1)$ are chosen, as illustrated at the bottom of Fig. 3.2(b). For a real-signal system (e.g. oscillator), the $H(-(\omega_0 + \Delta\omega - (k+1)\omega_0))$ and $H(\omega_0 + \Delta\omega - (k+1)\omega_0)$ are Hermitian symmetric, which means

$$|H(-(\omega_0 + \Delta\omega - (k+1)\omega_0))|= |H(-(k+1))|= \frac{V_{\mathrm{H1}} h_k}{4\Delta\omega} \tag{3.13}$$

$$\angle H(-(\omega_0 + \Delta\omega - (k+1)\omega_0)) = -\angle H(-(k+1)) = -(\theta + \theta_{\mathrm{h},k}). \tag{3.14}$$

Note that the $\theta_{\mathrm{h},0}$ can be only calculated by (3.6) rather that (3.12) and (3.14).

It would be easy to make a mistake using (3.11) and (3.12), since it requires special but easily overlooked settings for PXF. Thus, we recommend to extract the ISF based on positive sidebands (see (3.7)) rather than for the negative sidebands of PXF.

3.3 Flicker Noise Up-conversion and Reduction

The $1/f^3$ PN caused by a single MOS transistor in a cross-coupled pair of voltage-biased oscillator (e.g., M_1 in Fig. 3.4) can be written as [51],

$$\mathcal{L}(\Delta\omega) = \left(\frac{\sqrt{2}}{2\Delta\omega} \cdot \frac{1}{T} \int_0^T h_{\mathrm{DS}}(t) \cdot I_{1/f,\,\mathrm{rms}}(t) dt \right)^2 \tag{3.15}$$

where $T(= 2\pi/\omega_0)$ is the oscillation period and $I_{1/f,\,\mathrm{rms}}(t)$ is the periodically modulated rms value of flicker current noise at a specific low-frequency $\Delta\omega$ (e.g., $2\pi\times 10\,\mathrm{kHz}$), modeling the process of flicker noise modulation. It can be directly simulated by dc/NOISE engines using a discrete waveform point of V_{GS} and V_{DS} from periodic steady-state (PSS) simulations. The test-bench of $I_{1/f,\,\mathrm{rms}}(t)$ is shown in Fig. 3.5. Two dc voltage sources V_{GS} and V_{DS} are used to provide different dc bias conditions, modeling the steady-state oscillation waveforms. The corresponding current noise for each bias point is sensed by a 0 V dc voltage source (i.e., v_sense), then transferred to a voltage noise (i.e., $V_{\mathrm{out,noise)}}$ by a current-controlled voltage source (i.e., ccvs). The dc/NOISE engines can directly plot the noise of $V_{\mathrm{out,noise}}$, which numerically equals to $I_{1/f,\,\mathrm{rms}}$ by setting "hgain" = 1.0 Ω.

The waveforms of $I_{1/f,\,\mathrm{rms}}(t)$ and $h_{\mathrm{DS}}(t)$ provide an accurate and intuitive way in understanding the flicker noise up-conversion and reduction in oscillators.

3.3.1 Voltage-Biased Oscillator in Class-B and Class-C

Fig. 3.4 shows a conventional voltage-biased oscillator, where R_{ac} and C_{ac} are inserted to separate V_{B} from V_{DD}, thus enabling either class-B (e.g. $V_{\mathrm{B}} = V_{\mathrm{DD}}$) or class-C (e.g. $\frac{1}{3}V_{\mathrm{DD}} \le V_{\mathrm{B}} \le \frac{1}{2}V_{\mathrm{DD}}$) configuration. A two-turn inductor is employed to make the physical distance between local supplies (i.e., $V_{\mathrm{DD}}/V_{\mathrm{SS}}$) very short, leading to almost zero parasitic inductance (i.e., $L_{\mathrm{decap}} \approx 0$) of the decoupling capacitor network (i.e., $C_{\mathrm{decap}} \approx 100\,\mathrm{pF}$). Only a differential capacitor (C_{diff}) is used to model the capacitance of the switched-capacitor bank (sw-cap), which could be implemented by separating the supplies of sw-cap from the oscillator [51]. Thus, the common-mode (CM) capacitance in the implicit CM tank comes mainly from the parasitic capacitance of $M_{1/2}$.

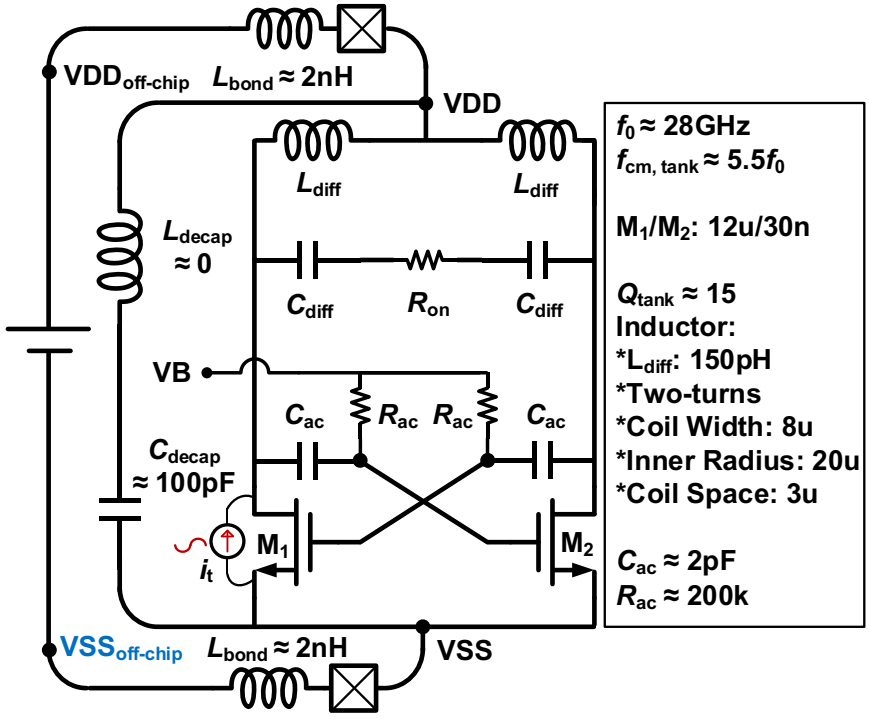

Figure 3.4: Schematic of a conventional voltage-biased oscillator in TSMC 28-nm LP CMOS with separated V_{B} from V_{DD} to enable either class-B (e.g., $V_{\mathrm{DD}} = V_{\mathrm{B}} = 0.96\,\mathrm{V}$) or class-C (e.g., $V_{\mathrm{DD}} = 1.2\,\mathrm{V}$, $V_{\mathrm{B}} = 0.58\,\mathrm{V}$) configurations.

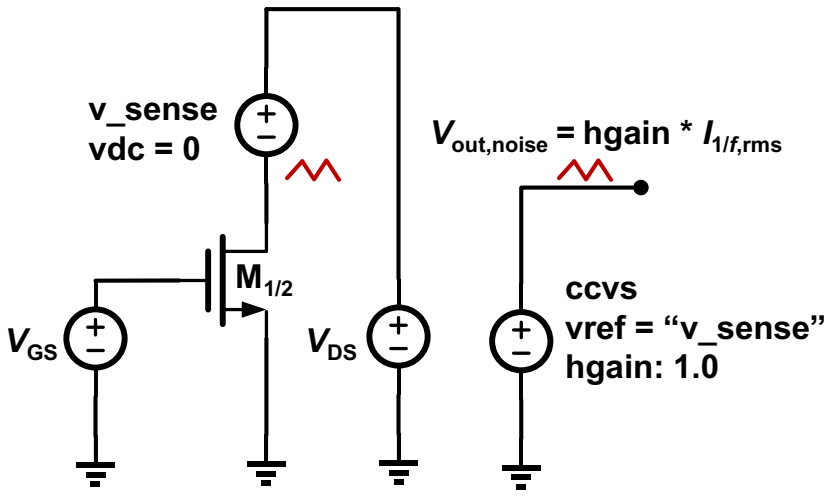

Figure 3.5: Test-bench for a periodically modulated rms value of flicker current noise $I_{1/f,\mathrm{rms}}(t)$ using dc/NOISE engines and the discrete waveform points of V_{GS} and V_{DS} from PSS simulations.

3.3.2 Flicker Noise Reduction Mechanism in Class-C oscillators

To study the $1/f^3$ PN reduction mechanism in class-C oscillators in an intuitive and comparative manner, the voltage-biased oscillator in Fig. 3.4 can be configured either in

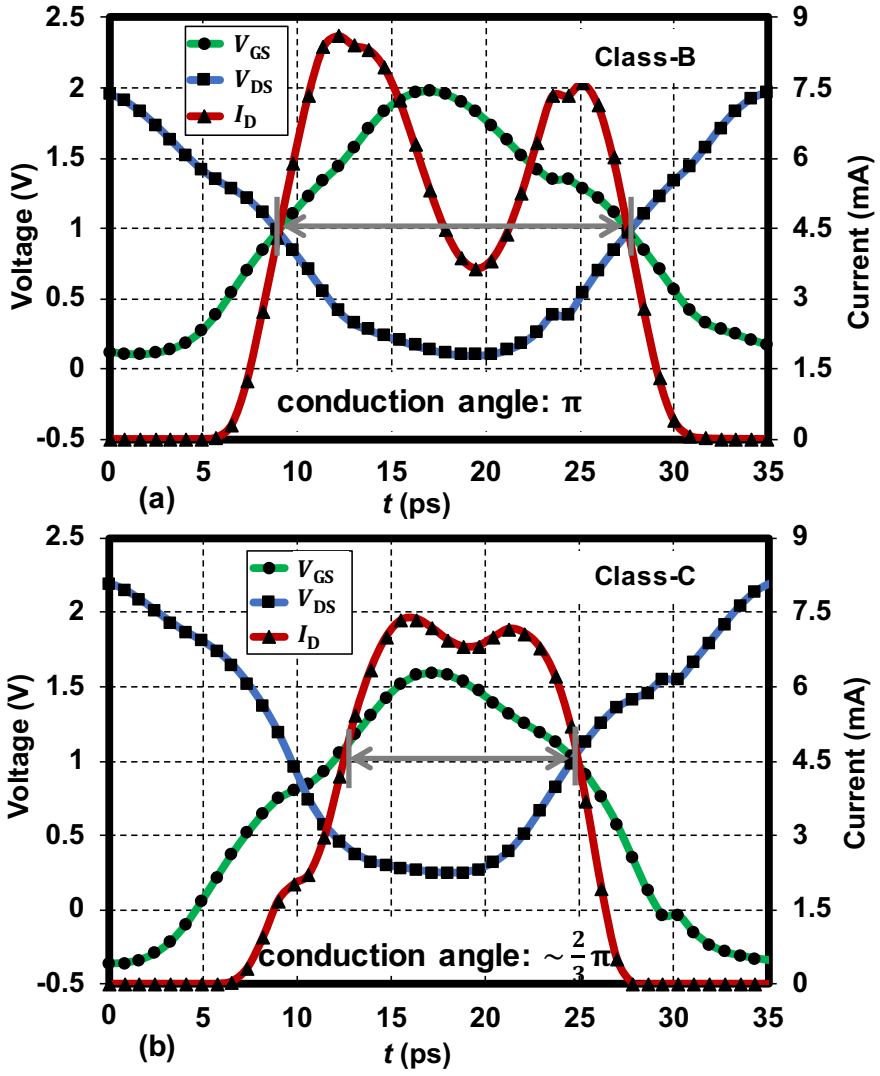

Figure 3.6: Simulated one period of V_{GS}, V_{DS}, and I_D waveforms in (a) class-B, and (b) class-C configurations.

class-C ($V_B = 0.58\,V$, $V_{DD} = 1.2\,V$) or as a reference in class-B ($V_B = V_{DD} = 0.96\,V$), while ensuring the same power consumption (6.62 mW). As per simulations, the resonance frequency of the implicit CM tank ($f_{cm,tank}$) is set to $\sim 5.5 f_0$, ensuring that the 2nd harmonic resonance technique cannot be availed of to explain the reduction of flicker noise up-conversion in either configuration. Fig. 3.6 presents the simulated waveforms of V_{GS}, V_{DS}, and I_D in both configurations, in which the conduction angle in class-C is reduced to about $\frac{2}{3}\pi$. Table 3.1 summarizes the overall performance. Compared with the class-B reference, the thermal PN (e.g., PN @10 MHz) of class-C reduces by a few dB, while its flicker PN (e.g., PN @10 kHz) decreases by as much as 13 dB (also see Fig. 3.9), leading to a 10× improvement in the

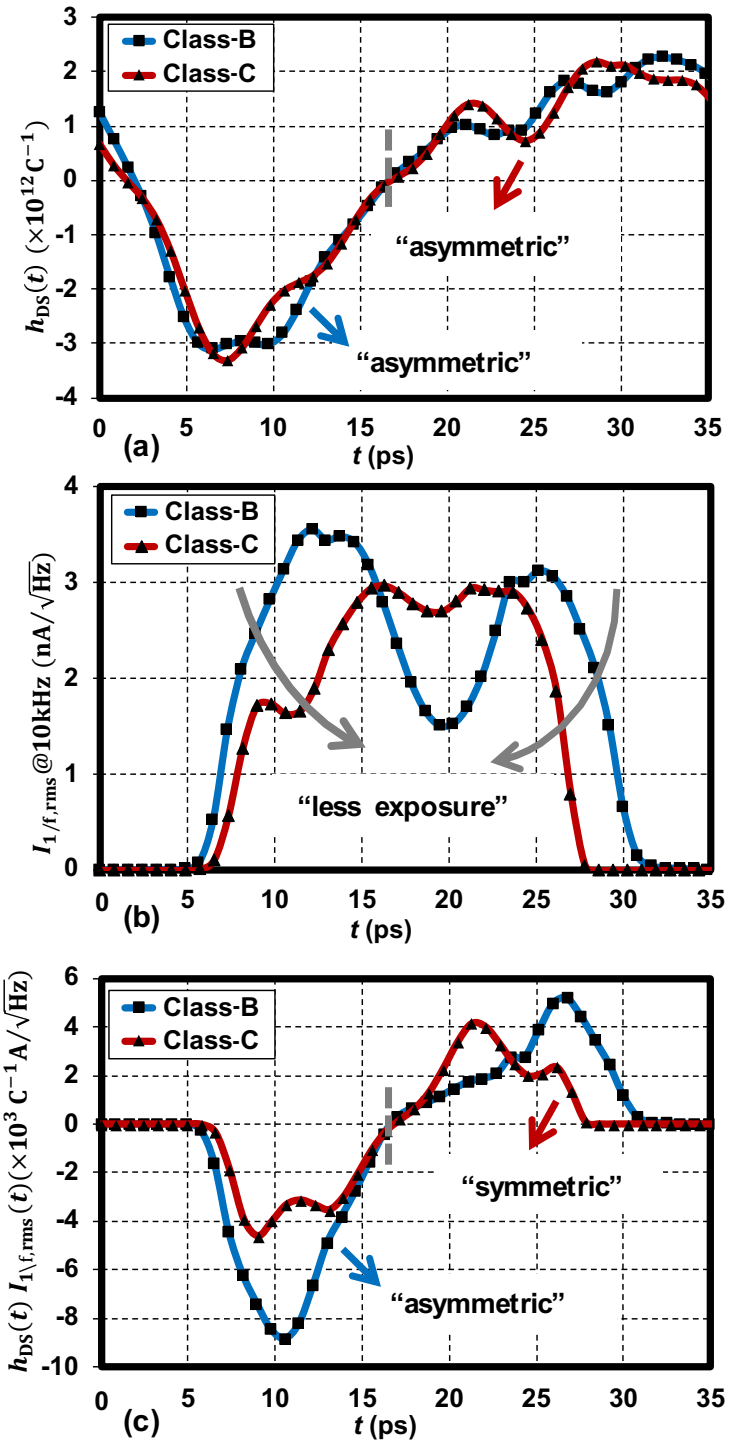

Figure 3.7: (a) Non-normalized ISF, $h_{\mathrm{DS}}(t)$. (b) Modulated rms value of flicker current noise at 10 kHz, $I_{1/f,\mathrm{rms}}(t)$. (c) Effective non-normalized ISF, $h_{\mathrm{DS}}(t) \cdot I_{1/f,\mathrm{rms}}(t)$.

$1/f^3$ corner. Obviously, the original thermal PN theory in [47] cannot explain the $1/f^3$ PN reduction in class-C oscillators due to the lack of consideration of higher ISF harmonics and,

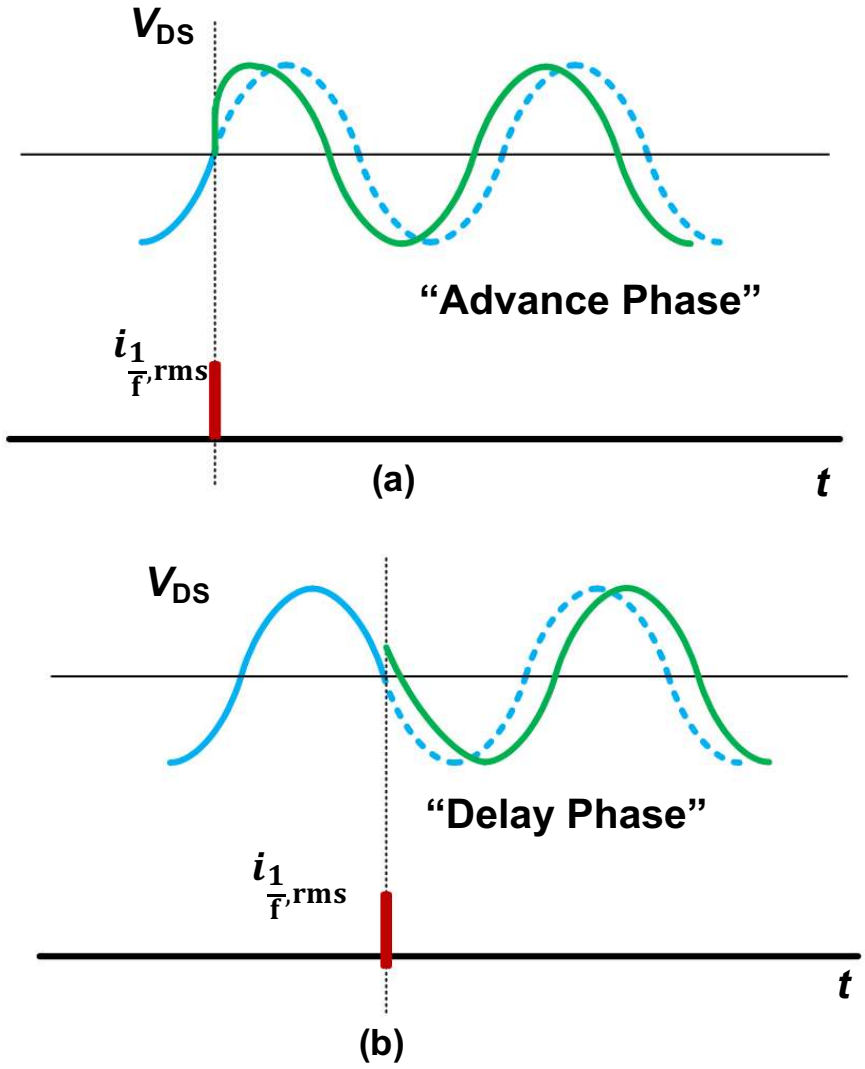

Figure 3.8: "Positive" flicker current noise injects into different portions of V_{DS}:(a) Injection at rising edge, advancing the phase. (b) Injection at falling edge, delaying the phase.

especially, the implicit CM tank.

In contrast to the thermal noise of MOS transistors spreading very wide in frequency, its $1/f$ noise only appears at very low frequencies (e.g., 10 kHz), which is much less than the oscillation frequency (e.g., 28 GHz). Thus, when the flicker current noise is injected into the tank to change the phase of V_{DS}, the "polarity" of the flicker current noise will likely not change, but only its magnitude (i.e., $I_{1/f,rms}$) will be modulated for one oscillation period (see Fig. 3.7(b)). Assuming that the "polarity" of the flicker current noise is positive (i.e., causing positive ΔV of V_{DS}) in a given oscillation period, it will introduce a negative

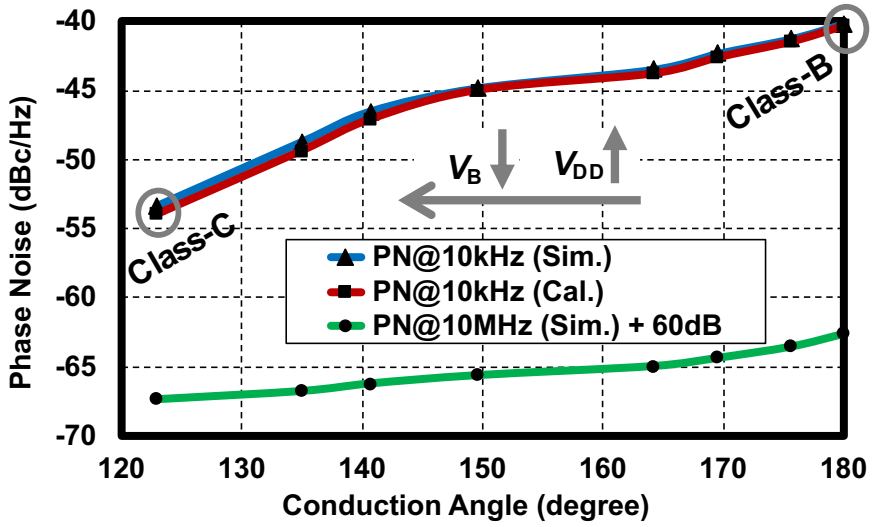

Figure 3.9: Numerical verification of PN @10kHz across conduction angle.

phase change (i.e., delaying the edge) of $V_{\rm DS}$ in the falling edge (e.g., $t \approx 5$ to 10 ps)(see Fig. 3.8(b)), while positive phase change (i.e., advancing the edge) in the rising edge (e.g., $t \approx 25$ to 30 ps) (see Fig. 3.8(a). Ideally, if $V_{\rm DS}$ is symmetric in the falling and rising parts, and the magnitude of the flicker noise current is also equally modulated in both parts, the phase change caused by this flicker noise current will cancel each other, resulting in no flicker noise upconversion. However, due to the resonant frequency of the implicit CM tank ($\sim 5.5 f_0$) being much higher than $2f_0$, the 2nd harmonic current enters an non-resistive (i.e., inductive) path, causing the asymmetry between the falling and rising edges of $V_{\rm DS}$ (i.e., more sensitive $h_{\rm DS}$ in falling edge of $V_{\rm DS}$) in both class-B and class-C configurations (see Fig. 3.7(a)). The effective non-normalized ISF, $h_{\rm DS}(t) \cdot I_{1/f,\rm rms}(t)$, of class-B, illustrated in Fig. 3.7(c), shows that the negative phase change in the falling part (i.e., negative area) is much larger than the positive phase change in the rising part (i.e., positive area), leading to a large net phase change in one period (i.e., asymmetry in $h_{\rm DS}(t) \cdot I_{1/f,\rm rms}(t)$, and flicker noise up-conversion).

Different from the 2nd harmonic resonance resulting in symmetric waveform [51], the flicker noise reduction mechanism in the class-C configured oscillator is due to the small exposure of the flicker current noise to the unbalanced sensitive regions of the ISF. As shown in Fig. 3.7(a), $h_{\rm DS}(t)$ values in both class-B and -C configurations are almost identical and asymmetric due to the lack of 2nd harmonic resonance. However, the class-C configuration

Table 3.1: Simulated and calculated performance of the voltage-biased oscillator in class-B and class-C configurations.

	Class-B	Class-C
Technology (nm)	28	
VDD (V)	0.96	1.2
VB (V)		0.58
Freq. (GHz)	28	
PN @10kHz (Sim./Cal.) (dBc/Hz)	-40.2/-40.3	-53.4/-54
PN @1MHz (dBc/Hz)	-96.9	-104
PN @10MHz (dBc/Hz)	-122.7	-127.5
Power (mW)	6.62	
FoM @10MHz (dB)	-183.4	-188.2
1/f³ Corner (kHz)	~2000	~200

has much smaller flicker noise in the two sensitive regions, as illustrated in Fig. 3.7(b), since the transistor in class-C operation is almost turned-off at the rising and falling edges of $V_{\rm DS}$. It ultimately results in symmetry the $h_{\rm DS}(t) \cdot I_{1/f,{\rm rms}}(t)$ product in class-C operation, thus reducing the $1/f^3$ PN (see Fig. 3.7(c)).

The numerical verification of PN @10kHz with a sweep of conduction angles (implemented by different biasing configurations of $V_{\rm B}$ and $V_{\rm DD}$ while keeping the same power) from class-B to class-C is shown in Fig. 3.9. The agreement between the calculations based on (3.15) and simulations is better than 0.6 dB, thus demonstrating the effectiveness of the proposed numerical method.

Further, to demonstrate the incorrectness of the linking equations in [72, 78], we verify the non-normalized ISF $h_{\rm DS}$ for the point of conduction angle of 175° (i.e., the 7th point of Fig. 3.9) using the proposed (3.6), (3.12), (3.14) and equations suggested by [72, 78], respectively. The flicker PN @10kHz calculated by proposed $h_{\rm DS}(t)$ is -41.4 dBc/Hz, fully matching the simulated PN @10kHz (i.e., -41.26 dBc/Hz). However, $h_{\rm DS}(t)$, suggested by [72, 78], shows wrong PN @10kHz as -30.37 dBc/Hz.Thus, as shown in Fig. 3.10, $h_{\rm DS}(t)$ based on our proposed equations are exactly same and correct (i.e., blue lines in Fig. 3.10), while $h_{\rm DS}(t)$

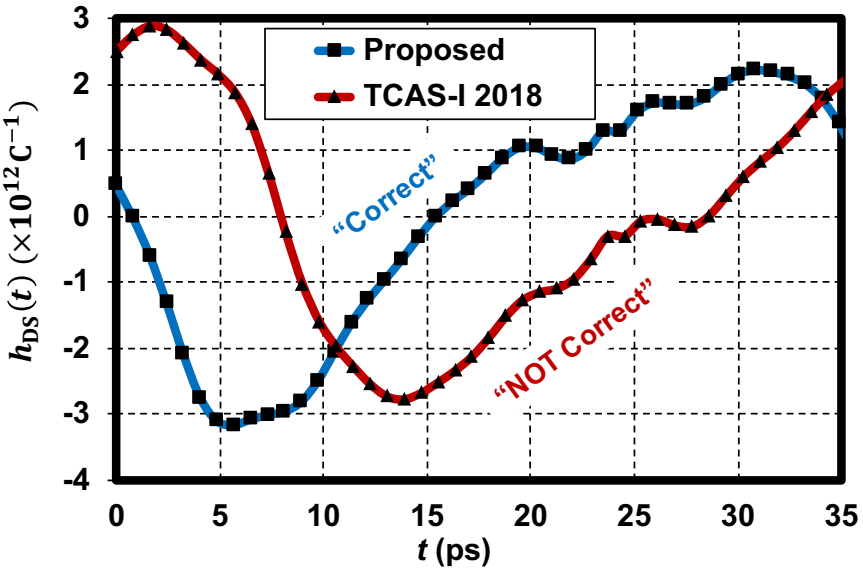

Figure 3.10: Comparison of simulated non-normalized ISF $h_{\mathrm{DS}}(t)$ between using the proposed (3.6), (3.12), (3.14) (all shown as blue lines), and using counterparts in [72, 78] (all shown as red lines).

based on equations in [72, 78] (i.e., red lines in 3.10) are wrong.

3.4 Conclusion

The $1/f^3$ phase noise reduction mechanism in a voltage-biased class-C oscillator is discussed and numerically verified. We identify that the reduced conduction angle leads to the reduced $1/f$ noise exposure to the notorious *asymmetric* rising and falling edges of oscillation waveform (i.e., due to the lack of 2nd harmonic resonance), ultimately suppressing the flicker noise up-conversion. We further propose a clear ISF extraction method based on positive sidebands of PXF and clarify the confusing assumptions (i.e., input test current at $k\omega_0 - \Delta\omega$) in ISF extraction based on negative sidebands of PXF.

Chapter

4

A 2.4 GHz, Low Flicker Noise Corner, Wide Tuning-Range Digitally Controlled Oscillator

The unified theory of flicker phase noise (PN) upconversion and reduction has been applied to mm-wave (mmW) oscillators in the previous chapters. Now, we further demonstrate it by applying it to an ultra-low power oscillator for Internet-of-Things. This chapter[1] presents a sub-mW ultra-low-voltage (ULV) digitally controlled oscillator (DCO) in which all electronic devices are vertically embedded within the inductor coils. A special arrangement of native layer (NT_N) diminishes any adverse effects on the inductors. To suppress flicker noise upconversion while maintaining wide tuning range (TR), we propose a technique of reduced current conduction angle. Its robust start-up is ensured by a passive gain of the proposed high-k_{m} 2:3 transformer, which is an advantage over current approaches in class-C oscillators. Implemented in 28-nm CMOS, the proposed DCO achieves -95 dBc/Hz and -118 dBc/Hz at 100 kHz and 1 MHz offsets, respectively. The measured $1/f^3$ corner is from 60 kHz to

[1]This work was performed in collaboration with Jianglin Du. The author contributed to the architecture of low flicker noise oscillator and theory analysis, while Jianglin contributed to the scheme of vertical integration, all the circuits design, and measurements.

100 kHz over the 35% TR (from 2.02 GHz to 2.87 GHz). This results in a figure-of-merit with normalized TR (FoM_T) at 100 kHz and 1 MHz offsets of -196 dB and -199 dB, respectively, which is a record among $\leq$0.5 V and <1 mW oscillators.

4.1 Introduction

IoT devices sustained by energy harvesters must support ultra-low-power (ULP) and ultra-low-voltage (ULV) operation. This puts tough requirements on the area, tuning-range (TR), phase noise (PN), and power consumption of digitally controlled oscillators (DCO). For example, a large size of inductor is generally needed for an improved quality (Q) factor, unfortunately resulting in much wasted inner area, as shown in Fig. 4.1(a). To support the ULV operation of oscillators, Kwok *et al.* [80] first exploited the passive gain of the transformer at an expense of a relatively larger area and worse supply pushing, which is not desirable when integrating with energy harvesters. To solve the supply pushing issue while further boosting the passive gain supporting even lower supply voltage (i.e., 0.2 V), a trifilar-coil transformer was proposed at a cost of lowered TR [81].

Furthermore, as CMOS technology advances, flicker ($1/f$) noise up-conversion in oscillators has become a serious problem [44, 49, 51]. It is well known that minimizing the dc value of the effective impulse sensitivity function (ISF) could lead to suppression of $1/f^3$ PN. However, efforts to achieve that are still a topic of extensive research. Only recently, Shahmohammadi *et al.* [44] and Hu *et al.* [51] have demonstrated that this could be implemented by means of accurate 2nd harmonic resonance, resulting in symmetric rising and falling edges. However, the accurate implementation of 2nd harmonic resonance is challenging, especially for wide TR, since any common-mode (CM) parasitics could shift the desired 2nd harmonic resonance.

In this paper, a transformer-based DCO with vertically integrated digitally controlled switched-capacitor (sw-cap) banks is proposed, as shown in Fig. 4.1(b). Even though the large transformer is optimized for high Q to support ULP and ULV operation, the complete DCO layout is still very compact and fits within 0.14 mm^2. This is thanks to customized fringe capacitors for fine sw-cap arrays, which allow themselves to be embedded together with coarse/medium banks inside the proposed transformer. In addition, a low $1/f^3$ PN corner can be maintained throughout the whole TR (up to 35%) via a proposed conduction angle reduction technique. Section 4.2 describes a circuit implementation of the proposed

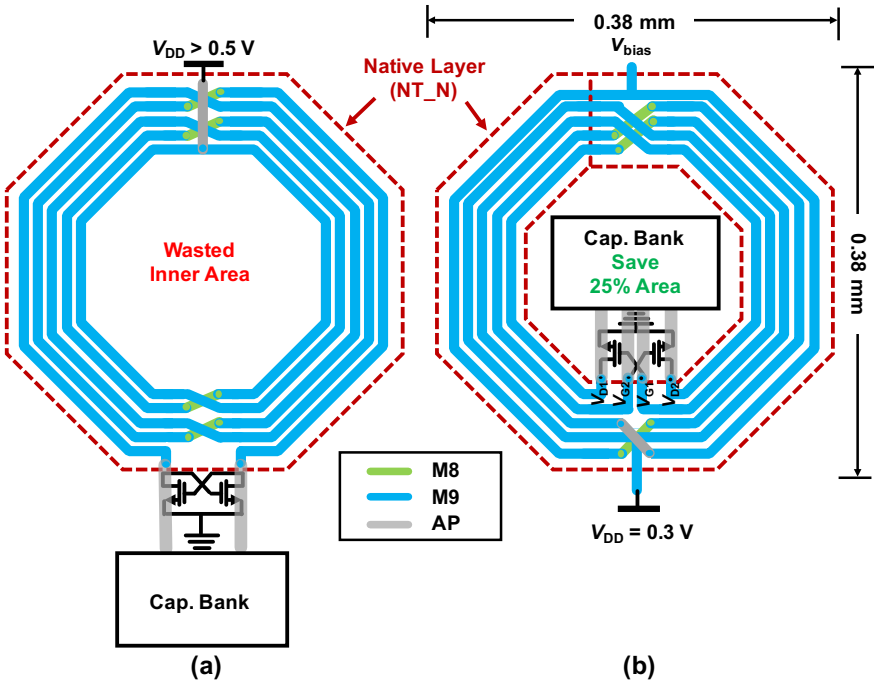

Figure 4.1: Simplified diagram and layout floorplan of 2.4 GHz DCO based on: (a) typical inductor with sw-cap banks next to it; (b) proposed 2:3 transformer with vertically integrated sw-cap banks.

DCO. The flicker noise reduction mechanism via narrowing of the conduction angle in ULV oscillators is revealed in Section 4.3. Section 4.4 provides experimental results.

4.2 Proposed Vertical Integration with Special Native Layer

A schematic of the DCO, shown in Fig. 4.2, reveals the cross-coupled pair, proposed 2:3 transformer, and three digital tuning capacitor banks. Compared with a conventional 1:2 transformer with a relatively low coupling factor k_m (e.g., 0.6–0.7) [82], the proposed 2:3 transformer is expected to achieve a larger inductance within the given area and higher k_m of 0.82 (due to the more compact primary and secondary coils). Thanks to the high k_m and 2:3 turns ratio, the transformer's passive gain is high enough to ensure the reliable ULV sub-mW operation of the DCO. For transformer-based oscillators [83, 84] but without class-F operation [51], it is not necessary to keep the secondary-to-primary capacitor ratio (i.e., X_2) at an accurate value in order to boost the 3rd harmonic voltage. Alternatively, we can keep the ratio within a quite large range (e.g., 1.5–3, this range is chosen by simulation) to make the oscillator operate over a region with enough passive gain and good thermal and flicker

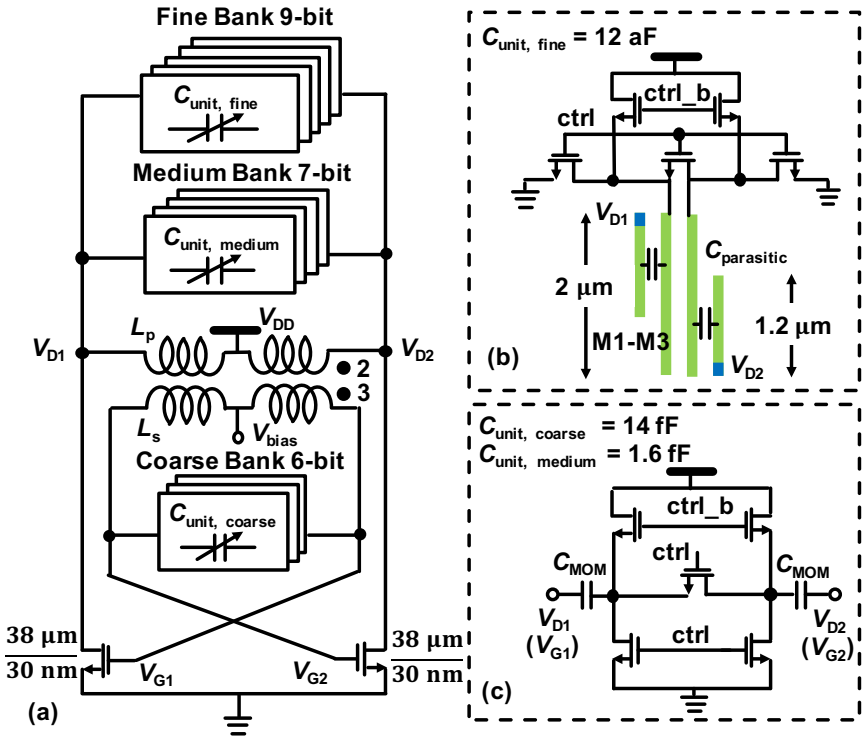

Figure 4.2: (a) Detailed schematic of proposed DCO. (b) Schematic of capacitor bank unit utilizing compact-sized customized fringe capacitor for fine tuning. (c) Schematic of capacitor bank unit for coarse and medium banks.

PN. Thus, the coarse bank (i.e., C_{coarse}) is connected to the secondary coil, while the medium and fine banks (i.e., C_{medium} and C_{fine}) are connected to the primary coil. The capacitor ratio X_2 is defined as

$$\frac{C_{\text{coarse}}}{C_{\text{medium}} + C_{\text{fine}}} = X_2 \tag{4.1}$$

where C_{coarse}, C_{medium}, and C_{fine} are the capacitance of the coarse bank, medium bank, and fine bank, respectively.

In this design, a 9-bit fine-tuning sw-cap bank and a 7-bit medium-tuning sw-cap bank are connected to the drain nodes, serving as the primary tank, while a 6-bit coarse sw-cap bank is placed at the gate nodes of the secondary tank. Medium and coarse banks are both implemented with MOM sw-caps with NMOS pull-up and pull-down devices [71], while a compact-size fine capacitor unit is realized by custom-designed MOM fringe-capacitor using M1 to M3 metal layers with a 1.2 μm length, achieving a step size of 12 aF.

A native layer (NT_N) is usually added under inductors or transformers in the nanoscale CMOS to define the non-doped high-resistance region of the substrate (see Fig. 4.1(a)), which

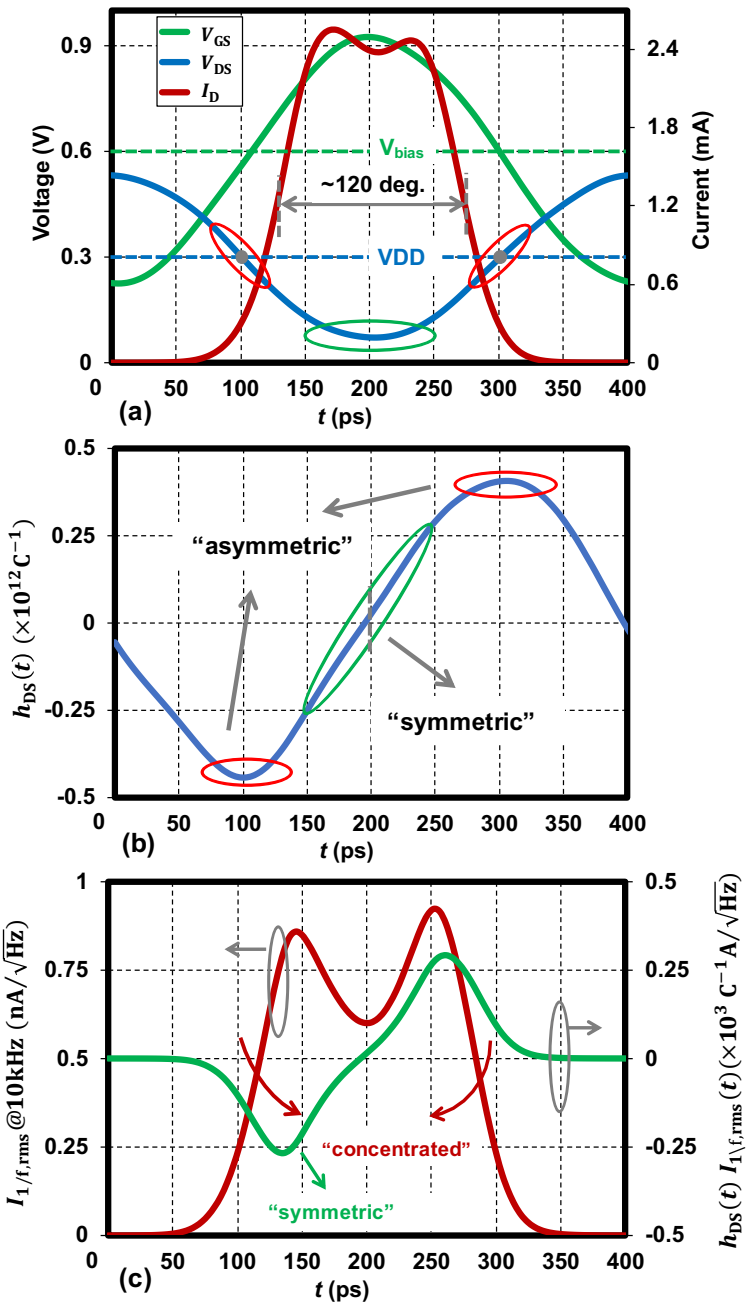

Figure 4.3: (a) Simulated one-period waveforms of V_{GS}, V_{DS}, and I_{D}. (b) Non-normalized ISF, $h_{\mathrm{DS}}(t)$. (c) Modulated rms value of flicker current noise at 10 kHz, $I_{1/f,\mathrm{rms}}(t)$ (left) and effective non-normalized ISF, $h_{\mathrm{DS}}(t) \cdot I_{1/f,\mathrm{rms}}(t)$ (right).

decreases eddy currents in the substrate, thus maintaining high Q of the coils. However, the active components (e.g., amplifying transistors and sw-cap banks) cannot be constructed on such a high resistance substrate due to the latch-up issues. Therefore, a special arrangement of native layer covers the coils with 0.02 mm margins to maintain high Q and leaves their strict

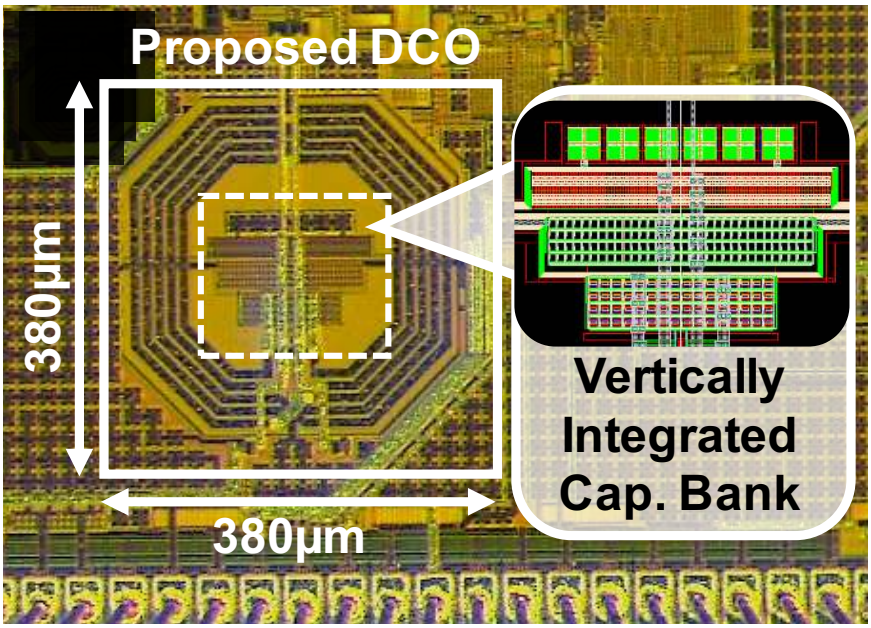

Figure 4.4: Chip microphotograph.

inner area for the sw-cap and amplifying transistors (see Fig. 4.1(b) and Fig. 3 in [75]). Due to the eddy current losses in the sw-cap inside the windings, Q of the transformer drops merely by 1.5–2 in the 2.4 GHz region, as shown in Fig. 4 of [75]. However, such Q degradation is similar to the conventional case of filling that inner area by non-functional dummy metal just to satisfy the increasingly strict density-rules in advanced CMOS technology [85].

4.3 Flicker Noise Reduction via Narrowing Conduction Angle

The $1/f^3$ PN caused by the cross-coupled pair of a voltage-biased oscillator (see Fig. 4.2) can be written as [51],

$$\mathcal{L}(\Delta\omega) = 2\left(\frac{\sqrt{2}}{2\Delta\omega}\cdot\frac{1}{T}\int_0^T h_{\mathrm{DS}}(t)\cdot I_{1/f,\,\mathrm{rms}}(t)dt\right)^2 \tag{4.2}$$

where $T(=2\pi/\omega_0)$ is the oscillation period, $I_{1/f,\,\mathrm{rms}}(t)$ is the periodically modulated rms value of flicker current noise at a specific low frequency $\Delta\omega$ (e.g., $2\pi\times10\,\mathrm{kHz}$), and $h_{\mathrm{DS}}(t)$ is the non-normalized ISF associated with V_{DS} of $\mathrm{M}_{1/2}$. The waveforms of $I_{1/f,\,\mathrm{rms}}(t)$ and $h_{\mathrm{DS}}(t)$ provide an accurate and intuitive way in understanding the flicker noise up-conversion and reduction in oscillators.

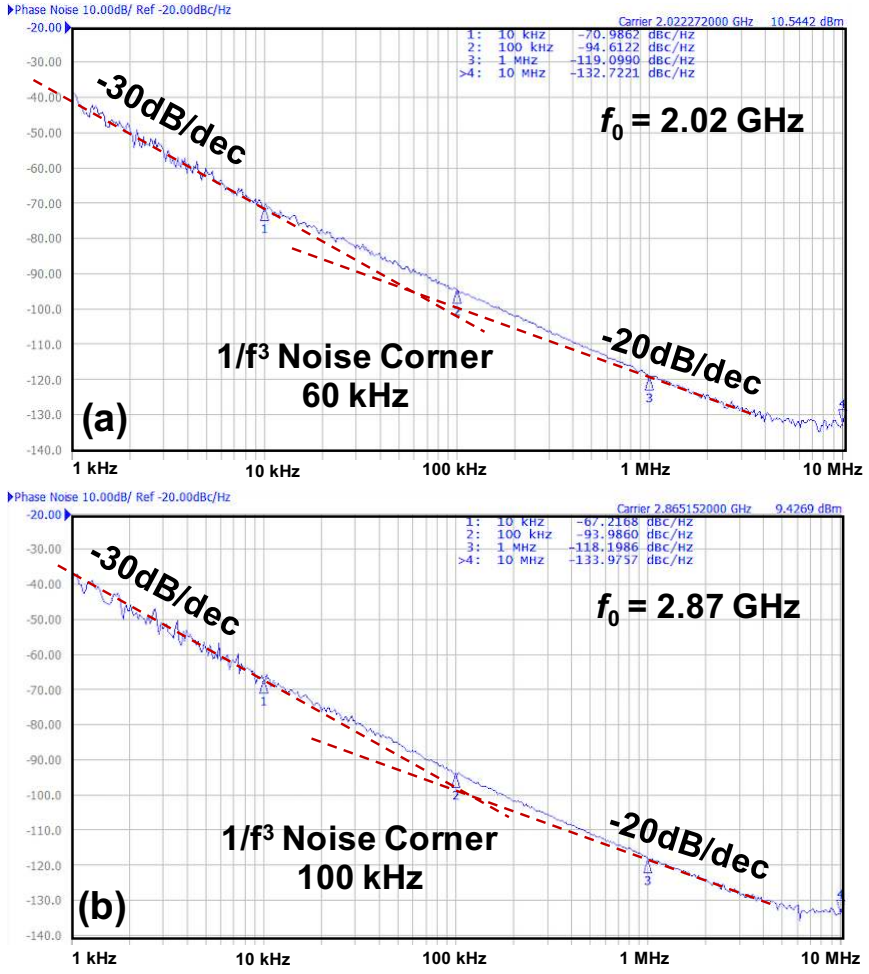

Figure 4.5: Measured PN plots at (a) 2.02 GHz, (b) 2.87 GHz.

Fig. 4.3(a) shows the simulated waveforms of V_{GS}, V_{DS}, and I_D of one transistor in the cross-coupled pair. Due to the low V_{DD} (i.e., 0.3 V) and low biasing V_{bias} (i.e., 0.6 V), the conduction-angle is reduced to about 120°, which means the $M_{1/2}$ is almost turned off around the falling edges (i.e., $t \approx 100$ ps) and rising edges (i.e., $t \approx 300$ ps). The resonant frequency of the implicit CM tank is set much higher than twice the oscillation frequency ($2f_0$), causing the 2nd harmonic current to enter the inductive path, introducing asymmetries between the rising and falling edges (see Fig. 4.3(a)(b) (red cycle)). Note that, due to the 2:3 turns ratio, the supply port (V_{DD}) and the ground port (V_{ss}) are both at the bottom side of the transformer, which provides a well-defined CM return path [51].

Interestingly, the flicker noise up-conversion is still suppressed by the reduced conduction angle. As illustrated in Fig. 4.3(c) (red line), narrowing the conduction angle makes the

Table 4.1: Comparison table of state-of-the-art oscillators with supply voltage ≤0.5 V.

	This Work	[84] ISSCC'18	[77] ISSCC'17	[82] RFIC'15	[83] VLSI'09	[75] JSSC'05
Technology	28 nm	28 nm	16 nm	40 nm	180 nm	180 nm
V_{DD} (V)	**0.3**	0.2	0.2	0.5	0.2	0.5
Power (mW)	**0.75**	0.67	0.6	0.48	0.16	0.57
Freq. (GHz) (TR)	**2.02-2.87 (35%)**	2.24-2.6 (14.9%)	3.2-4.0 (22%)	4.0 (22%)	4.5 (N/A)	3.8 (8.4%)
PN@100kHz (dBc/Hz)	-95.9	-95	-87	-89	-78	N/A
PN@1MHz (dBc/Hz)	-119.3	-119	-114	-114	-104	-119
FoM@1MHz (dBc/Hz)	-188.1	-188	-188	-189	-190	-193
FoM_T@100kHz (dB)	**-195.6**	-186	-186	-190	NA	NA
FoM_T@1MHz (dB)	**-199**	-190	-195	-195	NA	-191
1/f³ Corner (kHz)	60 - 100	150	700*	400	400	NA
Area (mm²)	0.14	0.15	0.11	0.14	0.29	0.76
Density Rule	Vertically Integrated Digital Cap. Bank	Dummy Fill	Dummy Fill	Dummy Fill	-	-

*estimated from the measured plot; $FoM_T = PN - 20\log((f_0/\Delta f)(TR/10)) + 10\log(P_{DC}(mW))$

modulated $1/f$ noise concentrating on appearing at the bottom of V_{DS} (i.e., $t \approx 150$–250 ps), which is a relatively symmetric and noise-insensitive region, see Fig. 4.3(a)(b) (green circle). It ultimately leads to a symmetric effective ISF, shown in Fig. 4.3(c) (green line). The simulations result in flicker PN @10 kHz of -79.65 dBc/Hz, while the calculation based on (4.2) yields -80 dBc/Hz, demonstrating the effectiveness of above analysis (also see [86]). Suppressing the flicker noise via narrowing of conduction angle is expected to achieve low flicker noise corner over wide TR due to the alleviation of special considerations for the 2nd harmonic resonance.

4.4 Experimental Results

The proposed DCO is implemented in TSMC 28-nm LP CMOS (see Fig. 4.4). The core DCO area is 0.38×0.38 mm^2, including the entire capacitor bank and cross-coupled pair, all vertically integrated underneath the transformer. The measured PN is shown in Fig. 4.5 at two extremes of the measured TR of 35% (2.02–2.86 GHz). At the mid carrier frequency of 2.4 GHz and 0.3 V supply, the DCO achieves -95.9 dBc/Hz and -119.3 dBc/Hz PN at 100 kHz and 1 MHz offsets, respectively, while consuming 0.75 mW. The FoM of -188.1 dBc/Hz @1MHz is maintained within 2 dB for the entire TR. Moreover, the low $1/f^3$ noise corner can be also maintained within 60–100 kHz across TR. Even at a 0.2 V supply, the proposed DCO can operate properly, keeping PN at -115 dBc/Hz at 1 MHz offset while consuming only 0.4 mW. The measured frequency pushing is 24 MHz/V (by sweeping V_{DD} from 0.25 V to 0.35 V) which

is comparable to [81] and [87] and suitable for an integration with energy harvesters.

4.5 Conclusion

This chapter described an ultra-low voltage (ULV) low-flicker-noise DCO with 35% TR and compact area by vertically integrating all active devices underneath its transformer windings. Contributed by the transformer's passive gain and conduction angle reduction, the proposed DCO achieves FoM and FoM_T @ 1 MHz of -188 dB and -199 dB, respectively. Low $1/f^3$ corner can be maintained within 100 kHz over the whole TR (35%). This results in FoM_T @ 100 kHz and FoM_T @ 1 MHz that are the best among state-of-the-art sub-mW ULV-oscillators.

Chapter

5

Conclusion

5.1 Summary

The extremely tough data-rate requirements of high-definition (HD) mobile video, augmented reality (AR), and virtual reality (VR) have been forcing the fifth-generation (5G) cellular networks to explore the near millimeter-wave (mmW) frequency bands (e.g., 28 GHz), since the crowded sub-6 GHz frequency bands cannot provide the needed bandwidth. To overcome the severe space attenuation of mmW signals, a beamforming with antenna array is introduced in the CMOS phased-array transceivers, which can also benefit from the miniaturized mmW antenna and high integration of CMOS technology. However, the flicker noise of MOS transistors is deteriorating in advanced CMOS technology, which could further worsen the $1/f^3$ phase noise (PN) corner of local oscillators (especially, mmW oscillators), thus limiting the data rate of CMOS phased-array transceivers. Furthermore, the mechanisms of flicker noise upconversion and reduction in mmW oscillators have never been properly understood by researchers so the existing theories contain significant misconceptions and ambiguities.

In this thesis, a unified theory about flicker noise upconversion and reduction mechanisms in voltage-biased LC oscillators has been constructed. The accurate numerical verification suggests that the 2nd harmonic current entering a non-resistive path is the main contributor to the flicker noise upconversion, which introduces asymmetries in rising and falling edges of oscillation waveforms. To reduce the $1/f^3$ PN, it can make the oscillation waveform symmetric through 2nd harmonic parallel/series-LC resonance or decrease the modulated $1/f$ noise exposure to the asymmetric waveform by narrowing the conduction angle. In addition, the proposed analysis methods and simulation techniques of ISF and flicker NMF are powerful tools to perform both qualitative and quantitative analyses of other low-flicker noise oscillator topologies.

By addressing the two mechanisms for suppressing the $1/f^3$ PN[1], a 30 GHz low flicker-noise corner oscillator for 5G mmW communications and a 2.4GHz low flicker noise corner oscillator for 5G RF (sub-6GHz) communications have been implemented in TSMC 28nm CMOS technology. The former uses the 2nd harmonic resonance featuring special considerations of CM return path, while the latter employs the narrowing of the conduction angle with a passive gain of transformer, further mitigating the start-up problems. The excellent $1/f^3$ PN corner measurements strongly support our claims.

5.2 Some Suggestions for Future Developments

Suggestions for future research are as follows:

- A 28 GHz low $1/f^3$ PN corner quadrature oscillator:

  Quadrature oscillators [90–98] show even worse $1/f^3$ PN corners than their non-quadrature counterparts, especially in mmW bands. In architectures exploiting active coupling [90, 91, 95, 97, 98], the coupling MOS transistors themselves directly contribute considerable flicker PN, while for passive coupling architectures [92, 93, 96], their flicker PN is still poor. Thus, new techniques and theories that lower the quadrature oscillators' flicker PN are also highly desired for 5G communications.

- A 28 GHz low $1/f^3$ PN corner oscillator with wide tuning range (TR) (e.g., >30%):

[1]The third flicker noise reduction mechanism that introducing an additional drain-gate phase-shift with consideration of 2nd harmonic termination is partly discussed in Chapter 2.

Although the technique of 2nd harmonic resonance has proven to be an effective way to reduce the flicker noise upconversion in mmW oscillators [51–54], its performance is very sensitive to the CM tank, limiting the TR to around 15%. To achieve a wide tuning range, another CM tuning capacitor bank could be added. Alternatively, we could apply a technique that narrows the conduction angle in mmW oscillators in order to increase the TR, since it can neglect whether the 2nd harmonic resonance happens or not.

- Analytic expression of ISF based on DM and CM harmonic waveforms with consideration of implicit CM tank:

  Although the accurate simulation technique of the ISF based on positive sidebands was proposed by us in [86], the analytic expression of ISF based on both CM and DM harmonic waveforms is still missing. The original analytic expression based on harmonic waveforms only considers the DM tank and DM waveforms [35], thus failing to explain the flicker noise upconversion.

- Apply the proposed simulation techniques (i.e., $h_{\mathrm{DS}}(t)$ and $I_{1/f,\mathrm{rms}}(t)$) to analyze flicker noise upconversion and reduction in different oscillator topologies, such as in RC/ring/relaxation oscillators [99–101], rotary-travelling-wave oscillators (RTWO) [102–105], crystal/MEMS oscillators, [106–108], and cryogenic oscillators for quantum computation (QC) [109]. This would further benefit from the small-area of RC/ring/relaxation oscillators, intrinsic multi-phase of ring oscillator and RTWO. In particular, the thermal PN in crystal oscillators (due to the ultra-high Q of crystals) [106–108] and cryogenic oscillators (due to the ultra-low operation temperature (e.g., 4 K in CMOS quantum computers)) [109] is very low, while their $1/f^3$ PN suffers substantially. Consequently, the proposed techniques have a very high-potential to reduce the flicker noise in crystal and cryogenic oscillators.

APPENDIX

Phase Noise Modeling Based on Verilog-AMS

A.1 Time-Domain Modeling of Flicker Phase Noise Using Verilog-AMS

Flicker phase noise (PN) has a large influence on 5G mmW systems, such as ADPLLs. However, a circuit-level model of an oscillator is likely to face huge difficulties when used in a system functional verification due to the extremely long simulation times. Thus, the time-domain modeling (event-driven) of PN (especially, the flicker PN) of oscillators is very important and time-saving for 5G system verification.

Thermal phase-noise time-domain modeling is relatively easy and well-studied, but it is difficult to apply it to the flicker phase noise since constructing a filter with a roll-off of 30dB/dec is very challenging. Staszewski *et al.* [74] proposed flicker PN modeling based on several multi-rate infinite impulse response (IIR) filters using a VHDL modeling and simulation language. In this chapter, we will provide a simpler modeling method based on single-rate IIRs (i.e., sampling rate is the oscillation frequency) using Verilog-AMS, since Verilog-AMS is a sign-off industry standard for verification, while supporting both analog

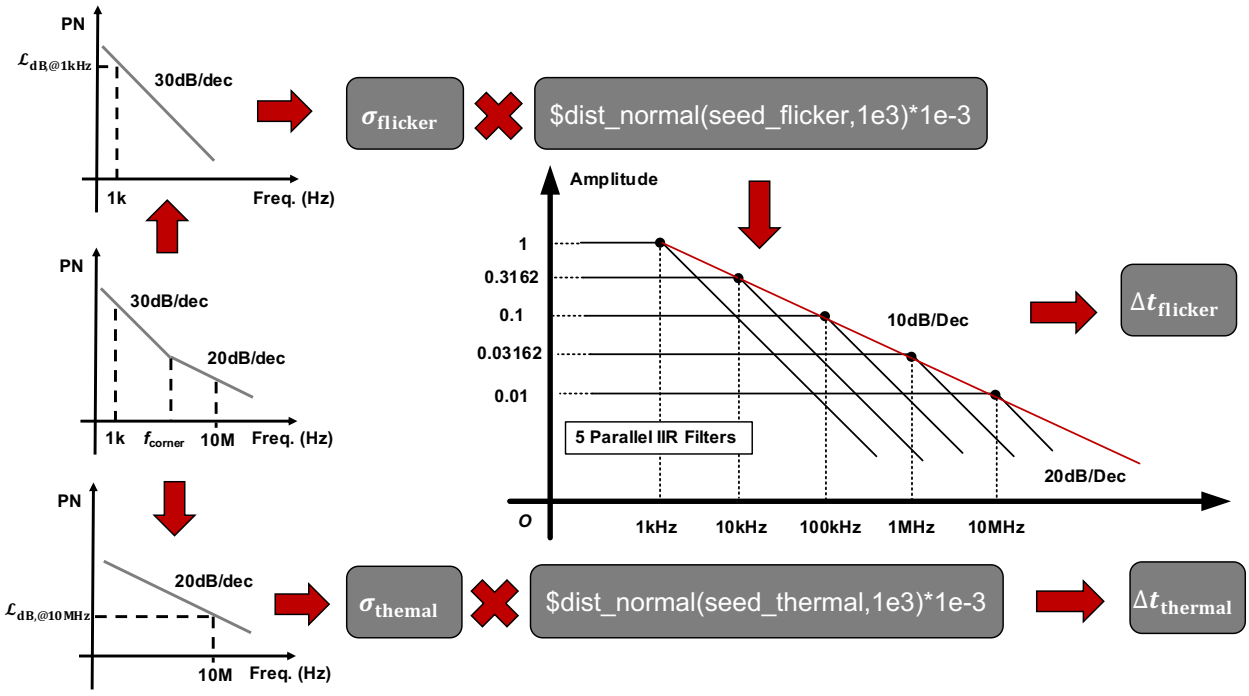

Figure A.1: Time-domain modeling of flicker phase noise and thermal phase noise.

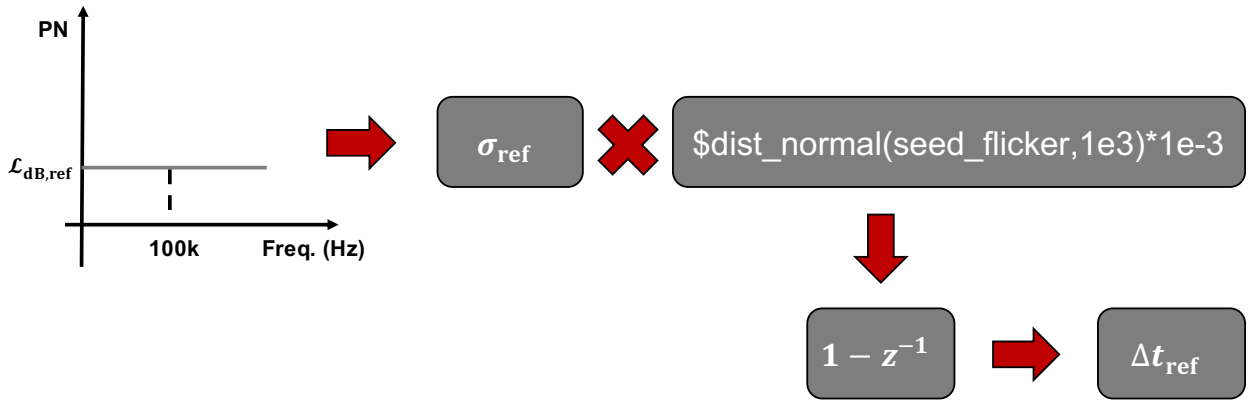

Figure A.2: Time-domain modeling of reference phase noise.

and digital system modeling. For comparison and better understanding, the time modeling of thermal PN and reference PN are also discussed.

A.1.1 Time-Domain Modeling of Thermal Phase Noise

The modeling process of thermal phase noise is shown as Fig. A.1. Assume the PN @10 MHz is dominated by the thermal phase noise, the amplitude of thermal jitter σ_{thermal} is

derived from [74],

$$\sigma_{\text{thermal}} = \frac{\Delta\omega}{\omega_0} \cdot \sqrt{\frac{2\pi}{\omega_0}} \cdot \sqrt{\mathcal{L}(\Delta\omega)} \tag{A.1}$$

where ω_0 is the free-runing frequency of oscillator (e.g., $2\pi\times$ 10GHz), $\Delta\omega$ is the offset frequency (e.g., $2\pi\times$ 10MHz), and $\mathcal{L}(\Delta\omega)$ is the phase noise at $\Delta\omega$ (e.g., $10^{\frac{\mathcal{L}_{\text{dB,@10MHz}}}{10}}$). Then, the amplitude of thermal jitter σ_{thermal} will multiply a normally distributed random number (modeling by function of $dist_normal in Verilog, whose output is an integer) to get the jitter $\Delta t_{\text{thermal}}$ in time-domain every cycle.

A.1.2 Time-Domain Modeling of Flicker Phase Noise

Assume that PN @1 kHz (could be replaced by PN @10 kHz+30 dB, if PN @1 kHz is not available) is dominated by the flicker phase noise. The amplitude of flicker jitter σ_{flicker} is derived as

$$\sigma_{\text{flicker}} = \frac{\Delta\omega}{\omega_0} \cdot \sqrt{\frac{2\pi}{\omega_0}} \cdot \sqrt{\mathcal{L}(\Delta\omega)} \tag{A.2}$$

where $\Delta\omega = 2\pi \cdot 1\text{kHz}$. As in the modeling of thermal phase noise, the amplitude of flicker jitter σ_{thermal} multiplies a normally distributed random number. Then, the output must pass through a low pass filter (LPF) with a roll-off of 10 dB/dec to shape the spectrum of $\Delta t_{\text{flicker}}$ with a roll-off of 30 dB/Hz (Note: the spectrum roll-off of $\Delta t_{\text{thermal}}$ is 20 dB/Hz).

The LPF with a roll-off of 10 dB/dec is constructed by using 5 parallel IIR filters (sampling rate f_{sampling}: oscillation frequency (e.g., 10 GHz)) (see Fig. A.1), whose corner frequency $f_{\text{IIR corner},k}$ are 1 kHz, 10 kHz, 100 kHz, 1 MHz, and 10 MHz, while the gains A_k are 1, $10^{-10/20}$ (i.e., 0.3162), 0.1, 0.03162, and 0.01, respectively. The 5 first-order IIR filters are described as

$$y_k[i] = (1 - a_k)y_k[i-1] + a_k A_k x[i] \tag{A.3}$$

where $k = 1, 2, 3, 4, 5$, and a_k depends on the IIR corner frequency,

$$a_k = 2\pi \frac{f_{\text{IIR corner},k}}{f_{\text{sampling}}} \tag{A.4}$$

The complete Verilog-AMS code is shown as Figs. A.3 and A.4.

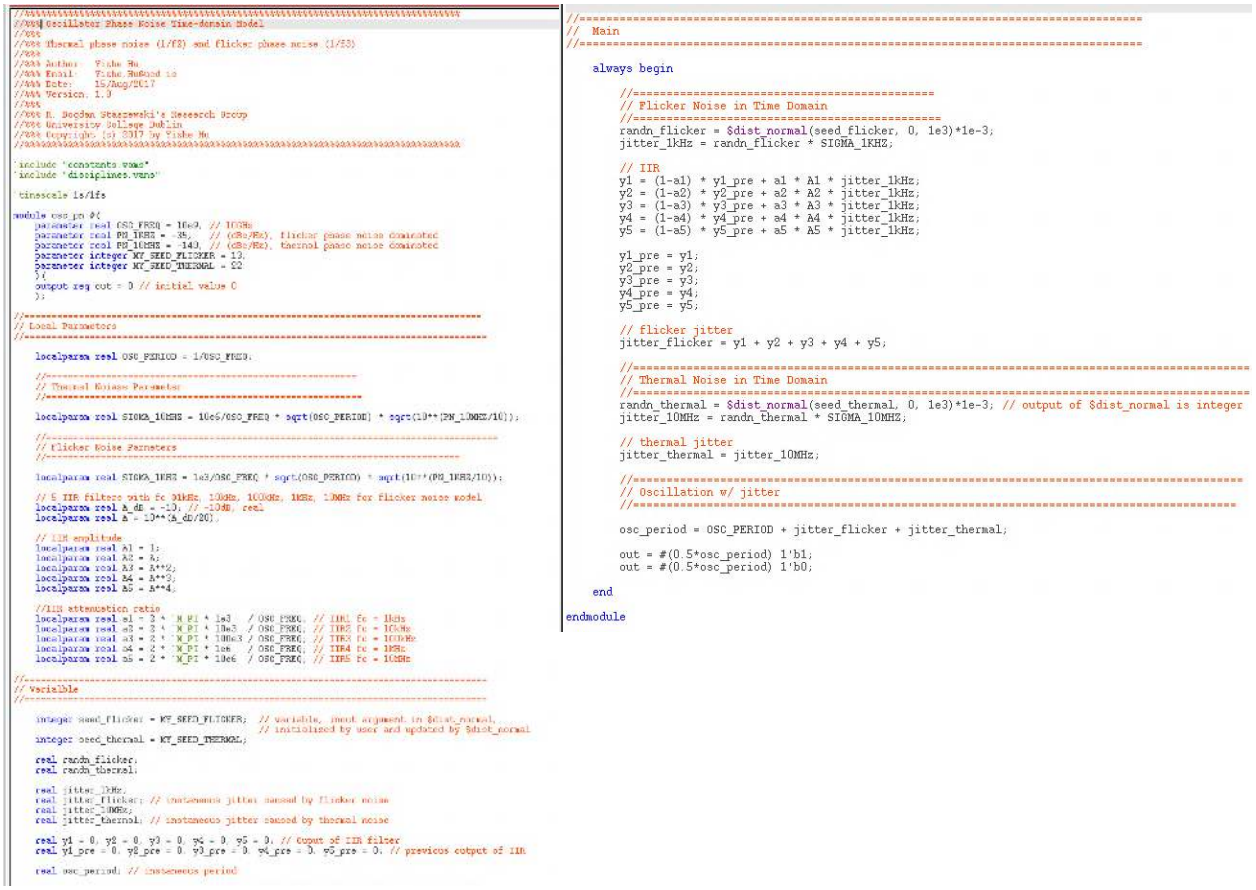

Figure A.3: Time-domain modeling of flicker phase noise and thermal phase noise in a 10GHz oscillator.

A.1.3 Time-Domain Modeling of Reference Phase Noise

Since the spectrum of the reference phase noise is relatively flat from ∼100 kHz to ∼100 MHz (no 20 dBc/Hz or 30 dB/dec roll-off), the amplitude of the reference jitter σ_{ref} is derived as [74]

$$\sigma_{\text{ref}} = \frac{1}{\omega_0} \cdot \sqrt{\frac{\omega_0}{2\pi} \cdot \mathcal{L}(\Delta\omega)} \tag{A.5}$$

where $\mathcal{L}(\Delta\omega)$ is the reference in-band PN. For a 50MHz reference with an in-band PN of -147dBc/Hz, σ_{ref} is calculated as $\frac{1}{2\pi \times 50\text{MHz}} \cdot \sqrt{50\text{MHz} \times 10^{\frac{-147}{10}}} \approx 1\text{ps}$. Since the reference noise is non-accumulative, it must pass through the "$(1 - z)$" filter, as shown in Fig. A.2.

The complete Verilog-AMS code is shown as Fig. A.5. Time-domain modeling of phase noise for system verification is also discussed.

Figure A.4: Time-domain modeling of a DCO.

```
//%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
//%%% Reference clock generator
//%%% Non-accumulative jitter
//%%%
//%%% Author:   Yizhe Hu
//%%% Email:    Yizhe.Hu@ucd.ie
//%%% Date:     2/July/2018
//%%% Version: 1.0
//%%%
//%%% R. Bogdan Staszewski's Research Group
//%%% University College Dublin
//%%% Copyright (c) 2018 by Yizhe Hu
//%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
`include "constants.vams"
`include "disciplines.vams"
`timescale 1s/1fs

module fref_500M_150pn #(

    parameter real F_REF       = 500e6,    // reference freq 500MHz
    parameter real PN_100KHZ   = -150,     // -160dBc/Hz
    parameter real DLY_INIT    = 100e-9,    // 100ns
    parameter integer MY_SEED_REF = 29  // set user's seed for pseudorandom  numbers


    )(

    output reg out = 1'b0

    );

//=============================================================================
// Localparam
//=============================================================================

    localparam real T_REF      = 1/F_REF;
    localparam real JITTER_RMS = T_REF /2 /`M_PI *sqrt(F_REF *10**(PN_100KHZ /10)); // reference non-accumulative jitter 1ps

//=============================================================================
// Variable
//=============================================================================

    integer seed_ref = MY_SEED_REF; // variable, inout argument in $dist_normal, initialized by user and updated by $dist_normal
    real    randn = 0; // normally distributed pseudorandom numbers
    real    jitter = 0;
    real    jitter_pre = 0;
    real    jitter_non_accu = 0;
    real    ref_period;

//=============================================================================
// Main
//=============================================================================

    initial begin

        # DLY_INIT

        forever begin
            //=====================================================
            // Non-accumulative jitter
            //=====================================================
            randn = 1e-3 * $dist_normal(seed_ref, 0, 1000); // output of $dist_normal is integer
            jitter = randn * JITTER_RMS;
            jitter_non_accu = jitter - jitter_pre; // non-accumulative jitter
            jitter_pre = jitter;

            //=================================================
            // clk w/ non-accumulative jitter
            //=================================================
            ref_period = 1/F_REF + jitter_non_accu;

            #(0.5*ref_period)
            out =  1'b1;

            #(0.5*ref_period)
            out =  1'b0;
        end
    end

endmodule
```

Figure A.5: Time-domain modeling of a 500MHz reference with in-band PN -150dBc/Hz.

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Journal Papers

- **Y. Hu**, T. Siriburanon, and R. B. Staszewski, "Intuitive understanding of flicker noise reduction via narrowing of conduction angle in voltage-biased oscillators," *IEEE Trans. on Circuits and Systems II (TCAS-II)*, vol. xx, iss. xx pp. xx–xx, xxx. 2019. DOI: 10.1109/TCSII.2019.2896483. [IEEE Xplore link (Open Access)] (Early Access)

- **Y. Hu**, T. Siriburanon, and R. B. Staszewski, "A low-flicker-noise 30-GHz class-F_{23} oscillator in 28-nm CMOS using implicit resonance and explicit common-mode return path," *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 53, no. 7, pp. 1977–1987, July 2018. DOI: 10.1109/JSSC.2018.2818681. [IEEE Xplore link (Open Access)]

Conference Papers

- J. Du, **Y. Hu**, T. Siriburanon, and R. B. Staszewski, "A 0.3V, 35% tuning-range, 60 kHz $1/f^3$-corner digitally-controlled oscillator with vertically integrated switched capacitor banks achieving FoM_T of -199dB in 28-nm CMOS," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, 17 Apr. 2019, ses. 26-4, pp. 1–4, Austin, TX, USA.

- **Y. Hu**, T. Siriburanon, and R. B. Staszewski, "A 30-GHz class-F_{23} oscillator in 28nm CMOS using harmonic extraction and achieving 120 kHz $1/f^3$ corner," in *Proc. IEEE Eur. Solid-State Circuits Conf. (ESSCIRC)*, sec. A4L-C1, pp. 87–90, 12 Sept. 2017, Leuven, Belgium. DOI: 10.1109/ESSCIRC.2017.8094532. [IEEE Xplore link]

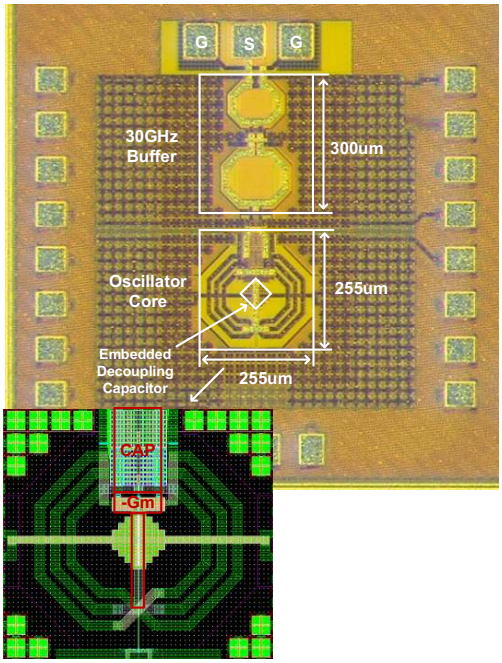
- **Y. Hu** and W. Li, "A modeling approach for mixed-mode FMCW synthesizer allowing frequency error analysis," in *Proc. IEEE International Symp. on Circuits and Systems*

(ISCAS), 2015, pp. 1490–1493.

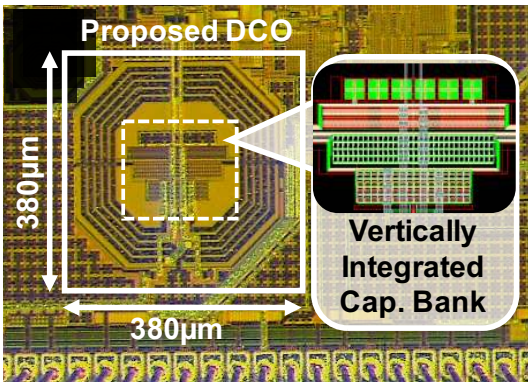
Seminars

- **Y. Hu**, "Intuitive understanding of flicker noise reduction via narrowing of conduction angle in voltage-biased oscillators,"*Webinar (1-hr) presented at Microelectronic Circuits Centre Ireland (MCCI)*, 27 March 2019.
- **Y. Hu**, "Flicker noise elimination in high-performance mm-Wave oscillators,"*Best Poster Award (GOLD), Seminar (1-hr) presented at IEEE SSCS MCCI Annual Forum*, 11 Oct. 2018.

Chip Micrograph Gallery



A Low-Flicker-Noise 30-GHz Class-F_{23} Oscillator in 28-nm CMOS using Implicit Resonance and Explicit Common-Mode Return Path [*ESSCIRC*'17 & *JSSC*'18 (invited)]



A 0.3 V, 35% Tuning-Range, 60-kHz 1/f^3-Corner DCO with Vertically Integrated Switched Capacitor Banks Achieving FoM_T of -199 dB in 28-nm CMOS [*CICC*'19] (with Jianglin Du)

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