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Flux-Based Active Filter Controller

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***Abstract*— This paper presents a synchronous frame flux-based control method for a parallel active filter application. The flux-based controller directly implements the inverter switchings in the synchronous reference frame by a hysteresis rule-based carrier-less pulse-width modulation (PWM) strategy to achieve high current bandwidth. This paper addresses the issues and impact on parallel active filtering requirements for utility interface of commonly used harmonic front-ends. The synchronous frame flux-based controller provides additional insights for harmonic current compensation requirements. Simulation results provide the validation of the flux-based active filter controller to meet IEEE Standard 519 recommended harmonic standards for large rated nonlinear loads under balanced and unbalanced supply conditions.**

I. Introduction

ACTIVE filtering as a means for harmonic compensation is becoming a cost effective solution for realizing a harmonic free utility interface for large nonlinear power electronic loads such as adjustable speed drives (ASD). Proliferation of power electronics loads, a prerequisite for realizing energy efficiency and productivity benefits, has brought utilities to crossroads. Utilities more frequently encounter harmonic related problems such as substantially higher system losses, required derating of distribution equipment, harmonic interactions between customers or between the utility and load, reduced system stability, and safe operating margins. Utilities are beginning to implement harmonic "standards" such as IEEE Standard 519 to alleviate harmonic related problems. It is important to note, however, that IEEE Standard 519 is only applicable at the point of common coupling (PCC) at a plant [1].

The parallel active filter approach as shown in Fig. 1 is based on the principle of injection of load harmonic currents and hence is characterized by nonsinusoidal current tracking and high current bandwidth requirements [2]–[3]. The achieved harmonic compensation characteristics are dependent on the filtering algorithm employed for the extraction of load current harmonics. It has been shown in [4] and [5] that synchronous frame-based compensators achieve better performance under all supply and load conditions, and without any assumptions on supply voltage and current waveform quality than state of the art compensators, such as instantaneous reactive power (IRP) or "p-q" theory-based compensators [6] and notch filter-based compensators. Control requirements and implementation issues of parallel active filters are discussed in Section II.

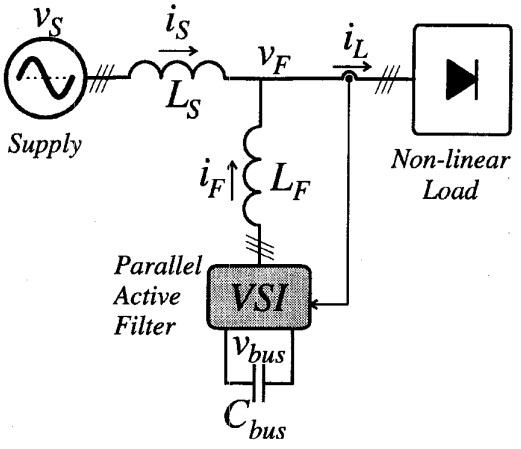

Fig. 1. Parallel active filter system diagram.

The flux-based controller utilizes the linear relation between the flux and current in a linear inductor and facilitates direct implementation of a current regulator without explicit generation of voltage references. Concept and implementation of the synchronous frame flux-based controller is discussed in Section III. Experimental measurements and discussion of various commonly used harmonic front-ends and their impact on active filtering requirements are given in Section IV. Sequencing and start-up issues of the parallel active filter are given in Section V. Simulation results for a commonly used utility interface front-end for large rated ASD load is given in Section VI. The flux-based inverter controller achieves implementation of a general current regulator which is well suited for both nonsinusoidal current tracking, such as for active filters, and sinusoidal current references, such as for motor/servo drive applications as discussed in [7].

II. Control Requirements for Parallel Active Filters

The parallel active filter is controlled as a harmonic current source to inject load current harmonics into the supply, and hence the supply line impedance does not influence its compensation characteristics. This requires implementation of a suitable current regulator for the parallel active filter inverter.

Paper IPCSD 95–77, approved by the Industrial Power Converter Committee of the IEEE Industry Applications Society for presentation at the 1995 IEEE Industry Applications Society Annual Meeting, Lake Buena Vista, FL, October 8–12. Manuscript released for publication November 6, 1995.

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Publisher Item Identifier S 0093-9994(96)02965-9.

Realization of harmonic free utility interface applications by parallel active filters are in general characterized by the following:

- nonsinusoidal multiple frequency current tracking by the current regulator of the parallel active filter inverter;
- ability to operate with low inverter output filter inductances ($<5\% = 0.05$ p.u.);
- minimization of low and high frequency current errors by the current regulator;
- High di/dt current tracking while minimizing low frequency current errors.
- high current bandwidth requirement of the parallel active filter inverter;
- desire for a constant inverter switching frequency.

Implementation of various current regulators can be classified as either carrier-based or carrier-less pulse-width modulation (PWM) schemes. Carrier-based current controllers explicitly generate an "average voltage" reference to be synthesized by the modulator, which can be either by a predictive scheme [8]–[10] or can employ a stationary/synchronous frame-based PI regulator to transform current errors into voltage references [11]. However, carrier-less schemes such as hysteresis current regulators do not explicitly generate an "average voltage" reference, but employ a hysteresis band—fixed or variable—to force switchings.

Hysteresis and predictive current regulators are the only two viable choices for nonsinusoidal multiple frequency current tracking. Synchronous or stationary frame PI-based current regulators have significant phase shifts for nonsinusoidal multiple frequency current tracking, due to frequency-dependent PI transfer function and hence cannot be used for such applications. Hysteresis current regulators have been widely used for such applications because of their high bandwidth and simple structure [12]. However, conventional hysteresis current regulators have the following problems [12]:

- do not maintain constant inverter switching frequency;
- per phase-based hysteresis current regulators suffer from phase interactions due to variability of per phase switching, which causes significant low frequency errors and increased peak current ripple;
- existence of unacceptable limit cycles in the current, especially with low inductances.

These problems are accentuated under nonsinusoidal current tracking conditions. Several different forms of estimating the back-EMF and phase-locked-loop (PLL) techniques exist, which modulate the hysteresis band to minimize the variable switching frequency limitation [13]–[14], but these methods do not address the other limitations. Further, per phase-based hysteresis current regulators, even including those that feature an explicit decoupling of the phases by the integration of the neutral voltages, do not alleviate the problems of low-frequency current errors, peak current ripple, and limit cycles in the current— especially with low inductance operation and under nonsinusoidal current tracking conditions, which are essential requirements of parallel active filters.

Complex dq vector-based current regulators—for both carrier and carrier-less modulation schemes—are imperative to alleviate the problems of per phase-based current regulators [10]. Their implementation implicitly decouples the phases and hence prevents phase interactions and facilitates prescribed adjacent state switching vectors to enable minimization of low frequency current errors and current ripple.

III. Flux Based Active Filter Controller

The block diagram of the synchronous frame flux-based controller shown in Fig. 2 is used for the extraction of load current harmonics and for the direct implementation of inverter switchings by means of a hysteresis rule-based carrier-less PWM scheme. The active filter terminal flux $\vec{\Psi}_F^s$, is measured and used as a feed-forward quantity to generate the inverter output filter *inductor flux reference* $\vec{\Psi}_\delta^{e*}$, as shown in Fig. 2. The active filter terminal flux $\vec{\Psi}_F^s$ cannot be estimated by means of an open-loop integration of the active filter terminal voltage $\vec{v}_F^s$ in practice and requires a special integrator structure as given by the transfer function $H(s)$ in (1). $H(s)$ has a large gain around 1 Hz, but zero gain at dc, and mimics a "pure integrator" adequately for all frequencies above 5 Hz, including the nominal 60-Hz supply frequency

$$\vec{\Psi}_F^s(s) = \frac{s\tau_a}{(s\tau_b + 1)(s\tau_c + 1)} \cdot \vec{v}_F^s(s). \tag{1}$$

However, the inverter flux $\vec{\Psi}_{inv}^s$ can be calculated by a pure integration of the measured inverter three-phase output voltages, as shown in Fig. 2, because it is used in a closed loop:

$$\vec{\Psi}_{inv}^s = \vec{\Psi}_{inv}^s(0) + \int_0^t \vec{v}_{inv}^s(\tau)\,\mathrm{d}\tau. \tag{2}$$

Equations (1) and (2) indicate that the voltage can be regarded as "flux speed." The PLL function is implemented by means of a PI regulator, voltage controlled oscillator (VCO), and counter as shown in Fig. 2, to lock onto the "almost circular" active filter terminal flux, by forcing $\vec{\Psi}_{Fq}^e = 0$ and generates a 12-b digital angle ξ. The measured load currents $\vec{i}_L^s$ are transformed to the synchronously rotating frame as shown in Fig. 2. In the synchronously rotating d^eq^e frame, the current components at the fundamental frequency (60 Hz), are transformed to dc quantities and all the harmonic current components are transformed to nondc quantities and undergo a frequency shift of 60 Hz in the spectrum. The resulting current in the synchronous d^eq^e frame $\vec{i}_L^e$ is low-pass filtered, which can be implemented by switched capacitor filters, to extract the fundamental frequency current component from $\vec{i}_L^s$. Extraction of the dc quantities by a low pass filter provides insensitivity to phase errors. This is a significant advantage of the synchronous frame controller since most other controllers, such as all notch filter-based implementations, will introduce significant phase errors at fundamental and at harmonic frequencies. The synchronous frame controller

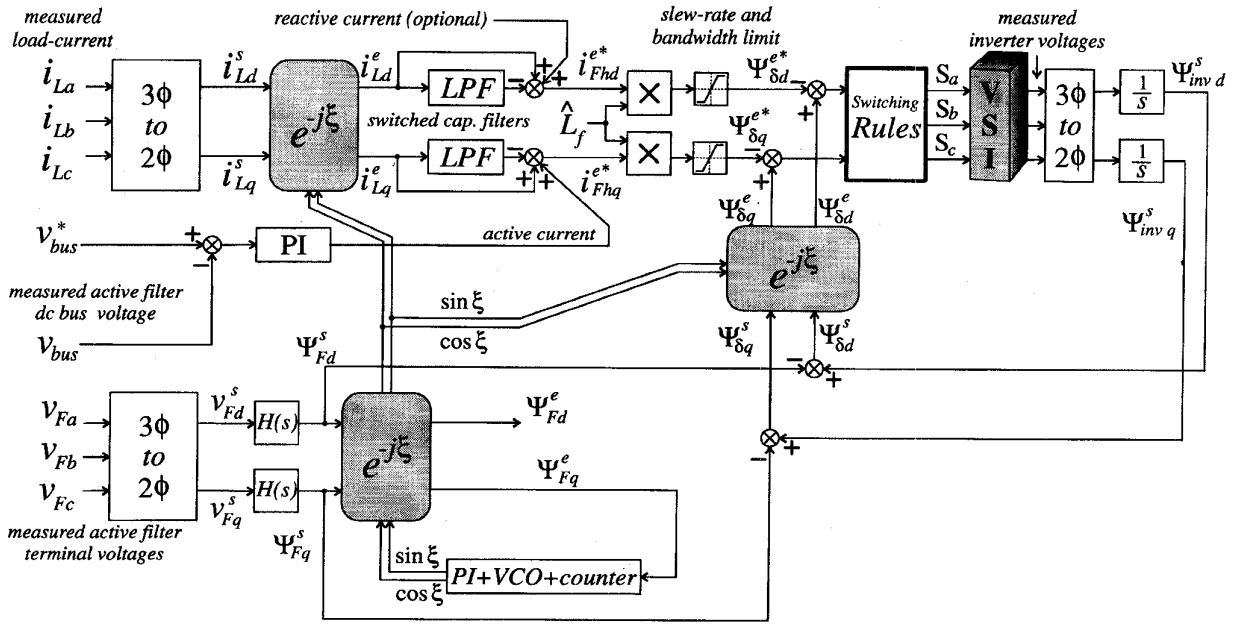


Fig. 2. Flux-based active filter controller.

implementation is sensitive to dc offsets and gains. This can be eliminated/minimized by a maximally flat Butterworth low-pass filter implemented by switched capacitor filters with input dc blocking capacitors. The sampling frequency of the switched capacitor filter determines the highest harmonic frequency possible which can be filtered without aliasing errors. This is a design trade-off for switched capacitor filter applications, since the cross-over frequency of the low-pass filter determines the maximum harmonic frequency limit and vice-versa. A fifth order low-pass filter with a cross-over frequency $f_0 = 30$ Hz implemented by switched capacitor filters achieves more than -40 db attenuation for the 5th harmonic frequency. The sampling frequency of the switched capacitor filter is 3 kHz ($100 \cdot f_0$) and this allows harmonic filtering up to 1.5 kHz (25th harmonic) without any aliasing errors.

In the flux model as shown in Fig. 3(a), the resistance of the inverter output filter inductor L_F is neglected. From this model, the required reference inverter flux $\vec{\Psi}^{s*}_{inv}$ (in the stationary $d^s q^s$ frame) is given as

$$\vec{\Psi}^{s*}_{inv} = \vec{i}^{s*}_F \cdot \hat{L}_F + \vec{\Psi}^{s}_F. \tag{3}$$

Fig. 3(b) shows the inverter reference flux vector $\vec{\Psi}^{s*}_{inv}$ orbit and the "almost circular" active filter terminal flux vector $\vec{\Psi}^{s}_F$ orbit. The inverter output filter inductance L_F has been increased from $L_F = 5\%$ p.u. to $L_F = 25\%$ p.u. for illustration purposes. The active filter reference current $\vec{i}^{s*}_F$ as shown in Fig. 3(b) has been rescaled. The flux model equation (3) neglecting resistance of the inverter output filter inductor L_F given in Fig. 3(a) is also valid for the synchronous $d^e q^e$ frame:

$$\vec{\Psi}^{e*}_{inv} = \vec{i}^{e*}_F \cdot \hat{L}_F + \vec{\Psi}^{e}_F. \tag{4}$$

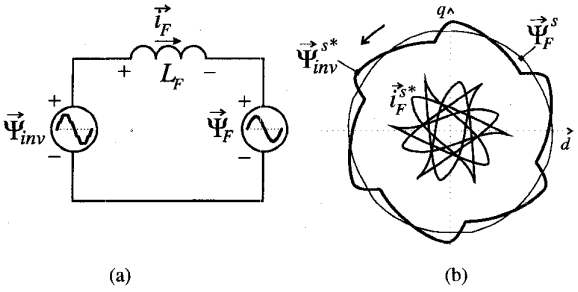


Fig. 3. (a) Flux model of active filter. (b) Reference flux generation according to (3) for a system with both ac side and dc side inductors.

The current vector $\vec{i}^{e*}_{Fh}$ as shown in Fig. 2 does not contain any dc-component and represents the extracted load harmonic current $\vec{i}^{e}_{Lh}$ to be compensated by the active filter. However, the active filter current $\vec{i}^{s}_F$ also needs to provide the inverter losses and the power to charge the dc-link capacitor C_{bus} of the inverter. A dc bus voltage feedback loop regulates active power flow to compensate for the inverter losses by a PI regulator output which is added to i^{e*}_{Fhq} as shown in Fig. 2. This results in a small fundamental active filter current in phase with the active filter terminal voltage $\vec{v}^{s}_F$, which regulates the required active power flow. The PI regulator output should be bandwidth limited to eliminate all harmonic frequency components present in the load current to avoid any power oscillation between the active filter and supply, or between the active filter and harmonic producing load.

Reactive power compensation of the load can also be achieved by the flux-based active filter controller by adding a reactive current command in the d^e-axis to i^{e*}_{Fhd} as shown in Fig. 2. This flexibility is a desirable feature in general and especially for thyristor-based front-end loads, which require

reactive power compensation to achieve unity input displacement factor, with slightly higher active filter rating.

The inverter flux control method to achieve active filter current regulation is based on [15]–[16]. A similar strategy for flux-based current regulator implementation for PWM rectifiers is given in [17]. The active filter inverter current can be considered to be a direct result of the inductor flux $\vec{\Psi}_\delta^e$ which is given as

$$\vec{\Psi}_\delta^e = \vec{\Psi}_{inv}^e - \vec{\Psi}_F^e. \tag{5}$$

Reference flux $\vec{\Psi}_\delta^{e*}$ as shown in Fig. 2 gives the required angular position and magnitude from which the actual inductor error flux vector $\Delta\vec{\Psi}_\delta^e$ is calculated according to (6)

$$\Delta\vec{\Psi}_\delta^e = \vec{\Psi}_\delta^e - \vec{\Psi}_\delta^{e*} \tag{6}$$

$$\Delta\vec{\Psi}_\delta^e = (vec\Psi_{inv}^s - \vec{\Psi}_F^s)e^{-j\xi} - i_F^{e*} \cdot \hat{L}_F. \tag{7}$$

The d^e and q^e vector components of flux deviation $\Delta\vec{\Psi}_\delta^e$ are the inputs to the switching rules decision unit. Note that the inductor flux across L_F is less than 5% of the active filter terminal flux $\vec{\Psi}_F$. The small "vector" difference between $\vec{\Psi}_{inv}^s$ and $\vec{\Psi}_F^s$ as can be seen in Fig. 3(b) necessitates the subtraction before the vector rotation, as shown in Fig. 2. An important requirement is the pure integration of $\vec{v}_{inv}^s$ (2) to generate the inverter flux vector $\vec{\Psi}_{inv}^s$. Note that additional filtering of this signal $\vec{\Psi}_{inv}^s$ is *not* required since the ac ripple in the synchronous d^eq^e frame itself provides the switching criterion. The switching rules, as explained below, apply to the deviation between the actual inductor flux and the reference inductor flux in the synchronous d^eq^e frame.

Four decision "box" boundaries denoted by $\pm\Delta_d$ and $\pm\Delta_q$ are predetermined by the desired minimum pulse-width of the inverter $T_{\min}$,, dc-bus voltage V_{bus}, supply frequency f_e and the inductor flux amplitude level Ψ_δ. Fig. 4 shows the confined "box" defined by the decision boundaries with respect to the tip of the rotating inverter flux reference vector in the stationary d^sq^s frame. The center of the "box" represents the actual inverter flux reference and the "box" dimension determines the resulting high and low frequency inverter flux/current errors due to the switching strategy.

As can be seen from the $2^3 = 8$ possible switching states in Fig. 4(a), the inverter flux vector $\vec{\Psi}_{inv}^s$ can only transverse in 6 predefined directions given by the corresponding 6 active vectors, and the inverter flux vector $\vec{\Psi}_{inv}^s$ incurs stops during the inverter zero states, indicated by 000 and 111. Synchronous d^eq^e frame implementation of the flux-based controller results in the identification of the duration of inverter active and zero vector states. This is advantageous and allows implementation of prescribed adjacent active vector and zero states for any given inverter flux reference by implementation of simple rules in the synchronous d^eq^e frame.

In the stationary frame the flux $\vec{\Psi}_{inv}^s$ stops during each zero vector. In the synchronous d^eq^e frame during each zero vector, the inverter flux vector revolves in the negative direction and hence the angular deviation between $\vec{\Psi}_{inv}^{e*}$ and $\vec{\Psi}_{inv}^e$ increases. However, during adjacent active vector states, the inverter flux $\vec{\Psi}_{inv}^s$ speed will be larger than that of $\vec{\Psi}_{inv}^{s*}$ and hence the angular deviation between them increases. This implies that the zero vectors mainly control the angular (tangential) flux advancement for high "modulation index" conditions and determine the peak current ripple in the q^e-axis [7].

Due to the discrete inverter active switching vectors, the actual trajectory of $\vec{\Psi}_{inv}^s$ will always be either on the inner side of the inverter reference flux direction of progress (leading), or on the outer side (lagging). Fig. 4(a) shows how a choice of radial tolerance band will force the actual inverter flux orbit to stay between the inner and outer circles with just the first two rules, as given below, which always guarantee adjacent state switching. The last two rules ensure accurate positioning of zero vectors, which are constrained by the "box" boundaries, to be all of equal duration.

A. The Switching Rules

The block "Switching Rules" in Fig. 2 carries out the following functions.

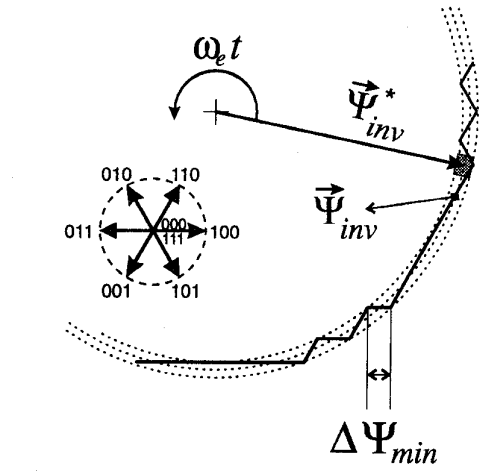
1) When reaching the outer radius ($\Psi_{inv\,d}^e > \Psi_{inv\,d}^{e*} + \Delta_d$) and lagging, switch to the active vector which leads the present vector by $+60°$.
2) When reaching the inner radius ($\Psi_{inv\,d}^e > \Psi_{inv\,d}^{e*} - \Delta_d$) and leading, switch to the active vector which lags the present vector by $-60°$.
3) If the tangential inverter flux error exceeds $+\Delta_q$, switch to the zero vector that involves one switch transition.
4) If the tangential inverter flux error is smaller than $-\Delta_q$, switch back to the same active vector before the zero vector.

In this way a tangential inverter flux ripple with constant peak to peak amplitude of $\pm\Delta_q$ is realized, yielding a minimal q-axis inverter current ripple, or an equivalent torque ripple for a machine drive application. The radial inverter flux ripple with an amplitude of $\pm\Delta_d$ corresponds to the d-axis inverter current ripple or equivalent magnetizing current ripple for a machine drive application. These rules constrain the inverter flux vector error to a rectangular "box" of dimensions $\pm\Delta_d$ and $\pm\Delta_q$ in the synchronous d^eq^e frame.

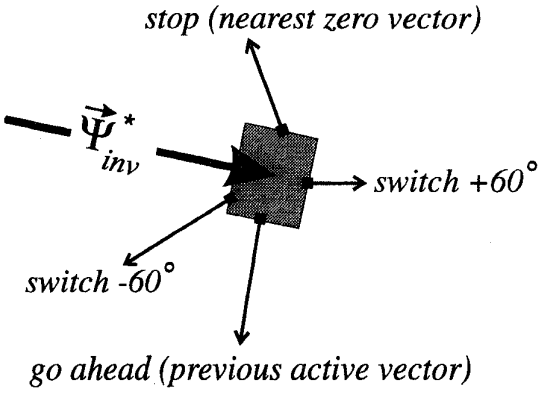
For small tracking errors of the inverter flux in both d^e and q^e directions, a square "box" is optimal. For single frequency inverter flux/ current tracking, such as for motor drive applications, the tangential inverter flux/current ripple [18]–[19] has much more impact on the generated torque ripple, thus effectively reducing the simultaneous need for a small radial ripple.

The implementation of the flux-based controller in the synchronous d^eq^e frame achieves implicit decoupling of the phases and prevents adverse effects of phase interactions and undesirable limit-cycles in the current. The motivation for carrying out the above inverter switching rules in the synchronous d^eq^e frame as opposed to the stationary d^sq^s frame are simple implementation and the fact that the load harmonic current extraction is already performed in the synchronous d^eq^e frame by the synchronous frame-based controller [4].

The above rule-based hysteresis (or carrier-less) inverter switching strategy implemented in the synchronous d^eq^e frame



(a)



(b)

Fig. 4. (a) Principle of switching rules in the synchronous frame and the 8 possible switching states. (b) The four switching rules.

achieves disturbance rejection of dc-link fluctuations, nonsinusoidal voltages on the rectifier input due to commutation, unbalanced supply and load conditions, turn-on and turn-off delays and voltage drops are automatically compensated for, due to the integration of the actual inverter output voltages. This disturbance rejection feature is desirable since it does not require implementation of additional feedforward compensators for disturbance rejection.

The flux-based active filter controller is amenable to analog-digital hardware implementation. Hardware implementation of the controller is desirable since it circumvents the sampling and computation delay problems associated with any digital signal processor-based (DSP) implementation, which are the major limitations for high frequency inverter flux/current tracking. Analog controller implementation also effectively alleviates the high-frequency tracking issues related to high-frequency reference change of the inverter flux/current, compared to a sampled current regulator implementation.

Suppression of the inverter switching frequency ripple by a capacitive filter and other related issues have not been addressed in this paper.

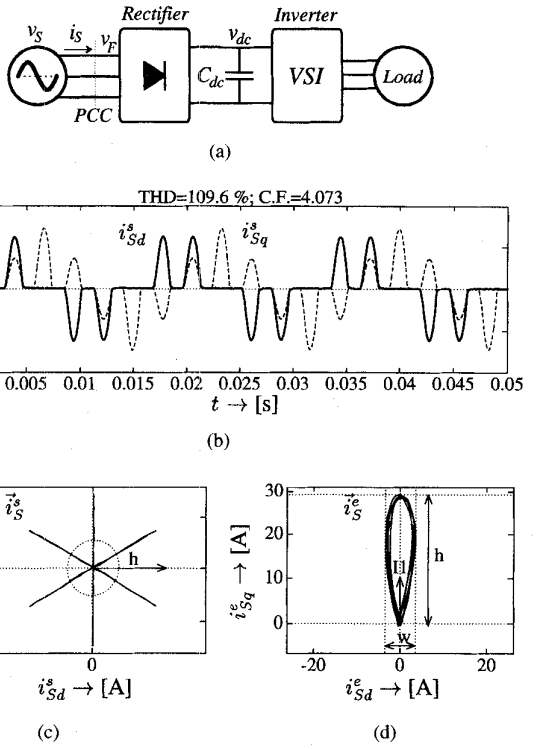


Fig. 5. Case A. (a) Utility interface. (b) Measured line currents by flux controller. (c) In stationary frame. (d) In synchronous frame.

IV. Harmonic Producing Loads and Active Filtering Requirements

Diode and thyristor bridges constitute common utility interface front-ends. The IEEE Standard 519 recommended harmonic standard is a PCC specification and its short circuit ratio (SCR) determines the allowable total harmonic distortion (THD) supply current limits at the PCC. The utility interface characteristics depend on the PCC transformer percentage leakage inductance and on the filtering elements used in the harmonic front-end system. The PCC transformer usually supplies diverse loads in an industrial plant and active filtering solutions should be applied at the PCC in such cases. A simple classification of harmonic performance of various utility interface systems is given below. The experimental waveforms are given for 115 V, 3ϕ, 60 Hz system with 25 μH PCC transformer leakage inductance and a dc bus capacitor $C_{\rm dc} = 1340\,\mu$F. The utility transformer is considered as the PCC, as shown in Figs. 5–8. Implementation issues for parallel active filter system for various commonly used utility interface front-ends are discussed below.

A. Diode Rectifier with DC Side Capacitor System

Fig. 5(a) shows the most common topology for ASD utility interface front-ends. The supply current i_S is discontinuous with very high peak currents. The supply current THD's are typically around 60% to greater than 130%. The supply peak current, THD and di/dt significantly increase for stiff ac supply systems. Fig. 5(b) shows experimental stationary $d^s q^s$

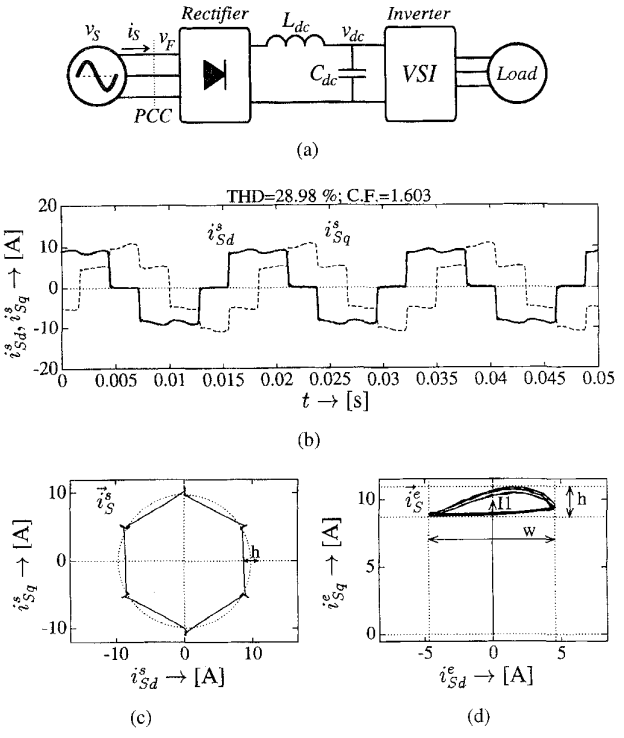


Fig. 6. Case B. (a) Utility interface. (b) Measured line currents by flux controller. (c) In stationary frame. (d) In synchronous frame.

frame supply current components i^s_{Sd} and i^s_{Sq} waveforms with THD value of 109.6% and crest factor (CF) of 4.0 at 1.1 kW load. Fig. 5(c) shows supply current vector $\vec{i}^s_S$ and its extracted fundamental component in the stationary d^sq^s frame. Fig. 5(d) shows the supply current vector $d^s\vec{i}q^e_S$ and the affect of supply voltage V_s unbalance in the synchronous d^eq^e frame. The markers w, h, and $I1$ indicate the width (d-component ripple), height (q-component ripple), and fundamental component of the supply current respectively. From Fig. 5(d) it is inferred that harmonic compensation for such diode-capacitor front-ends without any ac or dc side filtering elements requires high tangential flux/current excursions (indicated by h). Hence a cost-effective parallel active filter cannot be implemented for harmonic compensation of such harmonic producing front ends to meet IEEE Standard 519.

B. Diode or Thyristor Rectifier with DC Side Inductor System

Fig. 6(a) shows another common topology for diode- and thyristor-based ASD utility interface front-ends. In this case the supply current tends to be quasi-square and continuous with THD's of approximately 30–40% and substantially reduced peak values compared to Case A. Fig. 6(b) shows experimental stationary d^sq^s frame supply current components i^s_{Sd} and i^s_{Sq} waveforms with THD of 29% and CF of 1.6 at 1.1 kW load and dc side inductor $L_{\rm dc} = 8$ mH. The supply current components i^s_{Sd} and i^s_{Sq} are the horizontal (real) and vertical (imaginary) component respectively of the supply current vector $\vec{i}^s_S$ in the stationary d^sq^s frame. The supply current vector $\vec{i}^s_S$ is shown in Fig. 6(c) and has a hexagonal shape in the dq stationary frame. The vertices of the hexagon represent locations of almost constant $\vec{i}^s_S$ whereas, the lines joining two vertices represent the commutation process from one phase to another in the diode/thyristor rectifier. The distance (from the origin) between the highest and the lowest amplitude is indicated by h in Fig. 6(c). The fundamental component of this "jumping" supply current vector $\vec{i}^s_S$ is depicted by the dotted circle in Fig. 6(c).

Transformation of the supply current $\vec{i}^s_S$ from the stationary d^sq^s to the synchronous d^eq^e frame yields $\vec{i}^e_S$ as shown in Fig. 6(d). Just after a commutation, the supply current vector $\vec{i}^e_S$ reaches the left most point in Fig. 6(d). Since the supply current $\vec{i}^s_S$ in the stationary d^sq^s frame is almost constant between commutations, the corresponding supply current vector $\vec{i}^e_S$ in the synchronous d^eq^e frame turns in the negative direction (clock-wise) with an angular speed $\omega_e t$. After the supply current vector $\vec{i}^e_S$ has turned by almost 60°, it reaches the right most point, where the next commutation starts. During the commutation period, the supply current vector $\vec{i}^e_S$ "jumps" from the right (30° lagging) back to the left (30° leading). Hence the supply current vector $\vec{i}^s_S$ transitions from one vertex of the hexagon in Fig. 6(c) to the next, and completes one full revolution after six such "jumps" over a fundamental period of the supply frequency. In the synchronous d^eq^e frame these six "jumps" all appear at the same position and this implies that it is sufficient to consider just one 60° sector. The time average of the supply current vector in the synchronous d^eq^e frame $\vec{i}^e_S$ [indicated by $I1$ in Fig. 6(d)] represents the fundamental component of the supply current vector $\vec{i}^s_S$ in the stationary d^sq^s frame. The vertical size h relates to the supply current amplitude ripple and the width w relates to the angular deviations with respect to the fundamental component as shown in Fig. 6(d).

Note that the dc side inductor $L_{\rm dc}$ has the effect of increasing the angular deviation of the supply current vector $\vec{i}^e_S$ (increase in width w) and reduces the supply current amplitude ripple (decrease in height h). This results in a reduction of the peak harmonic current value and increase in the bandwidth requirement of the active filter for harmonic compensation in order to meet IEEE Standard 519. Note the change in the supply current vectors $\vec{i}^e_S$ in Figs. 5(d) and 6(d).

The supply voltage unbalance effect on the supply current $\vec{i}^e_L$ can be compared between Figs. 6(d) and 7(d). The significant decrease in peak supply current value is clearly from a much smaller h-value.

The supply current THD depends on the dc side inductor $L_{\rm dc}$ value and the operating point of the load. These front-ends are beset with very high di/dt problems for stiff ac systems and hence require a high bandwidth active filter for harmonic compensation, particularly in order to meet IEEE Standard 519 higher harmonic limits. The dc side inductor smooths the dc link current, minimizes supply voltage unbalance effects and enables the application of cost-effective parallel active filters, albeit, with the concomitant penalty of high active filter bandwidth requirement. Hence they do not offer an optimal front-end for harmonic compensation if they are required to

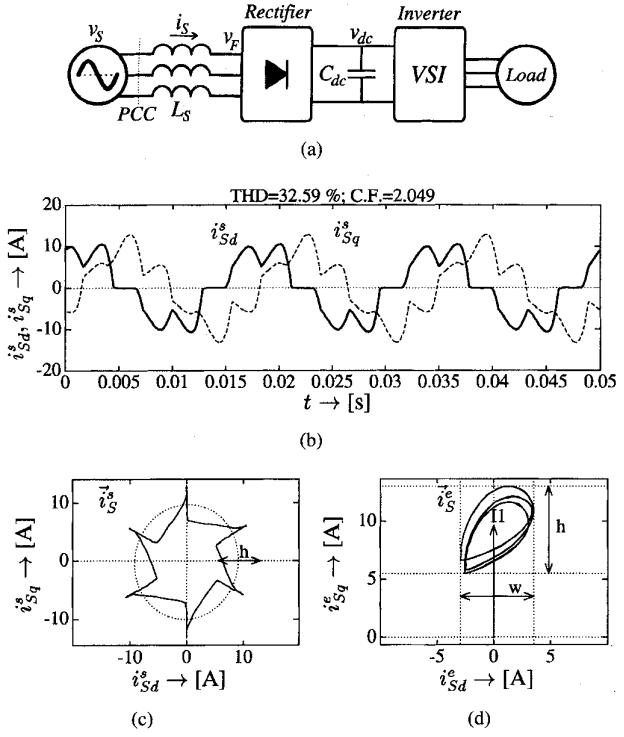


Fig. 7. Case C. (a) Utility interface. (b) Measured line currents by flux controller. (c) In stationary frame. (d) In synchronous frame.

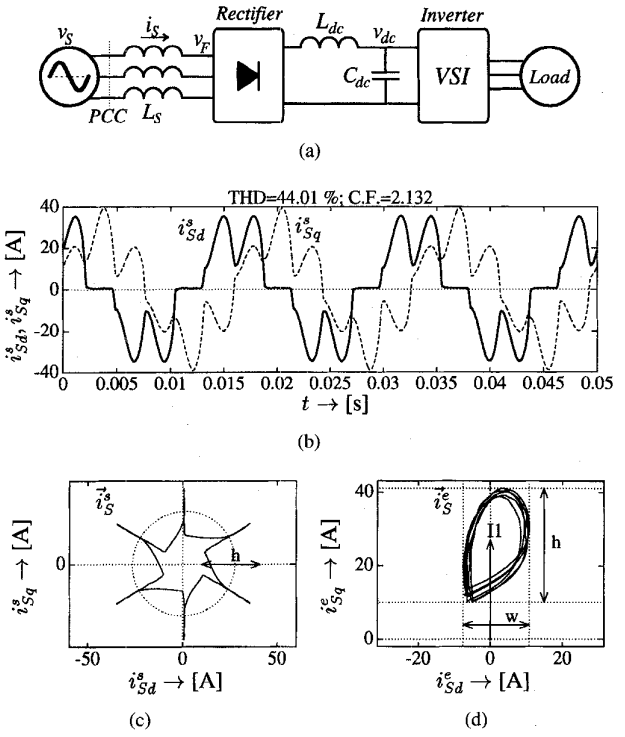


Fig. 8. Case D. (a) Utility interface. (b) Measured line currents by flux controller. (c) In stationary frame. (d) In synchronous frame.

meet IEEE Standard 519. Thyristor front-ends require reactive power compensation depending on their operating point. The flux-based active filter controller can meet reactive power demands with slightly higher active filter rating as explained in Section III.

C. AC Supply Side Line Inductor and Diode Rectifier with DC Side Capacitor System

Fig. 7(a) shows a similar utility interface front-end topology to that shown in Case A, but has supply side ac line inductors L_S with the intention of reducing the peak supply current and THD value (typically limited to 40%). Fig. 7(b) shows experimental stationary $d^s q^s$ frame supply current components i^s_{Sd} and i^s_{Sq} waveforms with THD of 32.6% and CF of 2.0 at 1.1 kW load and $L_S = 1.25$ mH. Fig. 7(c) shows supply current vector $\vec{i}^s_S$ and its extracted fundamental component in the stationary $d^s q^s$ frame. Fig. 7(d) shows the supply current vector $\vec{i}^e_S$ and the effect of supply voltage unbalance in the synchronous $d^e q^e$ frame. Fig. 7(d) shows that the supply current vector $\vec{i}^e_S$, d-component i^e_{Sd} (w) is significantly reduced compared to Case B, whereas the q-component i^e_{Sq} (h) is increased compared to Case B.

Supply-side ac line inductor L_S increases the commutation overlap angle, consequently reducing the di/dt and bandwidth requirement of the active filter for harmonic compensation to meet IEEE Standard 519 harmonic limits. Note that the ac side inductor L_S has the effect of reducing the angular deviation of the supply current vector $\vec{i}^e_S$ (reduces w) and increases the supply current amplitude ripple (increases h), compared to the dc side inductor Case B as shown in the synchronous $d^e q^e$ frame. AC side line inductors result in significant peak supply current and THD reduction compared to Case A and thus enable the application of cost-effective parallel active filters without the penalty of high bandwidth requirement as required in Case B. However this utility interface front-end has higher cost.

D. AC Supply Side Line Inductor, Diode Rectifier with DC Side Inductor, and DC Side Capacitor System

Fig. 8(a) shows the most desirable utility interface front-end topology for ASD's and other loads such as dc power supplies. This front-end combines the advantages and eliminates the disadvantages of Cases B and C. Fig. 8(b) shows experimental stationary $d^s q^s$ frame supply current components i^s_{Sd} and i^s_{Sq} waveforms with THD of 44% and CF of 2.13 at 3 kW with $L_S = 125\,\mu$H and $L_{\rm dc} = 250\,\mu$H. Fig. 8(c) shows supply current vector $\vec{i}^s_S$ and its extracted fundamental component in the stationary $d^s q^s$ frame and Fig. 8(d) shows the d-axis and q-axis supply current components i^e_{Sd} and i^e_{Sq} in the synchronous $d^e q^e$ frame with the effect of supply voltage unbalance, which are slightly higher compared to Fig. 6(d) due to smaller dc ($L_{\rm dc}$) and ac side line inductors (L_S) used in the laboratory experiment.

Supply-side ac line inductors L_S reduce the peak value, THD and the di/dt of the supply current. The dc side inductor $L_{\rm dc}$ results in continuous supply currents and helps reduce supply voltage unbalance effects on the supply side as can be

seen from Figs. 8(d) and 6(d). This utility interface front-end has the highest cost.

V. Sequencing and Start-Up

The active filter sequencing and protection functions are provided by a sequencer hardware. The active filter sequencer is implemented as a state machine. The start-up process has three states; viz. precharging state, charging state, and compensation state.

During the precharging state, the active filter dc bus capacitor $C_{\rm bus}$ is charged through a diode and resistor to the peak of the supply voltage (650 V). The antiparallel diodes provide a three phase rectifier operation when the active filter contactor is closed.

During the charging state, the dc bus PI controller regulates $V_{\rm bus}$ to its nominal value of 750 V and the harmonic references are isolated by analog switches. This mode allows the low-pass filters of the synchronous frame controller to achieve steady-state values.

Harmonic references are enabled during the compensation state. This facilitates a transient-free start-up process. The sequencing and start-up of the active filter is shown in the simulation results in Section VI.

VI. Parallel Active Filter Implementation for ASD Loads: Simulation Results

The validation of the flux-based active filter controller is provided by simulation results of a 3ϕ, 460-V, 60-Hz, 310-kW ASD load with diode rectifier front-end and a dc side inductor. The PCC transformer percentage leakage inductance is 3.0% ($L_S = 50\,\mu$H) and constitutes the total ac side supply line inductance, which results in a commutation duration of 600 μs at rated load condition. The dc link capacitance is $C_{\rm dc} = 30$ mF and the dc side inductor value is $L_{\rm dc} = 340\,\mu$H. The dc side $L_{\rm dc}$–$C_{\rm dc}$ filter is tuned to 50 Hz. The simulated parallel active filter inverter has a filter inductance of $L_F = 100\,\mu$H, nominal dc bus voltage $V_{\rm bus} = 750$ V and dc bus capacitance $C_{\rm bus} = 10$ mF.

Figs. 9–11 show the simulation results of the active filter operating under balanced supply and load conditions. The supply (and load) current THD of the ASD utility interface front-end is 27% and hence, a parallel active filter is viable for such an application. The synchronous d^eq^e frame representation of the load current vector $\vec{i}_L^{\,e}$ in Fig. 10(a) still contains the fundamental component, which is given by the time average of $\vec{i}_L^{\,e}$. The harmonic current reference for the active filter is extracted from the load current vector $\vec{i}_L^{\,e}$ by means of synchronous frame-based active filter controller given in Fig. 2, which subtracts the average—low-pass filtered—value of $\vec{i}_L^{\,e}$ (representing the fundamental component in the stationary d^sq^s frame) from the actual $\vec{i}_L^{\,e}$ itself. This dc removal can be graphically interpreted as moving the load current vector $\vec{i}_L^{\,e}$ to the origin.

During the first 0.04 s as shown in Fig. 9 the dc bus ($V_{\rm bus}$) of the active filter inverter is charged up to 750 V. The active power needed to charge up the dc bus capacitor $C_{\rm bus}$ of the

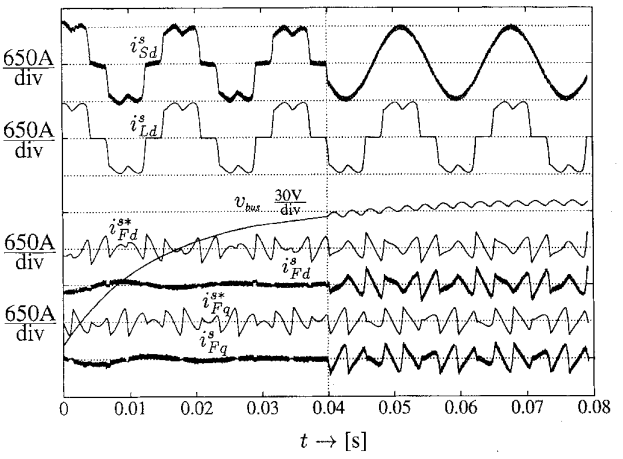


Fig. 9. Active filter start-up for 310-kW ASD; balanced supply.

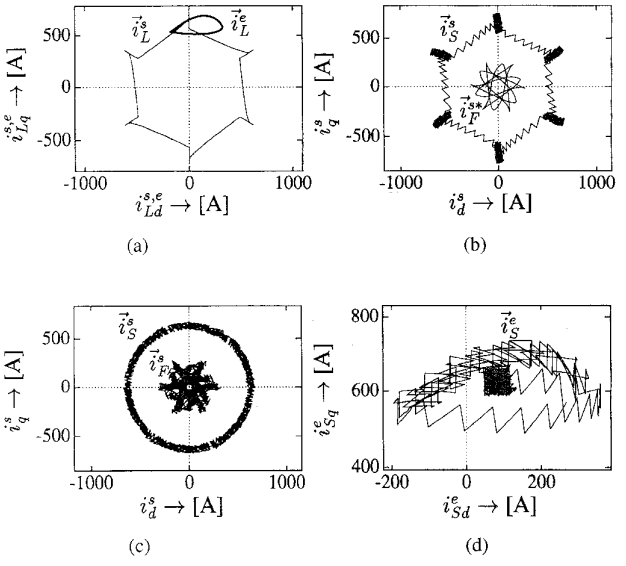
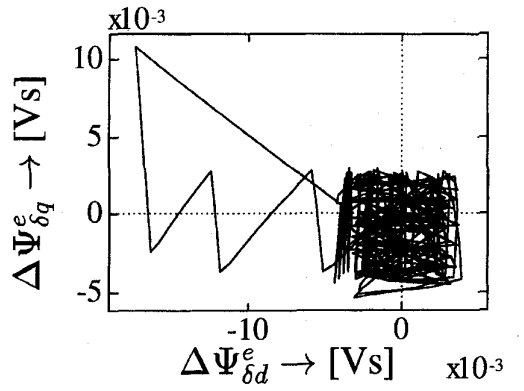


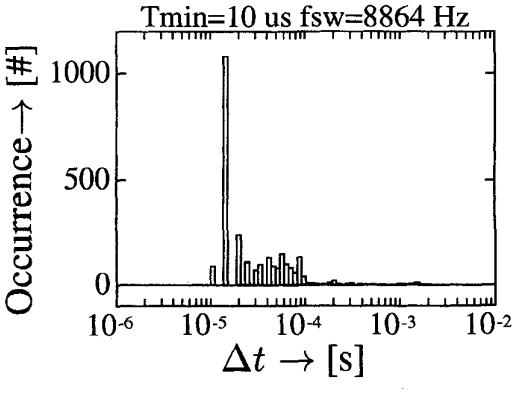
Fig. 10. Balanced supply. (a) Load current. (b) Supply current before $t = 0.04$ s. (c) Supply current after $t = 0.04$ s. (d) Synchronous frame supply current around 0.04 s.

active filter inverter is controlled by the dc bus controller. The dc bus controller generates active filter fundamental current components i_{Fd}^s and i_{Fq}^s in phase with the active filter terminal voltage V_F to regulate active power flow. During the charging of the dc bus voltage, supply current vector $\vec{i}_S^{\,s}$ is very close to the load current vector $\vec{i}_L^{\,s}$, except for the additional switching ripple of the active filter inverter. At $t = 0.04$ s, the active filter is switched on and provides harmonic compensation of the load current. The active filter reference current components in the stationary d^sq^s frame are given by i_{Fd}^{s*} and i_{Fq}^{s*} as shown in Fig. 9. The active filter reference current vector $\vec{i}_F^{\,s*}$ in the synchronous d^eq^e frame is shown in the center of Fig. 10(b).

Fig. 10(b)-(c) shows the supply current in the stationary d^sq^s frame before and after the active filter is started, respectively. Tracking of active filter current reference vector



(a)

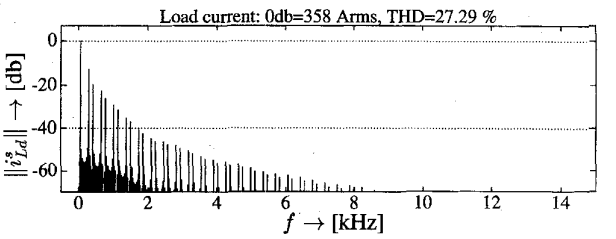


(b)

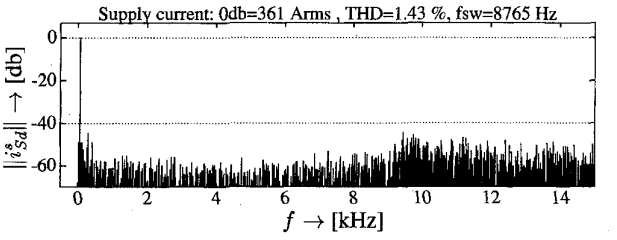
Fig. 11. (a) Error flux synchronous frame. (b) Switching time distribution ($\Delta t_{\min} = 10\,\mu$s, $\Delta t_{\max} = 1975\,\mu$s).

$\vec{i}^{s*}_F$ in Fig. 10(b) by the actual current vector $\vec{i}^s_F$ in Fig. 10(c) is clearly shown in Fig. 10(d), which also shows the supply current vector $\vec{i}^e_S$ around the point of transition of switching "ON" of the active filter inverter. Before the transition, the supply current vector $\vec{i}^e_S$ follows the load current vector $\vec{i}^e_L$ in Fig. 10(a). The transition occurs just after the start of a rectifier commutation. Supply current vector $\vec{i}^e_S$ quickly moves to a "steady" position, which is indicated by the "black box" after the active filter is started. Because the supply current vector is slightly lagging the supply voltage vector due to supply side PCC transformer leakage inductance L_S, the fundamental component of the supply current vector $\vec{i}^e_S$ is displaced to the right of the vertical axis. The synchronous d^eq^e frame in this simulation is attached to the active filter terminal flux $\vec{\Psi}^s_F$.

Fig. 11(a) shows that the error flux $\Delta\vec{\Psi}^e_\delta$ is constrained to a "box" with size $\pm 1/2 \cdot 460 \cdot T_{sw} = 2.3$ mVs for $T_{sw} = 10\,\mu$s. The large error on the left indicates the instant when the active filter is started at $t = 0.04$ s. Fig. 10(d) shows the supply current vector $\vec{i}^e_S$, in the synchronous d^eq^e frame just before and after this transition. The given dimensions of the "box" result in an average switching frequency of $f_{sw} = 8.8$ kHz. An important fact is that no pulses shorter than 10 μs occur, as verified from the Fig. 11(b).



(a)



(b)

Fig. 12. Balanced supply, compensation state: load current and supply current frequency spectra.

Fig. 12(a) shows the spectrum of the simulated load current $\vec{i}^s_L$. Fig. 12(b) shows that the synchronous d^eq^e frame flux controlled active filter reduces the supply current THD from 27.3–1.4%. The resultant supply current spectrum with this carrier-less flux controller does not show any dominant peaks around the switching frequency of $f_{sw} = 8.8$ kHz when a $T_{sw} = 10\ \mu$s is applied.

A. Unbalanced Supply

In practice, a balanced supply is an exceptional case and utility supplies usually have small (up to 10%) supply voltage unbalances. The simulation results in Figs. 13 and 14 are given for the same system as for the balanced case, with a supply voltage unbalance of $\pm 5\%$ in phases A and C, respectively. The effects of such supply voltage unbalance can be seen by comparing the stationary d^sq^s frame load current component i^s_{Ld} in Fig. 13 with the corresponding load current component i^s_{Ld} in Fig. 9. Since the synchronous d^eq^e frame controller low pass filters (see Fig. 2) have a cross over frequency of 30 Hz and due to the implementation of a three-legged inverter for the active filter, the supply current is forced to be symmetrical for all three phases, regardless of the unbalance in the supply voltage. This results in a 120-Hz dc bus current ripple which has to be absorbed by the dc bus capacitor C_{bus}. As a result, the ripple voltage on V_{bus} in Fig. 13 is much larger compared to that in the balanced case of Fig. 9. However, the ripple voltage on V_{bus} in Fig. 13 is within acceptable voltage bounds.

In Fig. 14(a) the unbalance in the load current vector $\vec{i}^s_L$ in the stationary d^sq^s frame is clear from its distorted shape compared to that for the balanced supply voltage case as shown in Fig. 10(a). The load current in the synchronous d^eq^e frame $\vec{i}^e_L$ shows three distinct orbits instead of just one as for the balanced case in Fig. 10(a). Fig. 14(b) shows the required

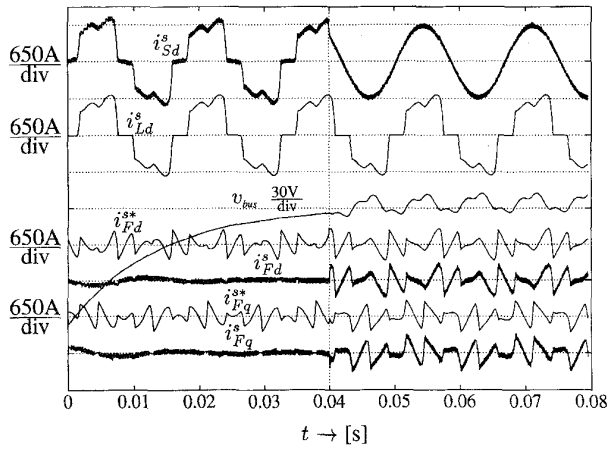


Fig. 13. Active filter start-up for 310-kW ASD; unbalanced supply.

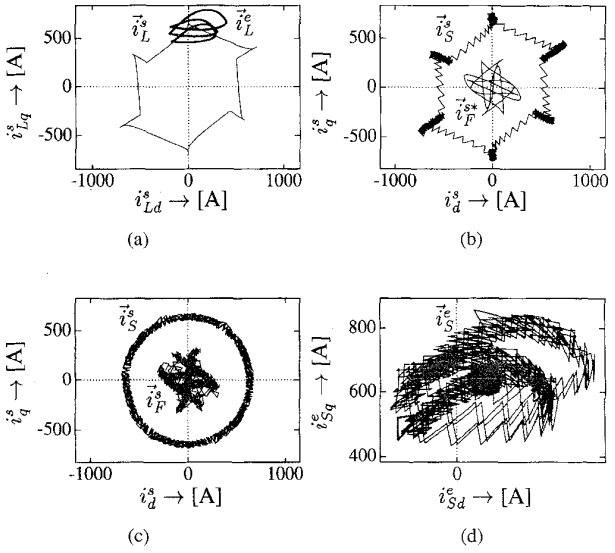


Fig. 14. Unbalanced supply. (a) Load current. (b) Supply current before $t = 0.04$ s. (c) Supply current after $t = 0.04$ s. (d) Synchronous frame supply current around 0.04 s.

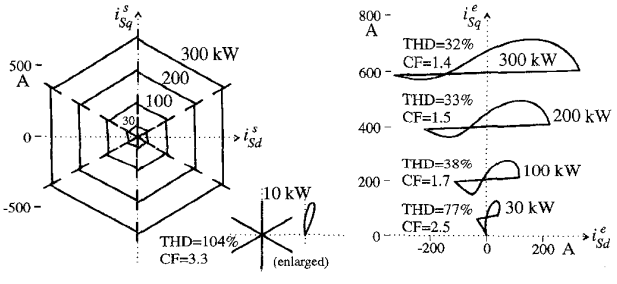


Fig. 15. Supply current waveforms as a function of dc loading. $C_{\rm dc} = 30$ mF, $L_{\rm dc} = 340\,\mu$H.

active filter reference current vector $\vec{i}_L^{s*}$ in the stationary d^sq^s frame for harmonic compensation of load current vector $\vec{i}_L^s$. The compensated supply current THD is 1.64%. Note that slightly larger peak active filter currents result under unbalanced conditions (in the stationary d^sq^s frame 355 A peak current versus 285 A peak current for the balanced case). If correction for unbalanced load currents is not required, the cross-over frequency of the low pass filters in the synchronous frame controller as shown in Fig. 2 can be increased from 30 Hz to over 120 Hz. Unbalance can be regarded as a negative sequence of -60 Hz in the stationary d^sq^s frame, which transforms to -120 Hz in the synchronous d^eq^e frame. Because the 5th and 7th harmonics in the stationary d^sq^s frame (corresponding 360 Hz in the synchronous d^eq^e frame) should not be attenuated by the low pass filters, a higher order low pass filter structure is required.

B. Input Harmonics as a Function of Load

The waveform shape of the load harmonic current vector $\vec{i}_L^s$ highly depends on the rectifier load and the values of dc side capacitors $C_{\rm dc}$ and dc side inductors $L_{\rm dc}$. Fig. 15 shows how the load current vectors in both the stationary d^sq^s and synchronous d^eq^e frame depend on the load power operating point (rated 300 kW) without any ac side line inductance ($L_S = 0$). In practice the dc side $C_{\rm dc}$–$L_{\rm dc}$ filter resonant frequency is below the supply fundamental frequency. In this case $f_e = 60$ Hz and $f_{filt} = 1/2\pi\sqrt{L_{\rm dc}C_{\rm dc}} = 50$ Hz. Given this constraint a higher $C_{\rm dc}$ value will reduce the value of $L_{\rm dc}$. However, a higher $C_{\rm dc}$ value will increase the ripple current and the load current THD, just as a lower load does in Fig. 15.

In the simulated case chosen, the rectifier load currents become discontinuous for loads smaller than 0.1 p.u. (10% load rating). As can be seen from Fig. 15, despite the reduction in the load current THD with increasing load, the active filter rating depends on the largest harmonic current peak which happens at rated load.

VII. Conclusions

- This paper demonstrates the validation of the synchronous frame flux-based controller for a parallel active filter application.
- The synchronous frame flux-based controller implements a hysteresis rule-based carrier-less PWM strategy directly in the complex d^eq^e synchronous frame. This method realizes the full potential of a hysteresis-based current regulator by effectively addressing the limitations of a conventional and other state of the art hysteresis-based current regulators. Direct control of the inverter flux (a continuous variable) enables implementation of the current regulator without explicit generation of voltage references. Simple rules ensure prescribed adjacent state inverter switching vectors and prescribes *equal duration* zero vectors.
- This paper emphasizes the need for a systems approach to active filtering. Distinct harmonic compensation requirements and related issues, such as load current THD, peak value of the harmonic current and the required active filter bandwidth, have been identified and addressed for various commonly used utility interface front-ends for ASD loads.

- It has been shown that for large rated ASD loads, the most desirable utility interface front-end for application of parallel active filters is the diode rectifier front-end with ac and dc side inductors.
- Transformation of the load current into the synehronous d^eq^e frame directly shows the harmonic compensation required by the parallel active filter in the radial (width w) and tangential (height h) directions. The flux-based regulator tracks the tangential ripple by means of zero vectors and the radial ripple by means of adjacent state vectors.
- The synchronous d^eq^e frame-based controller ensures extraction of harmonic components without any phase shift sensitivity.
- Simulation results for a utility interface of a large (310 kW) ASD load by a parallel active filter shows compliance with IEEE Standard 519 recommended harmonic standards (THD <5%), with balanced and also unbalanced supply voltage conditions with SCR of 20 at the PCC. The compensated supply current THD is less than 2% under balanced and unbalanced rated load conditions.

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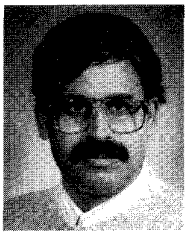

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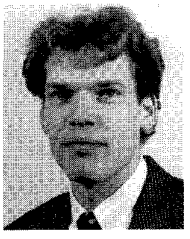

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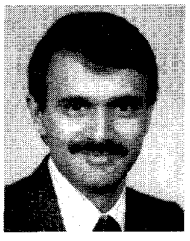

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