Focal-Plane Sensor-Processor Chips

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Preface

Vision is our most important sensory system. It receives the largest amount of data and at the same time the most complex signal composition. Our eye and brain can put together images from photons arriving from different angles, with different densities and different wavelengths. One third of the human brain is devoted to the processing of the visual information.

The processing starts already in the retina. It is responsible for adaptation and early image processing. Along the preprocessing phases, it reaches 1:100 data reduction. It is not surprising that the efficiency of the retina stimulated many research engineers to build vision chips, which mimic this amazing performance. The common properties of these sensor-processor chips are that they can perform both data capturing and processing.

The story of the focal-plane sensor-processor (FPSP) devices started about 20 years ago, when Carver Mead built his famous silicon retina [1], which was capable of performing local adaptation. This initialized a line of different FPSP chips in the 1990s [2–6]. These chips were implemented using analog VLSI technology. The main motivation for the analog implementation was twofold. On the one hand, in the 1990s the silicon area of the basic computational elements needed for image processing (adder, multiplier, storage elements with 6- to 8-bit accuracy) was 5 times smaller in the analog domain than in the digital. On the other hand, the combination of the wide spreading CMOS sensors technology and the analog processing elements led to very efficient circuits, because no analog-to-digital conversion was needed. These chips contained 400–4,000 processing elements and could perform 10,000 FPS image capturing and processing real-time providing 10–100 times more computational power than a PC at that time. A summary of these chips and their technology can be found in [7].

In the late 1990s to early 2000s, the digital technology could profit more from Moore's law than the analog ones; hence, the digital storage and computational elements became small enough to build vision chips with digital processors [8, 9]. Reference [10] shows an analysis of the different digital processor arrangements of these chips.

Nowadays, these chips are applied to embedded devices used in industries and in some devices we use in our everyday life. The most straightforward example is the

optical mouse, but these chips can also be found in 3D laser scanners, range sensors, safety equipments, and in unmanned aerial vehicles (UAVs). Besides the industry, an active scientific community focuses its effort to come out with new architectures and solution.

This book introduces a selection of the state-of-the-art FPSP array chips, design concepts, and some application examples. After a brief technology introduction (chapter *Anatomy of the Focal-Plane Sensor-Processor Arrays*), six different sensor-processor chips are introduced with design details and operation examples. The first three chips are general purpose while the last three ones are special purpose. The first in the row is the SCAMP-3 chip. It is an extremely power-efficient FPSP chip with tricky operator execution methods (chapter *SCAMP-3: A Vision Chip with SIMD Current-Mode Analogue Processor Array*). The second chip (MIPA4k, chapter *MIPA4k: Mixed-Mode Cellular Processor Array*) has both digital and analog processors and supports some special operators, such as rank-order filtering and anisotropic diffusion. The third general purpose chip (ASPA, chapter *ASPA: Asynchronous–Synchronous Focal-Plane Sensor-Processor Chip*) has a very special feature. It can implement extremely fast asynchronous binary wave propagation.

The next three FPSP array chips are special purpose chips optimized for efficient execution of different tasks. The first special purpose chip (chapter *Focal-Plane Dynamic Texture Segmentation by Programmable Binning and Scale Extraction*) is designed for dynamic texture segmentation. It is followed by a high-dynamic range high-temporal resolution chip, called ATIS (chapter *A Biomimetic Frame-Free Event-Driven Image Sensor*). Its special feature is the event based readout. The row is closed with a 1D sensor-processor (chapter *A Focal Plane Processor for Continuous-Time 1-D Optical Correlation Applications*), which is designed for continuous time optical correlation.

The next two chapters introduce future concepts. The first one describes a design, which steps through the conventional planar silicon technology, by using 3D integration. Other interesting feature of the introduced VISCUBE design (chapter *VISCUBE: A Multi-Layer Vision Chip*) is that it combines a fine-grain mixed-signal pre-processor array layer with a coarse-grain digital foveal processor array layer. Then in chapter by Jiang and Shi, the concept of a nonlinear resistive grid built from memristors is shown. The resistive grid, which can be one of the future building blocks of these FPSP chips, extracts the edges almost in the same way as the human visual system does.

The last four chapters explain different applications of the technology. The tenth chapter (*Bionic Eyeglass: Personal Navigation System for Visually Impaired People*) introduces the concept of a mobile device, called "Bionic Eyeglass," which provides visual aid for blind persons to navigate and to identify colors in their everyday life. The 11th chapter (*Implementation and Validation of a Looming Object Detector Model Derived from Mammalian Retinal Circuit*) describes the implementation of a vertebrate retina circuit, responsible for identifying looming objects, on an FPSP chip-based embedded vision system [11]. After this, an industrial application is shown in chapter by Nicolosi et al. The same embedded vision system, which was

used in the previous chapter, is applied in ultra-high speed real-time visual control of a welding robot. The last chapter of this book introduces a 3D finger tracking application to control cursor in a mouseless computer.

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