Folded Multiple-Capture: An Architecture for High Dynamic Range Disturbance-Tolerant Focal Plane Array

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ABSTRACT

Earlier studies have shown that multiple capture can achieve high SNR, but cannot satisfy the high dynamic range (HDR) and high speed requirements of the Vertically-Integrated-Sensor-Array (VISA) project. Synchronous self-reset, on the other hand, can achieve these requirements, but suffers from poor SNR. Extended counting can achieve high dynamic range at high frame rate and with good SNR, but at the expense of high power consumption. The paper proposes a new HDR focal plane array architecture, denoted by folded-multiple capture (FMC), which by combining features of the synchronous self-reset and multiple capture schemes, can satisfy the VISA requirements at a fraction of the power dissipation and with more robustness to device variations than extended counting. The architecture is also capable of detecting subframe disturbances, e.g., due to laser jamming, and correcting for it.

Keywords: IR focal plane array, ROIC, high dynamic range, vertical integration

1. INTRODUCTION

Significant developments in focal plane array technologies and architectures have been made in recent years. CMOS technology scaling has enabled the integration of analog and digital processing in the focal plane down to the pixel level. New architectures that take advantage of such integration to enhance image sensor performance have been developed (e.g., [1, 2]). An example is the Digital Pixel Sensor, where digitization is performed at the pixel-level providing ultra high speed and dynamic range imaging capabilities.[3] Vertical integration provides the promise for even higher levels of pixel-level integration.[4–7] This is of particular importance to tactical IR imaging applications. An IR imaging system may be used in different environments with widely varying temperature ranges and object speeds. It also needs to be able to tolerate undesired disturbances, e.g., due to laser jamming or sun reflection. Such disturbances cause spikes in the photocurrent resulting in partial or complete loss of information. The wide range of inter-scene temperature and the presence of disturbances require very high dynamic range of 120dB or more at 1000 frames/sec or more.[8] These requirements cannot be achieved with today's IR imaging systems.

To address the high dynamic range problem of conventional focal plane arrays, several sensor readout architectures have been proposed in recent years. In previous papers,[9–11] we compared several of these schemes based on their SNR, implementation complexity, and power consumption. In [10], we found that multiple capture achieves high SNR over the extended range, but cannot achieve the required 120dB of dynamic range at 1000 frames/sec. On the other hand, synchronous self-reset can achieve very high DR at high frame rate, but suffers from poor SNR at both the low and the extended ends. In a companion paper,[11] we analyzed the extended counting scheme[12] and showed that it can achieve high dynamic range at high frame rate and with good SNR at the extended end, but at the expense of high power consumption.

In this paper we describe a new high dynamic range FPA architecture, which we denote as folded-multiple-capture (FMC). The architecture combines synchronous self-reset for signal folding and disturbance detection with multiple capture for achieving high SNR at both the high and low ends of the dynamic range. It comprises a per-pixel analog-front-end (AFE), a fine ADC stage, and a digital-signal-processor/controller (DSPC) stage. The AFE, which is the key part of the architecture, performs programmable gain control, synchronous self-reset, sample-and-hold, as well as enables disturbance detection. It can be implemented with relaxed circuit requirements and is robust to device variations. The ADC is shared by several neighboring pixels and is optimized

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for low power. The DSPC is also shared among several pixels. It estimates each pixel's signal from the ADC and AFE outputs and controls the AFE and ADC in order to adapt the operation to the imaging conditions. The FMC architecture can be readily implemented using vertical integration and is compatible with its area, interconnection and power constraints.

In the following section, we describe the FMC architecture, analyze its dynamic range and SNR, and discuss how it can be used to combat disturbances. In Section 3, we argue that FMC can achieve comparable, if not better SNR, at the same DR as extended counting[12] with significantly lower power consumption and more robust AFE implementation. Needed background, terminology, and notations follow the companion paper[11] and will not, therefore, be repeated here.

2. FOLDED MULTIPLE CAPTURE

In the following subsection we describe the FMC architecture, and discuss its dynamic range. In Subsection 2.2, we analyze SNR for different capture schemes and show how capture times may be selected. In Subsection 2.3, we show how disturbance detection is performed and its limitations.

2.1. FMC Architecture and DR

The block diagram of the FMC scheme is shown in Figure 1(a). The scheme employs a synchronous self-reset modulator but uses a different capture and filtering scheme than the synchronous self-reset with residue readout scheme[13] analyzed in [10]. The integrator output is periodically compared, at the rising edge of the clock signal CLK, to a threshold voltage $V_{\rm th}$. When $v(t) > V_{\rm th}$, the comparator flips and the integrator is reset. During this operation, the integrator value is captured and digitized by the fine ADC at times t_1, $t_2, \ldots, t_n$, where $t_i \in \{(k_i + 1/2)t_{\rm clk} : 0 \le k_i < t_{\rm int}/t_{\rm clk}\}$, as shown in Figure 1(b). We define the effective integration time $t_{\rm last\_i}$, $1 \le i \le n$, to be the time from the last reset before t_i to t_i as shown in Figure 1(b). Clearly, the effective capture integration times $t_{\rm last\_1}, t_{\rm last\_2}, \ldots, t_{\rm last\_n}$ can be readily calculated from the reset sequence. Using the capture values and their effective integration times $(v(t_i), t_{\rm last\_i})$, $1 \le i \le n$, the photocurrent is estimated. This estimation can be performed using only the nonsaturated capture with the longest integration time, by an appropriate least-squares fit of the captures.

Since the FMC architecture exploits the accuracy of clock references, it can be implemented with relaxed circuit requirements. The AFE part of the FMC architecture corresponds to the modulator block in Figure 1(a) and is implemented per-pixel. It comprises a CTIA, a comparator with relaxed specifications, and a sample-and-hold. The $V_{\rm th}$ and clock signals as well as a control signal for the sample-and-hold are routed to all pixels. The accuracy of $V_{\rm th}$ and the CTIA bias are also relaxed, while the accuracy of the clock jitter is critical (better than 1nsec), which is not difficult to achieve in sub-micron technologies. The ADC, which is shared by a block of several neighboring pixels, is optimized for low power and only needs to run at modest speed. Candidate ADC architectures include multi-channel pipeline and successive approximation. The filter is implemented as part of a DSPC, which is shared by a block of pixels. It estimates the reset periods and effective integration times for each pixel in its block. It then sorts the capture values and detects anomalies due to saturation, motion, or disturbance and estimates the photocurrent. These functions can be implemented using a few counters, memory for storing the times and capture values, an ALU, and glue logic. The DSPC also provides the control signals for the AFE and ADC in order to adapt the system operation to the imaging conditions.

In a vertically integrated implementation, the detector would occupy the top layer, the AFE would occupy one or more layers optimized for analog performance, the ADC would occupy one or more layers optimized for mixed signal, and the DSPC would occupy one or more layers optimized for logic performance and memory density.

Now, we analyze the DR and SNR for the FMC architecture. To quantify DR, note that

$$i_{\rm max} = \frac{qQ_{\rm max}}{t_{\rm clk}/2}.$$

Also

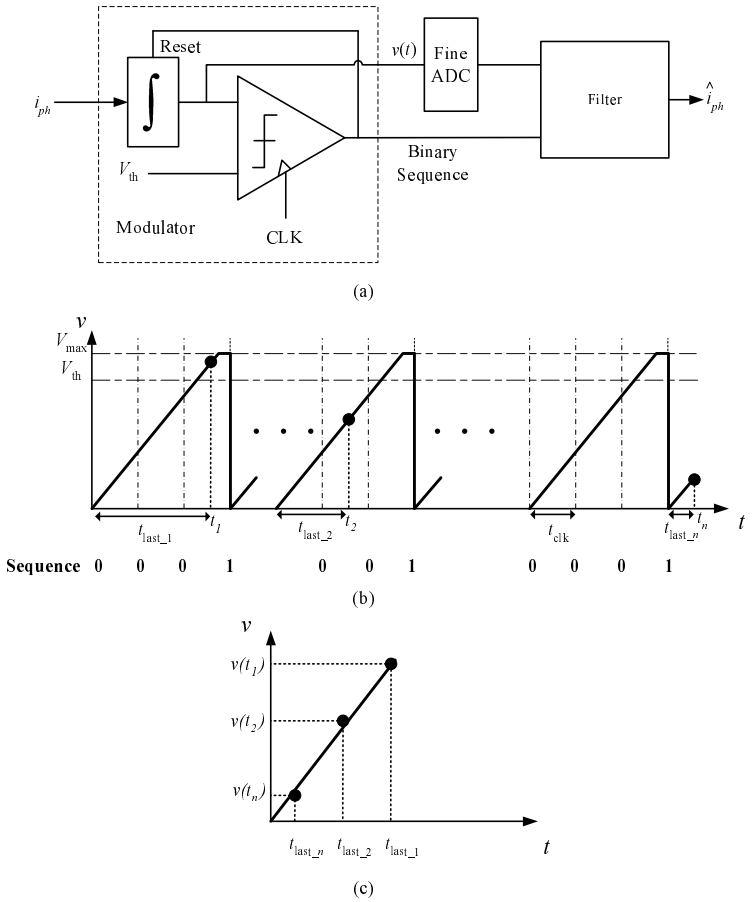

Figure 1. (a) Block Diagram of the folded-multiple-capture architecture. (b) Modulator output. (c) Use of n captures to estimate photocurrent.

$$i_{\min} = \frac{q\sigma_{\text{Readout-eff}}}{t_{\text{int}}},$$

where $\sigma_{\text{Readout-eff}}$ is the standard deviation of the effective readout noise. Thus,

$$\text{DR} = \frac{2Q_{\max}t_{\text{int}}}{\sigma_{\text{Readout-eff}}t_{\text{clk}}}.$$

2.2. Analysis of SNR

To quantify SNR, we need to consider the capture scheme, the number of captures, and the type of filter used. First we quantify SNR for a single capture at time $0 < t \leq t_{\text{int}}$ that is independent of pixel signal.

Note that, for a given i_{ph}, the time to saturation t_{sat}, reset period t_{reset}, and time after the last reset t_{last} are given by

$$t_{\text{sat}} = \frac{qQ_{\max}}{i_{ph}}, \quad t_{\text{reset}} = \left\lceil \frac{qQ_{\text{th}}}{i_{ph}t_{\text{clk}}} \right\rceil t_{\text{clk}}, \text{ and } t_{\text{last}} = t - \left\lfloor \frac{t}{t_{\text{reset}}} \right\rfloor \times t_{\text{reset}}.$$

Now, define

$$\phi(i_{ph},t) = \begin{cases} t_{\text{last}}/t_{\text{sat}}(i_{ph}), & \text{if } t_{\text{last}}/t_{\text{sat}}(i_{ph}) \leq 1 \\ 0, & \text{if } t_{\text{last}}/t_{\text{sat}}(i_{ph}) > 1. \end{cases}$$

Note that SNR monotonically increases with ϕ and is equal to $Q_{\max}$ when $\phi = 1$. Assuming shot noise dominates, i.e., $\phi > \sigma^2_{\text{Readout}}/Q_{\max}$, SNR for a single capture at time t is given by

$$\text{SNR}(i_{ph},t) \approx \phi(i_{ph},t)Q_{\max}.$$

ϕ is plotted in Figure 2. Note the large dips in ϕ as i_{ph} varies. Note also that these dips are largest when reset occurs right before the capture time t or when the integrator is saturated at t.

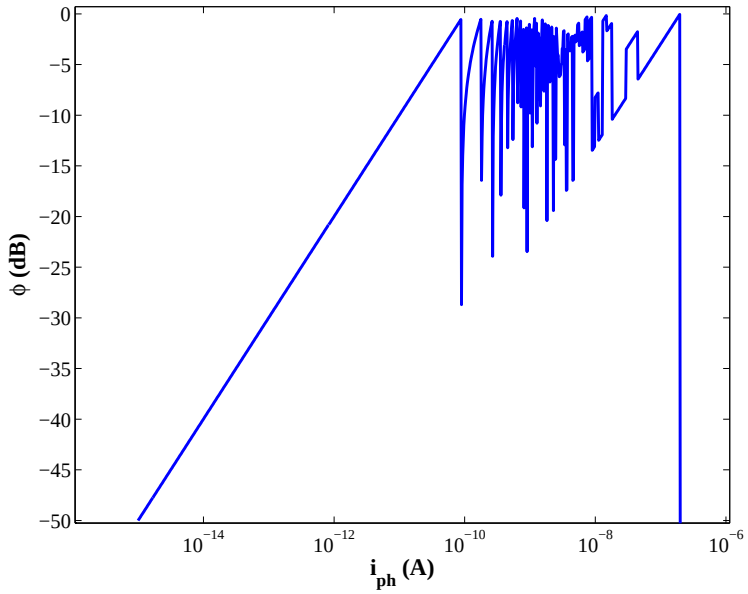

Figure 2. $\phi(i_{ph}, 999.5t_{\text{clk}})$ versus i_{ph}. $Q_{\text{th}} = 0.9Q_{\max}$, $t_{\text{clk}} = 1\mu$sec.

There are two approaches to eliminating these large dips and providing a guarantee on the minimum SNR in the extended range. The first approach is to adapt t to the photocurrent in each pixel. This approach guarantees close to peak SNR in the extended range, but at the expense of additional per-pixel circuits to select the best capture time after the first reset occurs. The second approach is to capture several samples at globally set times. This approach eliminates the need for extra per-pixel circuits, but at the expense of performing more A/D conversions. We now show that by judiciously selecting the capture times, one can guarantee good SNR across the extended range using no more than 4 captures.

Assuming n captures at times $0 \leq t_1 \leq t_2 \ldots \leq t_n$, where $t_i \in \{(k_i + 1/2)t_{\text{clk}}$, for $0 \leq k_i < t_{\text{int}}/t_{\text{clk}}\}$, define $\phi(t_i)$, for $1 \leq i \leq n$, as before. We wish to find the smallest number of captures and each capture's time to guarantees a prescribed minimum SNR in the extended range. Mathematically, we wish to find the smallest n and capture times $t_1, t_2, \ldots, t_n$ such that:

$$\max_i(\phi(t_i)) > \alpha \quad \forall i_{ph} > Q_{\max}/t_{\text{int}} \text{ and } 0 < \alpha < 1.$$

This problem can be reformulated as follows. For a given $m = t_{\text{reset}}/t_{\text{clk}} > 2$, the range of i_{ph} is between $qQ_{\text{th}}/mt_{\text{clk}}$ and $qQ_{\text{th}}/(m-1)t_{\text{clk}}$ (see Figure 3). Thus for a given α, assuming $Q_{\text{th}} = 0.9Q_{\max}$, the set of capture

time indices such that $\phi \geq \alpha$ are given by

$$\mathcal{K}_m = \begin{cases} \left\{ j : \alpha \leq \frac{j+0.5}{m} - \lfloor \frac{j+0.5}{m} \rfloor \leq \frac{m-1}{m} \right\}, & \text{for } 2 \leq m \leq 5 \\ \left\{ j : \alpha \leq \frac{j+0.5}{m} - \lfloor \frac{j+0.5}{m} \rfloor \leq 1 \right\}, & \text{for } 5 < m \leq n_{\max}, \end{cases}$$

where $n_{\max} = t_{\text{int}}/t_{\text{clk}}$.

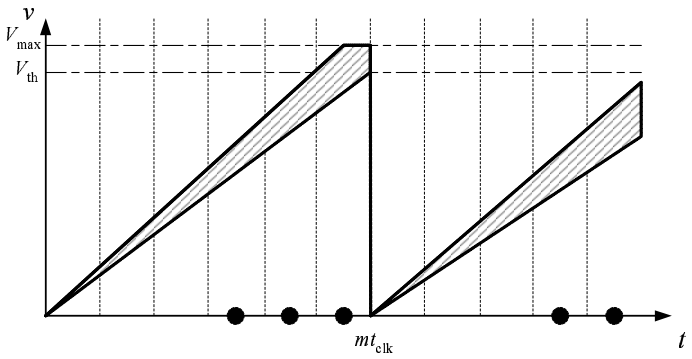

Figure 3. Range of i_{ph} values that generate the same m.

Now, consider the $(n_{\max} - 1) \times n_{\max}$ matrix $A_{(n_{\max}-1)\times n_{\max}}$ with entries

$$a_{mk} = \begin{cases} 1 & \text{if } k \in \mathcal{K}_m \\ 0 & \text{otherwise} \end{cases}$$

Note that the ones in the kth column correspond to the ranges of photocurrents for which $\phi \geq \alpha$. Thus the problem of determining the minimum number of captures and each capture's time reduces to selecting the minimum number of columns of A such that their logical OR is the all ones column vector. The indices of the capture times correspond to the indices of the selected columns. The problem as formulated is NP-complete.

Now we describe a heuristic algorithm for finding a suboptimal solution to the problem. The algorithm is greedy, it starts by choosing the column with maximum number of ones. If there is more than one column with the same maximum number of ones, we select one of them at random. Next, we form a new matrix by deleting the selected column and the rows corresponding to the ones in the column. The procedure is repeated until all rows of the matrix are deleted. The indices of the selected columns in the original matrix determine the capture times.

We applied this procedure to different values of α and $n_{\max} = 1000$ and found several 3 capture solutions with $\alpha = 0.33$ and several 4 capture solutions with $\alpha = 0.5$. Table 1 provides some of these solutions.

$\alpha = 0.33$	(101,157,370)	(143,334,818)	(250,333,383)
$\alpha = 0.5$	(143,157,335,502)	(148,335,502,969)	(143,337,502,850)

Table 1. Capture time indices for $\alpha = 0.33$ and $\alpha = 0.5$ for $n_{\max} = 1000$.

Figure 4 plots SNR versus i_{ph} for 3 captures with $\alpha = 0.33$ and compares it to the reference sensor with the same well capacity,[11] which is optimized for low read noise. In addition to the 3 captures, a readout at $t = 0$, for eliminating reset offset, is assumed for both plots. A least-squares fit is used to estimate the photocurrent. The results are obtained using Monte Carlo simulations and take into consideration finite reset duration, comparator and reset noise and offset, sample-and-hold switched capacitor noise, and ADC quantization. Note that in spite of

the large comparator noise $\sigma_{\text{Comparator}}$ and offset σ_{Offset}, close to optimal SNR is achieved in the extended range. Further, SNR is higher than that of the reference sensor due to the use of multiple captures and least-squares fit.

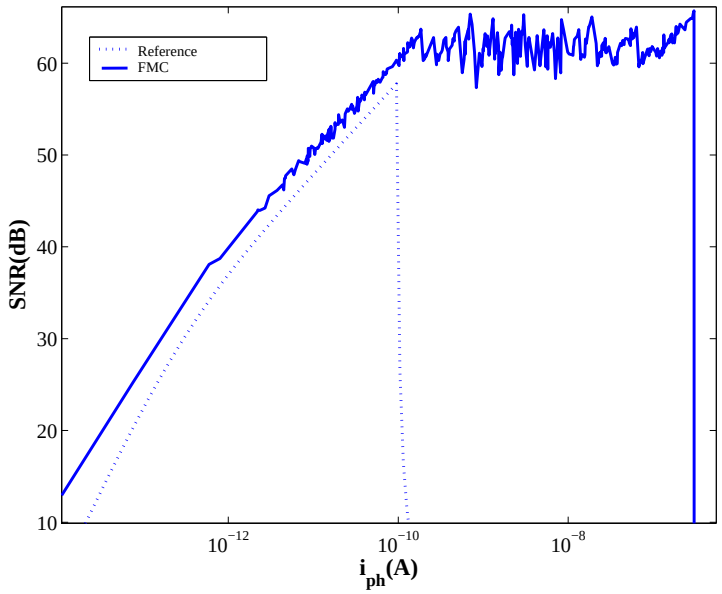

Figure 4. SNR versus i_{ph} for folded-multiple-capture with optimal four global capture times, assuming $Q_{\max} = 625,000e-$, $Q_{\text{th}}/Q_{\max} = 0.9$, $t_{\text{int}} = 1msec$, $t_{\text{clk}} = 1\mu$sec, reset duration of 0.1μsec, $\sigma_{\text{Switch}} = \sigma_{\text{Reset}} = 120e-$, $\sigma_{\text{Readout}} = 40e-$, $\sigma_{\text{Comparator}} = 1000e-$, $\sigma_{\text{Offset}} = 18000e-$ and achieves DR= 174dB.

2.3. Disturbance Tolerance

In a number of applications disturbances, for example, due to pulsed or fast moving laser jammer or sun reflection, instantaneously appear in the camera field of view. Such a disturbance causes large spikes in pixel photocurrent, resulting in complete or partial loss of information. Idealizing such a spike by a delta function current at t_s, the total pixel photocurrent during a frame can be represented by

$$i_{ph}(t) = i_{ph} + d\delta(t - t_s),\ 0 \le t_s \le t_{\text{int}},$$

where i_{ph} is the scene induced photocurrent. The integrator value is given by

$$v(t) = \begin{cases} \frac{1}{C}(i_{ph}t + d), & \text{if } v(t) < V_{\max} \\ V_{\max} & \text{otherwise,} \end{cases}$$

where C is the integrator capacitance.

In a conventional architecture, spikes may be detected by operating the focal-plane array at a very high frame rate, detecting each spike and eliminating it before performing frame addition and accumulation. This solution comes at the expense of high power dissipation and degradation in SNR, since the CTIA and the high resolution ADCs must run at very high speeds, and indeed may not be feasible to implement.

Using the FMC architecture, spikes can be detected without the need to operate at high frame rates. To explain how this detection can be performed, consider the example in Figure 5. The figure shows the output of the integrator for a low photocurrent, which would incur the most severe distortion due to a spike. Since the photocurrent is low, the reset sequence without a spike has no ones. In the presence of a spike, the integrator

saturates causing the reset sequence to contain a 1. This anomaly in the reset sequence is easily detected and used to determine whether or not a capture is used in the photocurrent estimation. If a capture occurs during the time between the disturbance and the reset (as shown in Figure 5), it is discarded. Otherwise, all captures are used.

In general, the reset sequence for a constant photocurrent is mostly periodic, with small variation in the period due to noise. To detect a spike, the capture values and their effective integration times are inspected after discarding saturated captures. If a capture value is outside the expected range as predicted by all capture values and their effective integration times, it is also discarded. Note that the same procedure can also be used to detect and correct for image blur as discussed in.[14]

Figure 6 demonstrates the disturbance tolerance feature of the FMC architecture. The top image is of a HDR scene. The left image below is a simulated image of the same scene with disturbance due to a laser shone across it, as would be captured by a conventional FPA. The third image simulates the output of the FMC scheme with disturbance detection and correction. Note that with the exception of minor artifacts around the person and the monitor, the presence of the disturbance is completely eliminated.

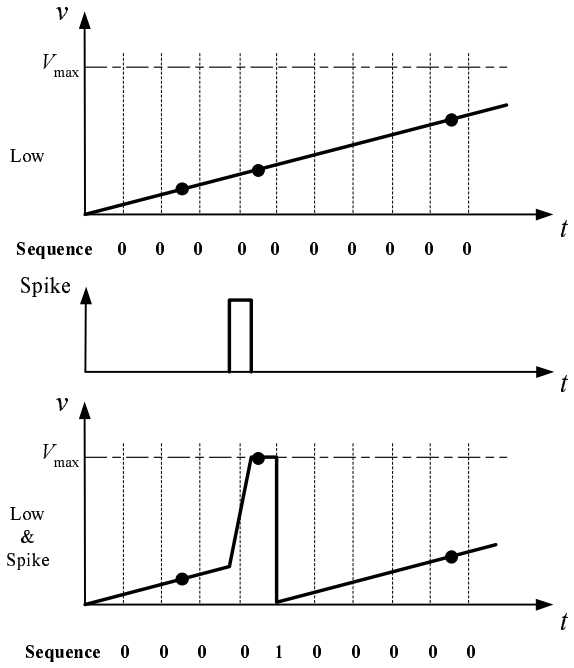

Figure 5. Modulator output with and without disturbance.

This detection scheme, of course, assumes that there are enough captures to detect an anomaly in the modulator output. Further, if multiple spikes occur, successful detection may be possible depending on the placement of the spikes and the number and placement of the captures.

3. FMC VERSUS EXTENDED COUNTING

In this section we compare the FMC architecture to the extended counting architecture[12] analyzed in the companion paper.[11] We first compare the two schemes' SNR. Then we show that FMC consumes significantly less power than extended counting for the same DR and frame rate. Finally we highlight the robustness advantages of FMC.

Figure 7 plots the SNR for FMC and extended counting for two values of the standard deviation of subtraction offset. Note that in both extended counting plots, FMC achieves better SNR in the low end due to multiple

Figure 6. Top: Image of HDR scene. Bottom left: Simulated image with moving laser. Bottom right: Simulated image using FMC with disturbance tolerance.

capture with estimation. At the extended range, the SNR of extended counting depends heavily on the process parameter variations and can be higher than FMC under optimistic assumptions.

To estimate the power consumption for the two architectures, note that in extended counting power consumption is dominated by the CTIA component.[11] Assuming an ADC figure-of-merit(FOM) of 0.5pJ/conversion,[15] which is quite aggressive, to achieve 20 bits of DR at 1000 frames/sec for a 256×256 array, power consumption would be $0.5\text{pJ} \times 2^{20} \times 1000 \times 256 \times 256 = 34\text{Watt}$.

Now by comparing the DR formulas for extended counting[11] and FMC (see Section 2.1), it is easy to see that FMC requires 1/4th the clock speed of extended counting to achieve the same dynamic range and frame rate. The CTIA gain-bandwidth requirement of the AFE amplifier in the FMC architecture is also more relaxed than that for extended counting, since settling time error is cancelled in the self-reset operation of FMC but not in charge subtraction. Assuming that at the same clock speed, the CTIA in the extended counting scheme requires approximately twice the bandwidth of the CTIA in the self-reset scheme, the gain-bandwidth of the self-reset CTIA is $2 \times 4 = 8$ times lower. As a result, assuming MOS square-law, the power consumption of the CTIA in FMC is lower than that in the extended counting scheme by a factor of 64. Using the same FOM for the fine ADC stage the power consumption of the ADC stage of FMC assuming four captures is $0.5\text{pJ} \times 2^{13} \times 1000 \times 4 \times 256 \times 256 = 1\text{Watt}$. In conclusion, for the same 120dB DR and 1000 frames/sec speed, the FMC architecture dissipates less than 2Watt compared to 34Watt using extended counting.

Further, as demonstrated in the previous section, the FMC scheme is capable of detecting and correcting disturbances at the subframe scale. The extended counting scheme cannot detect such disturbances without increasing frame rate, and consequently power consumption.

We now compare the robustness of FMC and extended counting to device mismatches and noise. First note that in FMC, reset and comparator offsets are cancelled via background calibration,[16] since only the slope of the integrator ramp is estimated. Another important robustness feature of FMC is that the settling error component

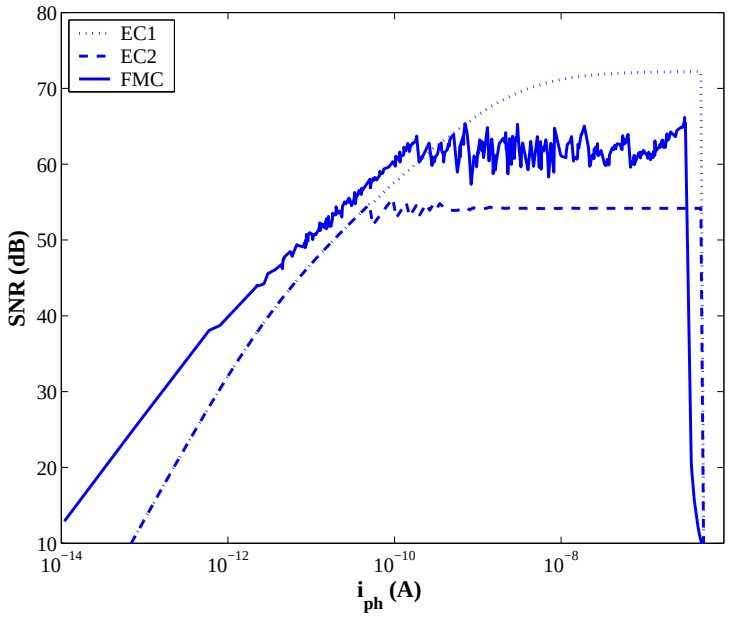

Figure 7. SNR versus i_{ph} for folded-multiple-capture vs. extended-counting. Assuming $Q_{\max} = 625,000e-$, $t_{\text{int}} = 1m\text{sec}$, $\sigma_{\text{Readout}} = 40e-$, $\sigma_{\text{Comparator}}$, $\sigma_{\text{Switch}} = 127e-$. FMC (four captures) assumes $Q_{\text{th}}/Q_{\max} = 0.9$, $\sigma_{\text{Offset}} = 18000e-$, $t_{\text{clk}} = 1\mu\text{sec}$. EC 1 assumes $t_{\text{clk}} = 0.1\mu\text{sec}$, $\sigma_{\text{Offset}} = 76e - \sigma_{\text{Switch}} = 127e-$; EC 2 assumes $t_{\text{clk}} = 0.1\mu\text{sec}$, $\sigma_{\text{Offset}} = 610e-$, $\sigma_{\text{Switch}} = 127e-$.

of reset offset is equal for all resets. This makes it possible to reduce reset duration without increasing the amplifier bias current. Comparator offset is also immaterial in extended counting. However, by contrast, no background calibration is possible for extended counting. The charge subtraction offset, which is due switch pedestal error, capacitor mismatch, bounces in reference voltage, and settling error, is accumulated during the integration time and therefore cannot be cancelled. Although some of these offset components can be cancelled by foreground calibration,[16] the component due to settling error cannot since it is time varying and signal dependent, and therefore cannot be cancelled.

At low photocurrents the dominant noise components are reset, switched capacitor and read noise. In FMC reset noise is cancelled as part of the background calibration. The other components as well as the $1/f$ noise are reduced by the least-squares fit [17]. By comparison, at low photocurrents the aforementioned noise sources are not cancelled in extended counting.

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