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by Inductively Coupled Plasma Etching

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ABSTRACT

This paper will review the top down technique of ICP etching for the formation of nanometer scale structures. The increased difficulties of nanoscale etching will be described. However it will be shown and discussed that inductively coupled plasma (ICP) technology is well able to cope with the higher end of the nanoscale: features from 100nm down to about 40nm are relatively easy with current ICP technology. It is the ability of ICP to operate at low pressure yet with high plasma density and low (controllable) DC bias that helps greatly compared to simple reactive ion etching (RIE) and, though continual feature size reduction is increasingly challenging, improvements to ICP technology as well as improvements in masking are enabling sub-10nm features to be reached. Nanoscale ICP etching results will be illustrated in a range of materials and technologies. Techniques to facilitate etching (such as the use of cryogenic temperatures) and techniques to improve the mask performance will be described and illustrated.

Keywords: Nanoscale, ICP, etching, nanotechnology, cryogenic

1. INTRODUCTION

Nanotechnology may be defined as the ability to precisely manipulate matter on nanoscale dimensions (usually agreed to be within the range 1nm to 100nm). This ability is enabling extension of the performance of conventional devices (such as the CMOS transistor), and the development of completely new devices and technology. The application of nanotechnology is increasing exponentially and finds application in information and communication (memories, novel semiconductor and optoelectronic devices, displays and quantum computing), as well as other areas of technology such as medical and energy[1].

To fabricate devices, layer patterning techniques have long been used and this continues into the nanoscale era. Overwhelmingly, the most popular method of patterning for devices is by the selective removal of solid material through a mask (usually photoresist)[2]. This of course is the 'top-down' technique of etching. The classic example is in the etching steps required for CMOS transistor chips with feature sizes on the micron scale and now much less. Etching for such microelectronics evolved from wet chemistry in the 1960s and 70s (usable down to about 5μm dimensions), to dry etching with parallel plate plasma systems (RIE) usable down to 0.1μm or less in favorable cases and finally, since

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roughly the early 1990s to dry etching with high density plasma (HDP) systems, especially inductively coupled plasma (ICP) taking us below 100nm into nanoscale dimensions. Indeed CMOS technology has long since progressed into the nanoscale: The International Technology Roadmap for Semiconductors (ITRS) 2011 update indicates this occurred in about 2003 when considering half pitch gate widths for flash or DRAM technology[3]. See Figure 1.
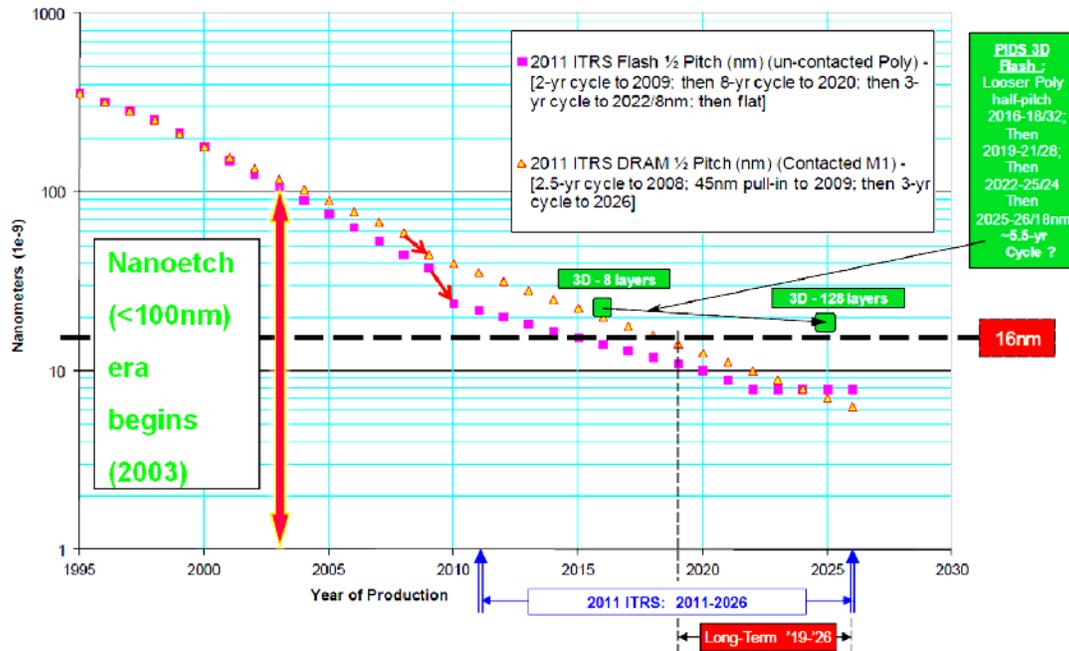

Figure 1. Extract from ITRS Executive Summary for 2011: trends for DRAM and flash memory half pitch.

2. EQUIPMENT

The tools used for nanoscale etching processes described in this paper are all based on the Oxford Instruments PlasmaPro System 100 platform and are configured with various ICP sources for different sized wafers up to 300mm. A schematic of an ICP etch chamber is given in Figure 2.

The ICP sources are of the cylindrical design. Radio frequency (RF) power is applied to a coil outside of an insulating tube to generate a high density inductively coupled plasma (ion density generally $>10^{11}$/cm^3). Capacitively coupled power (CCP, also known as RIE bias power) is applied to the wafer electrode to provide independent control of the ion energy at the substrate.

The wafers are clamped either mechanically or electrostatically to the temperature-controlled lower electrode. Helium pressure is applied to the back of the wafers to provide good thermal conductance between the electrode and the wafer. Smaller samples or pieces (as often used for nanoscale etch research) may be attached to a carrier wafer with a thermally conductive compound.

The systems are generally operated over a pressure range 0.5 to 100mT by automatic pressure control. Gases are fed in through the top of the source or through a gas ring around the wafer electrode.

An optional wide temperature electrode is often useful in nanoscale etching. Electrode temperature is controllable over a range of -150°C to +400°. In general substrate temperature has a marked effect on the etch result, as it controls the volatility of the etch species and hence influences the chemical component of the process, affecting not only etch rate, selectivity and profile, but also surface roughness.
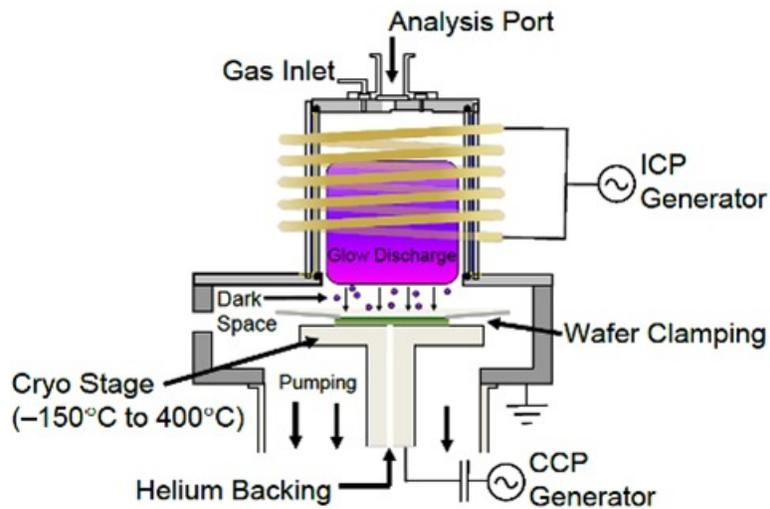
Figure 2. Schematic of cylindrical ICP chamber design.

Other options include: a magnetic spacer between the tube and the wafer which enables independent control of ion distribution and for optimized etching uniformity across the electrode, pulsing of the ICP power for adjustment of ion radical ratios and enhanced high aspect ratio etching, and bias power pulsing to improve profiles and reduce aspect ratio dependent etching (ARDE).

3. DIFFICULTIES AND LIMITS OF NANOSCALE ETCHING

Etching on the nanoscale is a fundamentally more difficult for two basic reasons: 1) more difficult transport of neutral species in and out of smaller features and 2) increased effects of charging by ions and electrons as sidewalls get closer together. The situation is compounded by the fact that in the design of smaller devices, usually the lateral shrink is greater than the vertical shrink so the aspect ratio h/d rises as illustrated in Figure 3.

Figure 3. Design rules dictate increasing aspect ratio (AR) as critical dimension (d) shrinks for nanoscale devices

3.1   Profile control

Profile control in nanoscale etching is made harder by effects of both neutrals and charged species.

The neutrals and their effect on profile will be discussed first. Neutral etching species and neutral etch products move isotropically by diffusion (unaffected by the perpendicular sheath field) but when AR increases, the number of collisions with the sidewalls increases. Each collision slows the progress of etching species towards the bottom of a feature where it needs to react. Similarly the escape of resulting product species is slowed by collisions with the sidewalls. If species stick on the sidewall, progress will be impeded further. The sticking coefficient is a number between 0 (zero chance of sticking upon collision with the sidewall) and 1 (certain sticking). The control of neutral gas species type and their sticking coefficients becomes more important at the nanoscale for profile control. Low sticking coefficients are preferred for rapid transport of etching species down the feature and product species back up the feature. Simultaneously, sidewall passivant species (often polymer) need a high sticking coefficient if the protection is to be effective. See Figure 4. If the

correct balance is not found, poor profiles may result as illustrated in Figure 5. Note that substrate temperature is often a good way of controlling sticking coefficients without affecting the species type.
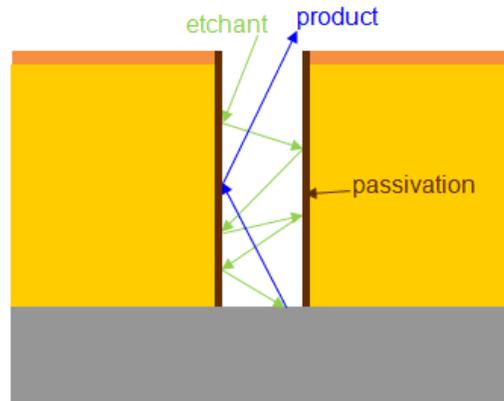

Figure 4. Etchant species, product species and sidewall passivation during etching
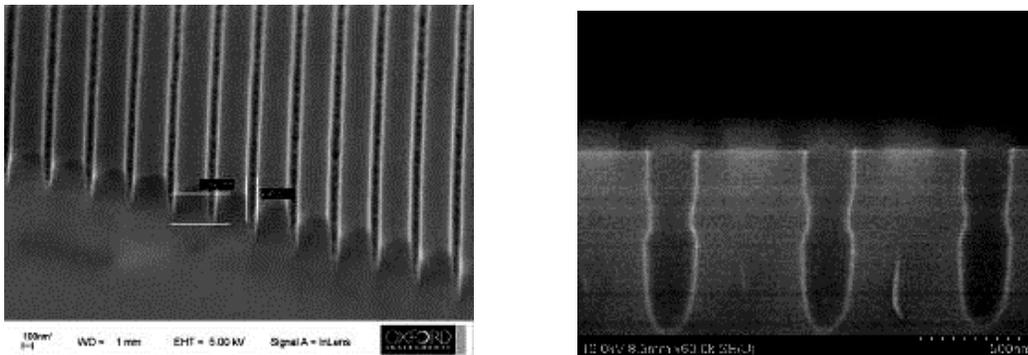

Figure 5. Left: Too much passivation (or sticking coefficient too high) leading to a tapered profile (closing up).
Right: Too little passivation (or sticking coefficient too low) leading to underetching of the profile.

The second basic reason for the greater difficulty nanoscale etching profile control is the increased effect of charging by ions and electrons as sidewalls get closer together. Charged species experience a lateral force (charge q multiplied by the electric field E) which is inversely proportional to the square of the distance y from the sidewalls. The constant of proportionality is greater for conductive or polar material making up the sidewall (because charge can move to enhance the effect). The result is that ions moving vertically from the plasma are deflected towards the sidewalls, and at higher aspect ratio there are a higher percentage of ions experiencing significant deflection. See Figure 6.

There is a further charging effect that can lead to greater ion deflection: electrons with their much greater mobility in the plasma move isotropically, both in the bulk plasma and close to surfaces, and they tend to build up at the mouths of openings in the surface. This negative charge repels further electrons and deflects positive ions at the top of the feature as well. If the substrate is conductive, then balancing currents can flow to alleviate such charge build up. However, if the substrate is insulating or electrically isolated like silicon-on-insulator (SOI) then charge build up will be worse. See Figure 7 middle.

Figure 7 gives examples where positive ion deflection causes "notches" at the top or bottom of the feature, or removing the passivation in the middle causing bowing. The additional fault of trenching at the base (deeper etching against the sidewall, see Figure NIL) is also associated with ion deflection. In these cases there is a need to raise passivation or enable better discharging e.g. by using pulsed plasmas or by adding conductive layers.
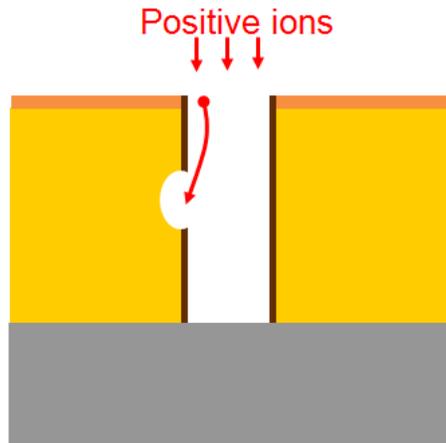
Figure 6. Ions are nearly vertical on approach but experience a lateral force towards the sidewall. Ions thus deflected can destroy protective passivation and lead to profile damage.
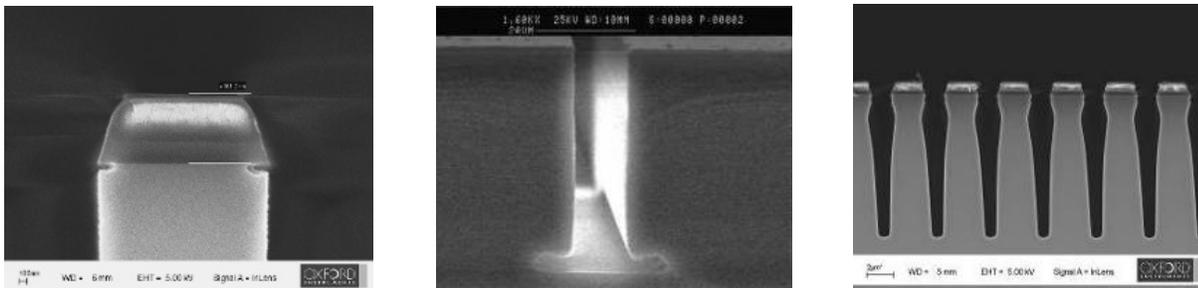

Figure 7. Left: Notch at top of feature.   Middle: Notch at base of feature (SOI interface).   Right: Ion deflection causing bowing in the middle

Of course, the profile faults shown in the examples of Figure 5 and 7 are seldom due to just one effect – it is a usually a combination, or an interaction of the two effects discussed in this section.

3.2   Aspect ratio dependent etching (ARDE)

Poorer transport of etching species and product species as introduced in the last section, leads also to aspect ratio dependent etching (ARDE). This is an undesired effect manifesting in two ways: larger features are etched deeper than smaller features for a given time (Figure 8 left), and if the etch time is doubled, less than double the depth results for a given feature (Figure 8 middle) i.e. the etch rate decreases with etch time or depth.

Coburn and Winters[4] showed that this reduction of the neutral flux towards the bottom of the feature can be described by a Knudsen transport model developed for vacuum systems. The concept of the transport probability is introduced. As AR becomes large the unhindered transport probability becomes vanishingly small (Figure 8 right).

ARDE can be a severe problem for some devices, necessitating re-design and it is usually unavoidable, except for some process conditions where heavy polymer deposition can be used to slow the etching of larger features enough to balance the etch rates across different feature sizes (the process window tends to be small and the process dirtier in these cases).

3.3   Other difficulties

ARDE of course means etch rates get steadily lower the deeper one etches. Low etch rate is not usually an issue in the fabrication of nanoscale devices (because they tend to very high value) but another consequence of ARDE is often a real difficulty – this is reduced selectivity over the mask. The mask at top of a feature is in a low AR situation and etches at the constant rate whilst the material to be etched in the HAR feature etches ever slower. Thus the selectivity over the mask is reduced for nanoscale features which can create limitations in depth and damage to profiles from thinned masks. Finally, process window for nanoscale etching is usually reduced, and of course, not to be underestimated, metrology and analysis become ever more difficult as feature sizes shrink.
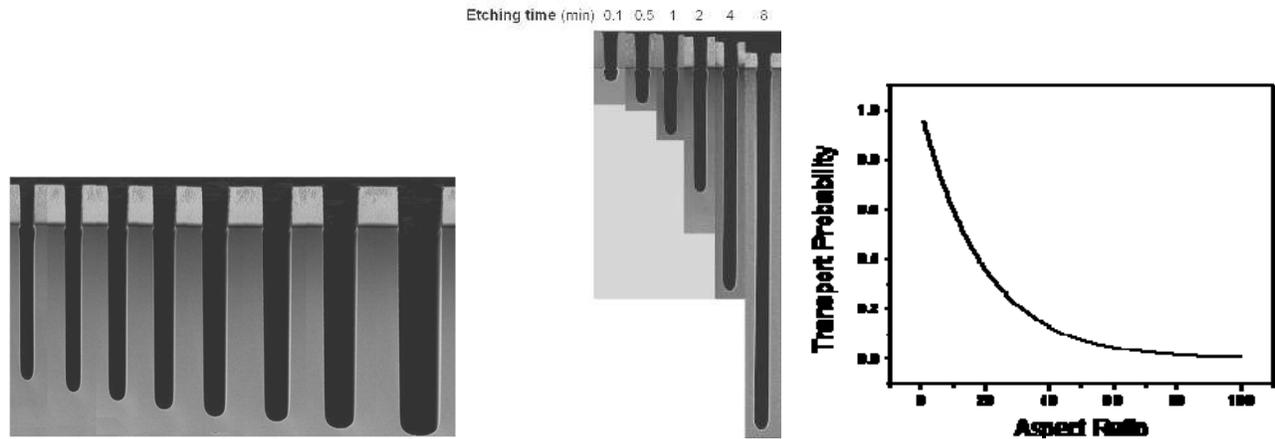
Figure 8. Left: ARDE (constant time).   Middle: ARDE (constant feature size) Right: Knudsen transport probability model.

3.4   ICP capability and limits

Alleviating the situation, at least for the near future of nanoscale etching is the fact that ICP technology is well able to cope with the higher end of the nanoscale: less than 100nm and down to about 40nm is relatively easy with current ICP technology. It is the ability of ICP to operate at low pressure yet with high plasma density and low (controllable) DC bias that helps greatly compared to simple RIE. Low pressure improves anisotropy by minimizing scattering of species by gas phase collisions. Producing good masking is still more of a limit in 2012 (though there is a helpful trend towards hard masking - see Section 4.4.4). Probably ICP technology will be sufficient to reach 20nm half pitch features fairly routinely and it will enable cutting edge device fabrication for some years to come without huge modification. However, going below 20nm and on to sub 10nm will be ever more challenging. An estimate of the ultimate limit of small trench etching has been given as about 5nm. This is based on the thickness of sidewall passivation films (2 or 3 nm per side) needed to prevent sideways etching[5].

4.   NANOSCALE ICP ETCHING RESULTS

4.1   Etching for nano-imprint lithography

Nano Imprint Lithography (NIL) is a versatile, cost effective, flexible and high throughput (parallel) method for fabrication of down to 10nm (and shrinking) structures even over large areas (wafers)[6]. It has applications in semiconductor memory, micro and nano fluidics, optical devices (e.g. LEDs and lasers), life science (e.g. lab-on-a-chip systems, bio-sensors), radio frequency components, renewable energy and new nanotech devices. The basic process flow of NIL is shown in Figure 9.
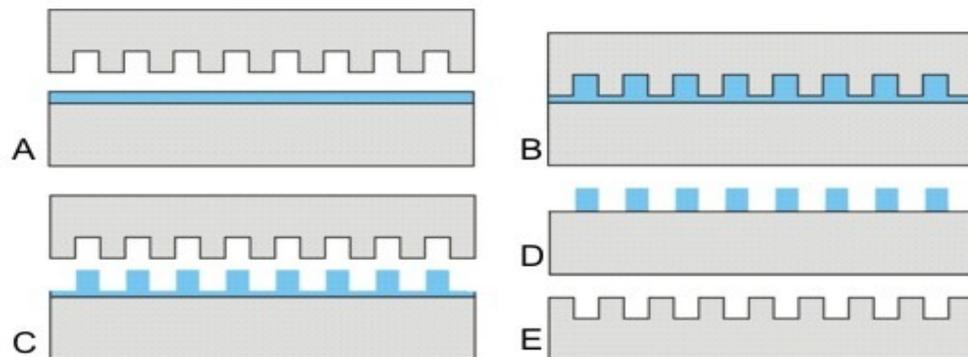

Figure 9. Schematic of the NIL process. A) A stamp is fabricated by electron beam lithography (EBL) and dry etching. B) The stamp is pressed into a soft thermoplastic, thermosetting or UV-curable polymer on a substrate combined with heating or UV radiation. C) The polymer is cured and the stamp released from substrate. D) Residual imprint polymer under stamp protrusions removed by 'descum' process. E) Imprinted pattern transferred into substrate by dry etching.

Dry etching by RIE and especially ICP is very important in three of these five basic steps of fabrication by NIL:

A. Nanoscale etching of the stamp: Si, SiO$_2$ (quartz), Ni, Cr, PDMS etc.

D. Descum of residual layer

E. Nanoscale etching of the substrate

4.1.1   Stamp etch

The requirements for a good stamp etch are vertical or near vertical profiles (but no negative slope at all to avoid damaging the NIL polymer as the stamp is pulled out), smooth sidewalls, uniform depths and uniform CD. It is also desirable to avoid trenching (Figure 10 left).

Figure 10 shows a Cr masked quartz stamp etched by ICP using Ar-C$_4$F$_8$-O$_2$ chemistry. 30nm features were etched to a depth of 200nm at a rate of 85nm/min ±<1% across a 2inch wafer. The selectivity over Cr was >170: 1. The profile is 89-90°, smooth and trench-free at the base.
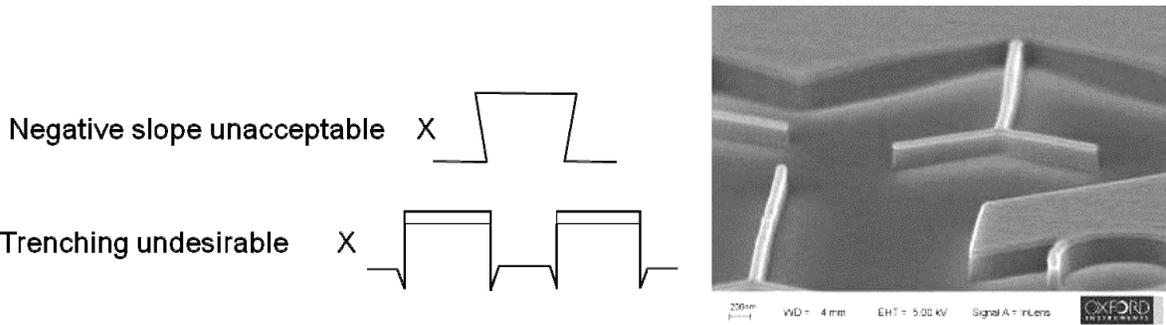

Figure 10 Left: Faults to avoid in NIL stamp etching.   Right: High quality nanoscale quartz etching for NIL stamp.

The quartz profile was optimized by means of the set electrode temperature as shown in Figure 11, while trenching was eliminated by using an optimum low DC bias – see Figure 12.
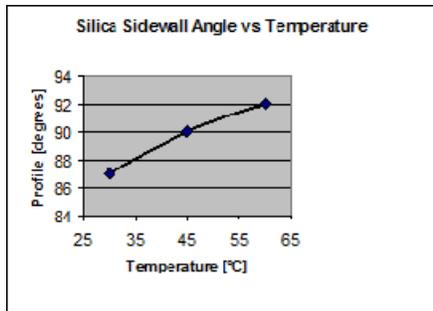

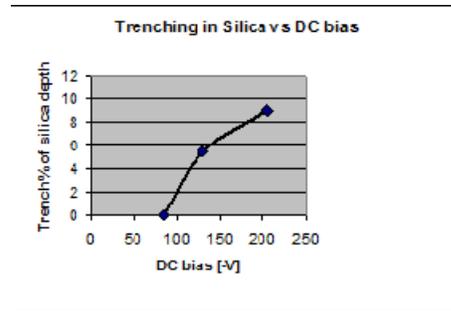Figure 11. Simple profile control by temperature   Figure 12. Trench control by DC bias reduction

Cr is often used as a hard mask for the quartz stamp etch. Figure 13 shows a nanoscale Cr ICP etch with features down to 70nm. Process gases were Cl$_2$-O$_2$-He. The etch rate was 15 nm/min with selectivity >5:1 over HSG and profile >85°.
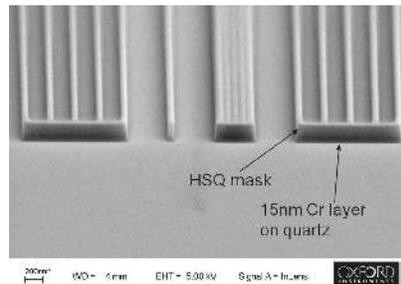

Figure 13 Nanoscale (70nm) Cr mask etch before quartz etch (picture courtesy of AMO GmbH)

4.1.2 Descum of NIL residual

The second area requiring an etch process is the descum of the NIL residual. Some "scum" is inevitable after the stamp presses into the NIL polymer and releases. Low scum is preferable of course (a ratio of H_R/H_L of 0.1 is considered good e.g. 20nm of scum for a 200nm polymer film. See Figure 14).

Figure 14. Residual NIL polymer after stamping step

Requirements for a good descum are to remove the scum whilst minimizing changes in profile and CD. It is inherently challenging as there is no 'mask' to protect the top of the pattern. Although most processes are O_2-based, new plasma chemistries will be needed as more NIL polymers are developed. For instance AMONIL[7] is descummed with a chemistry often used for SiO_2 etching: CHF_3-Ar.

ICP provides superior performance for descum: low pressure processing minimizes isotropic etching and loss of profile and CD control. Low temperature processing also helps – down to -50° C or less). Low bias processing by ICP also minimizes faceting at the top of the lines. Figure 15 is an example of a descum process of benzocyclobutene (BCB) polymer leaving 10nm lines intact using a low pressure O_2-SF_6 ICP process.
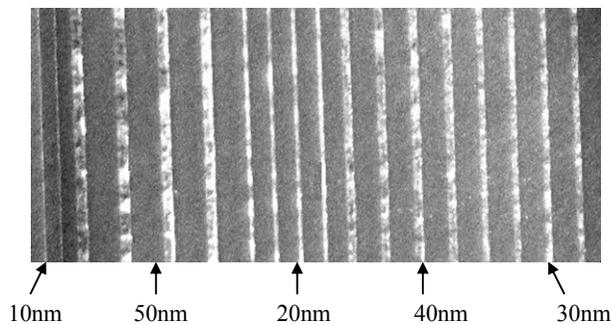

Figure 15. Nanoscale BCB lines descummed by ICP

4.1.3 NIL nanoscale etching

Having prepared the imprinted polymer it is very often used as an etch mask (although it may also be used as a lift-off mask or even as the final device e.g. polymer based microfluidics or optical devices). The requirements of the final substrate etch depend on the application and so are much more diverse than the stamp etch and descum. This is general nanoscale etching and examples will follow in later sections.

4.2 Etching of nanoscale holes

The etching of holes is required for some devices such as photonic crystals[8,9]. Generally the requirements are to produce holes with smooth, notch-free, vertical walls; sometimes with high aspect ratio. Etching holes is more inherently more challenging than trenches because of confinement in two dimensions instead of one. Sidewall collisions have a stronger effect: it is more difficult to control unwanted deposition or unwanted isotropic etching. Furthermore charging of the sidewall, mask and any underlayer interface has a stronger effect: it is more difficult to control unwanted notching.

Figure 16 illustrate typical problems in the etching of holes. Figure 16 left shows a 100nm hole etch with a bowed profile that has led to breakthrough between adjacent holes while Figure 16 right shows a significant notch at the top due charging and passivation loss. Figure 17 shows an optimized result for an 8:1 aspect ratio cryogenic silicon hole etch

obtained by using a multiple step recipe to control the profile. Figure 18 shows a good result for 100nm holes etched in quartz: the profile is >88° and selectivity over the ZEP520A mask >1.5:1.
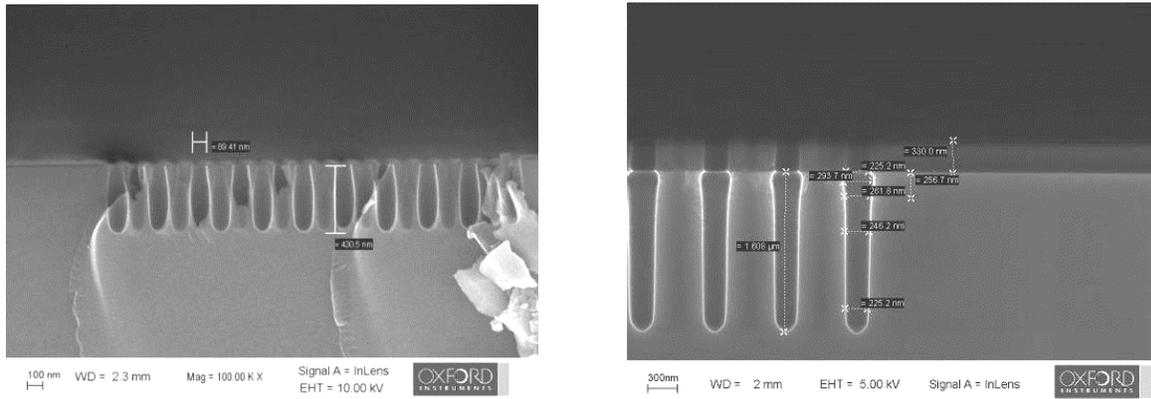

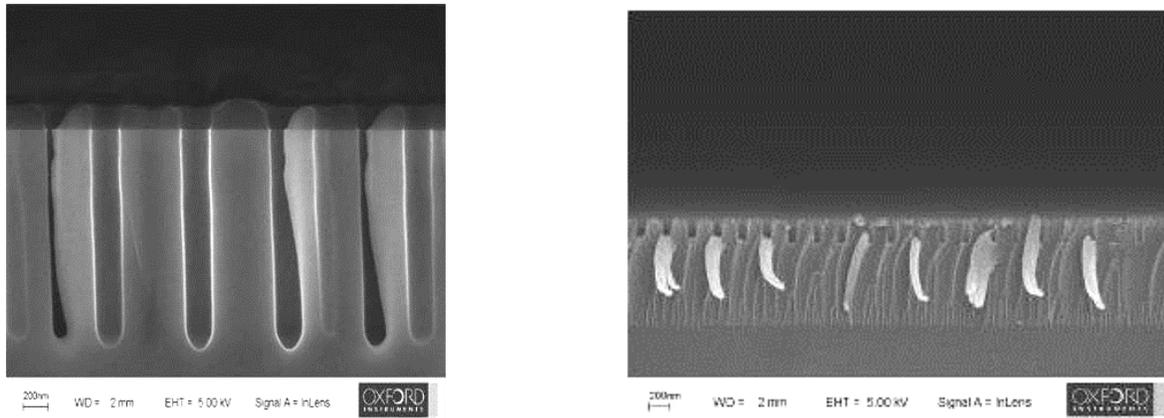Figure 16. Problems with holes Left: Bowed and with breakthrough between holes. Right: Holes with notching at the top

Figure 17. Optimized hole etch in silicon.   Figure 18. 100nm holes etched in quartz

4.3   Cryogenic etching for nanoscale features

Cryogenic etching is attractive for some nanoscale etching applications because the reduced temperature decreases the reactivity of the gas species with the sidewall and can enable more effective passivation than at higher temperatures. Excellent selectivities can also result if the reactivity of the mask is decreased relative to that of the etching substrate. Furthermore, cryogenic processes generally avoid organic passivant gases such as CHF_3 or C_4F_8 and so are cleaner processes. This tends to make reproducibility better and enables very long intervals between chamber cleans.

4.3.1   Cryogenic silicon etching

The cryogenic silicon etch has been used for deep silicon etching (DSE) for MEMS applications etc. since the early 1990s as a complementary process to Bosch DSE[10]. However, it was only relatively recently realized the cryo process is a very good option for nanoscale silicon etching[28]. The process uses a mixture of sulfur hexafluoride (SF_6) and oxygen (O_2) with the wafer electrode temperature below -90°C in order to etch Si anisotropically (with profile control from tapered (85°) to re-entrant (92°)). The mechanism of the anisotropy is illustrated in Figure 19. A silicon oxyfluoride species protects the sidewall due to reduced volatility at cryogenic temperatures[11].
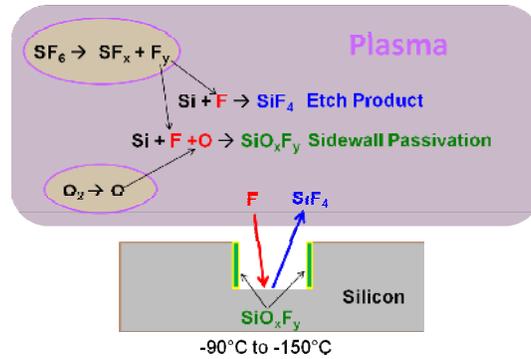
Figure 19. Principle of the cryogenic silicon etch process

The cryo process is attractive for nanoscale etching not only because the passivation layer is inorganic for very clean etching but also the layer is very thin which facilitates sub-10 nm etching. Furthermore, higher selectivities than alternative processes are achievable (e.g. >15:1 for ZEP520A electron beam resist) because the low temperature reduces the chemical attack of the mask. Finally, the gases are not alternated like the Bosch process so scallop-type sidewall roughness due to the isotropic SF_6 etch step is avoided. Thus with the cryo process, extremely smooth sidewalls are possible. Figure 20 contrasts the Bosch and cryo processes for nanoscale etching.
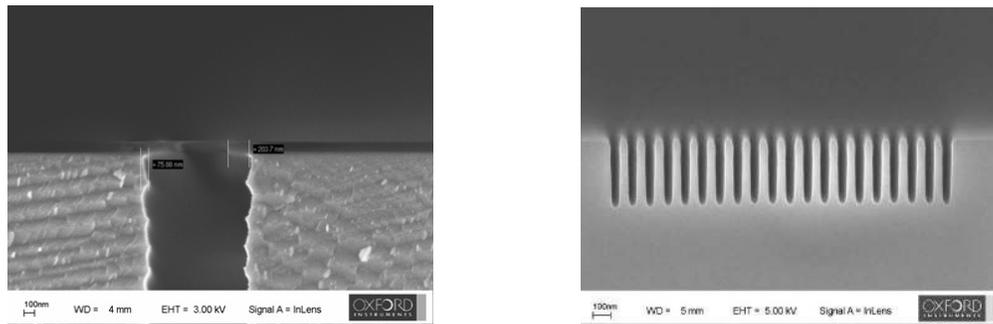

Figure 20. Left: A 500nm trench etched with the Bosch process etch shows 'scallops' with dimensions >100nm i.e. roughness is more than a nanoscale feature dimension. The scallops are due to the alternating SF_6 etch and C_4F_8 passivation steps. Right: Smooth 50nm trenches etched with the cryo process: the gases are mixed so scallops are not produced. Therefore the cryogenic silicon etch is more suited to nanoscale etching than the Bosch process.

Wu et al[12] have used the cryo process to produce 22nm wide trenches. An example result is shown in Figure 21. The selectivity over ZEP 520A resist here was 9:1 and the silicon etch rate was 200nm/min. The depth is 169nm so AR is 8:1. The process has been extended to 14nm trenches etched to a shallower depth of 36nm. The cryo process is quite feature size dependent in its etch rate (ARDE) and profile dependency. The same work reports that both ARDE and profile dependency can be reduced by adding higher energy bias. This may be because the transport of ions down the trench is enhanced by increased energy and reduced scattering due to passage of the ions within fewer RF cycles.
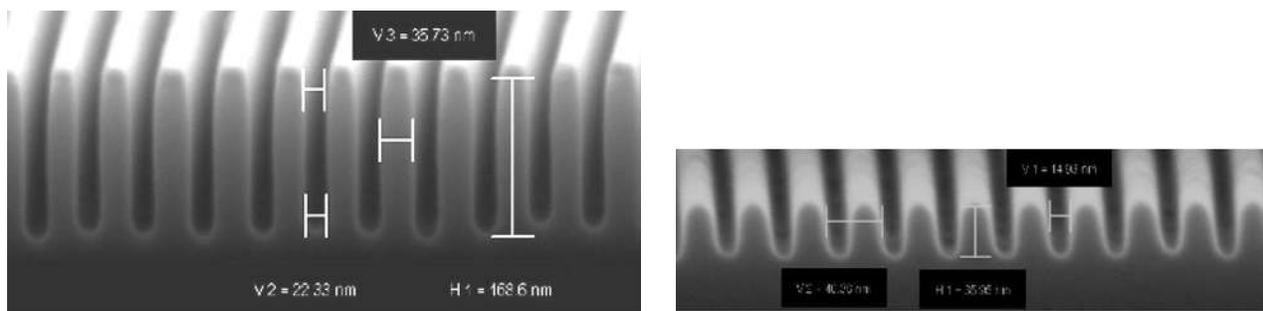

Figure 21. Left: 22nm Si trench etched with the cryo process to 169nm. Right: 14nm trenches to 36nm depth

4.3.2 Cryogenic tungsten etching

Cryogenic tungsten (W) etch is attractive because profile can be difficult to control at higher temperature without the use of organic passivant gases which make the process dirtier. Reinspach et al[13] have produced 12nm half-pitch W features for an application in soft x-ray zone plates using a bilayer mask scheme and cryogenic ICP W etching with SF_6-O_2. See Figure 22. The W etch is optimized at -50°C for the most vertical profile. Above that temperature, the Cr mask is undercut, while below it, the profile is overpassivated and becomes sloped. The passivation is likely to be a tungsten oxyfluoride species such as WOF_4 which has a much higher boiling point (186°C) than the gaseous etch product WF_6 (17°C)[14]. The process produced excellent results down to 12nm half pitch features (the mask is starting to fail for 11nm half-pitch). See Figure 23.
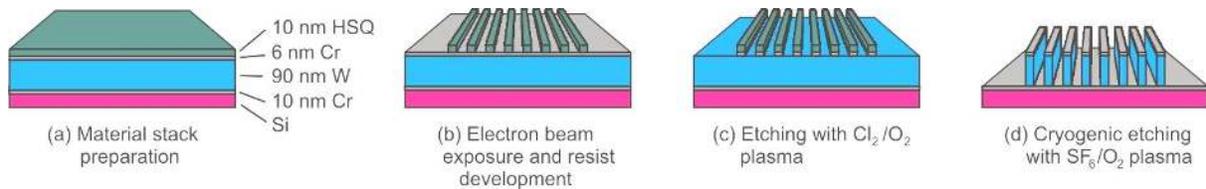

Figure 22. Left: Fabrication scheme for nano-tungsten gratings. After substrate preparation a) the grating pattern is first written in the HSQ resist and then developed b). Subsequently, the pattern is transferred to the Cr layer by RIE with Cl_2-O_2 c) and finally into the W by cryogenic ICP etching with SF_6-O_2 d).
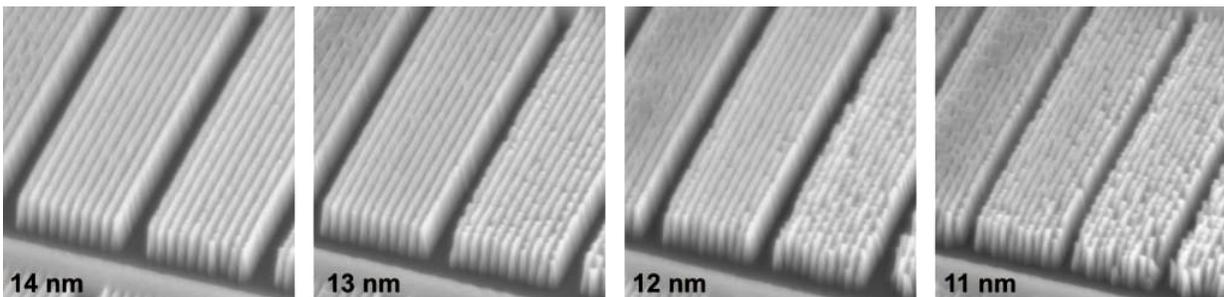

Figure 23. W gratings etched with half-pitches of 11nm to14nm. The pattern transfer down to 12nm is good. The W thickness is 90nm so AR is 7.5:1

4.3.3 Cryogenic polymer etching

It can be difficult to find suitable sidewall passivation for polymer etching because the material is obviously organic so gases such as CHF_3 are not useful. Thus in polymer etching re-entrant or bowed profiles can be a problem, especially as feature sizes reduce to the nanoscale. Inorganic passivants such as CO_2 and SO_2 can provided some benefit[15] but the passivation tends to be quite weak. The use of lower temperatures can reduce the reactivity at the sidewall and so enable better profile control without the need for additives[16]. Figure 24 gives a good example for nanoscale polyimide ICP etching. An e-beam evaporated Ti mask 10nm thick was etched by RIE using BCl_3 gas before cryogenic ICP etching at -100°C with pure O_2 (no additional passivant gas). The result is nearly vertical nanoscale polyimide features etched to a depth of 500μm with 50nm half-pitch[17].
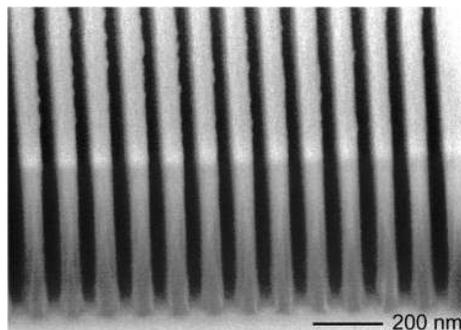

Figure 24. 50-nm half-pitch polyimide-grating, 500 nm high (AR 10:1). 10nm Ti mask

4.4 Enhancing the mask for nanoscale etching

Providing a mask of sufficient quality can be a major problem in realizing a good nanoscale etch. Currently it is fair to say that most limitations arise in the mask fabrication for the low tens of nanometer feature sizes and less (although it should be added low selectivity over the mask in the etching process is an interlinked problem). Proximity effects in resist exposure limit the half-pitch dimensions achievable[18], while in order to provide sufficient mask for the subsequent etching, the resist must be thick enough. However, with increasing resist thickness, pattern collapse due to capillary forces and swelling becomes a major issue for densely packed features[19].

4.4.1 Enhancing the mask: novel technique using atomic layer deposition (ALD) to shrink lateral dimensions

Peroz et al[20] have used a novel scheme to reduce the trench width on a NIL stamp. The principle is shown in Figure 25. Firstly a pattern in HSQ is formed on the quartz substrate, and then a thin conformal layer of alumina (Al_2O_3) is grown over the HSG by ALD[21, 22]. This reduces the trench width by twice the layer thickness (as well providing a durable coating for the HSG).
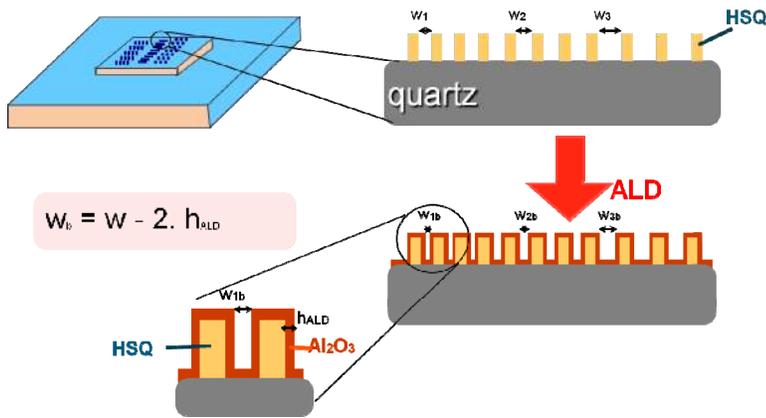

Figure 25. Reducing the stamp trench width using ALD of alumina

Figure 26 shows how 45 ALD cycles reduce the trench width to 10nm, while a total of 90 cycles leaves a width of 4nm. The trench depths are about 30nm.
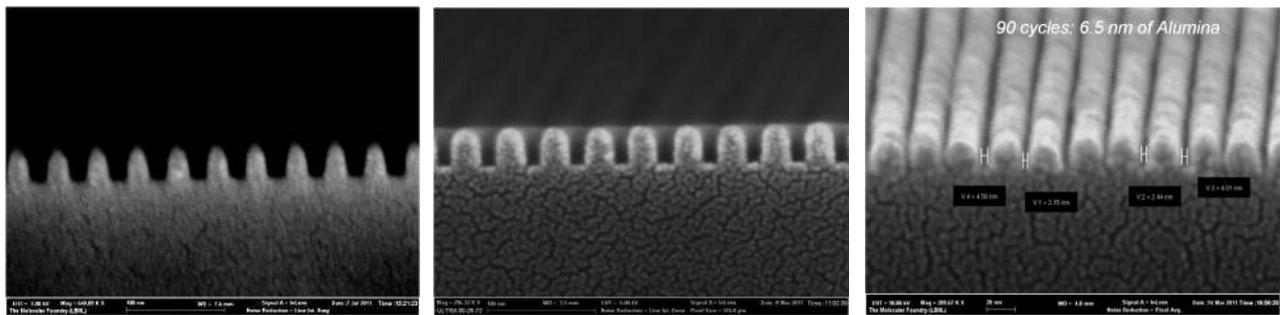

Figure 26. Left: Original HSQ with trench width 18nm. Middle: 45 ALD cycles - width 10nm. Right: 90 cycles - width 4nm

The composite HSG-Al_2O_3 stamp is then used to imprint into NIL resist on a Si substrate. After descum, the Si is etched with the cryo process. Figure 27 shows near vertical 15nm lines and a 6nm line (though with a slightly bowed profile) that have been produced by this method.
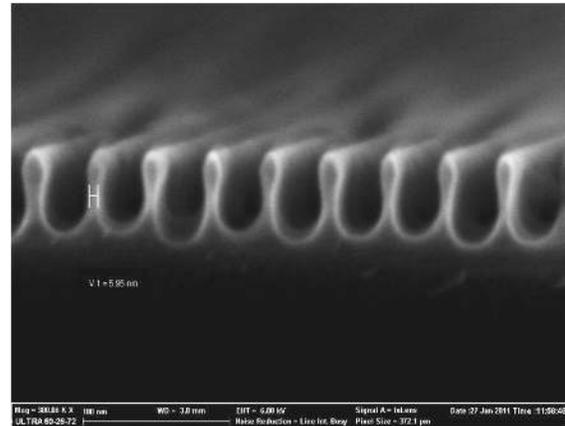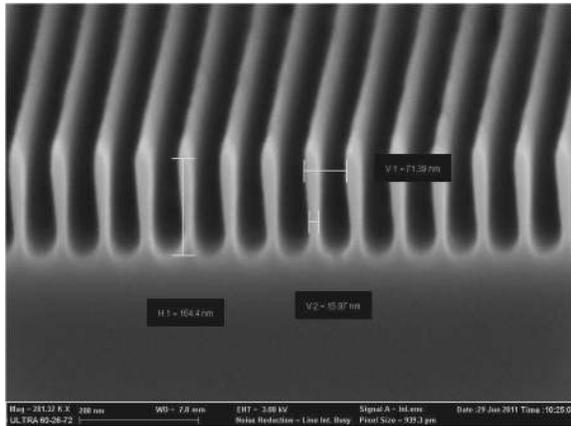
Figure 27. Left: 15nm lines 71nm deep cryo Si etch   Right: State of the art 6nm lines ~50nm deep

4.4.2 Enhancing the mask: illustrations with the mixed gas process for nanoscale silicon etching

The mixed process uses the Bosch gases, SF_6 and C_4F_8 (or CHF_3) mixed together rather than in alternating steps. It is capable of the smooth etching of sub-20nm features. Profile is readily controllable in the range 80 to 92° by means of the polymer gas percentage (Figure 28). It runs at room temperature and is robust, well understood and it is generally straightforward to set up a good recipe. The main disadvantage over the cryo Si process is low selectivity over resists – for nanoscale etches selectivities can be as low as 1:1 which limits the attainable depth. Even if there is theoretically enough resist to etch the required depth, unsatisfactory sidewall roughening can occur if the resist is thinned too much. In this case lateral etch back of the resist can lead to etch roughening at the top of the profile.
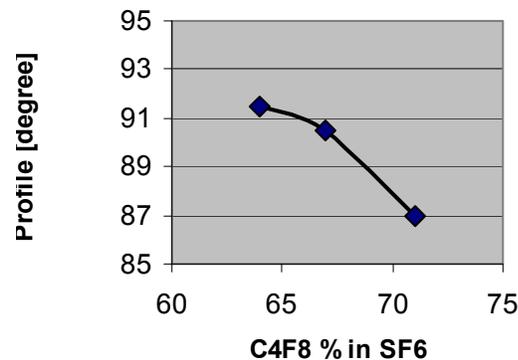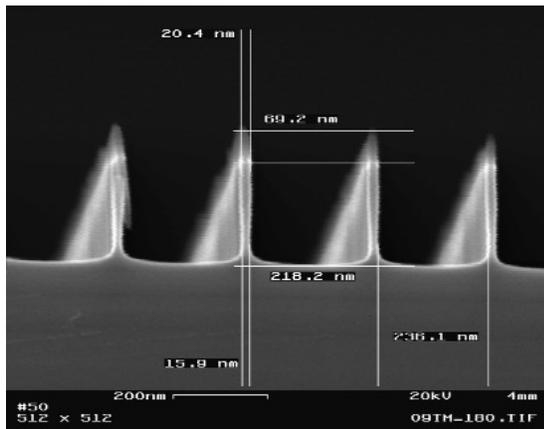

Figure 28. Left: 16nm lines etched in Si with an HSQ mask. Right: Profile slope is increased by raising C_4F_8 %.

4.4.3 Enhancing the mask thickness and mechanical properties using a fullerene-based mask: illustration with the mixed gas process

Frommhold et al[23, 24] report a tri-layer resist scheme to fabricate a thick and mechanically stable mask with the novel use of a fullerene-based material for the thick bottom layer. The aim is to achieve high AR 20nm half-pitch features in Si with such a mask. Figure 29 is a schematic of the mask preparation. A thin fullerene-based negative tone resist pattern is formed on a 50nm thick top Si layer. A very short mixed process is then used to etch the top Si layer, which is in turn used as a mask to etch the 350nm thick fullerene-based Spin-on-Carbon (SoC) layer with a low pressure O_2 ICP process.
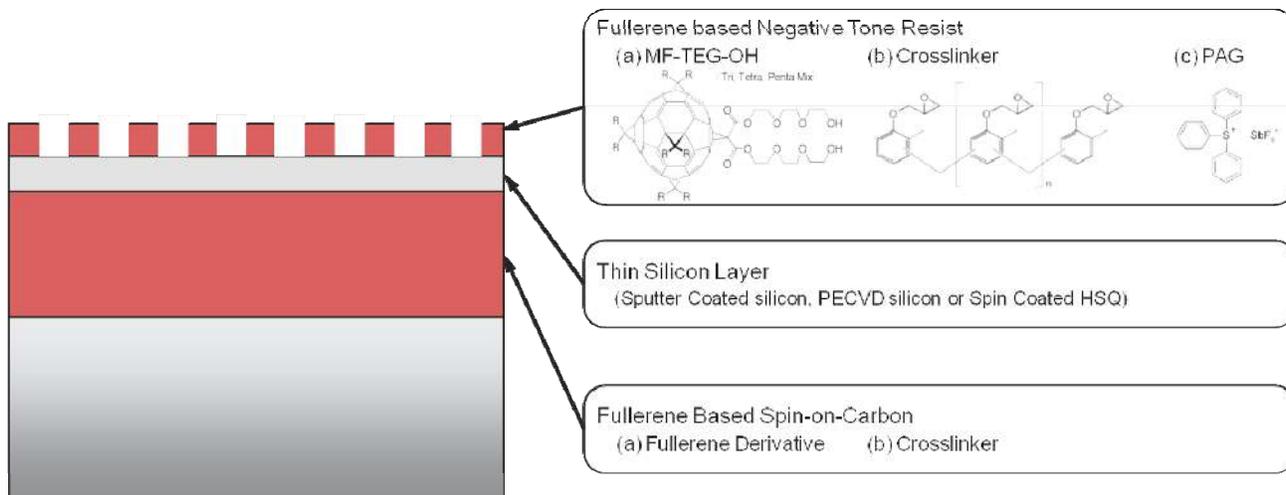
Figure 29. Schematic of the tri-level mask based on fullerene.

Figure 30 shows 40nm close packed 'fins' of SoC. AFM tip indentation tests indicate excellent film hardness (800MPa) and high Young's Modulus (up to 6GPa) which confers better resistance to pattern collapse than standard resist and so permits thicker films with smaller half-pitches. Having prepared the SoC mask, it is used to etch the underlying Si with the mixed process (SF_6-CHF_3 version). Figure 30 shows good near vertical silicon etching for 40nm half-pitch and 20nm isolated lines.
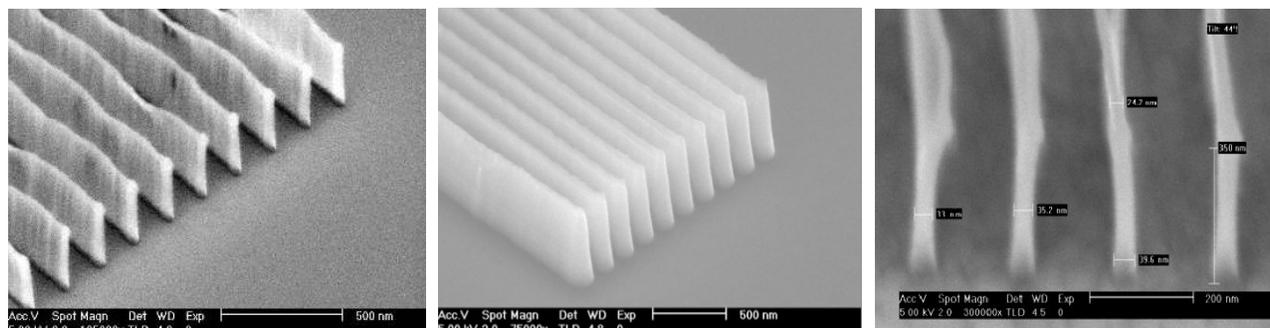

Figure 30. Left: 40nm x 350nm deep SoC mask etched by O_2 ICP Middle: 40nm half-pitch lines etched in Si with the mixed Si etch Right: 20nm lines etched to 350nm depth

4.4.4 Improving the selectivity and aspect ratio by using a hard mask: illustrations with the mixed gas process

If a suitable material can be found that has high selectivity in the nanoscale etching process, and can be deposited as a thin hard mask layer and easily patterned, great benefits can result. Firstly, problems in fabricating the mask such as pattern collapse and proximity effect issues are sidestepped (provided the resist for patterning the hard mask can be kept thin enough). Secondly, the aspect ratio is kept to the minimum without the mask thickness adding to it significantly – see Figure 31. Thirdly greater depths and aspect ratios can be achieved without mask loss or sidewall roughening due to lateral mask loss. The disadvantage is greater complexity and cost from more processing step (at least one more deposition and etch cycle plus usually a hard mask removal step at the end).
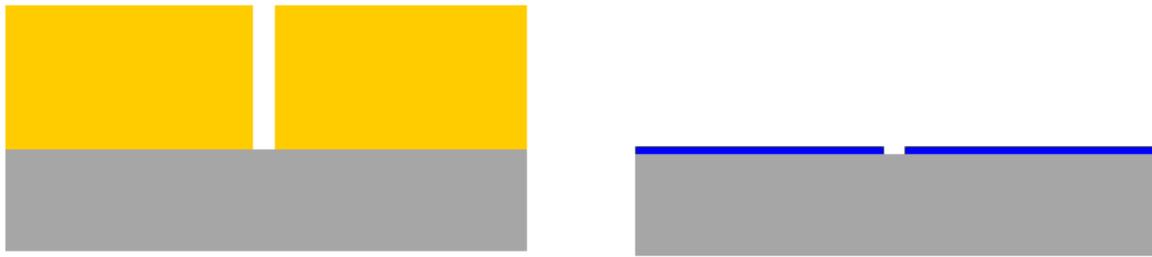
Figure 31. Left: Thick resist mask: high AR even before etching.　　Right: Thin durable hard mask: AR starts low

A suitable hard mask is alumina (Al_2O_3). This may be deposited by DC sputtering of an Al target in an O_2 containing atmosphere or by ALD. The alumina may be patterned by lithography and a short etch process (for instance Ar-CF_4 ICP) or a lift-off procedure. Henry et al[25] show that the thin alumina is highly selective (68:1) in the mixed Si etch and deep high AR structures are possible. See Figure 32. It is noteworthy that the cryo Si etch (with its very low DC bias) shows extremely high selectivity over alumina masking. Henry et al show >5000: 1 and up to 70,000: 1 has been reported[26].
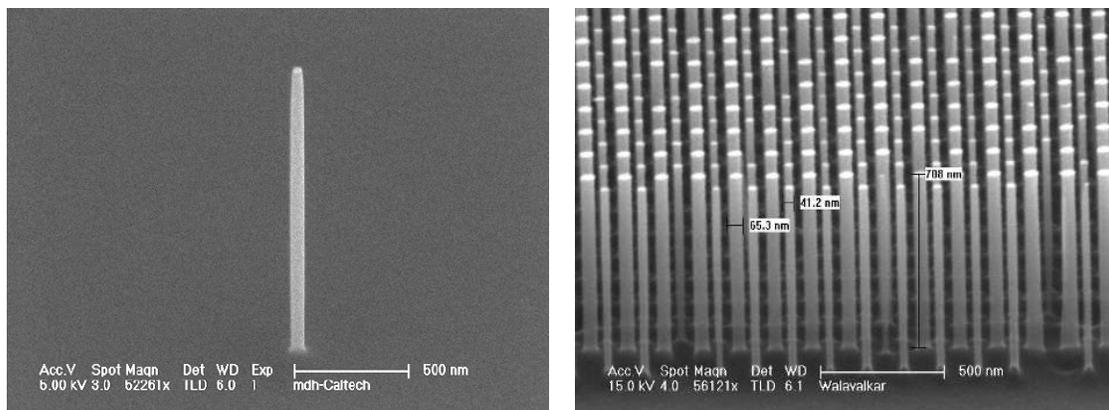

Figure 32. Mixed gas Si etching with an alumina mask　　Left: Isolated 40 nm pillar 1750nm tall. Right: Dense 40 and 60nm pillars 700nm tall

Gallium is another material that is not significantly etched by the fluorinated chemistry of the mixed process. A novel way of producing gallium mask is to use the familiar focused ion beam technology to implant Ga[27]. This technique avoids the use of resist at all stages of fabrication, is of high throughput and adds no aspect ratio at all at the start of the etch. Good selectivity is obtained in the mixed process (though not as high as alumina) by means of fluoridation of the Ga to non volatile GaF_3. Linear selectivity versus implanted Ga density enables the possibility of grayscale lithography. High fidelity structures down to 30 nm with aspect ratio structures of 17:1 have been demonstrated. See Figure 33.
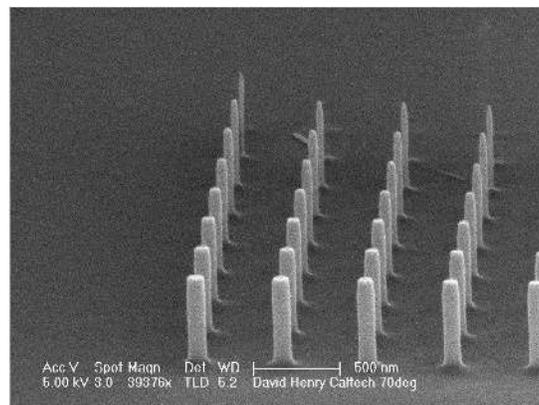

Figure 33. Mixed gas Si etching with a FIB implanted Ga: pillars down to 30nm and 450nm tall (AR 15:1).

4.5 Other nanoscale etch processes

4.5.1 HBr-based Si etch

The HBr-based etch process is another option for nanoscale silicon etching[28]. This process is useful when very high selectivity over a silicon dioxide insulator is required, such as for nano-scale MOSFETS[29] where the gate oxide is extremely thin. It is also a good choice for other SOI applications because the reduced reactivity of HBr makes it much easier to avoid notching at the silicon-insulator interface (Figure 34 left and middle). Such applications include 2d-photonic crystals where the addition of an insulator layer such as silicon dioxide provides vertical confinement of light in the silicon (SiO2 having a lower refractive index than Si). The HBr-based process has other benefits of smooth controllable profiles, high aspect ratio capability and is very clean. The processing temperature is around room temperature. Oxygen substitution is may be used to raise selectivity of Si over SiO_2. The graph in Figure 34 shows that extremely high selectivities can be achieved if the O_2 gas flow rate is raised to a critical level. Because of the use of O_2 in the process masking, selectivity over organic resists is low. SiO_2 is a preferable mask and HSQ resist (which is develops to an 'oxide-like' material) is an excellent choice.
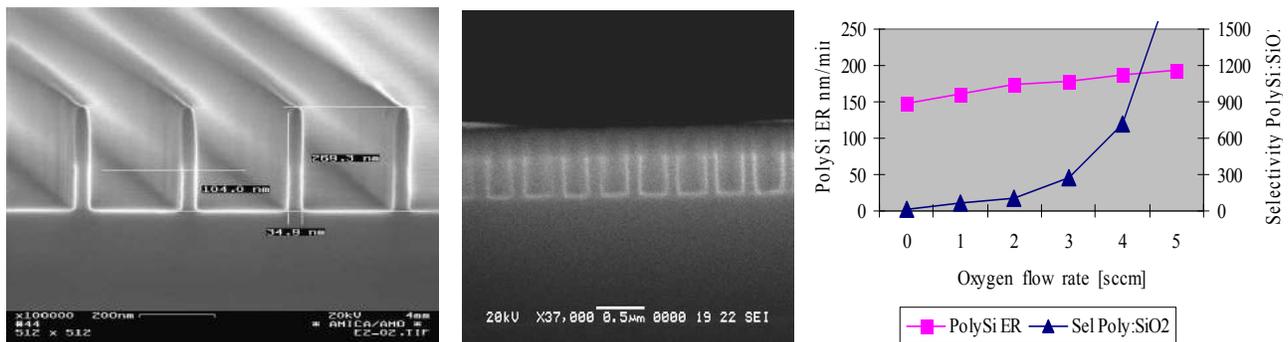

Figure 34. HBr-O_2 Si etching Left: 34nm polysilicon gates with stop on 3nm SiO_2. Image courtesy of AMO, Aachen. Middle: Notch-free vertical SOI etch for photonic crystal holes stopping on SiO_2. Right: Selectivity over SiO_2 control by means of O_2 substitution

4.5.2 Nanoscale fused silica etch

Fused silica is a dense SiO_2 material that etches in a similar fashion to quartz. Figure 35 shows a good example of a deep nanoscale etch formed using a novel C_4F_8-CO_2 ICP etch chemistry[30] and a thin Cr mask. The lines are 68nm wide and 940nm deep – an isolated feature aspect ratio >13:1. The profile was optimized to vertical by means of gas ratio (1:1) to give suitable sidewall passivation without excessive polymerization, and low bias power to minimize ion energy and consequent re-entrant etching.
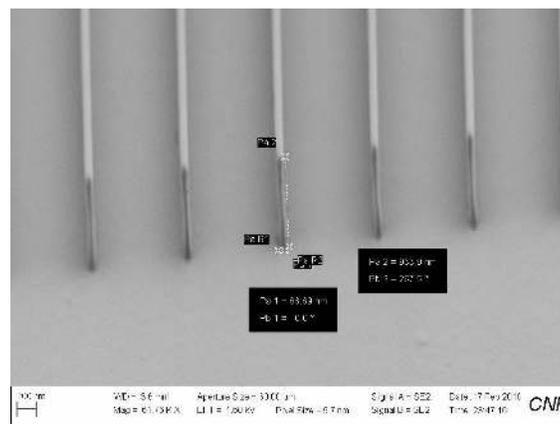

Figure 35. Nanoscale fused silica etching with a Cr mask. The lines are 68nm wide and 940nm deep

4.5.3 Other nanoscale metal etches

Figure 36 shows a pattern etched in platinum (Pt) with a 10nm gap resolved. This is a simple sputter etch with pure argon gas. Redeposition is avoided by means of a very low pressure etch made possible by ICP processing and by nearly consuming the entire ZEP520A mask, which etches any redeposition away (at the cost of beveling the top on the features).

Figure 37 shows 60nm pillars etched in tantalum (Ta) with an HSQ mask using CHF_3-CF_4 ICP chemistry. The application is in magnetoresistive random access memory (MRAM) devices for data storage purposes. Ta has relatively low electrical resistance and is used in this technology as intermediate conductive etchable mask[31]. The ICP enables easy fabrication of sub-100nm Ta pillar arrays with good shape and size uniformity as required by the MRAM devices. The Ta depth is 50nm, the etch rate is 23nm/min and selectivity over HSQ resist 1:1.
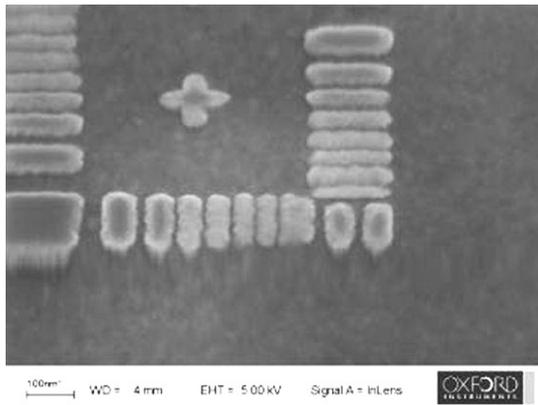

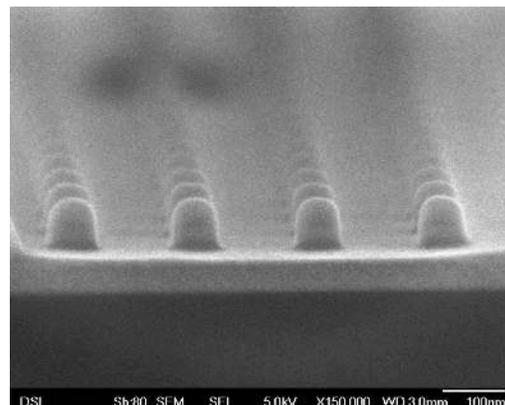Figure 36. Pt nanoscale etch with a 10nm gap resolved.

Figure 37. 60nm HSQ masked Ta pillars with 87° profile

5. CONCLUSION

A review of ICP etching for nanotechnology has been given. The increasing difficulty of nanoscale etching has been explained and it has been stated that current ICP technology is good for several years more to below 20nm half pitch. To get smaller and to what may be the ultimate limit for etching of around 5nm will require advances in the technology to achieve better control of neutrals and charged species. Chamber design and efficiency will have to be optimized. This may include careful control of temperature control for all reactor internal surfaces. New hardware developments may involve controllable frequency and pulsed plasmas, better substrate temperature control and advanced software control – for instance feedback loops using optical emission spectroscopy and other diagnostic techniques, and advanced recipe management.

ACKNOWLEDGEMENTS

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