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Forward-biased nanophotonic detector for ultralow-energy dissipation receiver

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Generally, reverse-biased photodetectors (PDs) are used for high-speed optical receivers. The forward voltage region is only utilized in solar-cells, and this photovoltaic operation would not be concurrently obtained with high efficiency and high speed operation. Here we report that photonic-crystal waveguide PDs enable forward-biased high-speed operation at 40 Gbit/s with keeping high responsivity (0.88 A/W). Within our knowledge, this is the first demonstration of the forward-biased PDs with high responsivity. This achievement is attributed to the ultracompactness of our PD and the strong light confinement within the absorber and depleted regions, thereby enabling efficient photo-carrier generation and fast extraction. This result indicates that it is possible to construct a high-speed and ultracompact photo-receiver without an electrical amplifier nor an external bias circuit. Since there is no electrical energy required, our estimation shows that the consumption energy is just the optical energy of the injected signal pulse which is about 1 fJ/bit. Hence, it will lead to an ultimately efficient and highly integrable optical-to-electrical converter in a chip, which will be a key ingredient for dense nanophotonic communication and processors.
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I. INTRODUCTION

The energy consumption and footprint of a photoreceiver are critical issues as regards increasing the integration density in an on-chip/off-chip photonic network designed to provide high-performance computing and data management. To deal with these issues, the conventional photoreceiver configuration, which generally needs an energy-hungry amplifier/bias circuit, should be reduced to the femtojoule per bit (fJ/bit) level to meet the energy requirement for future on-chip optical links.[1]

One concern is that the energy consumption of transimpedance amplifiers (TIAs) and certain voltage amplifier stages integrated with a photodetector (PD) to generate sufficient output voltage is as much as several hundred fJ/bit.[2,3] One way to overcome this problem is to use an amplifier-less PD (or so-called receiver-less PD).[2,4,5] Sufficiently large resistance (kΩ level) load connected to the PD realizes current-to-voltage transimpedance conversion without a large electrical energy supply. A compact PD with ultralow capacitance is needed to achieve this because the resistance-capacitance (RC) product strictly limits the transimpedance conversion efficiency and operation bandwidth. Recently, we demonstrated an ultra-small InGaAs PD based on a photonic crystal (PhC) waveguide. This PD with a length of only 1.7 μm and implemented in an air-bridge structure allowed

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a device capacitance as small as 600 aF. This provides an amplifier-free resistor-loaded PD with a kV/W level light-to-voltage conversion efficiency and an operation bandwidth of >20 GHz,[5] which are comparable to or even higher than those of amplifier-integrated receivers.

There is yet another issue related to the main topic of this paper that also contributes to the PD energy consumption, which is induced by the external bias voltage. A p-i-n PD generally needs to be driven under a reverse bias voltage for the fast extraction of photo-generated carriers. However, when the photo-generated charge Q_{pc} flows under an external reverse bias voltage V_{bias}, it consumes a photocurrent energy of $E_{pc} = V_{bias}Q_{pc}$, which corresponds to the work done for the photocurrent by the external voltage supply. If we assume both perfect absorption and perfect photocurrent collection for the incident optical energy of E_{opt}, the generated charge and the photocurrent energy would be $Q_{pc} = E_{opt}(e/\hbar\omega)$ and $E_{pc} = eE_{opt}V_{bias}/\hbar\omega$, respectively. Therefore, under a high V_{bias} ($\gg\hbar\omega/e$), the electrical energy consumption becomes larger than the optical counterpart, that is, $E_{pc} > E_{opt}$. For instance, if we assume a light-to-voltage conversion efficiency of 10 kV/W for a non-return-to-zero (NRZ) optical signal with a bit rate of 10 Gbit/s, to obtain a signal voltage of 0.2 V would require an optical energy of 2 fJ/bit (=0.2 V/10 kV/W/10 Gbit/s), but it would need an additional electrical energy of 4 fJ/bit when V_{bias} = 2 V. Furthermore, if the bias circuit has a large parasitic capacitance due to the surrounding circuitry, the load resistance needs to be reduced to maintain the bandwidth, which results in a smaller conversion efficiency and consequently a larger E_{opt} and E_{pc}. A bias-free operation is therefore desirable in terms of reducing the energy consumption.

Consequently, if amplifier-free bias-free operation is realized, the energy consumption of the receiver can be extremely low since only the energy of light generates the output voltage. A zero-bias-voltage operation that maintains a high-speed response has been demonstrated with several types of waveguide PDs.[6–9] However, combining these bias-free PDs with amplifier-free voltage generation by connecting them to a large resistance (kΩ level) load has never been envisioned. To pursue an amplifier-free and bias-free combination, we need to consider the fact that a resistor-loaded PD would lead to a *forward* voltage across the PD,[10] as discussed later. Such a forward voltage region for a p-i-n-PD is generally used for a solar cell or photo-voltaic cell and would not be concurrently obtained with both the high efficiency and the high speed operation (e.g., GHz range) demanded for the optical receiver. Reports on forward-biased PDs have been limited to very few specific devices such as a uni-traveling carrier (UTC) PD for the radio-over-fiber applications.[8,11] However, they suffer from low optical responsivity as low as 0.2 A/W and still only consider a 50-Ω termination, which requires an optical energy of pJ/bit level and is hence not suitable for on-chip com application.

In this letter, we present the forward-biased operation for our PD based on a PhC waveguide and discuss the capability of a nanophotonic PD as a bias-free amplifier-free receiver. Our experimental results show that the PhC-PD achieves a high optical responsivity of 0.88 A/W, which it maintains even in the forward voltage range. The impulse and random signal responses suggest 40-Gbit/s operation at a forward bias of 0.2 V. Based on these experimental results, we simulate a resistor-loaded PD receiver circuit when assuming a kΩ-level load resistance and an ultralow capacitance of about 1 fF, which are possible for a few-μm PhC-PD. As a result, we theoretically confirm the feasibility of the receiver for high bit-rate voltage generation without the need for electrical amplifiers or a bias circuit. This will offer a way of realizing a fJ/bit-energy photoreceiver with a μm^2 footprint.

II. EXPECTATION FOR FORWARD-BIASED PD

To explain our operation scheme, we presume that an amplifier-free PD is configured by connecting the PD with a load resistor and an external bias voltage source, as shown in Fig. 1. Here we first consider that the external reverse bias voltage (V_{bias}) is applied to the PD to efficiently extract photo-generated carriers. The photocurrent I_{pd} flows and generates the output voltage (V_{out}) by incorporating the load resistance (R_{load}), as indicated by the photocurrent-voltage curve and the load curve. This results in a reduction in the applied voltage across the PD, namely, $V_{bias} - V_{out}$. If this reverse voltage is still sufficiently high to maintain the fast carrier extraction, there is no degradation in optical responsivity. However, the photocurrent consumes an extra electric power of $I_{pd}V_{bias}$ supplied by an external voltage source, in addition to the incident optical power P_{opt}.

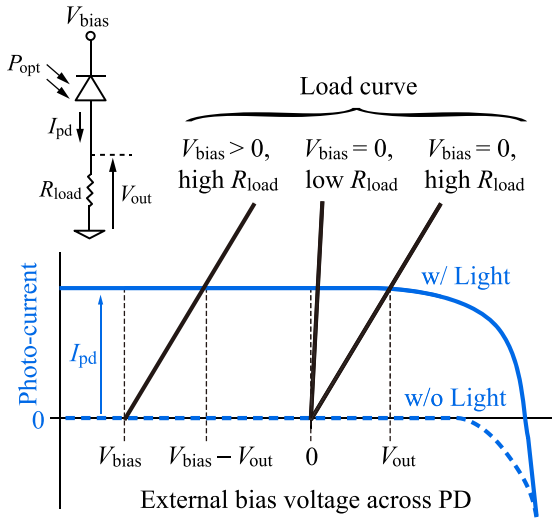

FIG. 1. PD response curves and load curves under different bias voltage conditions. The blue curves are photocurrent curves with and without light injection. The black curves are the load curves under different conditions (non-zero-bias or zero-bias condition, and low-R_{load} or high-R_{load} condition).

Such extra power is not consumed during zero-bias operation (V_{bias} = 0), for example, solar-cell operation. This condition is not useful when R_{load} is small (<100 Ω) such as with previously reported zero-bias PDs[6–9] because a large voltage V_{out} cannot be generated unless strong light is input into the PD. On the other hand, when R_{load} is sufficiently large, a large voltage V_{out} can be generated. This voltage generation acts as a forward voltage across the PD and hence causes a reduction in the internal built-in electric field, which may degrade the responsivity and operation speed. Therefore, to realize a resistor-loaded bias-free photoreceiver, it is essential to maintain the fast carrier extraction even when the forward voltage is applied. In the present experiment, our aim is to demonstrate the efficient and fast operation of a PhC-PD under an external forward voltage bias to emulate a resistor-loaded PD. As far as we know, there has been no such demonstration for small PDs with a capacitance in the fF regime.

III. DEVICE STRUCTURE AND STATIC RESPONSE

Figure 2(a) shows a scanning electron microscopy (SEM) photograph of our PhC-PD. The device was formed by combining an InP-PhC waveguide, a lateral p-i-n junction, and an ultra-small BH that was embedded in an InGaAsP absorber, resulting in both the strong photon/carrier confinement and a small junction capacitance.[12] The fabrication process is referred in our previous literature.[13] During the process, InGaAsP with a width of around 350 nm and 150 nm thick was embedded in a 250-nm-thick InP-PhC slab. The lattice constant a and air hole diameter $2r$ of the PhC were 420 and 200 nm, respectively. A lateral p-i-n junction was formed by employing Zn diffusion and Si ion implantation for the p- and n-type doping, respectively, where the doping concentration for both types was around 10^{18} cm^{-3}. PhC air holes were formed by electron-beam lithography and Cl_2-based dry etching. After metallization, an InAlAs sacrificial layer was etched to form an air-bridge structure. The PL wavelength of InGaAsP was 1.45 μm, and the waveguide length was 35 μm. The device capacitance, which included that of the parallel-plate part and the fringing part, was estimated to be only 5 fF with the three-dimensional finite-element method (3-D FEM).

Figure 2(b) shows the simulated optical field profile and the internal static electric field for different bias voltages. There are several requirements for forward-biased operation. First, the strong concentration of light in the absorber is needed to obtain high optical responsivity. We can expect an optical confinement factor of as high as 0.5 for our PhC-PD. Second, a small cross section for the absorber and the intrinsic region will lead to full carrier depletion even under a forward bias voltage. Compared with our previous PhC-PD, which requires the reverse bias voltage more than 2 V for the

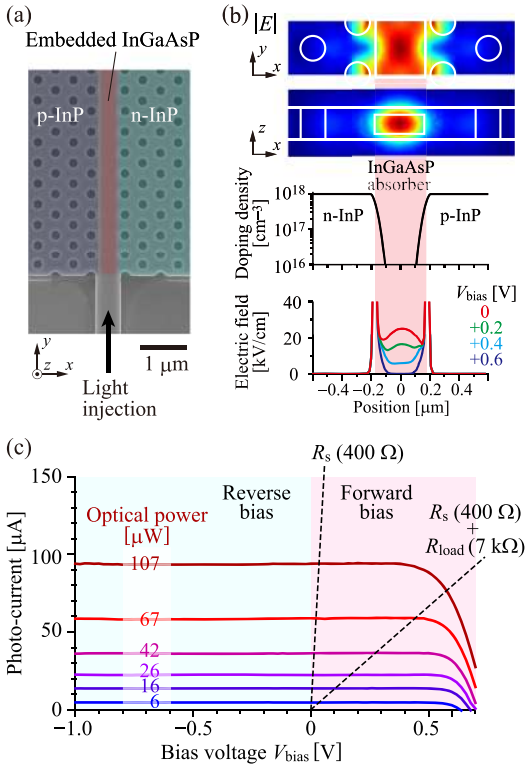

FIG. 2. Device structure and static photo-response. (a) SEM photograph of the device. (b) Calculated optical field and static electric field. The optical field profile |*E*| (top), the doping profile (middle), and the static electric field (bottom) for different external bias voltages. An absorber width of 350 nm and a p/n separation of 400 nm were assumed. (c) Measured photocurrent versus bias voltage characteristics. The optical power for 1.31-μm-wavelength CW light was varied. The dashed lines denote the load curves, for which R_s = 400 Ω is the experimental series resistance of the PhC-PD and $R = R_{load}$ (7 kΩ) + R_s (400 Ω) is for the resistor-loaded PhC-PD discussed in Fig. 5.

frequency of 10 GHz,[5] the p- and n-doped regions are closely attached to the absorber to obtain the strong internal built-in electric field. In the simulation, the internal field of >10 kV/cm is expected for a V_{bias} of +0.2 V, which will result in electron and hole drift velocities of $>10^7$ and $>10^6$ cm/s,[14] respectively. The carrier transit time will be limited by the hole velocity but will be <35 ps with the designed absorber width of 350 nm.

For the static-response measurements, a continuous-wave (CW) light at a wavelength of 1.31 μm was injected into a waveguide through a lensed fiber. The coupling loss between the fiber and the waveguide facet was approximately −9.5 dB, and this was used to estimate the on-chip optical power. The dark current was less than 500 pA for a bias voltage range of −1 to 0 V. Note that there is no dark current in a bias-free operation. The photocurrent (I_{pd}) for different optical powers (P_{opt}) was measured under a bias voltage (V_{bias}), as shown in Fig. 2(c). The optical responsivity was approximately η_{pd} = 0.88 A/W at a reverse voltage of −1 V, and this responsivity clearly remains constant for a forward voltage of up to +0.5 V in a photocurrent range of $I_{pd} < 70$ μA. This implies that the internal built-in field under these forward voltages still works for carrier extraction overcoming the carrier recombination loss. Our previous work reported the carrier recombination lifetime as slow as 7 ns for the InGaAsP-BH in InP-PhC slab,[15] which should lead to the efficient carrier collection in our PD. For a higher optical input power or higher forward voltage, the charge carriers that remain in the absorber may degrade the internal field due to the space charge effect, hence reducing the responsivity. This optical power and the incorporated load resistance limit the possible output voltage, as shown by the load curve in Fig. 2(b). The series resistance (400 Ω) of the present PD does not affect the operation because no significant voltage drop occurs. If we assume a termination with a high load resistance of 7 kΩ and a photocurrent of 30 μA, we can expect a voltage exceeding 0.2 V to be generated,

which corresponds to the above-threshold voltage for a CMOS field-effect transistor (FET).[2,16] The responsivity of our PhC-PD is not degraded for this photocurrent and forward voltage.

IV. DYNAMIC RESPONSE

A more important and challenging task is to achieve high-speed operation with such a forward voltage range. The quasi-impulse response and the random signal response were measured under different V_{bias} conditions. First, a short-pulse response measurement was performed by injecting a 2-ps-wide optical pulse, which was generated by a mode-locked fiber laser with a repetition rate of 10 MHz and a wavelength of 1.53 μm. Light at a wavelength longer than the bandgap can still be absorbed due to tailing in the absorption spectrum of InGaAsP, and here we adjusted the optical power to obtain a peak photocurrent of 30 μA. The output time response was observed by using a sampling oscilloscope with a bandwidth of 60 GHz. The time responses for different V_{bias} values were measured as shown in Fig. 3(a). A reference response (black) was obtained by using a commercial 70-GHz PD, giving a full-width at half maximum (FWHM) of 9.0 ps. Our PhC-PD exhibited a FWHM of 16.4 ps for V_{bias} = 0 V and maintained a value of 17.8 ps even for V_{bias} = +0.2 V. Figure 3(b) shows the 3-dB bandwidth (f_{total}), which was evaluated from the fast Fourier transform of the quasi-impulse response. The f_{total} for V_{bias} = 0 V and +0.2 V were 19 and 17 GHz, respectively. Since a bit rate of twice f_{total} is generally expected for a non-return-to zero (NRZ) signal format,[17,18] the capacity of nearly 40 Gbit/s can be expected. We measured the time response for a pseudo-random bit sequence (PRBS) optical signal with an NRZ format and a light wavelength of 1.31 μm, as shown in Fig. 4. To acquire the eye diagram, an NRZ optical signal with a $2^{11} - 1$ PRBS frame was repeatedly injected, and 128 frames were averaged to exclude the intrinsic electrical noise of the oscilloscope sampling head. Eye opening for a bit rate of 40 Gbit/s was observed for a forward bias voltage of up to +0.2 V as well as for a bit rate of 20 Gbit/s up to +0.4 V. Such a fast operation with a forward bias voltage has not previously been demonstrated for small waveguide PDs. Although the acceptable bit rate practically depends on the noise level when configuring the receiver circuit, this eye opening reveals the potential responsivity for the high-speed on-off keying format in the optical communication.

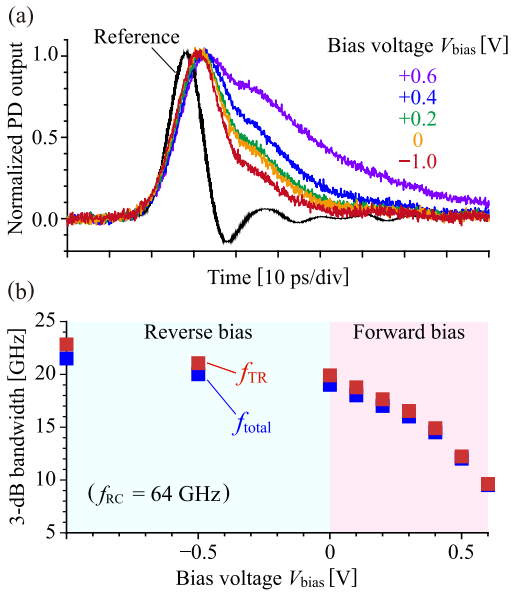

FIG. 3. Photo-response to 2-ps optical pulse. (a) Output electrical pulse under different bias voltages. The reference response (black) was obtained by detecting the input optical pulse with a 70-GHz photodetector. The light wavelength was 1.53 μm, and the input optical power was adjusted to generate a peak photocurrent of 30 μA. (b) 3-dB bandwidth versus bias voltage. The total bandwidth f_{total} (blue) was estimated from the FFT curve of the output pulse in (a). The bandwidth for the carrier transit time f_{TR} (red) was estimated from the RC bandwidth f_{RC} = 64 GHz and the total bandwidth $f_{total} = (f_{TR}{}^{-2} + f_{RC}{}^{-2})^{-1/2}$.

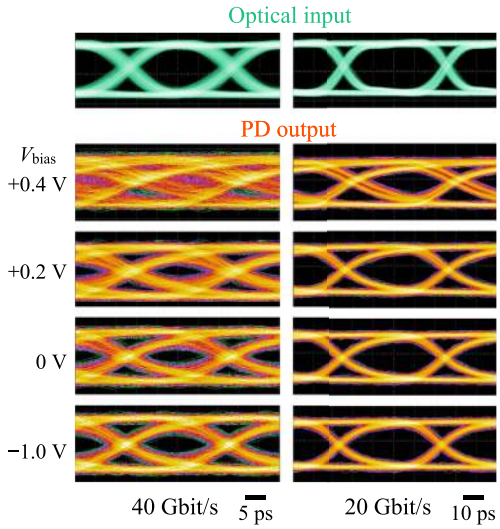

FIG. 4. Eye diagrams for different bias voltages. An NRZ optical signal with a $2^{11} - 1$ PRBS was repeatedly injected, and 128 frames were averaged. The signal bit rate was 20 Gbit/s (right) and 40 Gbit/s (left). The light wavelength was 1.31 μm, and the input optical power was adjusted to generate a peak photocurrent of 30 μA.

As well as the static photocurrent response, the dynamics observed here suggest that the optical absorption and the fast carrier extraction were maintained even when the built-in field weakened. This is thanks to the spatial matching of the narrow depletion region and the optical field which is strongly confined in the absorber, as suggested in Fig. 2(b). The total bandwidth f_{total}, which was experimentally observed in Fig. 3(b), must be limited by the bandwidth for the carrier-transit time f_{TR} and that for the RC time f_{RC}, as approximated by $f_{total} = (f_{TR}{}^{-2} + f_{RC}{}^{-2})^{-1/2}$.[19] Indeed, the quasi-impulse response shown in Fig. 3(a) exhibits a multiple decay slope. The RC bandwidth can be estimated as follows (see the supplementary material for details). The PD capacitance C_j and the parasitic capacitance of the electrical pad C_p, both of which include the fringing capacitance, were both estimated from 3-D FEM to be 5 fF. With a series resistance R_s of 400 Ω and a load resistance R_{load} of 50 Ω (of the sampling oscilloscope head), the calculated RC bandwidth was approximately $f_{RC} = \{2\pi[R_sC_j + R_{load}(C_j + C_p)]\}^{-1} = 64$ GHz. The transit-time bandwidth f_{TR} was estimated with this f_{RC} and the experimental f_{total} and is plotted in Fig. 3(b). f_{TR} is lower than f_{RC} over the experimental voltage range and hence dominates f_{total}. The internal field across the p-i-n junction is weakened under the forward voltage, as shown in Fig. 2(b). This decreases the carrier drift velocity, and especially the velocity of hole should limit the f_{TR} because it is much slower than that of electron. Indeed, the slow decay component in the quasi-impulse response in Fig. 3(a) becomes dominated under the forward voltage. This implies that the fast decay and slow decay indicate the photocurrents induced by the electron and hole, respectively. For example, UTC-PDs specifically adopt the complicated layer structure to prevent from the slow decay of hole and obtained the ultrafast bandwidth close to 100 GHz, with sacrifice of low responsivity (~0.2 A/W).[8,11] Our PD does not require such a complex layer, but exhibits the high responsivity (0.88 A/W) and high bit rate operation (40 Gbit/s), thanks to its concentration of the light, absorber, and depletion region in the narrow dimension, which would be particularly suited for on-chip receiver applications.

V. CIRCUIT ANALYSIS FOR RESISTOR-LOADED PD

Finally, we discuss the potential configuration of an amplifier-free bias-free PD. Figure 5(a) shows our proposed resistor-loaded PhC-PD without a bias circuit, by which an above-threshold gate voltage for a CMOS FET would be generated. The PD would be integrated with a CMOS layer through a three-dimensional via connection, which should be possible to realize with the InP-on-Si heterogeneous integration technique.[20] To overview the performance of this receiver, here we assumed a photocurrent of 30 μA and a load resistance of 7 kΩ, which would result in a transimpedance of

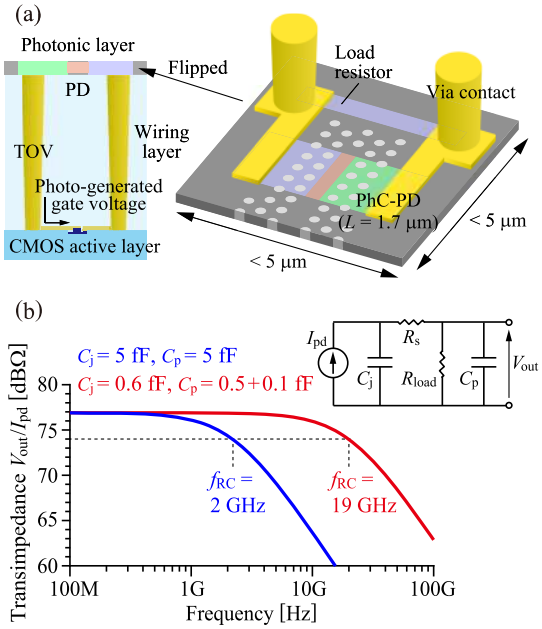

FIG. 5. A resistor-loaded bias-free photoreceiver. (a) Device schematic. A PhC-PD with a length of 1.7 μm is connected to a load resistor to generate an output voltage by which an integrated FET gate would be switched through 3-D integration. (b) The equivalent circuit and calculated trans-impedance V_{out}/I_{pd} of the receiver. As circuit parameters, the PD serial resistance (R_s = 400 Ω) and load resistance (R_{load} = 7 kΩ) are fixed, while two sets of PD capacitance and parasitic capacitance (C_j = 5 fF and C_p = 5 fF for the experimental condition, C_j = 0.6 fF and C_p = 0.5 + 0.1 fF for the expected condition with integrated PD) are assumed.

77 dB Ω. As shown in Fig. 1(b), the load curve for (7 + 0.4) kΩ allows us to keep the responsivity at a forward bias voltage of >0.2 V. Therefore, we can expect to generate an output voltage of around V_{out} = 30 μA × 7 kΩ = 0.21 V. Even under this condition, an f_{TR} of 18 GHz can be expected according to the dynamics in Fig. 3. We also simulated the expected total bandwidth limited by the f_{RC} for the equivalent circuit, as shown in Fig. 5(b). When we employ the device parameters used in the present experiment, namely, a device capacitance of C_j = 5 fF and a parasitic capacitance of C_p = 5 fF, we estimated the f_{RC} for the transimpedance (V_{out}/I_{pd}) to be 2 GHz. Although the present device has a length of 35 μm, the effective absorption length should actually be a few μm for upper-bandgap wavelengths. (In this experiment, λ = 1.31 μm was used when measuring the static response in Fig. 2 and the dynamic response in Fig. 4.) Actually, we have already demonstrated a much smaller PhC-PD with a length of only 1.7 μm and a high responsivity of 1 A/W,[5] for which the device capacitance can be as low as C_j = 0.6 fF. In addition, a fully integrated receiver is capable of exhibiting a parasitic capacitance of C_p = 0.5 fF, which counts a pair of through-oxide-via connections, which are assumed to have a radius of 1 μm, a height of 7 μm, and a separation of 5 μm.[21] We also include a transistor gate capacitance of 0.1 fF to assume a low-C Fin-FET.[22] These parameters support an f_{RC} of 19 GHz while maintaining the high transimpedance. The expected total bandwidth $f_{total} = (f_{TR}^{-2} + f_{RC}^{-2})^{-1/2}$ will still be >13 GHz, which is capable of a bit rate of >25 Gbit/s in the NRZ format. This will enable us to realize a receiver that does not require any electrical energy consumption but only an optical energy of E_{opt} = 0.21 V/7 kΩ/1 A/W/25 Gbit/s = 1.2 fJ/bit. This is much smaller than those for the conventional receiver with amplifiers consuming several hundred fJ/bit and the amplifier-free receiver with reverse bias (for example, −2 V) consuming 3.6 fJ/bit (1.2 fJ/bit for optical energy plus 1.2 × 2 = 2.4 fJ/bit for electrical energy). In addition, an ultrasmall footprint of less than 25 μm^2 is expected for this receiver, as shown in Fig. 5(a). This is also much smaller than that reported for a Ge-waveguide PD integrated with a CMOS amplifier circuit, which occupies >10^4 μm^2.[2,23] Thanks to the high load resistance, the low thermal noise should be also expected for the high signal-to-noise ratio.[10] Consequently, these analyses reveal that our PhC-PD promises the ultimately low energy consumption as a nanophotonic receiver and

encourage us to experimentally demonstrate by actually terminating the PD with kΩ-level load resistance.

VI. SUMMARY

We demonstrated the highly efficient and fast operation of a forward-biased PhC-waveguide PD and discussed a way to realize an amplifier-free bias-free receiver. In the experiment, a static responsivity of 0.88 A/W was maintained up to a bias voltage V_{bias} of +0.5 V, and the operation dynamics at bit rates of 40 and 20 Gbit/s were observed for V_{bias} values of +0.2 and +0.4 V, respectively. Such a high-speed operation with a forward voltage for small waveguide PD was demonstrated for the first time. Through the circuit simulation, we showed that our PhC-PD can expect efficient voltage generation (>0.2 V) with a high bit rate of >25 Gbit/s when implementing the resistor-loaded photoreceiver with an ultralow capacitance (<1 fF) PhC-PD. Such a receiver will not need to consume any of the electrical energy normally consumed by amplifiers and bias sources and only requires an optical energy of about 1 fJ/bit. This operation cannot be expected at present for the ultrasmall plasmonic PDs[24] because they basically have a low responsivity of 0.1 A/W or less, require the external bias to extract carriers, and the narrow metal slit induces the higher capacitance. The ultralow energy consumption and the anticipated compact footprint of $<5 \times 5\ \mu\mathrm{m}^2$ for our receiver design are attractive as regards dense device integration. These features offer an ultra-compact amplifier-free bias-free receiver that cannot be realized with other PDs and enable us to realize an unprecedented form of the integrable receiver for use in dense nanophotonic communication and processing.

SUPPLEMENTARY MATERIAL

See supplementary material for the theoretical bandwidth of the PD equivalent circuit.

ACKNOWLEDGMENTS

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