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FPGA-BASED CHIRP GENERATOR FOR HIGH RESOLUTION UAV SAR

M. Y. Chua and V. C. Koo

Faculty of Engineering and Technology
Multimedia University
Jalan Ayer Keroh Lama, Melaka 75450, Malaysia

Abstract—This paper discusses the design and development of a FPGA-based chirp generator for high resolution Unmanned Aerial Vehicle (UAV) Synthetic Aperture Radar. The desired bandwidth of the chirp signal is 100 MHz (combination of I and Q channels) with a chirp rate of 5 MHz/μs. Two algorithms based on the Memory-based architecture and the Direct Digital Synthesizer (DDS) architecture are presented. The measurement results indicate that the DDS chirp generator is a preferred choice for high-resolution SAR application.

1. INTRODUCTION

Radar is a common tool used in many applications such as imaging, missile guidance, remote sensing and global positioning [1]. The Synthetic Aperture Radar (SAR) was first proposed by Carl Wiley in 1951 [2] which described the use of Doppler frequency analysis to improve radar image resolution. SAR has been proven to be very useful over wide ranges of applications, including high resolution geological and topological mapping, snow monitoring, military surveillance, and classification of earth terrain [3, 4].

An Unmanned Aerial Vehicle (UAV) is an aircraft that is capable of operating without the presence of pilot or crew in the aircraft's cabin. It can be found extensively in the area of reconnaissance and surveillance as well as military purposes [5]. In recent years, the usage of UAV in research area is rapidly growth and it has become an alternative platform for SAR. As compared to conventional airborne or space-borne SAR systems, UAV-based SAR system has lower operation cost, lower risk, and suitable for *in-situ* measurement where frequent revisit is required.

Corresponding author: M. Y. Chua (mychua1221@gmail.com).

Table 1. UAV SAR system specifications.

System Parameters	Specifications
Mode of Operation	Stripmap
Operating Frequency	5.3 GHz (C-band)
Bandwidth	80 MHz
Polarization	Single, VV
Spatial Resolution	5 m × 5 m
Nominal Platform Speed	30 m/s
Payload Weight	< 25 kg
Allowable Working Space	$12'' \times 12'' \times 12''$
Operating Platform	UAV, Aludra MK1 (UST)

A new UAV SAR has been designed by Multimedia University, in collaboration with Malaysian Remote Sensing Agency (ARSM). The system specifications of the UAV SAR system are summarized in Table 1.

Due to the limited working space and payload capacity of the UAV, the SAR sensor must be very compact and small in size. In particular, there is no room to mount instruments such as signal generator and workstation onto the UAV platform. In this paper, the design and development of a miniature, single-board chirp signal generator using Field Programmable Gate Array (FPGA) is presented. It is capable of generating high performance chirp signal and has the flexibility to reconfigure its parameters on-the-fly.

2. THE CHIRP SIGNAL

A *chirp* signal is usually referred as linear FM signal (LFM) and it has an interesting characteristic of possessing very large time bandwidth product [6]. In time domain, an ideal linear FM pulsed signal, $x(t)$, is given by,

$$x(t) = \text{rect}\left(\frac{t}{T}\right) Ae^{j\pi\beta t^2} \tag{1}$$

where,

A = amplitude

T = pulse duration

t = time variable in seconds

β = LFM rate or chirp rate in hertz per second

The phase of the LFM signal is given by the argument of the exponential expressed in radians,

$$\phi(t) = \pi\beta t^2 \tag{2}$$

While the instantaneous frequency is the derivative of Equation (2) with respect to time,

$$f(t) = \frac{1}{2\pi}\frac{d\phi(t)}{dt} = \frac{1}{2\pi}\frac{d\left(\pi\beta t^2\right)}{dt} = \beta t \tag{3}$$

In SAR system, chirp is usually modulated over a specific range of frequency BW, within short pulse duration of T, and the pulse is transmitted in an interval of PRI (Pulse Repetition Interval). Figure 1 shows an example of chirp pulse. Alternatively, the signal can also be expressed in sine and cosine terms. Using the Euler's theorem, Equation (1) can be expressed as,

$$x(t) = \text{rect}\left(\frac{t}{T}\right)\left[\cos\left(\pi\beta t^2\right) + j\sin\left(\pi\beta t^2\right)\right] \tag{4}$$

The most important characteristics of LFM waveform is its correlation property. When a LFM chirp signal correlates with itself, it will produce a result with a sinc function. A SAR receiver can beneficiate this property by using a pulse-matched filter to pass reflected pulses that match the pattern of the outgoing pulse and to reject noise and other signals. The ratio of the transmitted pulse duration to the duration of the compressed pulse, known as pulse compression ratio, is equal to $BW \cdot T$. Figure 2(a) shows the uncompressed LFM signal and Figure 2(b) shows the auto-correlated LFM signal.

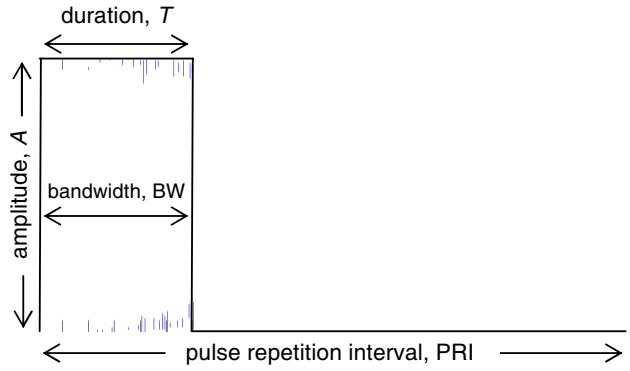
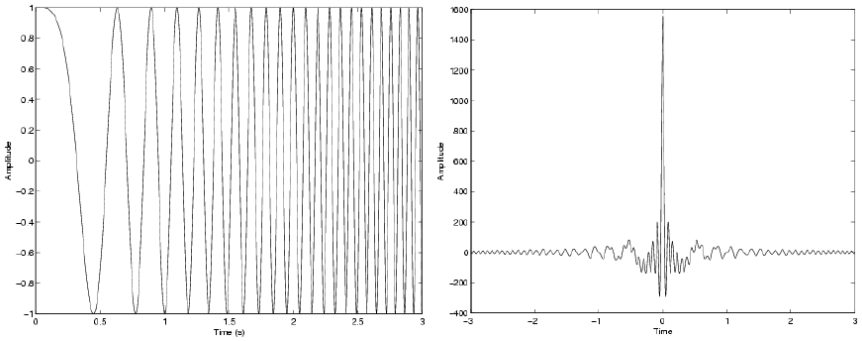


Figure 1. Time domain signal for a LFM chirp signal.



(a) (b)

Figure 2. An (a) uncompressed and (b) compressed LFM chirp.

Table 2. Analog chirp generator vs. Digital chirp generator [6].

System Performance	Analog CG	Digital CG
FM noise	Good	Good
Frequency response	Good	Excellent
Linearity	Good	Excellent
Microphonics	Poor	Excellent
$N + 1$ compatibility	Degrade performance	Excellent
Spurious	Minimum filtering	Requires filtering
Complexity	Low	Moderate to high
Digital compatible	No	Yes

Several techniques to generate the chirp signal have been proposed over the past few decades. Generally, the techniques can be categorized into analog approach and digital approach. In analog chirp generator, a voltage controlled oscillator (VCO) is used to generate the chirp signal [7]. Up-chirp and down-chirp signal can be generated by applying linear ramp-up and ramp-down voltage signal to the VCO. However, due to several limitations of VCO, such as large response or settling time and non-linearity of VCO, digital approach has slowly takes the role as the chirp generator for SAR systems. Table 2 summarizes the advantages and disadvantages of digital signal generator over analog signal generator.

Unlike analog chirp generator, the property of the digitally generated waveform (type of modulation, start and stop frequency, waveform output duration) can be configured easily by changing the

firmware and memory contents of the digital generator. Table 3 summarizes the specifications of various chirp generators used in existing SAR sensors [8–12].

In terms of implementation scheme, digital chirp signal generator can be realized using digital electronics or field programmable gate array (FPGA). In digital electronics, the chirp generator is built from various integrated circuits (IC) which may comprises of counter ICs, memory ICs, controller and DAC. In an alternate approach, rather than using various kinds of ICs, the digital portion of chirp generator is built in a single IC. The FPGA is a semiconductor device containing programmable logic components and programmable interconnects.

Table 3. The specifications of various chirp generators in worldwide SAR system.

SAR System	Microwave Band	Bandwidth (BW)	Pulse Duration (T)	Data Format
AIRSAR (NASA)	P-band	20/40 MHz	10 or 5 μs	8-bit
	L-band	20/40 MHz	10 or 5 μs	8-bit
	C-band	20/40 MHz	10 or 5 μs	8-bit
SAR (ERS)	C-band (5.3 GHz)	15.55 MHz	37.1 μs	8-bit
SASARII	X-band	50 MHz (I & Q each)	3–5 μs	8-bit
CCRS	C-band	26.3 MHz (I channel) 8.3 MHz (Q channel)	7 μs (I channel) 8 μs (Q channel)	8-bit
	X-band	31.2 MHz (I channel) 7.5 MHz (Q channel)	15 μs (I channel) 30 μs (Q channel)	8-bit
JERS-1	L-band	15 MHz	35 μs	3-bit
SIR	L-band	40 MHz	33.8, 16.9, 8.5 μs	8,4 bits/word
	C-band	40 MHz	33.8, 16.9, 8.5 μs	8,4 bits/word
	X-band	10 & 20 MHz	33.8, 16.9, 8.5 μs	8,4 bits/word

Table 4. Chirp specifications for UAV SAR.

Parameters	Value
Bandwidth	50 MHz (I channel) 50 MHz (Q channel)
Pulse duration	10 μs
Data-format	14-bit
Number of channel	2 (I & Q)
Pulse Repetition Interval	1 ms

The firmware of FPGA is a combination of hardware interconnects which wire-up the programmable logics together to perform complex combinational functions (counter, multiplexer and decoder, memory) or merely simple logic gates such as AND, OR and NOT.

Two of the most popular digital chirp generator architectures are the Memory-based architecture and Direct Digital Synthesizer (DDS) architecture. Following sections describes the design and development of a digital chirp generator using both the architectures. The chirp generator is built using the Altera STRATIX III FPGA. The specifications of the proposed chirp signal are summarized in Table 4.

3. MEMORY-BASED CHIRP GENERATOR (CG) DESIGN

Memory-based CG is the simplest type of digital chirp generator architecture. Figure 3 shows the functional block diagram of the memory-based CG. It consists of a binary counter, a memory block (ROM), a DAC driver, a phase lock loop (PLL), a DAC module, and a reconstruction filter. The CG works by retrieving a pre-stored data (pre-calculated amplitude level of the signal) in a memory device such as ROM or PROM.

The CG design is divided into two stages; simulation stage and FPGA firmware design stage. In simulation stage, a linear FM signal is simulated in Matlab® using the parameters shown in Table 5. The simulated waveform in time domain is then converted to a set of digital data format which is used as the initial state of the memory elements during the FPGA firmware development stage. Figure 4 shows the simulated LFM chirp signal with bandwidth of 50 MHz while Figure 5 shows the signal spectrum. The binary counter starts to count from 'zero' until the pre-defined 'stop' value once a PRF signal is detected. The binary counter's output is used as the address of the memory block

which points to the current location of memory element. The output data from the digital circuitry (in digital domain) is then converted to analog signal. The DAC module is capable to deliver 14-bit data format with data throughput of 250 MSps. A reconstruction filter (typically a low pass filter) is used to construct a smooth analog signal from the output of the DAC module.

The digital circuitry (binary counter, memory block, DAC driver and PLL) are designed and synthesized by the Altera Quartus II software. All of the digital circuitry shares a common clock signal from PLL. The PLL acts as a clock frequency multiplier by multiplying the on-board 125 MHz oscillator clock signal to 250 MHz.

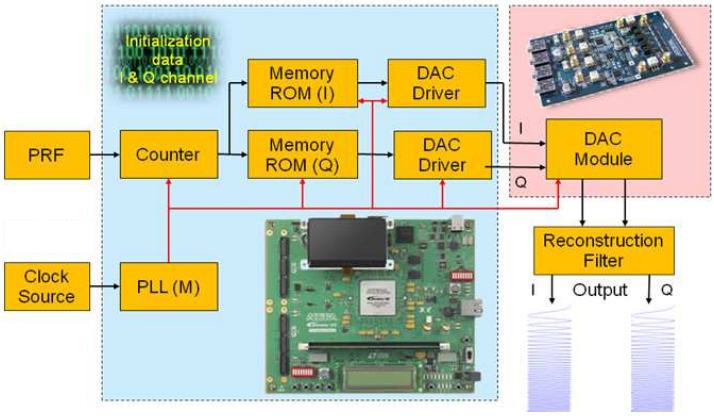


Figure 3. Functional block diagram of the memory-based CG design.

Table 5. Parameter used to simulate the linear FM chirp signal in MATLAB®.

Parameter	Value
Sampling frequency	250 MHz
Sampling interval	4 ns
Total sample point	2500
Chirp bandwidth	50 MHz
Chirp duration	10 μs
Chirp slope	5 MHz/μs
Data bit resolution	14

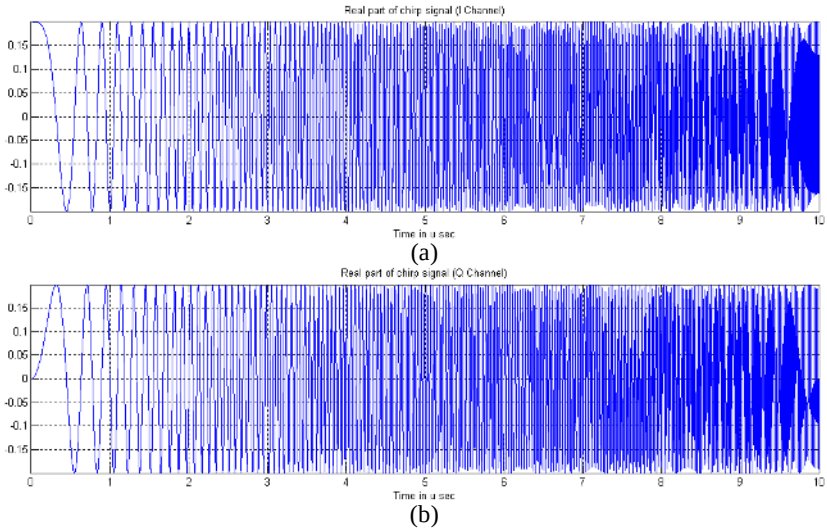


Figure 4. Simulated 50 MHz linear FM chirp signal generated using memory-based architecture. (a) I channel (b) Q channel.

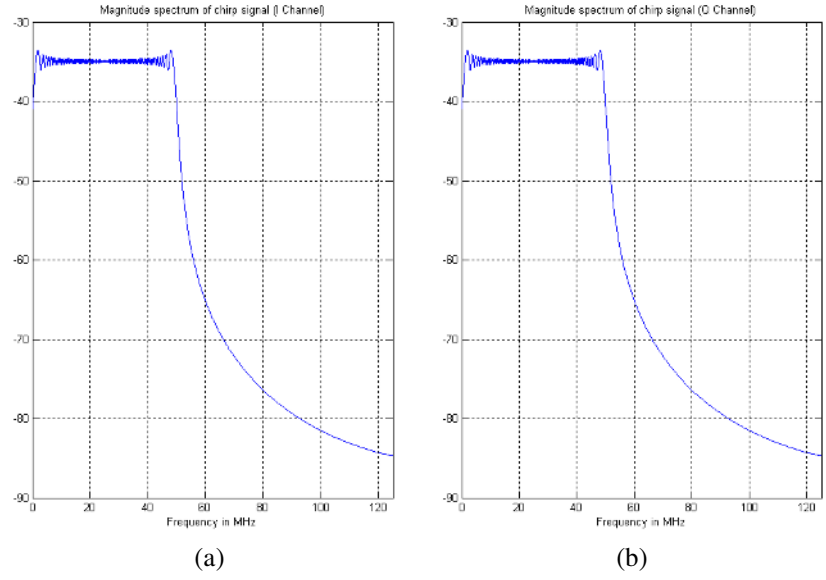


Figure 5. Simulated 50 MHz linear FM chirp signal spectrum using memory-based architecture. (a) I channel (b) Q channel.

4. DIRECT DIGITAL SYNTHESIZER (DDS) CHIRP GENERATOR (CG) DESIGN

An alternate architecture in digital chirp generator is the Direct Digital Synthesis (DDS) architecture. It is a method of producing an analog waveform, usually a sinusoid, by generating a time-varying signal in digital form and then performing a digital-to-analog conversion. DDS offers fast switching between output frequencies, fine frequency resolution, and operation over a broad spectrum of frequencies.

The simplest form of a DDS can be implemented as shown in Figure 6. It consists of a precision reference clock source (f_c), an address counter, a programmable read only memory (PROM) block, and a D/A converter [13]. The digital amplitude information of a complete cycle of a sinusoid is stored in the PROM. The address counter will steps through each of the PROM's memory location and retrieve the contents of the memory. The retrieved memory location contents are sent to a DAC and a corresponding sinusoid is generated.

The output frequency of this DDS implementation is only dependent on the frequency of the reference clock, f_c, and the sine-

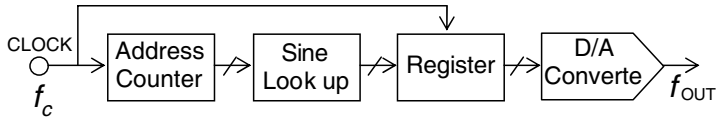


Figure 6. Simple direct digital synthesizer.

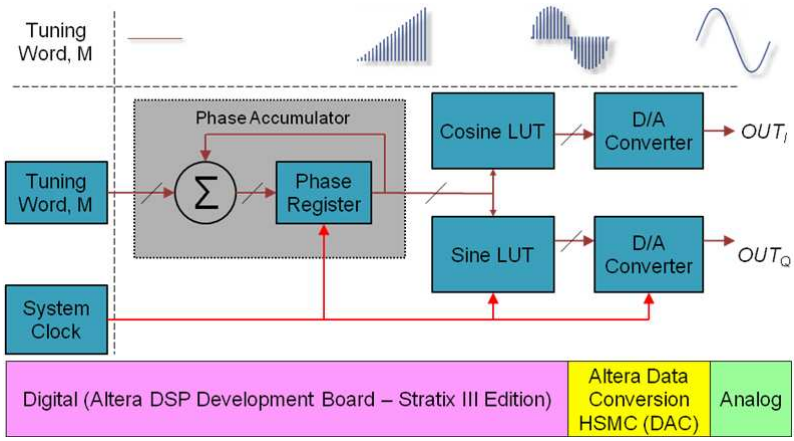


Figure 7. General block diagram of the DDS CG design.

wave step size (2^n) that is programmed into the PROM. The output frequency generated by the simple DDS can be formulated as,

$$f_{\text{OUT}} = \frac{f_c}{2^n} \tag{5}$$

where,

f_{OUT} = output frequency of the DDS
f_c = internal reference clock
n = length of the phase accumulator, in bits

In order to change the frequency, amplitude or phase of the output signal, the PROM content has to be re-programmed with the correct data set. An enhanced version of DDS is developed to introduce a phase accumulator block into the digital signal chain, enables tuning capability of DDS.

Figure 7 shows the proposed DDS CG architecture. It consists of a phase accumulator block, two LUTs namely the Cosine LUT (I channel) and Sine LUT (Q channel), and a two-channel DAC. The phase accumulator block possesses the carry function that allows accumulator to function as a "phase wheel".

The working principle of the DDS is based on the phase-frequency relationship in a sinusoidal signal [14]. A complete sine-wave oscillation can be visualizes as a rotating vector that rotates around a phase circle from 0° to 360° as shown in Figure 8. When the rotating vector is rotating at a constant speed, the linear phase information of a sine-wave is produced. Since the output frequency is a function of the number of steps to be taken to complete a wheel cycle, the number

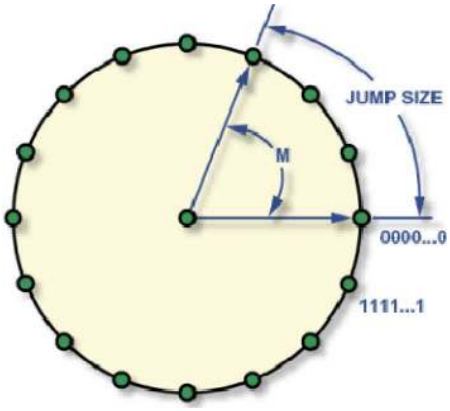


Figure 8. Digital phase wheel.

of discrete phase points contained in the wheel is determined by the resolution, n, of the phase accumulator.

The phase accumulator is a modulus 2^n counter that increments its stored number each time it receives a clock pulse. The magnitude of the increment is determined by a digital tuning word, M, that is summed with the overflow of the counter. The tuning word forms the phase step size between reference clock updates. The larger the step size, the faster the phase accumulator overflows and completes it's equivalent of a sine-wave cycle. The relationship of the phase accumulator and tuning word forms the basic tuning equation for DDS architecture. Changes to the value of M in the DDS architecture result in immediate and phase-continuous changes in the output frequency. Thus, the output frequency of the DDS can be determined by Equation (6) as shown below.

$$f_{\text{OUT}} = \frac{M \times f_c}{2^n} \tag{6}$$

where,

f_{OUT} = output frequency of the DDS

M = binary tuning word

f_c = internal reference clock

2^n = length of the phase accumulator

The Nyquist theorem dictates that there is a minimum of two samples per cycle is required to reconstruct the desired output waveform. Thus, the maximum output frequency of the DDS is determined by dividing the length of the phase accumulator by two, which is,

$$f_{\max} = 2^{n-1} \tag{7}$$

Substituting Equation (3) into DDS output frequency Equation (6) constitutes Equation (8) which can be used to generate the DDS tuning word for generating a LFM chirp signal.

$$M = \text{rect}\left[\frac{t}{T}\right] \frac{\beta t \times 2^n}{f_c} \tag{8}$$

where,

M = DDS binary tuning word

T = chirp duration

β = chirp slope

The output of the phase accumulator is linear and cannot directly be used to generate a sine-wave or any other waveform except a ramp. Therefore, a phase-to amplitude lookup table is used to convert the

phase accumulator's instantaneous output value into the sine-wave amplitude information that is presented to the D/A converter.

The same set of parameters in Table 5 is used to simulate the output of a DDS-based CG. The simulated output of the DDS is presented in Figures 9 and 10. Figure 9(a) shows the input tuning word of the DDS generated using Equation (8) and the output signal of the DDS is shown in Figure 9(b). Figure 10 shows the spectrum of the simulated output in frequency domain.

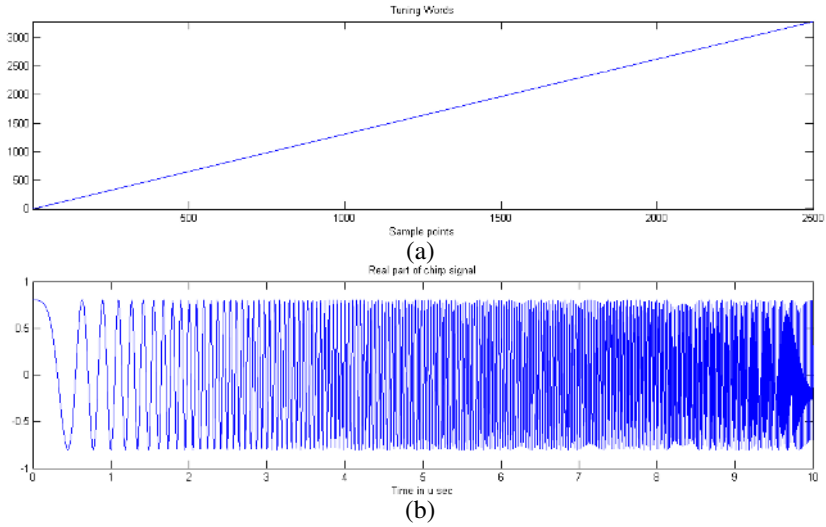


Figure 9. Simulated 50 MHz linear FM chirp signal generated using DDS architecture. (a) Linear tuning word. (b) Generated output waveform.

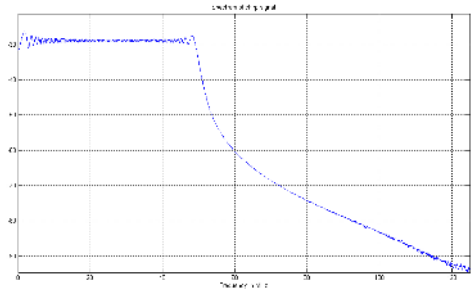


Figure 10. Simulated 50 MHz linear FM chirp signal spectrum using DDS architecture.

5. MEASUREMENTS AND VERIFICATIONS

This section presents the simulated and measured signal generated by both the Memory-based algorithm and DDS algorithm. For both the

Table 6. Waveform generated by the chirp generator.

	Single Tone Sinusoid	LFM
Frequency	1 MHz	0 to 50 MHz sweep
Amplitude	$+V_{ref}$ to $-V_{ref}$	$+V_{ref}$ to $-V_{ref}$
Duration	-	10 µs

Table 7. Recorded waveform and spectrum.

Architecture	Measured Signal	Type of Measurement	Figure
Memory-based	1 MHz single tone	Time-domain waveform	11
		I channel spectrum	12(a)
		Q channel spectrum	12(b)
	50 MHz Chirp	Time-domain waveform	13
		I channel spectrum	14(a)
		Q channel spectrum	14(b)
DDS	1 MHz single tone	Time-domain waveform	15
		I channel spectrum	16(a)
		Q channel spectrum	16(b)
	50 MHz Chirp	Time-domain waveform	17
		I channel spectrum	18(a)
		Q channel spectrum	18(b)

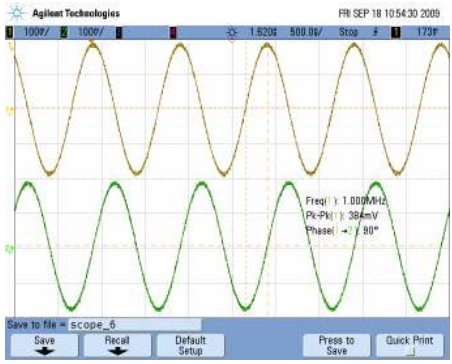


Figure 11. Measured 1 MHz single tone signal generated using memory-based architecture. (I signal at channel 1 and Q signal at channel 2).

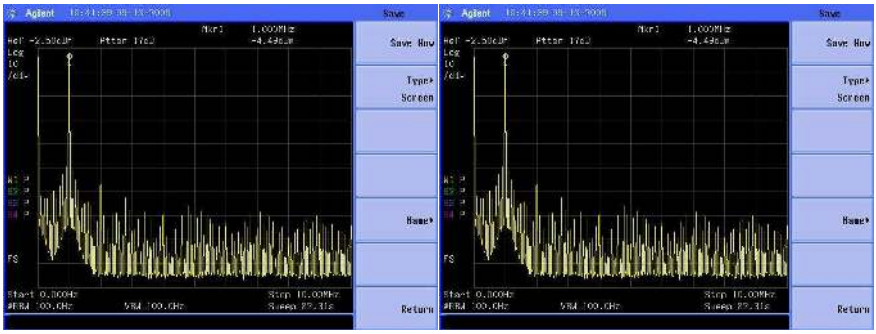
architectures, the FPGA firmware is configured to output the signals as listed in Table 6. The generated signal is recorded using a mixed signal oscilloscope while the spectrum is observed using a spectrum analyzer. Table 7 summarizes the recorded generated signal.

Table 8 lists the measured signal parameter for Figure 11 to Figure 18. The measured phase difference for the single tone signal generated by both the memory-based and DDS architecture are 90° phase apart as shown in Figure 11 and Figure 15. The spectrum of single tone signal generated using memory-based architecture shows many spurious harmonics in noise floor level while there is only one spurious harmonic in the signal generated using DDS architecture. The high spurs power level from carrier is −52.5 dB for memory-based architecture and −63.4 dB for DDS architecture.

For the chirp signal, both the architecture has flat passband response from 0 to 50 MHz as shown in Figure 14 and Figure 18.

Table 8. Measured signal parameters.

Architecture	Measured Signal	Signal Channel	Measured Signal Parameter	Measured Value
Memory -based	1 MHz single tone	I	Frequency	1 MHz
			Signal power level	–4.5 dBm
			Highest spur	–57.0 dBm
		Q	Frequency	1 MHz
			Signal power level	–4.7 dBm
			Highest spur	–48.0 dBm
		I & Q	I & Q Phase Difference	90°
	50 MHz Chirp	I	Passband power level	–31.2 dBm
			Power level @ 80 MHz	–52.0 dBm
			Power level @ 90 MHz	–54.0 dBm
		Q	Passband power level	–31.0 dBm
			Power level @ 80 MHz	–60.0 dBm
			Power level @ 90 MHz	–62.0 dBm
DDS	1 MHz single tone	I	Frequency	1 MHz
			Signal power level	–4.6 dBm
			Highest spur	–68.0 dBm
		Q	Frequency	1 MHz
			Signal power level	–4.9 dBm
			Highest spur	–68.0 dBm
		I & Q	I & Q Phase Difference	90°
	50 MHz Chirp	I	Passband frequency	0 to 50 MHz
			Passband power level	–31.6 dBm
			Power level @ 80 MHz	–63.0 dBm
			Power level @ 90 MHz	–75.0 dBm
			Power level @ 100 MHz	–79.0 dBm
		Q	Passband frequency	0 to 50 MHz
			Passband power level	–31.9 dBm
			Power level @ 80 MHz	–64.0 dBm
			Power level @ 90 MHz	–75.0 dBm
			Power level @ 100 MHz	–77.0 dBm



(a) (b)

Figure 12. Measured 1 MHz single tone signal spectrum using memory-based architecture. (a) I signal, (b) Q signal.

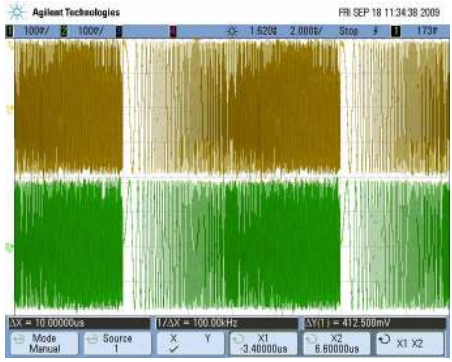
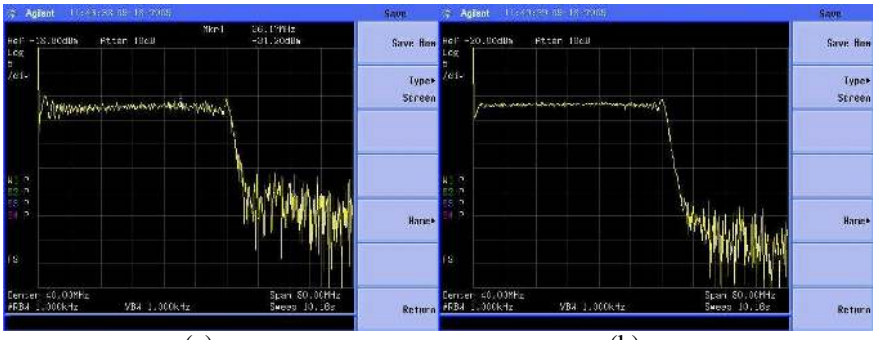


Figure 13. Measured 50 MHz chirp signal generated using memory-based architecture. (I signal at channel 1 and Q signal at channel 2).



(a) (b)

Figure 14. Measured 50 MHz linear FM chirp signal spectrum generated using memory-based architecture. (a) I signal, (b) Q signal.

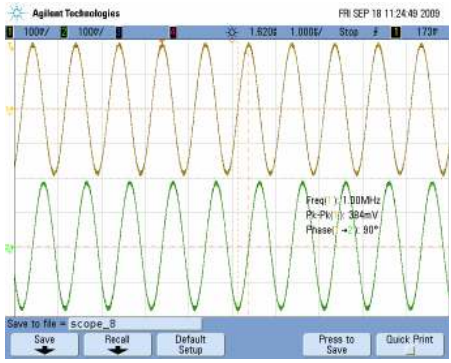
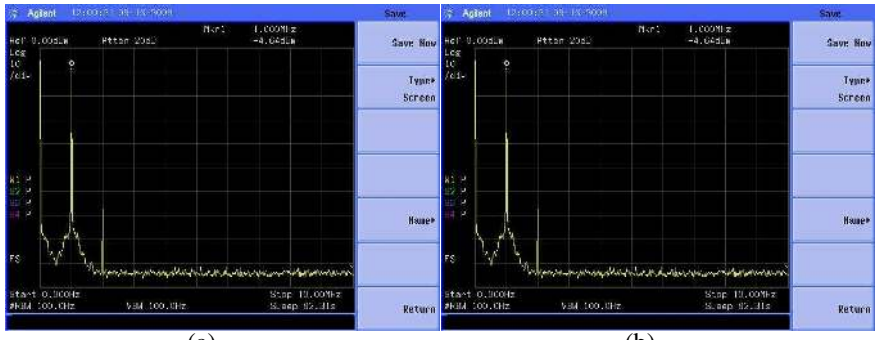


Figure 15. Measured 1 MHz single tone signal generated using DDS architecture. (I signal at channel 1 and Q signal at channel 2).



(a) (b)

Figure 16. Measured 1 MHz single tone signal spectrum using DDS architecture. (a) I signal, (b) Q signal.

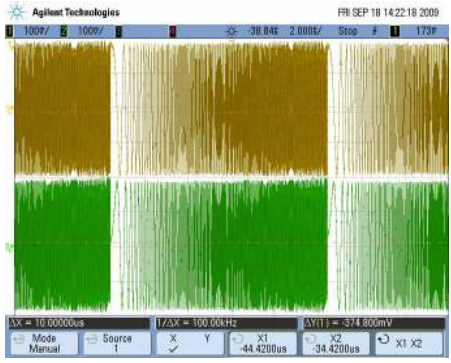
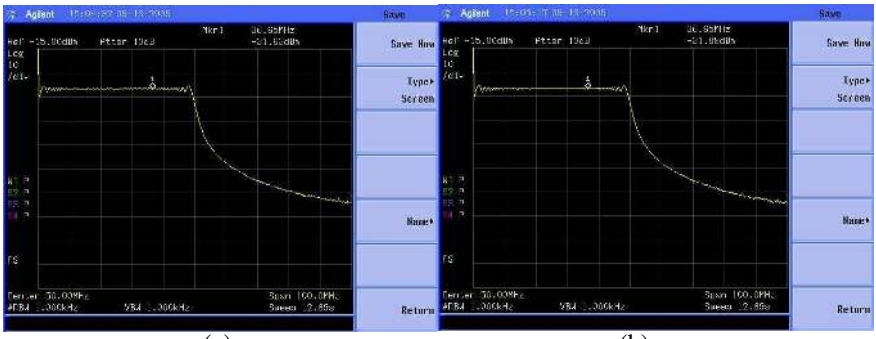


Figure 17. Measured 50 MHz chirp signal generated using DDS architecture. (I signal at channel 1 and Q signal at channel 2).



(a) (b)

Figure 18. Measured 50 MHz linear FM chirp signal spectrum generated using DDS architecture. (a) I signal, (b) Q signal.

The spectrum of the chirp signal generated using memory-based architecture contains many harmonics and spurs after the passband while for DDS architecture, harmonics and spurs are non-noticeable in the spectrum. Other than that, signal generated using DDS architecture has lower level of spurs as compared to the signal generated using memory-based architecture.

6. CONCLUSION

A chirp generator for high resolution SAR based on Altera Stratix III FPGA has been developed. Both the memory-based and DDS architectures have been synthesized and implemented on the FPGA platform. The measurement results show excellent purity of synthesized waveform by the DDS architecture.

ACKNOWLEDGMENT

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