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Paper

FPGA Controller Design for High-Frequency LLC Resonant Converters

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Conventional digital controllers have limited switching-frequency resolution and computational speed. This results in a large output voltage ripple and poor dynamic performance with a low control bandwidth in high switching frequency resonant converters using an inductor-inductor-capacitor (LLC)-type resonant tank. This paper proposed a controller design based on a field programmable gate array (FPGA) for an LLC resonant converter to improve the switching-frequency resolution and dynamic performance. The improved performance is analyzed using theoretical methods compared with that of a general-purpose digital signal processor (DSP). The performance improvement is verified through circuit simulations and signal-level tests using a hardware-in-the-loop (HIL) test system.

Keywords: LLC resonant converter, Digital Signal Processor (DSP), field programmable gate array (FPGA), dynamic performance

1. Introduction

Nowadays, several industrial fields, such as UHD TVs, computer adapters, home appliances, and other consumer electronics require power converters with high power density and high power quality to miniaturize products without any performance degradation [(1)–(4)]. The high switching frequency operation can improve the power density of the switch mode power supply (SMPS). In terms of controller, the DSP is widely used to implement power converters for various industrial fields, since it has high noise immunity, an ability to implement complex control techniques, and a less susceptibility from environmental conditions compared with analog controllers. However, the DSPs have limited switching frequency resolution to regulate the power converter. It causes large output voltage ripple and primary- and secondary-side current variations at high switching frequency operation [(5)]. In addition, the high switching frequency can increase the crossover frequency of the loop gain, which induces fast dynamic performance. However, the limited computational speed increases the time delay of the high frequency switching, which degrades the dynamic performance of the LLC resonant converter [(6)–(8)].

In previous work, several control methods have been proposed to overcome the limited switching frequency resolution [(9)(10)]. It can improve the output voltage regulation performance with the control algorithm. However, they could not improve the dynamic performance because of the limited computation speed of the controller. In terms of dynamic performance, the control methods have been proposed to improve the dynamic performance and the stability [(6)–(8)]. They were analyzed the dynamic performance according to the time delay effect. In addition, the control algorithm was introduced to improve the dynamic performance. However, they could not overcome the limited switching frequency resolution. Therefore, the solution is necessary to obtain the tight output voltage regulation and fast dynamic performance for the high switching frequency converter.

The previous control methods cannot overcome both the limited PWM resolution and dynamic performance at the same time. In this paper, the FPGA controller is developed to improve both the switching frequency resolution and dynamic performance compared with the conventional DSP. The FPGA controller utilizes its fast computation and intrinsic parallelism. In addition, it has flexibility of bit width to optimize the digital computation. The PWM resolution is analyzed with the time step of each controller. In addition, the stability and dynamic performance is analyzed with the small signal analysis with the calculated computation speed of each controller. The performance of each controller is verified with the signal-level tests through the PSIM simulation and controller hardware-in-the-loop (CHIL) test system.

2. Performance Improvement of FPGA Controller

The LLC resonant converter with a feedback controller is shown in Fig. 1, which is composed of a primary half bridge structure, a transformer, the LLC resonant tank, and a digital controller [(11)].

2.1 Enhancement of Switching Frequency Resolution The general-purpose DSP (TI TMS320F28335) and the proposed FPGA (Xilinx XC7A100T) controller have 150 MHz and 450 MHz clock frequency, respectively. Figure 2 shows the operational principle to generate the gate signals. The clock speed determines the time step used to

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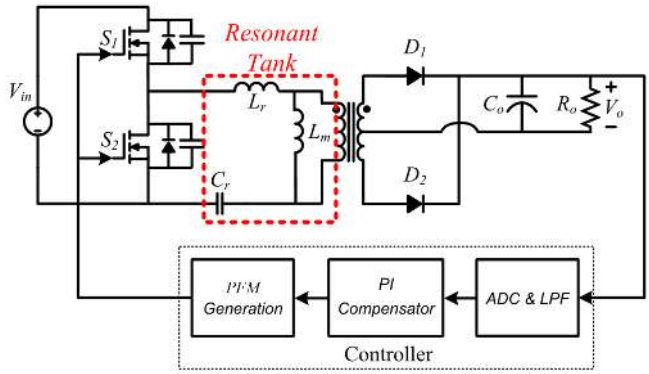


Fig. 1. Scheme of LLC resonant converter with a feedback controller

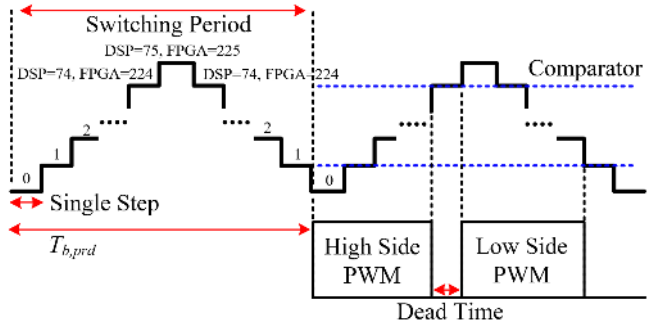


Fig. 2. Principle of gate signal generation

generate the triangular waveform that implements the pulse frequency modulation (PFM) gate signals. The time steps can be calculated as follows [9]:

$$T_{b,prd} = \frac{T_s}{2T_{tb,clk}} \cdots\cdots (1)$$

where $T_{b,prd}$ is the number of time steps, T_s is the switching period, and $T_{tb,clk}$ is the period of the system clock. $T_{b,prd}$ determines the switching frequency resolution according to a single bit change in control variables. The switching frequency resolution can be calculated as follows [9]:

$$\Delta f_s = \frac{1}{2T_{tb,clk}}\left(\frac{1}{T'_{b,prd}} - \frac{1}{T_{b,prd}}\right) \cdots\cdots (2)$$

The controller has limitations in terms of the PWM resolution and the computation speed as the increment of the switching frequency. The 1 MHz switching frequency is selected to verify the performance limitation of the controller. From (1) and (2), the DSP controller has 75 $T_{b,prd}$ steps and 13.158 kHz switching frequency resolution at 1 MHz switching frequency. The FPGA controller has 225 $T_{b,prd}$ steps and 2.2 kHz frequency resolution. From (1), the input-output voltage gain variation can be derived in terms of $T_{b,prd}$ as follows:

$$G\left(\Delta T_{b,prd}\right) = \left\| H_r\left(\frac{T'^{-1}_{b,prd}}{2T_{tb,clk}f_r}\right) - H_r\left(\frac{T'^{-1}_{b,prd}}{2T_{tb,clk}f_r}\right)\right\| \cdots\cdots (3)$$

where H_r is the voltage gain of the LLC resonant converter and f_r is the resonant frequency. From (3), when the input and output voltages are 400 V and 20 V, the output voltage resolutions of the LLC resonant converter using the DSP

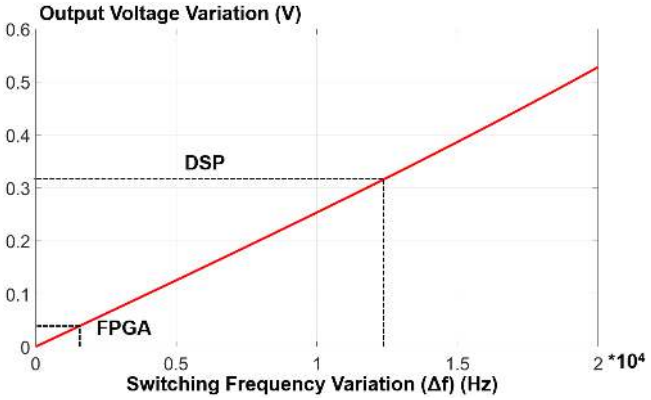


Fig. 3. Output voltage variation according to switching frequency variation

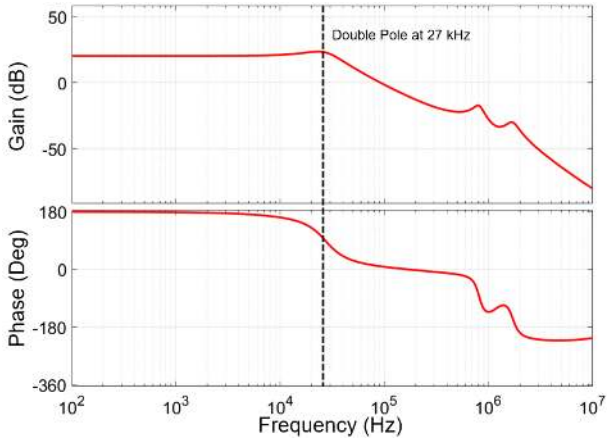
and FPGA controllers are 200 mV and 13.4 mV, respectively. They are larger than the sampling resolution, 4.88 mV, of the 12 bit ADC which are used in the controllers. Having lower output voltage resolution than the ADC sampling resolution induces high steady state error in the output voltage regulation. The controller frequently changes the switching frequency to compensate the error, which generates large output voltage ripple and primary- and secondary-side current fluctuation. However, the FPGA controller has 15 times smaller output voltage variation than that of the DSP controller, which induces the primary- and secondary-side current variations. Figure 3 shows the output voltage variation according to the limited switching frequency resolution. Therefore, the FPGA has tight output voltage regulation performance compared with the DSP.

2.2 Enhancement of Dynamic Performance The LLC resonant converter operating at high switching frequency has a high crossover frequency in the open loop transfer function due to the high resonant frequency and small output capacitance [12][13]. An ideal digital controller completes all the computation processes and updates the switching frequency within a single switching period [14]. However, with a typical digital controller is difficult to achieve the cycle-by-cycle control at high switching frequency due to its limited computational speed. The DSP controller using a PI compensator requires 14 μs time delay (= 72 kHz delayed frequency, f_d) to complete a single control process. On the other hand, the proposed FPGA controller requires 1 μs delay for the computation and another 1 μs delay for analog-to-data conversion from the integrated ADC (= 500 kHz delayed frequency). The transfer function of the time delay can be derived as follows [6]:

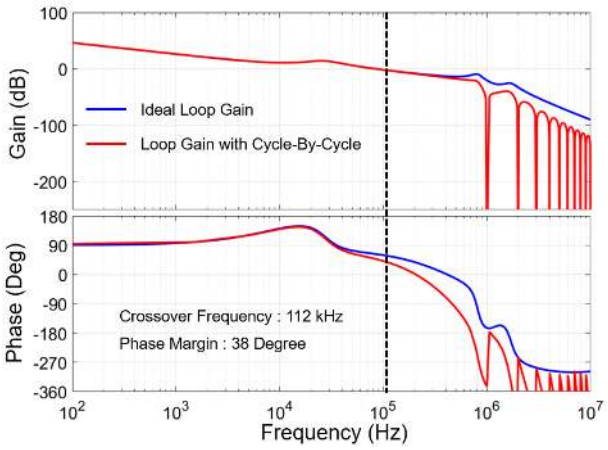
$$G_{delay}(s) = \frac{1 - e^{-sTdelay}}{sT_{delay}} \cong \frac{1}{1 + \frac{sT_{delay}}{2}} \cdots\cdots (4)$$

where T_{delay} is the time delay. T_{delay} makes the drastic decrease of gain and phase near the delayed frequency. Therefore, the crossover frequency (i.e. control bandwidth, C_{BW}) should be sufficiently lower than the delayed frequency to avoid drastic phase drop.

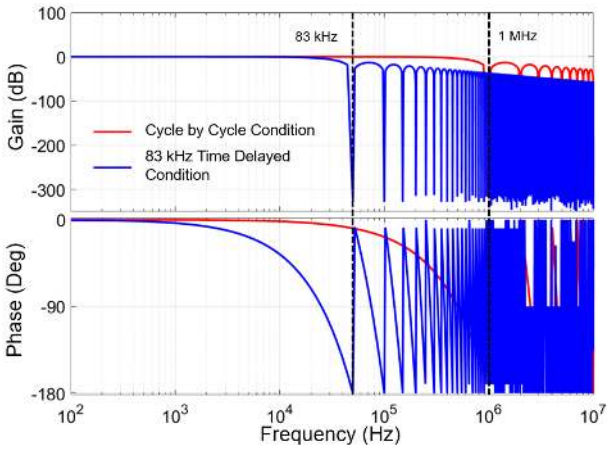
Figure 4 shows the theoretical transfer function (v_o/ω_{sn}) and loop gain of LLC resonant converter using MATLAB [15]. Where v_o is the output voltage and ω_{sn} is the normalized



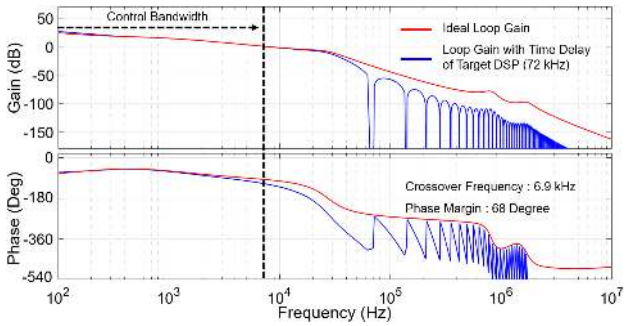
(a) Transfer function of LLC resonant converter



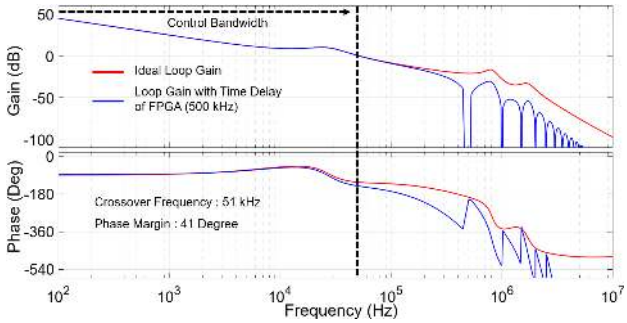
(b) Loop gain with cycle-by-cycle control



(c) Time delay effect by the limited computation time



(d) Loop gain of the general-purpose DSP



(e) Loop gain of the proposed FPGA controller

Fig. 4. Loop gain according to the controller

switching frequency. The LLC resonant converter can obtain a high control bandwidth with the first double pole compensation as shown in Fig. 4(a). The cycle-by-cycle control has maximum control speed. Figure 4(b) shows the loop gain at the cycle-by-cycle control condition. It has high crossover frequency with enough phase margin. However, the 83 kHz delayed frequency of the DSP controller is located near the first double pole (27 kHz). The DSP controller cannot obtain high control bandwidth because the crossover frequency should be lower than the first double pole frequency to avoid drastic phase drop. On the other hand, the FPGA controller can achieve higher control bandwidth than that of the DSP controller, since the 500 kHz delayed frequency is sufficiently far from the first double pole. Figure 4(c) shows the time delay effect of DSP compared with the cycle-by- cycle control. It shows the large phase drop near the frequency of time delay.

The DSP controller does not require the first double pole compensation, because it has drastic phase drop near the first double pole. A two-pole and one-zero (2P1Z) compensator has a pole at the origin to eliminate steady state error and a single zero to boost the phase margin. The additional pole results in -20 dB/dec gain drop after the single zero such that the crossover frequency is located before the first double pole. The 2P1Z compensator shows 14 times higher control bandwidth (7 kHz crossover frequency) than that of the PI compensator (495 Hz crossover frequency), as shown in Fig. 4(d).

The FPGA controller requires the first double pole compensation, because it shows drastic phase drop at high frequency region (500 kHz). A three-pole two-zero (3P2Z) compensator has a single pole at the origin, double zero at the first double pole, and double pole after the crossover frequency to achieve sufficient phase margin and enough damping at high frequency region. The theoretical results show that the FPGA shows approximately seven times higher control bandwidth (50 kHz crossover frequency) than that of the DSP controller, as shown in Fig. 4(e).

3. Controller Verification Using Signal-Level Test

Figure 5 shows the HIL test structure to implement the signal-level test. The HIL test system operates as a virtual converter which is configured with the voltage source and the electric load to simulate the output side of the power converter. The target output voltage is 20 V, which has variation

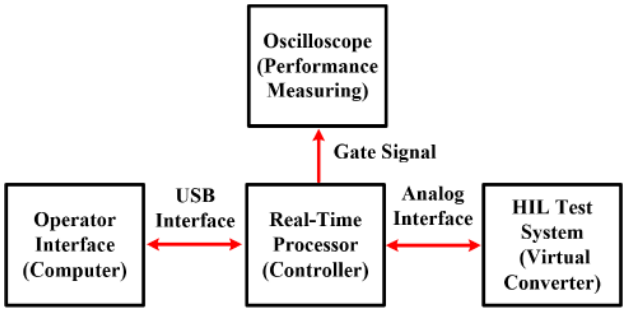
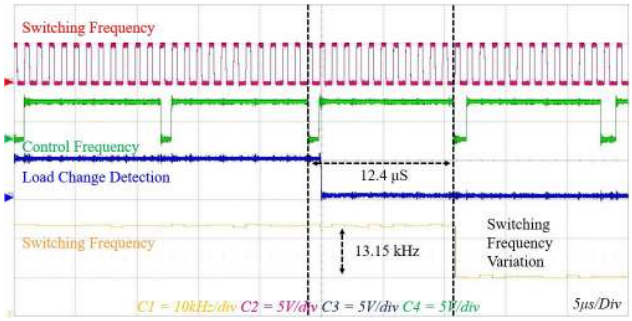
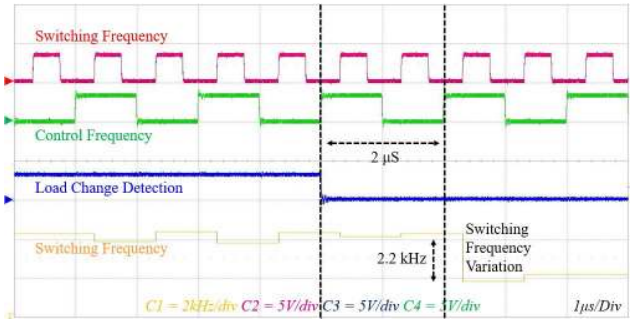


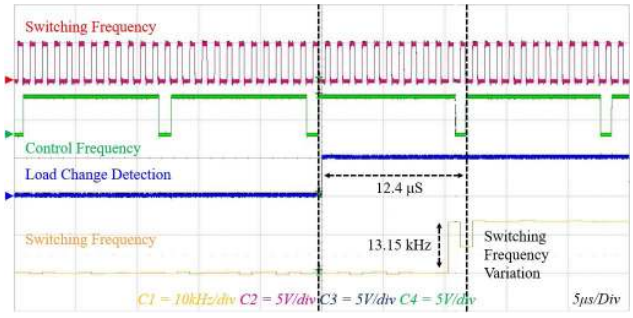
Fig. 5. Hardware-in-the-Loop (HIL) system for the signal-level test



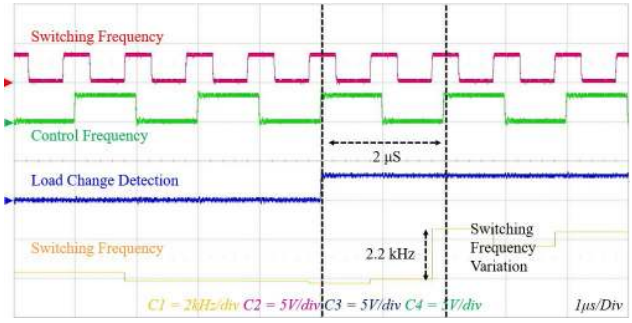
(a) DSP controller with light to heavy load change



(b) FPGA controller with light to heavy load change

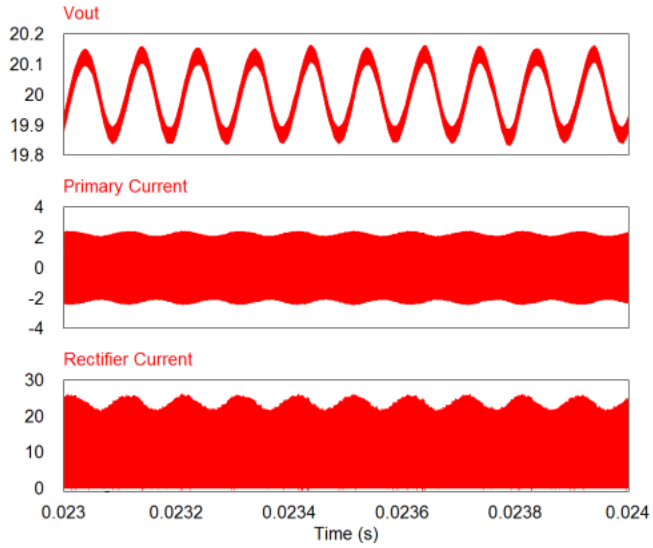


(c) DSP controller with heavy to light load change

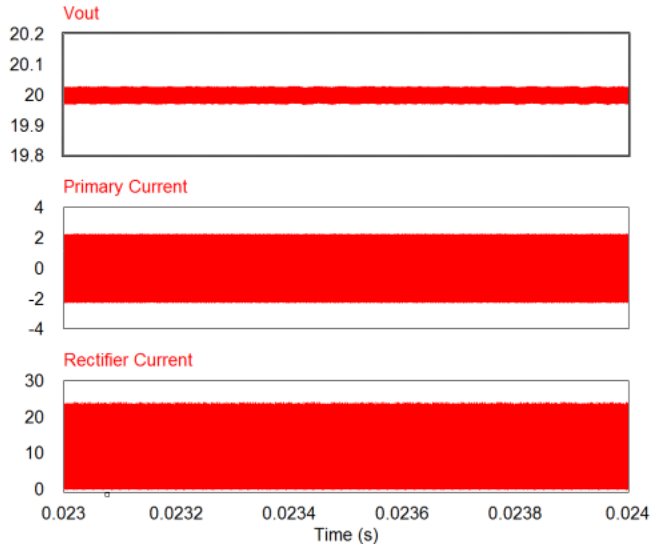


(d) FPGA controller with heavy to light load change

Fig. 6. Comparison of time delay and frequency resolution



(a) DSP controller case



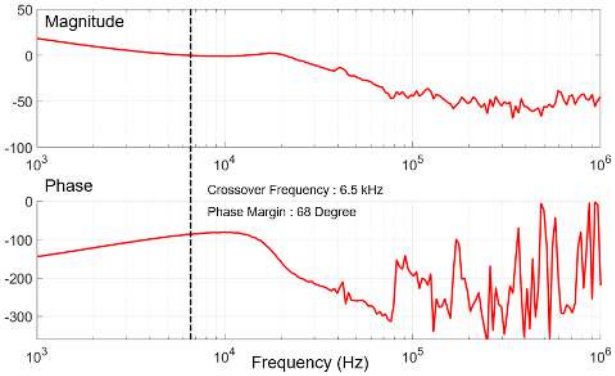
(b) FPGA controller case

Fig. 7. Simulation results of output voltage ripple

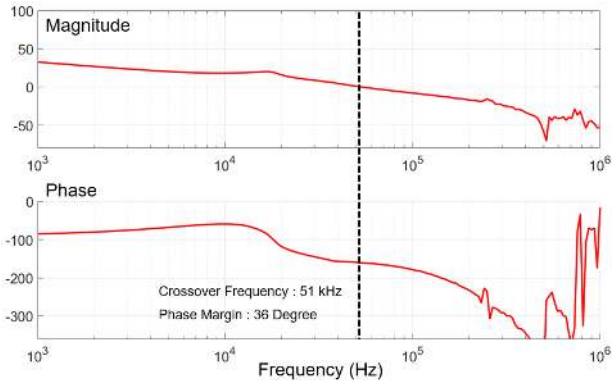
according to the load condition to test the controller performance. The controller generates the PWM signals. The switching frequency of the PWM signal has variation according to the output voltage variation. The computation speed is measured by using the GPIO port of the controller. The controller obtains the real-time dynamics of the output voltage measurement through the analog interface, which shows the switching frequency resolution and computation performance [16][17]. The time delay and switching frequency resolution are measured by experimental signal-level tests shown in Fig. 6. The load change detection shows the variation of the load condition, which has variation from the high signal to the low signal for the load variation from the light to heavy condition, vice versa. The case in Figs. 6(a) and (b) is to emulate the load changing from light to heavy, which reduces switching frequency. In these cases, the FPGA controller shows seven times smaller time delay (2 μs) than that of the DSP controller (14.08 μs). In addition, the FPGA controller has approximately 5.9 times higher switching frequency resolution (2.2 kHz) than that of the DSP controller (13.15 kHz).

Table 1. Simulation Results of Converter's Performance

Specification	DSP controller	FPGA controller
Input/Output	400V/20V, 12 A	
F_r	1 MHz	
$V_{o,r}$	0.366 V	0.062 V
$I_{p,p}$	2.767 A	2.238 A
$I_{s,p}$	28.549 A	23.838 A
F_d	72 kHz	500 kHz
C_{BW}	6.5 kHz	51 kHz
T_{up}	87 µs	10 µs
T_{down}	97 µs	15 µs

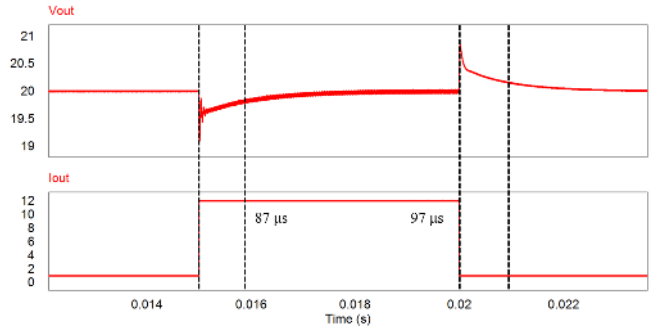


(a) 71 kHz delayed frequency with two-pole one-zero compensator

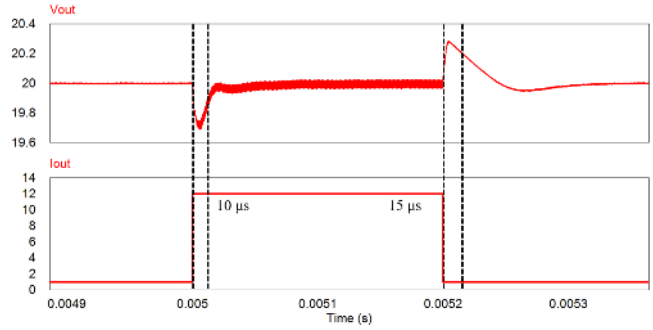


(b) 500 kHz delayed frequency with three-pole two-zero compensator

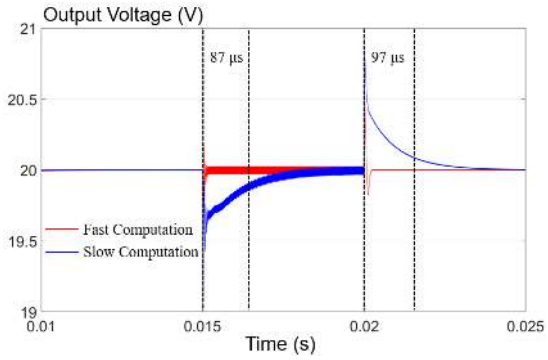
Fig. 8. Loop gain according to time delay



(a) DSP case



(b) FPGA case



(c) Comparison of dynamic performance

Fig. 9. Step load response according to the controller

The case in Figs. 6(c) and (d) is to emulate the load changing from heavy to light, which increases switching frequency. In these cases, the FPGA and the DSP have the same time delay according to the previous cases, respectively. Consequently, the FPGA has approximately 6.1 times higher switching frequency resolution (2.2 kHz) than that of the DSP controller (13.51 kHz).

Using the switching frequency resolution and computation time, the simulation model can be designed to measure the output voltage ripple and small signal response according to the controllers. Figure 7 shows the output voltage ripple and primary- and secondary-side current variation using PSIM simulation software. The FPGA based converter reduces output voltage ripple (83%) and primary and secondary-side peak current variation (19.1% and 16.5%, respectively) compared with the DSP based converter. All the performance improvements are listed in Table 1, where F_r is the resonant frequency, $V_{o,r}$ is the output voltage ripple, $I_{p,p}$ is the primary side peak current, $I_{s,p}$ is the secondary side peak current, and T_{up} and T_{down} are the load transient time according to load increment and decrement, respectively. Figure 8 verifies theoretical control bandwidth with PSIM simulation results. The FPGA controller has 51 kHz crossover frequency which is 7.28 times higher than that of the DSP controller. In the time domain, Fig. 9 shows the dynamic performance with output voltage settling time (1% voltage error) based on the load variations using the PSIM simulation software. The settling time of the FPGA controller is 8.7 times (increment) and 6.5 times (decrement) faster than that of the DSP controller, respectively.

The selected FPGA is not a state-of-the-art FPGA chip. However, in terms of the cost-effectiveness, the implemented FPGA (XC7A100T-1CSG324C) is five times more expensive than the DSP (TMS320F28335). However, the cost of the FPGA chip depends on the number of look-up tables (LUT). The implemented FPGA controller uses only 2,069 LUTs, which corresponds 3% of total LUTs. It also uses 1 DSP

slice out of 240 total DSP slices and 63 slice registers out of 126,800 slice registers. The cost of the FPGA can be decreased if we use an FPGA with a smaller number of LUTs. For example, the cost of XC7A15T-1FTG256C is similar to that of the DSP without any performance degradation.

4. Conclusion

In this paper, an FPGA controller for LLC resonant converter is developed to overcome the limited switching frequency resolution and dynamic performance of the DSP controller at a high switching frequency (1 MHz). Theoretically, the FPGA controller has approximately six times higher switching frequency resolution and seven times higher control bandwidth using a three-pole two-zero compensator compared to the DSP controller. The simulation results and experimental signal-level tests verify the improved switching frequency resolution and higher control bandwidth of the proposed FPGA controller. In future work, the prototype converter based on the FPGA controller will be implemented to verify the output voltage ripple, primary- and secondary-side current variations, stability, and controllability improvement.

Acknowledgment

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