# FPGA Implementation of an LFSR based Pseudorandom Pattern Generator for MEMS Testing

Md. Fokhrul Islam
Department of Electrical and Electronic Engineering
Islamic University of Technology
Board Bazar -1704, Gazipur, Bangladsh

M. A. Mohd. Ali
Department of Electrical, Electronic and Systems Engineering
Universiti Kebangsaan Malaysia
43600 Bangi, MALAYSIA

Burhanuddin Yeop Majlis
Department of Electrical, Electronic and Systems Engineering
Universiti Kebangsaan Malaysia
43600 Bangi, MALAYSIA

## ABSTRACT
Recent strides in programmable logic density, speed and hardware description language (HDL) have empowered the engineer with the ability to implement high-performance digital functionality within field programmable gate array (FPGA). Linear feedback shift resister (LFSR) has become one of the central elements used in testing and self testing of contemporary complex electronic systems like processors, controllers and integrated circuits (ICs). This paper presents the FPGA implementation of an LFSR based pseudorandom pattern generator. This LFSR has the characteristics of high speed, low power consumption and it is especially suited in processing environment where uniform distribution random numbers are required. A typical application of the pattern generator considered in this work is the testing of micro-electro-mechanical-system (MEMS), where low power consumption is required. Very high speed integrated circuit HDL (VHDL) was used to implement the LFSR on FPGA. A testbench in VHDL was used to verify the correctness of the design. The compiled VHDL code was been synthesized into gate level. Area and timing optimization were done to achieve a very low gate count of 436 and increase the design speed to 178MHz Mentor Graphics and Xilinx ISE 6, electronic design automation (EDA) tool suite and DIGILENT D2SB PROTO BOARD were used for the overall FPGA implementation process.

## General Terms
Design and testing.

## Keywords
Field programmable gate array (FPGA), linear feedback shift resister (LFSR), very high speed integrated circuit HDL (VHDL).

## 1. INTRODUCTION
According to the International Technology Roadmap for Semiconductors (ITRS), the manufacturing test of microelectronic systems has always been an area of special concern. Its importance is increasingly driven by new extremely complicated design techniques and advanced manufacturing technologies [1]. In many cases the cost of verification and testing of a semiconductor device, such as a general purpose IC or a microprocessor unit (MPU) outgrows the design and manufacturing costs. Such expenses are unavoidable for a company that wants to keep the product quality at an acceptable level.

During the last several years, ITRS reports indicate the strong shift of test technologies to the concept of self-testing. The industry demands highly structured standard built-in-self-test (BIST) solutions [2-3]. At the heart of the BIST approach, lie a pseudo-random binary sequence (PRBS) generator and a signature register [4]. The PRBS generator is most easily implemented using an LFSR which allows designers to generate almost all of the required binary patterns for the circuit under test (CUT). Hence, the contemporary education in microelectronics must follow these latest industrial and research trends in order to supply the society with high-level engineers and researchers [5].

This paper presents the FPGA implementation of an LFSR in a modular manner which can be used to both generate the test sequence for the CUT that is to incorporate BIST, and with slight modification, can be used to capture the response of the CUT and generate a signature. The very large scale integrated (VLSI) implementation of the LFSR is completed with Xilinx FPGA XC2S200E [6]. The rest of this paper is organized as follows. In Section 2 the general architecture of LFSR is presented with an example of 3-bit PRBS generator. Section 3 gives a description of the VHDL modeling technique. In Section 4, the hardware structure for the pseudorandom testing technique is discussed. The discussion of FPGA implementation and simulation results of a 10-bit LFSR is presented in Section 5, which is followed by conclusions.

## 2. ARCHITECTURE OF LFSR
An LFSR is a shift register that, when clocked, advances the signal through the register from one bit to the next most-significant bit as shown in Figure 1. Some of the outputs are combined in exclusive-OR (XOR) configuration to form a feedback mechanism. An LFSR can be formed by performing XOR on the outputs of two or more of the flip-flops together and feeding those outputs back into the input of one of the flip-flops as shown in Figure 2 [7].

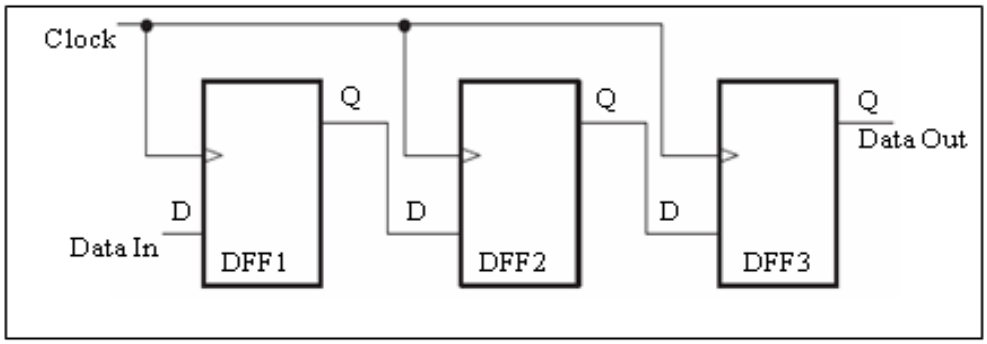


**Fig 1: A 3-bit shift register**

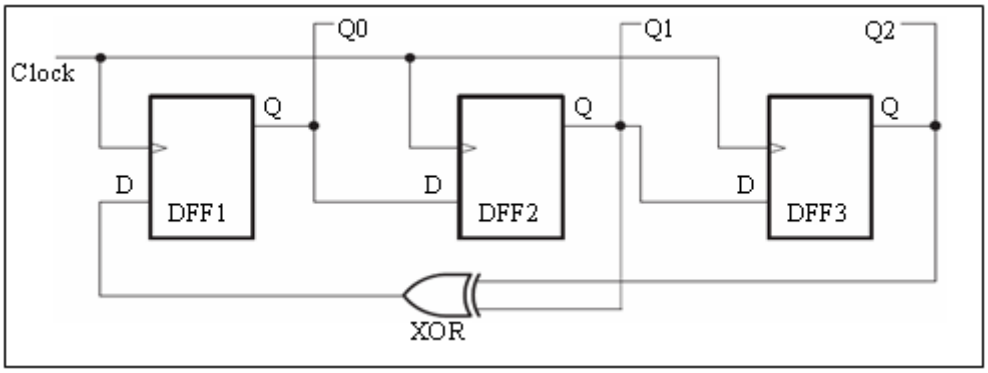


**Fig 2: Linear feedback shift register**

Additionally the operation of a PRBS generator can be discussed according to the simple LFSR presented in Figure 2. The XOR gate and shift register act to produce a PRBS at each of the flip-flop outputs. By correctly choosing the points at which we take the feedback from an *n* -bit shift register, we can produce a PRBS of length $2^n - 1$, a maximal-length sequence that includes all possible patterns (or vectors) of *n* bits, excluding the all-zeros pattern [8-9].

Table 1 shows the maximal-length sequence, with the length of $2^3 - 1 = 7$, for the 3-bit LFSR shown in Figure 2. Notice that the first (clock tick 1) and last rows (clock tick 8) are identical. Rows following the seventh row repeat rows 1–7. It should be assumed that the register is initialized to the all-ones state, but any initial state will work and produce the same PRBS, as long as the initial state is not all zeros (in which case the LFSR will stay stuck at all zeros).

**Table 1. LFSR example of Figure 2**

| Clock tick | Q0 | Q1 | Q2 | Q0Q1Q2 |
|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 7 |
| 2 | 0 | 1 | 1 | 3 |
| 3 | 0 | 0 | 1 | 1 |
| 4 | 1 | 0 | 0 | 4 |
| 5 | 0 | 1 | 0 | 2 |
| 6 | 1 | 0 | 1 | 5 |
| 7 | 1 | 1 | 0 | 6 |
| 8 | 1 | 1 | 1 | 7 |

## 3. DESIGN METHODOLOGY OF LFSR

The LFSR in a modular manner has been designed using VHDL. VHDL supports both behavioral and structural modeling. Digital circuit models using VHDL need not to be exclusively behavioral or structural. Circuit designs that contain both behavioral and structural modeling are referred to as mixed-mode modeling [10], which has been used to design the LFSR. The performance of the LFSR was verified using Mentor Graphics ModelSim simulation tool. Later, the design was synthesized and optimized using XST to create Xilinx specific netlist files. The XST was also used to generate the technology schematic of the design. Figure 3 shows the technology schematic view of the synthesized LFSR. With specially optimized algorithms to leverage the advanced architectures of the Virtex and Spartan FPGA families, XST offers designers a low-cost design solution to achieve optimal design results.

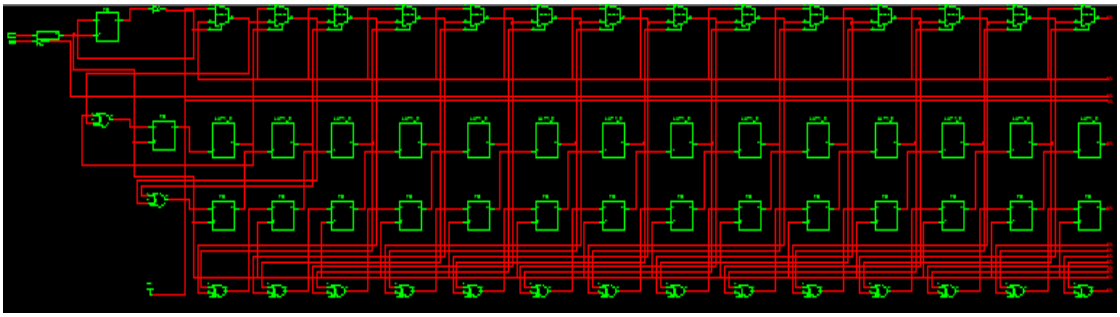

**Fig 3: Technology schematic view of the LFSR**

## 4. MEMS TESTING SCHEME

The development of testing methodologies for MEMS is extensively making use of the results obtained in the standard IC's test field [11]. Most MEMS sense physical signals (acceleration, force, pressure, radiation …) and convert them into electrical signals processed by the associated electronics. In most cases, this operation is described by means of a first or second-order transfer function, that is linear to a large extent, and that can be verified using a pseudorandom test scheme. Since MEMS are essentially analog devices, we are approaching their test as an extension of the field of analog and mixed-signal electronic testing [12]. This section introduces the application of the pseudorandom test methodology to MEMS testing which was previously introduced for mixed-signal devices [13].

The technique is based on impulse response (IR) evaluation using pseudorandom test sequences. The IR of a system provides enough information about the functional evaluation of the system. From the theory we know that the output of a system is equal to the input signal convoluted with the system IR. These facts were exploited in order to present a pseudorandom testing approach for mixed-signal circuits [14]. The architecture of our pseudorandom testing technique consists of three steps: 1) modeling the MEMS under test (MUT) as a digital system by embedding the MUT between a DAC and an ADC, 2) applying digital pseudorandom test patterns generated from LFSR to the modeled digital system, and 3) constructing the signature set (the cross correlation between the input and the output responses) for classification of the faulty and fault-free circuit. Because the flat spectrum of the pseudorandom signal essentially contains an infinite number of tones, we can use it as a universal stimulus for any linear time invariant circuit. Therefore, by using the pseudorandom patterns as input stimuli, we have completely eliminated the test generation problem. The overall block diagram of the pseudorandom test approach is shown in Figure 4.

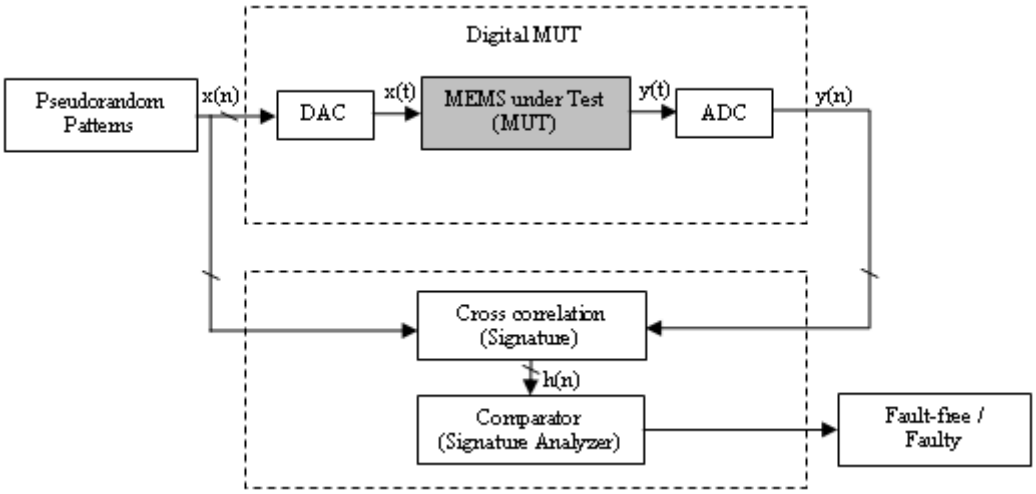


**Fig 4: The conceptual pseudorandom testing structure**

## 5. RESULTS AND DISCUSSION

Nowadays designers are facing challenges to meet time-to-market and cost constraints while product life cycles decrease and product complexity and functionality increase. FPGA helps to meet these challenges by combining the short design cycle of programmable logic device (PLD) with the application flexibility and higher integration of gate array technology. The VLSI implementation of the LFSR is completed with Xilinx FPGA XC2S200E which comprises of two major configurable elements: configurable logic blocks (CLB) and input/output blocks (IOB). Each CLB is composed of two slices as shown in Figure 5. A slice contains 4 inputs, 1 output LUT and two registers. Interconnections between these elements are configured by multiplexers controlled by SRAM cells programmed by a user's bitstream. The LUT allows any function of five inputs, and two functions of four inputs, or some functions of up to nine inputs to be created within a CLB slice. This structure allows a very powerful method of implementing arbitrary, complex digital logic circuits. The hardware uses only 436 of a 200K gates FPGA which correspond to the four inputs LUT of about 26 and the bonded IOB of about 13. From timing analysis, the 10-bit LFSR chip could operate as fast as 178MHz and the total estimated power consumption is about 7 mW.

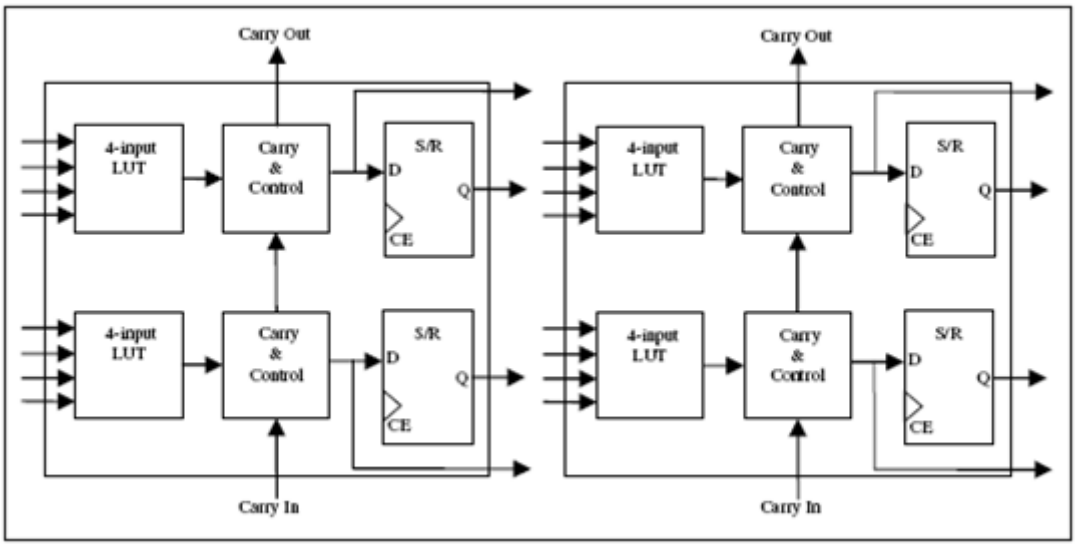


**Fig 5: Simplified architecture of configurable logic block**

Simulation result of a 10-bit LFSR which generate good PRBS is shown in Figure 6. In the simulation only the signal clock is necessary to generate the test patterns and the reset signal is used to set the initial state (1111111111) of the LFSR. The LFSR and PRBS techniques are often used to create functional patterns that provide a high level of fault coverage for the application specific integrated circuit (ASIC) with minimum effort by the designer or the test engineer. Pseudorandomly generated patterns have been proven to very quickly generate high-fault-coverage results. The PRBS technique works especially well for combinational logic but may also work well for certain cases of sequential circuits because each input signal stimulated by the LFSR is frequently changing from a 1 to 0 and back again (high bit-toggle rate).

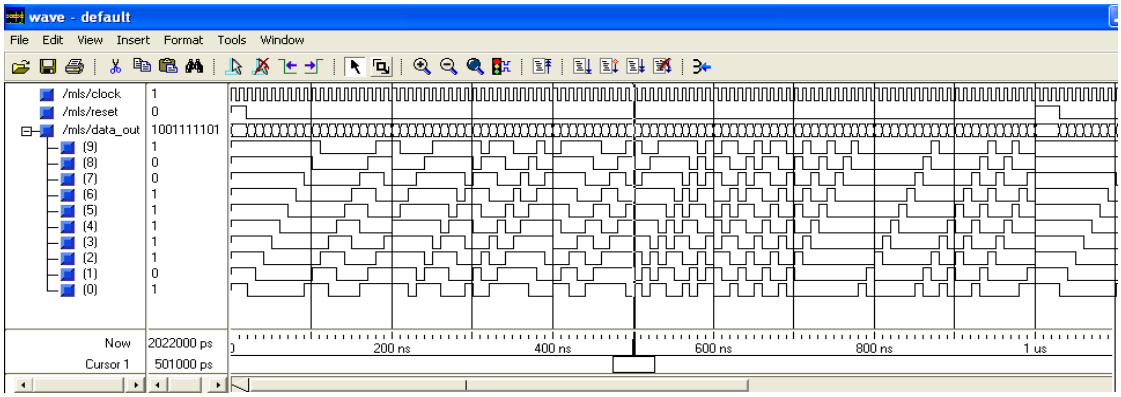


**Fig 6: Simulation result of a 10-bit LFSR**

## 6. CONCLUSIONS

LFSR are widely used in digital circuit diagnostics to generate test patterns and to compress the output sequences of the CUT. This paper presented the design of an LFSR using VHDL which has the characteristics of high speed, low power consumption and suitable in processing environment where uniform distribution random numbers are required. This paper also introduces the application of the pseudorandom test methodology to MEMS testing. A mixed-mode modeling technique in a modular manner has been used to design the LFSR. Hardware in FPGA has been optimized by taking advantage of the logic cell structure and the on-chip RAM blocks. The FPGA hardware uses only 436 gates and can deliver the PRBS at 178MHz.

## 7. ACKNOWLEDGMENTS

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