FPGA IMPLEMENTATION OF RUN LENGTH ENCODING WITH NEW FORMULATED CODEWORD GENERATOR

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Abstract

There are two major impacts in today industry while testing larger integrated circuits like large test data volume and high test power. In our proposed scheme target both two issues for achieving two aforementioned goals in full scan sequential circuits. Shift power is reduced by one of the adjacent filling. During testing we are filling the unspecified bits in the test pattern with either 0's or 1's depend on nearest specified bit from left side. After filling the don't care bits test data can be compressed by shifted alternate frequency directed run length encoding. A new formulated codeword generator is introduced and it generates infinite number of codeword for large size input test pattern. Using this codeword generator test data volume can be effectively compressed. The experimental results on ISCAS'89 benchmark circuit shows our scheme provides better efficiency as well as significant reduction in test power.

Keywords: *low power testing, X-filling, SAFDR encoding, codeword generation, Test data volume compression*

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1. INTRODUCTION

The goal of VLSI testing is achieving low test power and size of memory. The power consumption in test mode is much higher than normal mode of operation due to transition between consecutive bits are high. At the same time power dissipation also high. This high power degrades the circuit reliability and deduces the performance of circuit under test (CUT) [1]. In scan testing the test power is composed of both shift and capture power. Shift power is categorized into two (i.e.) shift-in power and shift-out power. The power consumption at loading of input to scan cells are called shift-in power similarly the power consumption at unloading of output from scan cells are called shift-out power. The shift-in power reduction prevents serious scan chain failures and yield loss [1].

In our novel scheme only concerns shift-in power reduction done by adjacent X-filling The don't care bits are largely present in the test pattern and these X-bits are filled directly affect the test power. This much high power is reduced by one of the adjacent X-filling technique. In first half of the paper X-bits are filled after that test data volume compressed for slightly reduces the storage of memory. Thus the storage of large test data volume is a serious for the semiconductor testing nowadays because it only prolongs the testing time of the integrated circuits (IC), but also raise the memory depth requirements. Here test data volume greatly reduced by shifted alternate frequency directed run length encoding scheme.

The rest of this paper organised as follows. Section II discusses about the related works. The test power reduction and new formulated test data compression is explained with illustration section III. In section IV, we present the experimental results obtained on ISCAS'89 benchmark circuits. The section V concludes the paper.

2. BACKGROUND

2.1 X-filling Techniques to Reduce the Test Power

The uncompressed test pattern have a large number of don't care bits. During test mode, small percentage of flip-flops changes its value in each clock cycle. But test mode larger percentage of flip-flops changes its value in every clock cycle which results in high switching activity. Various alternative ways are appropriately used to reduce the switching activity as well as test power. In prior works, normally use 0-filling and 1-filling. In 0-filling, the X-bits are filled in the pattern is changed to 0 similarly in 1-filling; all X-bits in the pattern are changed to 1.

After that these techniques are categorized based on filling such as preferred X-filling, random X-filling and adjacent X-filling. Namely popular shift power reduction is done by adjacent filling, in this method don't care bits are filled nearest specified bit. In random filling X-bits are X-bits are filled either 1 or 0 and it's done by our own preference. The capture power is effectively minimized by preferred filling; in this manner above two fillings are alternatively used [3].

Based on this above filling more X-fillings are developed for shift and capture power reduction such as i-fill, LSP fill, CSP fill. Thus the above filling techniques are not necessary to fill all unspecified bits in the test cube and it mainly concern to reduce both shift and capture power. Due to filling some or

most of the X-bits are filled, but it's not minimizing the power in sufficient manner. The shift-in power reduction is based on weighted transition metric WTM) calculation. In prior methods, the achievable fault coverage is very low. It's overcome by our proposed scheme.

2.2 Test Data Volume Compression Techniques

The compressed test data sets are very important for reducing the cost of testing IC's as well as test time. In prior works some additional hardware is used to compress and decompress the test stimuli due to this hardware reliability is high also chip size and power dissipation is too high. Various encoding schemes greatly reduce the test data volume for compression and decompression. In prior compression done by store and generate techniques, in this technique chip size is high because of decoder is included. After that golomb codes are analysed, in in this codes efficiently encode SOC test data. Conventional run-length codes to map variable-length blocks of data to fixed-length codeword's.

These codes are less efficient than more variable-variable length codes. Finally FDR, AFDR and SAFDR are focused to encode a test sequences including runs of 1's and 0's. the codeword generation for input data size is fixed (i.e.) codeword blocks fixed [4]. In FDR code, performs encoding like runs of 0's and 1's similarly AFDR woks like alternative runs of 0's and 1's. (i.e.) runs of 0's must be followed by runs of 1's as well as runs of 1's must be followed runs of 0's [5]. In SAFDR group of large elements are considered as single one depend on compression. Compare than golomb codes FDR codes provide better efficiency but above codes shouldn't effectively deduce memory consumption.

3. OVERVIEW

In this overview section, proposed scheme is explained in detail. Here our scheme targets the test power as shift-in power and its reduction on lowering the transition in test pattern during shift cycle after that bit specified test patterns are compressed. Fig. 1 describes the flow for reduction of test power and test data volume also this fig. 1 shows how to our scheme works on two phases (i.e.) shift-in phase and compression phase. In first phase shift-in power reduction makeup on two steps

At first test vector (X- bits) can be generated by Automatic test pattern generator (ATPG) and thus the sequence of test input patterns are given to adjacent X-filling and it's accomplished by below two steps. In first step X- bits are filled depend on nearest specified bit present from left side. In second step, unfilled X- bits are filled depend on specified bit from right side. This adjacent filling surely follows the WTM calculation, based on this minimum WTM input pattern only allows for current X-filling otherwise it's neglected [6]. After that flow enter into the compression phase. Here SAFDR used as encoding scheme for data compression. After the fully specified test set codeword is generated for each input until the process end.

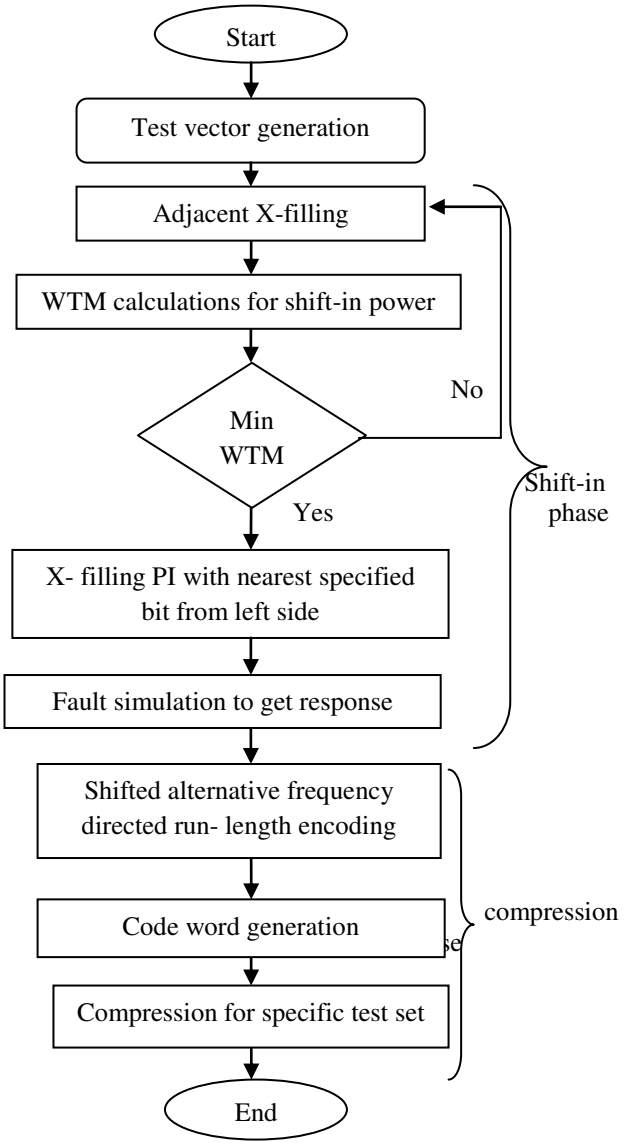

Fig -1: Overview flow diagram

3.1 Reducing Shift-in Power

Shift-in power is calculated by WTM (Weighted Transition Metric) approach to reduce transition between consecutive bits. The shift power not only depends upon the transition among consecutive bits but also the position of transition. Below Eq.(1) shows the calculation of WTM [6]. Here the test stimulus T the shift-in power in the *p*th test vector having *q* bits is calculated as

$$WTMp = \sum_{q=1}^{n-1}(Tp,q \oplus Tp,q+1)Xq$$

Here n is the number of scan cells in the scan chain and T*p,q* is the logic value of *q*th scan cell in *p*th test vector. For example: let T be a test pattern of 16bits.

T= XX1XX1XXXXX0XXXX

After the adjacent filling,

T=1111111111100000

The minimum transition metric of WTM=5. This has minimum transition among all possible X-filling techniques for shift-in power reduction.

3.2 Reducing Test Data Volume

The test data volume reduction is done by using SAFDR (shifted alternative frequency directed run-length encoding).it runs the consecutive group of specified pattern alternatively like group of 1's and 0's. This example encoding as shown in table (1) In proposed scheme run no specifies the number of run is currently processed. 2^n elements considered as one group and 2^n possible elements are generated as tail elements for corresponding 'n' group number. n is denoted as binary value. The codeword is combination of two parts, such as prefix and tail. The prefix considered as previous value of last number after that codeword is generated.

In our proposed scheme, codeword is generated for an infinite number of inputs based on two formulas.

$$\text{Prefix} = (2^{\text{Group no}} - 2) \qquad \text{Eq.(2)}$$

$$\text{Tail} = \text{Run length} - (2^{\text{Group no}} - 1) \qquad \text{Eq. (3)}$$

Large size input test patterns have more number of runs like 256. It can't be generated by normal codeword generator. This problem easily recovered by proposed codeword generator. Here, run length specifies runs of currently processed either group of 0's or 1's. The prefix and tail, both have the same bit size and the bit size will be same as the group number. The use of prefix is to determine the numbers in the group while decompression.

Table -1: Encoding scheme

Run	Group no	Prefix	Tail	Codeword
1	1	0	0	00
2			1	01
3	2	10	00	1000
4			01	1001
5			10	1010
6			11	1011
7	3	110	000	110000
8			001	110001
9			010	110010
10			011	110011
11			100	110100
12			101	110101
13			110	110110
14			111	110111

Example: length of pattern is 34

Run: 111111 (6) 000000000000 (12) 1111111111111111 (16)
Code: 1011 110101 11100001
Code length: 18

The original encoded test pattern length is 34 and it's compressed into 18. The compression ratio is calculated by below formula.

$$\text{Compression ratio} = \frac{|TD - Tc|}{|TD|} \times 100\%$$

$$= \frac{|34-18|}{|34|} \times 100\% = 47\%$$

Where TD represents the original test pattern test length and Tc represents the compressed test pattern length.

3.3 Compression Unit

The overall process control unit is shown in below. In this unit SAFDR and codeword generator are connected together. These two modules are DUT (i.e.) Design Under Test. Clk and reset are commonly given to both two modules. The codeword generator send codeword_ready request to SAFDR after that acceptance by SAFDR following information's are send to it such as prefix, tail, width and group no (i.e.) converted into FDR codes. Finally codeword_done acknowledgement resend from SAFDR to codeword generator. The overall compression operation is makeup on this unit it is shown in fig. (2). Outputs are shown by LED switches

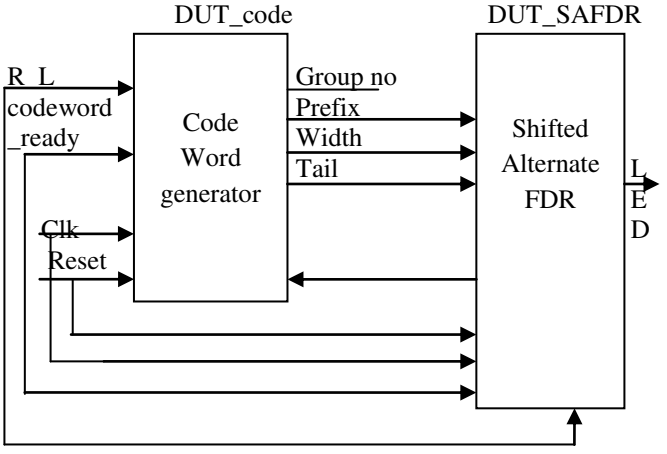

Fig -2: Overview flow diagram

4. EXPERIMENTAL RESULTS

The proposed scheme programmed on VHDL and its implemented into Spartan 3E NEXSYS2 FPGA kit. In order to analyze the power consumption while testing IC's and test data volume compression results also shown by modelsim output. Here modelsim 6.2c used. After the X-bits generation, the X-filled pattern is given to compactor. Xilinx 14.2 is used for synthesis the larger codes. The simulation results shows our whole operation.

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	2392	4656	51%
Number of Slice Flip Flops	2096	9312	22%
Number of 4 input LUTs	2964	9312	31%
Number of bonded IOBs	10	232	4%
Number of GCLKs	1	24	4%

Fig -3: Device utilization summary

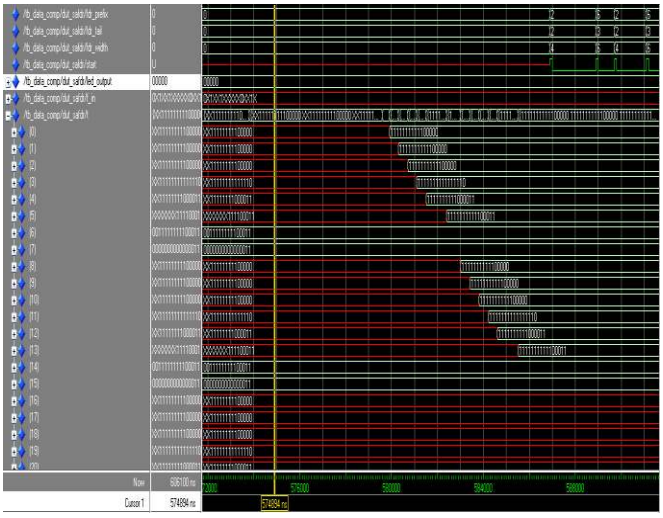

Fig- 4: Adjacent X-filling waveform

Fig. (3) shows whole device utilization summary of our FPGA and how much detection of devices also shown Fig. (4) shows input test patterns are frequently send to X-filling, after that X-bits are filled in every clock cycle. This operation accomplished within few seconds.

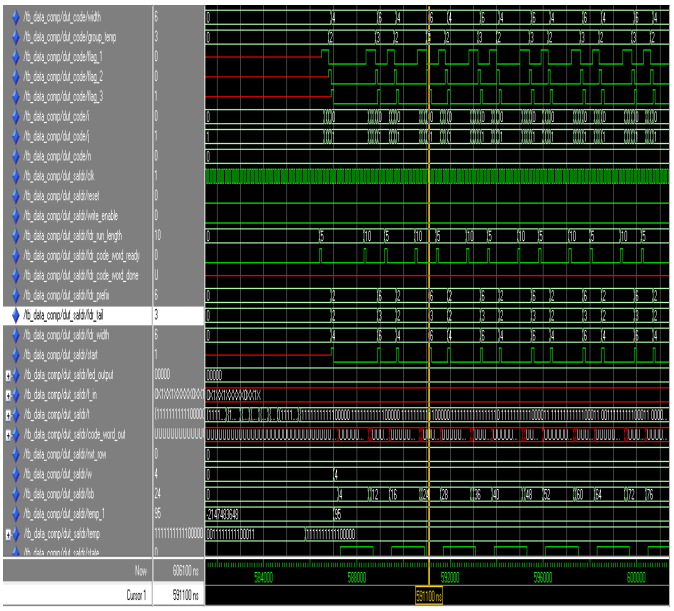

Fig- 5: Codeword generation waveform

Fig. (5) shows code generation waveform for each input, code word can be generated with same bit size and width size Fig. (6) shows overall compression waveform for large size input of benchmark circuit.

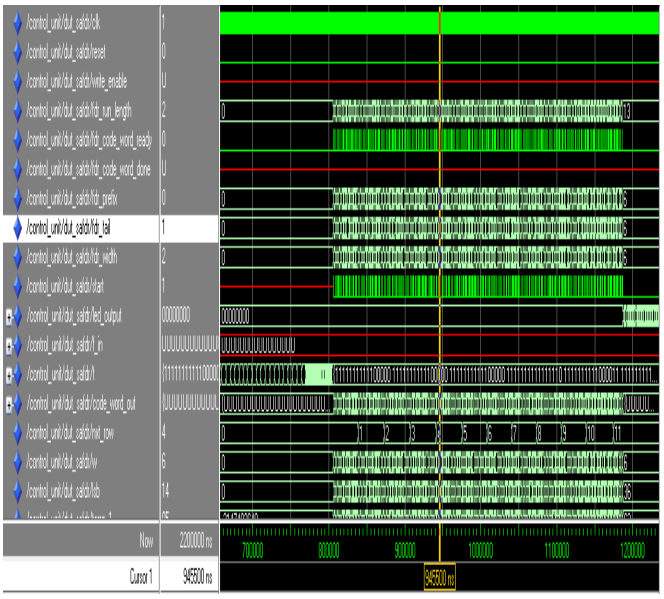

Fig-6: Compression waveform

Table-2. shows experimental results on shift-in power reduction. It can be accomplished by various CUT. Based on this results we easily analyze our scheme provide better shift-in power reduction. TABLE III. Shows comparison of compression ratio of various CUT,

Table -2: Experimental results on shift-in power reduction

CUT	Size of in/out	# SFF	# pattern	%X-bits	Average shift-in transition		
					0 fill	1 fill	ours
S15850	611/684	597	846	98.71	6059.45	6985.2	**1970**
S35932	214/213	179	641	49.08	854.68	706.7	**419**
S38417	1664/1742	1636	3498	98.23	12330.5	11001.4	**4524**

Table -3: Experimental results on shift-in power reduction

CUT	ORIGINAL TEST VOLUME	COMPRESSION RATIO		
		GOLOMB	FDR	OURS
s115850	137174	87.61	77.56	**80**
s13207	576800	89.03	84.73	**91**
s38417	5031936	**89.86**	79.00	87

5. CONCLUSIONS

Thus the proposed scheme of test data volume and high test power reduction are greatly achieved. Test power is minimized by adjacent X-filling and test data volume is compressed by SAFDR. In SAFDR codeword is generated by new formulated codeword generator for large number of bits in runs. Due to this storage of test pattern memory also effectively reduced so size of chip is minimized and degradation is very less. The experimental results on ISCAS' 89 benchmark circuit shows that our scheme provides better efficiency as well as significant reduction in test power.

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