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Frequency Characterization of Si, SiC, and GaN MOSFETs Using Buck Converter In CCM as an Application

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FREQUENCY CHARACTERIZATION OF Si, SiC, AND GaN MOSFETs USING BUCK CONVERTER IN CCM AS AN APPLICATION

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By

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I HEREBY RECOMMEND THAT THE THESIS PREPARED UNDER MY SUPERVISION BY Keshava Gopalakrishna ENTITLED Frequency Characterization Of Si, SiC, and GaN MOSFETs Using Buck Converter in CCM as an Application BE ACCEPTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF Master of Science in Engineering.

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Abstract

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Present day applications using power electronic converters are focusing towards improving the speed, efficiency, and robustness. This led to the implementation of new devices in such converters where speed and efficiency are of concern. As silicon (Si) based power devices are approaching their operational performance limits with respect to speed, it is essential to analyze the properties of new devices, which are capable of replacing silicon based devices. Wide band-gap (WBG) semiconductor materials such as silicon carbide (SiC) and gallium nitride (GaN) are such materials, whose material properties show promising advantages for power electronic applications.

This thesis focuses on the comparison of Si, SiC, and GaN based power devices. A detailed comparison in terms of the material performance based on their figures-of-merit will be discussed. In this thesis, a performance evaluation of Si, SiC, and GaN based power devices used as a high-side switch in a buck DC-DC converter will be performed. A buck converter having specifications: output voltage of 12 V and output power of 120 W. Initially, a design example for switching frequency of 100 kHz will be discussed. Further, an evaluation of the same for increase in switching frequencies will be performed. Finally, analyses of the power loss and efficiency of these devices will be made along with its validation using PSpice, SABER and MATLAB simulation software. It will be shown that the theoretical performance analyses are in accordance with the obtained simulated results. Finally, it will be shown that GaN based power devices have improved operational capabilities at high frequencies than those of Si and SiC.

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Acknowledgment

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1 Introduction

Power electronics is one of the fastest changing technologies in the field of engineering in the world today. The power electronics revolution was started by the invention of the thyristors and then continued further by the invention of power devices such as Bipolar junction transistors (BJT), Insulated-gate bipolar transistor (IGBT), Metal oxide semiconductor filed effect transistors (MOSFET), etc. The invention of these new devices insinuated new power electronic topologies, which in turn resulted in reduction in cost. This led to usage of power electronics application everywhere [21]. Power electronic systems are found in almost all electronic devices. A DC-DC converter is one such system, which is widely used in all devices and play an important role in maintaining a steady voltage irrespective of the voltage at the input.

1.1 Buck Converter

Over the last few decades in power electronic systems, there has been a growing trend towards achieving higher power density. Due to environmental concerns and rising energy costs that determine the performance, the efficiency has became an important performance criterion. In recent years, physical dimensions of devices have become a priority. Portable devices such as mobile phones, MP3 players, and palmtops are getting smaller and lighter with development in technology. In order to make the devices smaller, the components within the device have to be smaller. The power electronic converter is one of the most important parts of such a portable device. Such portable devices require very low voltage and that requires a voltage conversion from line voltage to the required voltage as per the application. A buck converter is one such converter.

A buck converter is a step down DC-DC converter. The switching network, which consists of a MOSFET S and a diode D chops or cuts down the dc input voltage V_I and produces a reduced output voltage V_O. A basic circuit diagram of a buck converter is shown

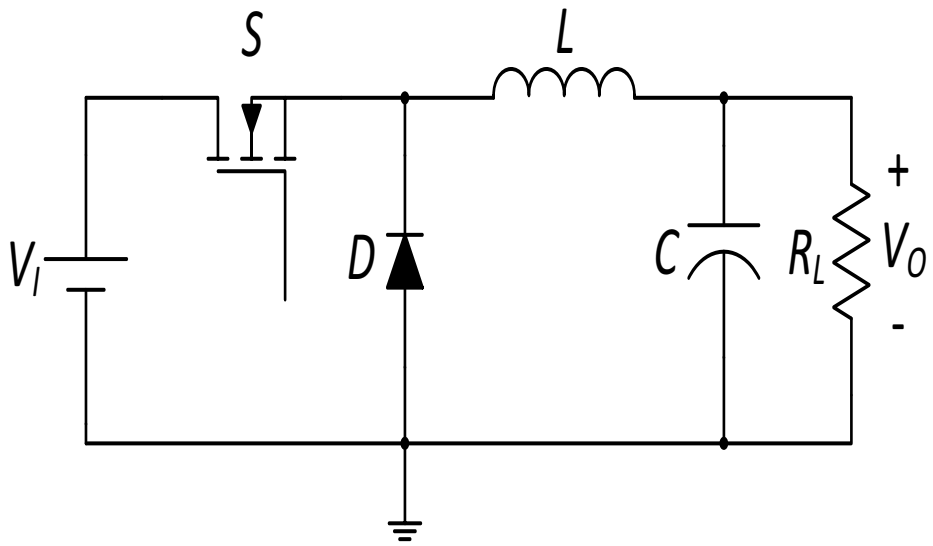

Figure 1.1: Circuit diagram of dc-dc buck converter.

in Figure 1.1.

In such portable devices, dimensions of the converter are an important factor. In order to reduce these dimensions, the component size has to be reduced [6]. Increasing the switching frequency is one way of reducing the size of the components. However, increasing the switching frequency results in increased switching losses and decreased efficiency. Hence, there is always a tradeoff between frequency and efficiency. With progress in technology, several attempts have been made and proved to be successful in developing high-frequency converters. For a long time now, silicon based power devices (MOSFETs) have dominated the field of power system applications. MOSFETs too had its advantages, which enabled new applications, which were not possible with IGBTs or JFETs. It proved to be more reliable, easier to use, and was less expensive [30]. As the need for smaller portable devices grows continuously, silicon power devices are on the verge of reaching their fundamental limit for high-frequency applications though tremendous improvements have been made to improve their high-frequency capability. The main requirements for semiconductor devices are efficiency and reliability. Without offering better efficiency and better reliability over the

previously developed device, a new device structure would prove to be less advantageous. There have been many new power devices offered after silicon and only some have been successful, offering better efficiency and better reliability [30].

It is time now for wide-band gap (WBG) semiconductor MOSFETs like silicon carbide (SiC) and the latest in technological development, gallium nitride (GaN) to prove their abilities in high-frequency applications. This is beacause of their superior material properties, which makes them suitable for high-frequency applications. Silicon carbide (SiC), which is a wide-band gap material, offers a much better critical field magnitude and is greater than that of Si. Hence, the blocking capability is increased. The fabrication is possible on a much thinner doped drift layer and the on-state resistance is low. The thermal conductivity is higher than that of silicon and can operate up to temperatures of 270°C to 300°C. These basic properties of SiC make it a better substitution to its silicon counterpart for operation at higher temperatures and voltage [20].

Gallium Nitride (GaN) High Electron Mobility Transistor (HEMT) with depletion mode was the first GaN transistor, which appeared in 2004. In the year 2009, the first enhancement mode GaN transistors were introduced as a better replacement to Si power MOSFETs in terms of frequency and efficiency. These transistors have an extra advantage over SiC and Si, i.e., the enhanced mobility of electrons, which in turn results in higher efficiency, smaller size, low on-resistance, and breakdown voltage. These transistors require less charge to turn ON and OFF, which results in lower switching losses. GaN transistors, however, remain to be more expensive to produce than their silicon counterparts [30].

With recent technological progress in manufacturing power devices based on wide-band gap materials, the operating voltage range and the switching speed can be improved significantly compared to silicon power devices. The application of these new devices in power electronic systems will have an impact on the performance of the device, which is measured by power density, efficiency, weight, reliability, and cost. In this research, the system level

performance of a DC-DC buck converter in CCM using Si, SiC, and GaN devices is evaluated by means of SABER and PSpice simulations.

1.2 Motivation

For the last couple of decades, bipolar transistor was the most widely used transistor until the Metal Oxide Field Effect Transistor (MOSFET) came along. Bipolar transistors are current-controlled and require a high base current to turn-on and relatively slow turn-off characteristics [6]. However, MOSFET is a device that is voltage controlled. The on-state resistance $r_{DS(ON)}$ is far more lower. Considering these advantages, MOSFET soon became the optimum device for power switching designs. The IGBT is a blend of a bipolar transistor and a MOSFET. It has the switching and conduction characteristics of a bipolar junction transistor, but is voltage controlled like a MOSFET. It has high current handling capability, easy to control, and can handle high amount of power. However, choosing between IGBTs and MOSFETs is dependent on the application requirements like cost, size, and speed [6].

As the gate is insulated in a MOSFET, this insulation causes low power consumption. This is an advantage and is usually used in CMOS logic for low power consumption. MOSFETs are usually preferred in low voltage applications, switch-mode power supplies, and high-frequency applications. The operating frequency determines the performance of the switch. There is now a growing trend in research work and new power supply designs for operations at high-switching frequencies. The higher is the switching frequency, the smaller are the reactive components, hence, smaller converter size [6]. There are many advantages of operating at high-switching frequencies such as:

a) smaller converter sizes.

b) Switching transient response can improve with a higher-switching frequency.

Since the present day technology is mainly focused on high-frequency power converters, and that a lot of work has already been done on Si power transistors. This thesis aims at comparing Si, SiC, and GaN transistors in a conventional DC-DC buck converter operating in CCM at high-switching frequencies keeping Si MOSFET as the base device. The main objectives of this thesis are explained in the following section.

1.3 Objectives

Work on wide-band gap (WBG)devices has been going on for the last few decades. The properties of these devices are very exciting as they offer substantial performance improvements over silicon based devices. Their ability to operate at high temperatures, high power densities, high voltages, and high frequencies make them interesting for its use in future electronic power conversion systems. Two very important materials are Gallium Nitride (GaN) and Silicon Carbide (SiC). There is a great deal of ongoing research about GaN and SiC materials and about, which device is best suited for various switching applications. Though Si has higher electron mobility than SiC, and GaN transistor's electron mobility is higher than that of SiC, electron mobility is not the only property that determines the performance for high-frequency applications. Both SiC and GaN have properties superior to Si for switching power devices [22].

This research focuses on the following:

1) Comparison of Si and WBG semiconductor materials, such as SiC and GaN based on their physical properties.

2) Detailed study of their properties and their use in power electronics applications, such as, high-frequency applications.

3) Designing a PWM DC-DC buck converter with Si, SiC, and GaN MOSFETs and evaluate its operation at various switching frequencies with the help of SABER and PSpice circuit simulations.

4) To determine the frequency at which the MOSFET fails to switch normally, and when the converter begins to perform inefficiently.

The methodology and performance criteria of the thesis includes:

1) The MOSFET models used here are level 7 PSpice. The comparison is dependent on the drain-to-source voltage v_{DS} of the MOSFET and the output of the buck converter i.e., the

output voltage V_O, output current I_O, and output power P_O.

2) A few wide-band gap semiconductor material MOSFETs continue switching effectively though the converter stops to step down the input voltage. Such transistors are tested for much higher frequencies where the efficiency is very low and approximate breakdown limit is determined.

3) Switching frequency ranging between 100 kHz to 500 kHz is considered as low switching frequency. The MOSFET, irrespective of the type of semiconductor material used, stops to switch normally at a certain frequency, which is to be determined as approximate cut-off frequency of the MOSFET. When the amplitude of the drain-to-source voltage v_{DS} of the MOSFET starts decreasing and does not match up to the maximum value of V_I, we determine this frequency to be the approximate cut-off switching frequency of the MOSFET in a buck converter operating in CCM.

2 Classification of Silicon (Si), Silicon Carbide (SiC), and Gallium Nitride (GaN) semiconductor materials and MOSFETs

The basic requirement of power semiconductor is reliability, efficiency, and cost [26]. High-frequency operation serves as an advantage in terms of size. Power semiconductor MOSFETs came into picture in the 1970s and since then, continuous work has been going on in developing components operable at higher frequencies. Over time, many semiconductor materials have been made use of to make better and more efficient power MOSFETs. The performance of semiconductor materials can be compared using the figure-of–merit. The different types of figures-of-merit used to compare the performance of semiconductor materials are given by

Baliga's figure-of-merit ($BFOM$) is given by [1]

$$BFOM = \epsilon_r \epsilon_0 \mu_n {E_G}^3. \tag{2.1}$$

where μ_n is the electron mobility at low field and E_G is the band-gap energy. Another figure-of-merit similar to $BFOM$, which considers the breakdown electric field E_{BD} is expressed as $MFOM$ given by

$$MFOM = \epsilon_r \epsilon_0 \mu_n {E_{BD}}^3. \tag{2.2}$$

ϵ_r is the dielectric constant of the material, ϵ_0 is the absolute permittivity or permittivity of free space, and E_{BD} is the breakdown electric field. This comparison of performance can also be made using the Johnson's figure-of-merit ($JFOM$) given by [1]

$$JFOM = \frac{E_{BD} v_{sat}}{2\pi}. \tag{2.3}$$

Another figure-of-merit used in integrated circuits is the Keyes figure-of-merit given by [9]

$$KFOM = X\sqrt{\frac{cv_{sat}}{4\pi\epsilon_r}}. \tag{2.4}$$

where X is the thermal conductivity.

2.1 Silicon (Si) MOSFET

One of the first power MOSFETs ever built made use of silicon. Over time, silicon proved to be less efficient at high-frequencies and new semiconductor materials had to come into picture. Few promising technologies used in high temperature and high frequencies are silicon carbide (SiC) and gallium nitride (GaN). These devices require an epitaxial layer of SiC or GaN to be deposited on either the same or a different material. A layer deposited on same material is called homoepitaxy and the other is called heteroepitaxy GSC. A brief classification of MOSETs based on the semiconductor material used is discussed later in this chapter.

Silicon MOSFET proved to be very efficient at the time and was a breakthrough in technology in the field of power MOSFETs.

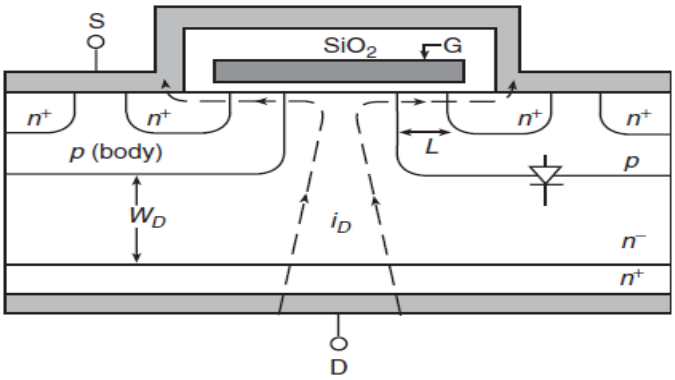

Figure 2.1: Cross-sectional view of Si MOSFET.

A cross-sectional view of a Si MOSFET [1] with source S, gate G, and drain D terminals is shown in Figure 2.1. Here, the drain and source are on the opposite sides. Two diffusions are used, one to form the p-type body, and the other to form n^+-type source regions. For these reasons, it is called vertical double-diffusion MOSFET or DMOS. It has

four semiconductor layers, viz. $n^+p\ n^-n^+$ layers. The fabrication of the transistor is on an n^+ substrate. An n^- drift layer is grown on the substrate. Then, p-wells are diffused, which are known as body regions and finally the n^+ sources are diffused. More about the physical structure, operation, current and voltage characteristics, and their short-channel effects can be found in literature [1]. Silicon's $BFOM$, $JFOM$, $MFOM$ and $KFOM$ are given by

$$BFOM_{(Si)} = \epsilon_r \epsilon_0 \mu_n {E_G}^3 = 12.8 \times 8.8542 \times 10^{-14} \times 1400 \times (1.12)^3 = 2.22 \times 10^{-9} \quad \mathrm{C^4Vcm/s}, \tag{2.5}$$

$$JFOM_{(Si)} = \frac{E_{BD} v_{sat}}{2\pi} = \frac{(2 \times 10^5) \times 10^7}{6.28} = 3.18 \times 10^{11} \quad \mathrm{V/s}, \tag{2.6}$$

$$MFOM_{(Si)} = \epsilon_r \epsilon_0 \mu_n {E_{BD}}^3 = 11.7 \times 8.8542 \times 10^{-14} \times 1400 \times (2 \times 10^5)^3 = 11.60 \quad \mathrm{MW/cm^2}, \tag{2.7}$$

$$KFOM_{(Si)} = 1.5\sqrt{\frac{3 \times 10^6 \times 10^7}{4\pi 12.8}} = 647 \quad \mathrm{mW/K \cdot s}. \tag{2.8}$$

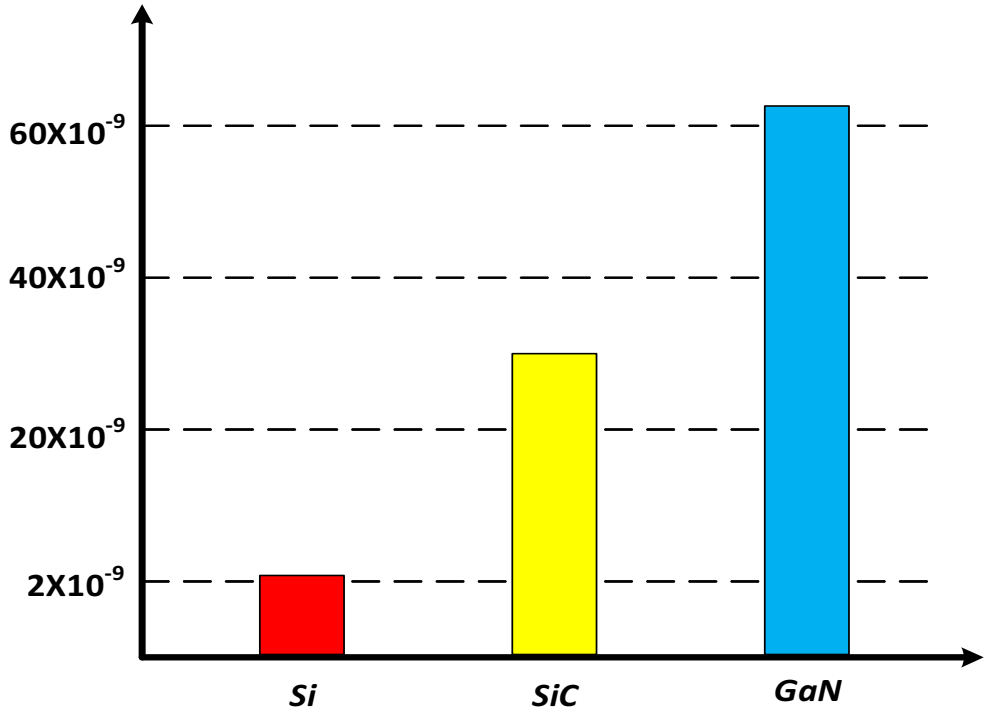

Figure 2.2: Comparison of baliga's figure-of-merit ($BFOM$) of Si, SiC, and GaN semiconductor materials.

2.2 Silicon Carbide (SiC) MOSFET

Silicon carbide (SiC) is a wide-band gap semiconductor material as well as a compound semiconductor material as it has elements from different parts of the periodic table. Homoepitaxial SiC is fabricated in a way similar to that of Si [22]. Its several properties has made its silicon counterpart less important in new applications, which require high-frequency and operational capability at higher temperatures. Though its electron mobility μ_e is much less than that of silicon, it has a high band gap energy of 3.3 eV. Its high critical field allows it to operate at higher voltages. It also conducts heat more efficiently. When high power is desired, SiC has an advantage over Si and GaN due to its high critical field and higher thermal conductivity [22]. These properties allow high voltage blocking ability, operation at high temperatures, and lower switching losses compared to that of Si, making it very attractive for power applications [14]. Many poly-types of SiC have been studied and out of which 4H-SiC has a wider band gap compared to 6H-SiC. The electron mobility is much higher when compared to its 6H-SiC poly type. A cross-sectional view of 4H-SiC SiC MOSFET [25] is shown in Figure 2.3.

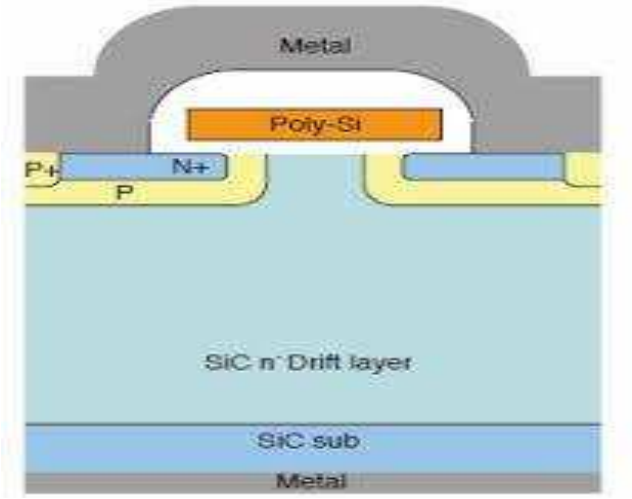

Figure 2.3: Cross-sectional view of SiC MOSFET.

$$BFOM_{(SiC)} = \epsilon_r \epsilon_0 \mu_n {E_G}^3 = 9.7 \times 8.8542 \times 10^{-14} \times 980 \times (3.26)^3 = 29.7 \times 10^{-9} \quad \mathrm{C^4Vcm/s}, \tag{2.9}$$

$$JFOM_{(SiC)} = \frac{E_{BD} v_{sat}}{2\pi} = \frac{(22 \times 10^5) \times 2.7 \times 10^7}{6.28} = 94.58 \times 10^{11} \quad \mathrm{V/s}, \tag{2.10}$$

$$MFOM_{(SiC)} = \epsilon_r \epsilon_0 \mu_n {E_{BD}}^3 = 9.7 \times 8.8542 \times 10^{-14} \times 980 \times (22 \times 10^5)^3 = 8962.22 \quad \mathrm{MW/cm^2}, \tag{2.11}$$

$$KFOM_{(SiC)} = 3.7 \sqrt{\frac{3 \times 10^6 \times 2.7 \times 10^7}{4\pi 9.7}} = 3017 \quad \mathrm{mW/K \cdot s}. \tag{2.12}$$

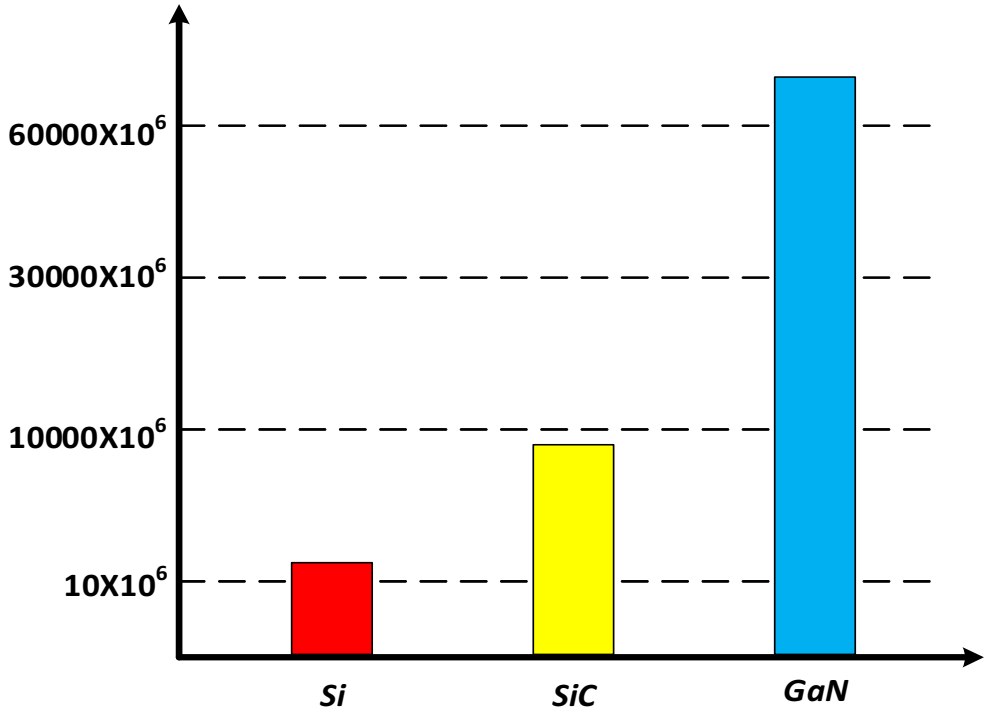

Figure 2.4: Comparison of figure-of-merit ($MFOM$) of Si, SiC, and GaN semiconductor materials.

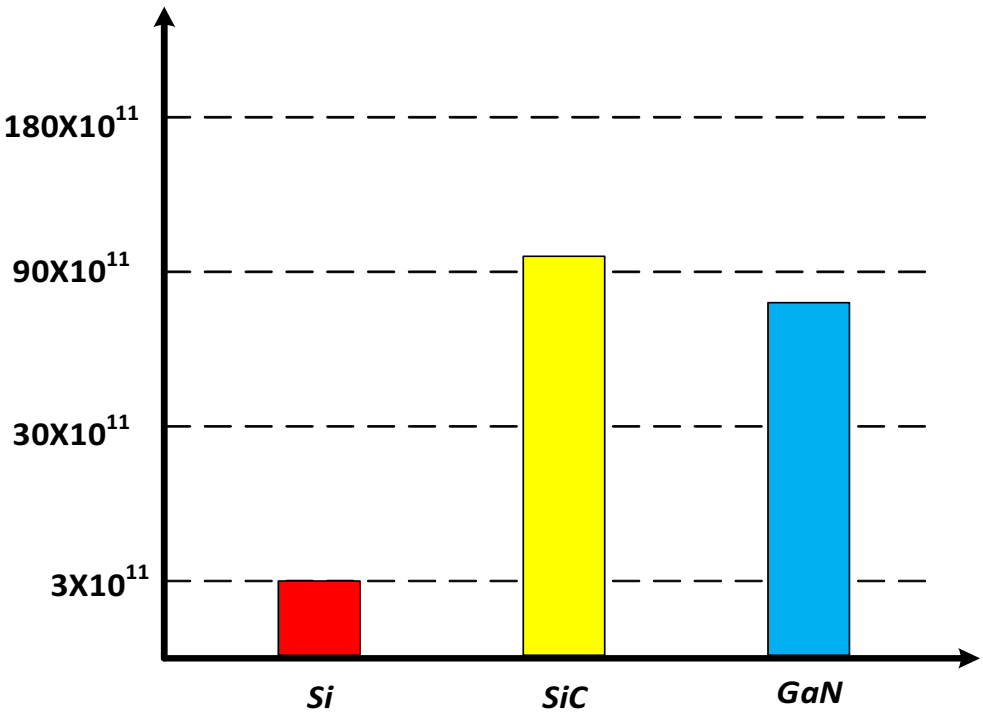

Figure 2.5: Comparison of Johnson's figure-of-merit ($JFOM$) of Si, SiC, and GaN semiconductor materials.

The $BFOM$, $JFOM$, $MFOM$ and $KFOM$ of SiC is higher when compared that of Si. SiC has a better figure-of-merit than Si. The ratio of figures-of-merit of Si and SiC is

$$\frac{BFOM_{(SiC)}}{BFOM_{(Si)}} = \frac{29.7}{2.22} = 13. \tag{2.13}$$

$$\frac{MFOM_{(SiC)}}{MFOM_{(Si)}} = \frac{8962}{11.6} = 772. \tag{2.14}$$

$$\frac{JFOM_{(SiC)}}{JFOM_{(Si)}} = \frac{94 \times 10^{11}}{3 \times 10^{11}} = 31. \tag{2.15}$$

$$\frac{KFOM_{(SiC)}}{KFOM_{(Si)}} = \frac{3017}{647} = 4.5. \tag{2.16}$$

In reference to the ratio of $BFOM$, SiC semiconductor materials performance is

13 times the performance of Si. Considering other figure-of-merit, the performance of SiC semiconductor material is superior to the performance of Si (2.8). This is as shown in equations (2.13)-(2.16).

Presently, SiC is one of the semiconductor materials to meet the requirements for performance at high voltages [23]. SiC is capable of high-temperature operation of theoretically up to 600°C. This in turn proves that it is capable of operating at 4 to 5 times higher temperature than that of Si. Higher breakdown electric field allows for thinner and more highly doped devices. Since it can be made thinner and doped higher, faster switching speeds can be achieved with higher breakdown electric field. This faster switching speed comparison with simulation results is discussed in detail in later chapters. The electron mobility is less than that of Si, which is a disadvantage at low voltages, but electron mobility is not the only factor that determines the fast switching ability of a MOSFET. The lower on-resistance can save conduction loss and help high-frequency application to an extent. At lower temperatures, there is an overall decrease in the on-resistance for the MOSFET [4]. The fast reverse-recovery time t_{rr} of the body diode of the SiC MOSFET plays an important role in switching times of the MOSFET. Another advantage is the ability to operate at high temperatures when compared to Si, which gives rise to the potential to operate at higher power densities. Si MOSFETs lack the ability to operate at such high power densities [13]. All this is possible only due to the fundamental properties of the devices. A comparison between different semiconductor material properties is given in Table 1.

Table 1: Fundamental properties of Si, SiC, and GaN at room temperature

Property	**6H-SiC**	**4H-SiC**	**GaN**	**Si**
Energy Bandgap (eV)	2.9	3.26	3.39	1.12
Breakdown Electric Field (MV/cm)	2.5	2.2	3.3	0.25
Dielectric Constant	9.6	9.7	9.0	12.8
Intrinsic Carrier Concentration (cm^{-3})	10^{-6}	8.2×10^{-9}	1.9×10^{-10}	10^{10}
Electron Mobility μ_e (cm^2/ V·s)	330 to 400	700 to 980	2000	1400
Hole Mobility μ_h (cm^2/ V·s)	75	120	200	450
Saturated Electron Drift v_{sat} (cm/s)	1.9×10^{7}	2.7×10^{7}	1.5×10^{7}	10^{7}
Thermal Conductivity (W/m· K)	490	370	130	150
Density (g/cm^3)	3.2	3.2	6.15	2.3

2.3 Gallium Nitride (GaN) MOSFET

Gallium nitride (GaN) is another compound semiconductor material like SiC. For a few years now, many such materials have been used in the manufacturing of MOSFETs. Some have been successful and others have their limitations. Gallium nitride is one such device, which has been successfully implemented in the manufacturing of MOSFETs. Gallium Nitride on different substrates has been developed and tested. One such substrate, which proved very efficient and economical, is the traditional low cost silicon. Generally, sapphire, silicon, and silicon carbide are used, but silicon and silicon carbide are more expensive when compared to sapphire. Silicon is proven to be excellent in terms of quality and thermal resistance and greatly influence the on-state resistance of the MOSFET $r_{DS(ON)}$ by providing a lesser $r_{DS(ON)}$ when compared to sapphire. Using a silicon substrate proves more cost effective than a full Si MOSFET [19]. It has been observed that the silicon substrate does not hinder the performance of nitride semiconductors and gives much flexibility for fabrication of new advanced nitride semiconductors [16]. Such GaN devices are called heteroepitaxial as the substrate is a different material. The $BFOM$, $JFOM$, and $MFOM$ of GaN are as follows.

$$BFOM_{(GaN)} = \epsilon_r \epsilon_0 \mu_n {E_G}^3 = 9 \times 8.8542 \times 10^{-14} \times 2000 \times (3.39)^3 = 62.6 \times 10^{-9} \quad \mathrm{C^4Vcm/s}, \tag{2.17}$$

$$JFOM_{(GaN)} = \frac{E_{BD} v_{sat}}{2\pi} = \frac{(3.5 \times 10^6) \times 1.5 \times 10^7}{6.28} = 83.59 \times 10^{11} \quad \mathrm{V/s}, \tag{2.18}$$

$$MFOM_{(GaN)} = \epsilon_r \epsilon_0 \mu_n {E_{BD}}^3 = 9 \times 8.8542 \times 10^{-14} \times 2000 \times (3.5 \times 10^6)^3 = 68330 \quad \mathrm{MW/cm^2}, \tag{2.19}$$

$$KFOM_{(GaN)} = 1.3\sqrt{\frac{3 \times 10^6 1.5 \times 10^7}{4\pi 9}} = 820 \quad \text{mW/K} \cdot \text{s}. \tag{2.20}$$

The $MFOM$ value obtained clearly shows that the performance of GaN is much better than that of Si or SiC. In $BFOM$ and $JFOM$, higher the value, higher is the performance of a semiconductor material. A table comparing the different types of figures-of-merit for Si, SiC, and GaN is shown in Table 2.

With reference to Table 2, one can say that GaN semiconductor material's superior performance surpasses that of Si or SiC. GaN devices can work at high frequency due to the higher electron mobility formed by the two-dimensional electron gas (2DEG) between the GaN and AlGaN layers. This transistor is called high electron mobility transistor (HEMT) [18]. The two-dimensional electron gas induced by piezoelectric polarization effects presents the conventional Aluminium Gallium Nitride layer over Gallium Nitride (AlGaN/-GaN) HEMTs as depletion-mode (D-mode) transistors with a negative threshold voltage of around negative 4 V. Generally, the threshold voltage V_{th} depends on the aluminum (Al) composition, doping concentration, and the thickness of the AlGaN layer. A common technique called as gate-recess technique is used to shift the threshold voltage to positive. This is done by reducing the AlGaN thickness layer, which results in a reduced 2DEG density along with the help of gate metal work function, the threshold can be shifted positively. This leads to an E-mode or enhancement-mode transistor. A number of applications like RF, microwave, and digital circuits require E-mode transistors [18]. E-mode HEMTs provide safer operation and greater simplicity and low energy consumption. In spite of all these advantages described, the GaN transistors cannot compete with Si MOSFETs in terms of its ability to handle the growing amount of work in a capable manner and the level of integration. A cross-sectional view of E-mode GaN HEMT [27] is shown in Figure 2.6.

Table 2: Figures-of-merit of Si, SiC, and GaN semiconductor materials

Semiconductor material	$BFOM$ **(C**^{4}Vcm/s**)**	$JFOM$ **(V/s)**	$MFOM$ **(W/cm**^{2}**)**	$KFOM$ **(mW/K**$\cdot s$**)**
Silicon (Si)	2.22×10^{-9}	3×10^{11}	11.6×10^{6}	647
Silicon Carbide (SiC)	29.7×10^{-9}	94×10^{11}	8962×10^{6}	3017
Gallium Nitride (GaN)	62.6×10^{-9}	83.59×10^{11}	68330×10^{6}	820

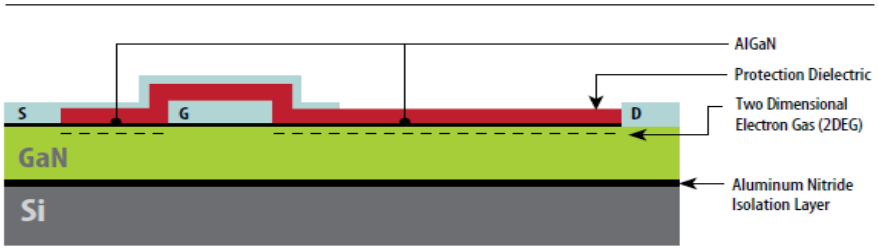

Figure 2.6: Cross-sectional view of E-mode GaN HEMT.

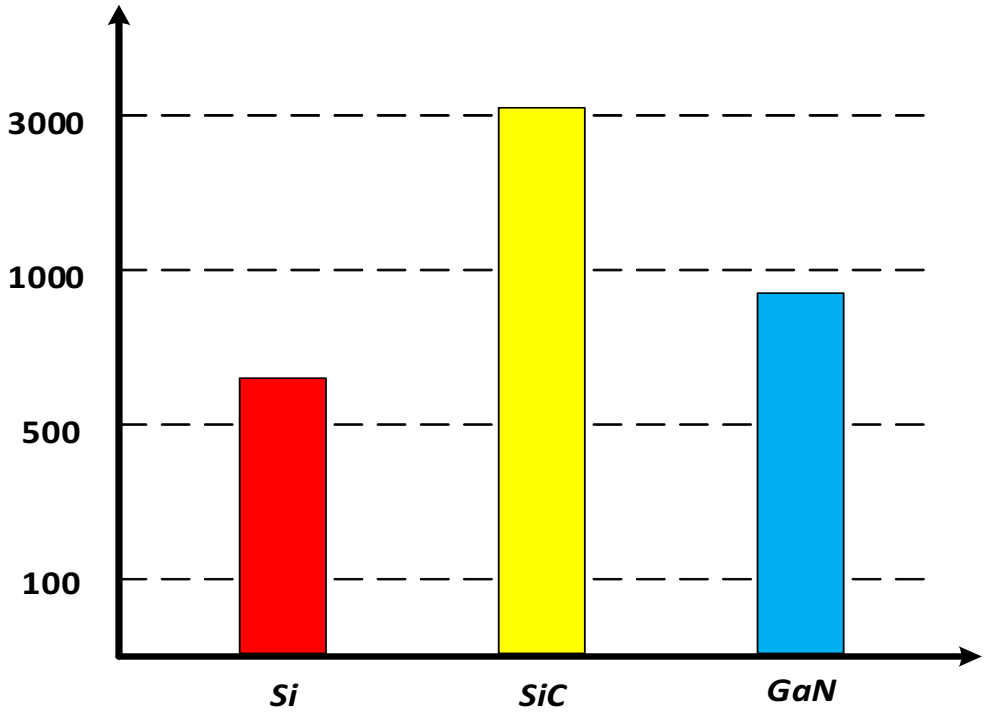

Figure 2.7: Comparison of Keyes figure-of-merit ($KFOM$) of Si, SiC, and GaN semiconductor materials.

$$\frac{BFOM_{(GaN)}}{BFOM_{(Si)}} = \frac{62.6}{2.22} = 28. \tag{2.21}$$

$$\frac{MFOM(GaN)}{MFOM(Si)} = \frac{68330}{11.6} = 5890. \tag{2.22}$$

$$\frac{JFOM_{(GaN)}}{JFOM_{(Si)}} = \frac{83.59 \times 10^{11}}{3 \times 10^{11}} = 28. \tag{2.23}$$

$$\frac{KFOM_{(GaN)}}{KFOM_{(Si)}} = \frac{820}{647} = 1.2. \tag{2.24}$$

GaN semiconductor maetrials performance is superior to Si semiconductor material with respect to the ratio figures-of-merit given above (2.21)-(2.24). When comparison is made with respect to SiC semiconductor material (2.25)-(2.28), GaN materials performance is less considering $JFOM$ and $KFOM$. The performance is almost the same as that of SiC when $JFOM$ is considered and is 8 times more than that of SiC when $MFOM$ is considered (2.8). The increase in performance of GaN semiconductor material when $BFOM$ is due to the enhanced mobility of electrons of GaN material, which is $\mu_{n(GaN)} = 2000$.

$$\frac{BFOM_{(GaN)}}{BFOM_{(SiC)}} = \frac{62.6}{29.7} = 2.1. \tag{2.25}$$

$$\frac{MFOM_{(GaN)}}{MFOM_{(SiC)}} = \frac{68330}{8962} = 7.6. \tag{2.26}$$

$$\frac{JFOM_{(GaN)}}{JFOM_{(SiC)}} = \frac{83.59 \times 10^{11}}{94 \times 10^{11}} = 0.88. \tag{2.27}$$

$$\frac{KFOM_{(GaN)}}{KFOM_{(SiC)}} = \frac{820}{3017} = 0.27. \tag{2.28}$$

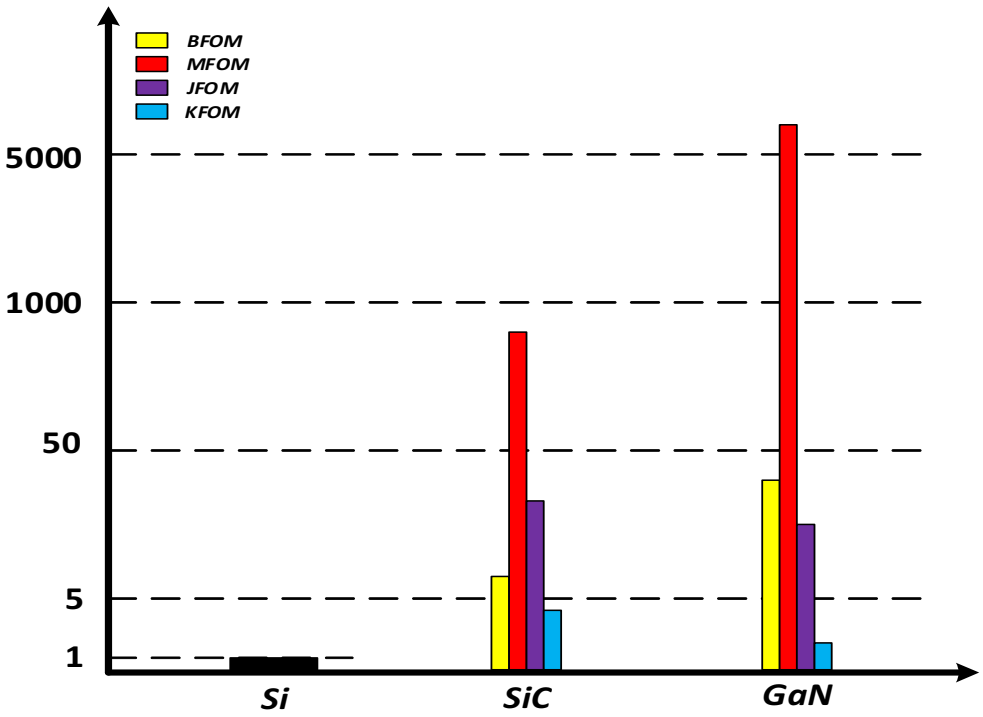

Figure 2.8: Comparison of Figures-of-merit of SiC and GaN semiconductor materials with respect to that of Si semiconductor material.

GaN HEMTs are lateral devices and are very similar to Si MOSFETs. As silicon substrates prove to be cost effective, they are the most commonly used substrates to build GaN transistors. A very thick layer of gallium nitride is grown on the silicon substrate. This layer provides a foundation to build the GaN transistor. An electron generating material is applied, which creates a layer highly abundant of electrons. The GaN transistor works similar to that of silicon MOSFET with a few exceptions. In silicon, the electrons are trapped in the lattice unlike GaN where the electrons are pooled. This results in low resistance of the channel. When the applied bias is removed, the electrons are dispersed back in-to the GaN, making it able to block voltage again [26]. The impact of the resistance increasing the blocking voltage is low when compared to silicon. This is explained in literature [26]. The on-state resistance $r_{DS(ON)}$ decreases with increase in the gate voltage. As the gate-to-drain capacitance C_{gd} is very low, it gives rise to fast voltage switching capability. Compared to

C_{gd}, the gate-to-source capacitance C_{gs} is very large, but still very small when compared to silicon. This results in the ability for excellent control at low duty cycle applications. Another major advantage is that the GaN transistor is a lateral device. The body diode function is different from that of silicon MOSFET but similar in function. The bipolar junction is absent, which is common in silicon MOSFETs. There are no holes involved in conduction and hence zero reverse recovery losses. Hence the output capacitance of the MOSFET C_{oss} has to be charged and discharged each cycle and GaN transistors have very low C_{oss} when compared to silicon [26]. Enhancement mode p-channel transistors are proven to be less efficient and are still under development. One can say that the GaN transistors have disadvantages as they are lateral devices. One of them is that the lateral devices require more space than vertical ones. Overall GaN on Si HEMTs prove to be highly efficient at low-voltage switching applications.

2.3.1 Summary

Based on the materials and their properties seen in Table 1, one can summarize as follows [22]:

1) GaN semiconductor materials performance in reference to $BFOM$ is much higher when compared to that of Si or SiC.

2) GaN on Si technology is already on the verge of dominating the power electronics field.

3) GaN on Si HEMTs may replace conventional Si MOSFETs in low-voltage switching applications in the market.

4) SiC devices will dominate switching applications at higher voltages beyond 500 V and for high power applications. This is because,

5) Homoepitaxial SiC is lower in cost compared to heteroepitaxial GaN on SiC [22].

6) GaN on Si is easier to build when compared to GaN on SiC.

7) GaN on Si may be good for low voltages but higher voltage devices do not exist as of now.

8) GaN on Si HEMTs do not have higher thermal conductivity when compared to SiC MOSFETs and hence when it comes to operation at higher temperatures, SiC is the obvious choice.

On the whole, we can conclude that for higher power applications, homoepitaxial SiC is preferred and GaN on Si HEMTs might win over SiC for low voltage applications [22],[16] and [17].

3 Operation and Design of DC-DC Buck Converter in CCM

3.1 Operation

Circuit diagram of a buck converter is shown in Figure 3.1. It mainly consists of a MOSFET S and a diode D. The output filter network consists of an inductor L, a capacitor C, and a load resistor R_L. The MOSFET S, along with the diode D, makes up for the switching network of the buck converter. The switching network chops or cuts down the dc input voltage V_I and produces a square wave to the input of the $L - C-_L$ filter. The $L-C-R_L$ low-pass filter converts the square wave to an average output voltage V_O [1]. The MOSFET here is controlled by a Pulse Width Modulator (PWM), which turns the MOSFET ON and OFF at a switching frequency where $f_s = 1/T$. The duty cycle D is given by

$$D = \frac{t_{ON}}{t_{ON} + t_{OFF}} = f_s t_{ON} = \frac{t_{ON}}{T}, \tag{3.1}$$

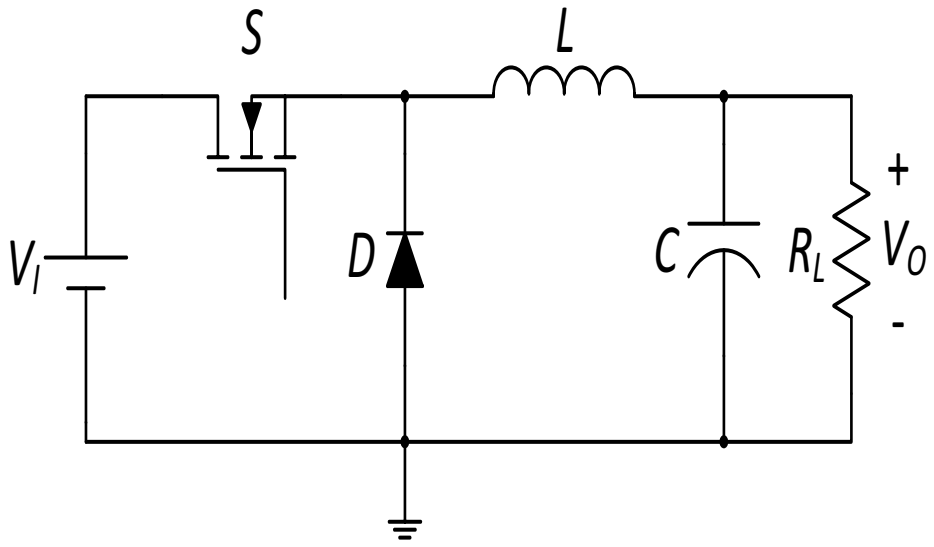

Figure 3.1: Circuit diagram of dc-dc buck converter.

As this thesis is based on the characterization of MOSFET at different switching

frequencies, the gate driver used here is ideal in nature. The gate driver is represented by its Thevenin's equivalent voltage source v_{GS}. An ideal driver is used in order to check the switching limit of the MOSFET and due to the lack of availability of high speed drivers. Generally the buck converters are difficult to drive as the gate of the MOSFET is not referenced to ground. Since the MOSFET driver voltage is rectangular and the MOSFET is turned ON at a high voltage, buck converter is operated at hard switching. The buck converter can operate both in continuous conduction mode (CCM)or in dis-continuous conduction mode (DCM). In this thesis, analysis is made based on the buck converter operating in CCM. The buck converter operating principle is explained with reference to Figure 3.2. The driving voltage applied to the MOSFET S turns the MOSFET ON at time $t = 0$. The diode D voltage at $t = 0$ is $v_D = -V_I$ and is reverse biased. The inductor current starts increasing with a slope of $(V_I - V_O)/L$. The inductor flows through the MOSFET S and hence, switch current $i_S = i_L$ [1].

At time $t = DT$, the MOSFET is turned OFF. Since the conduction is continuous, the inductor current continues to flow in the same direction. Now the inductor L, starts to act like a current source and turns the diode D ON and the MOSFET voltage reaches V_I. The inductor current starts to decrease with a slope of $-V_O/L$. At this moment, since the source is disconnected from the circuit, the inductor along with the capacitor maintains the output voltage V_O and output current I_O [1].

The switching network, which comprises of the MOSFET S and the diode D convert the source voltage V_I into a square wave to the input of the $L-C-R_L$ filter. The $L-C-R_L$ filter acts as a second order low pass filter and converts the square wave from the switching network into a dc output voltage with low-ripple. The average output voltage V_O is equal to the square wave average. The width of the square wave is the ON time of the MOSFET S, which is controlled by the duty cycle D [1]. The average value of the square wave is $V_O = DV_I$. The duty cycle D can be varied from zero to 100%, but the practical range is

only from 5% to 95% due to resolution. This means that the output voltage can be varied from zero to V_I depending on the duty cycle D. The maximum value of drain-to-source voltage v_{DS} is given by equation (3.3). The amount of energy transferred from the source V_I to the load can be controlled by ON time of the duty cycle [1]. Waveforms of drain-to-source voltage v_{DS}, gate-to-source voltage v_{GS}, diode voltage V_D, switch current i_S, and inductor current i_L are shown in Figure 3.2. The inductor current i_L rises for the duration $0 - DT$ for a maximum value of Δi_L.

$$\Delta i_L = \frac{V_O(1-D)}{f_S L} = 20 \text{ A}, \tag{3.2}$$

$$v_{DS} = V_I. \tag{3.3}$$

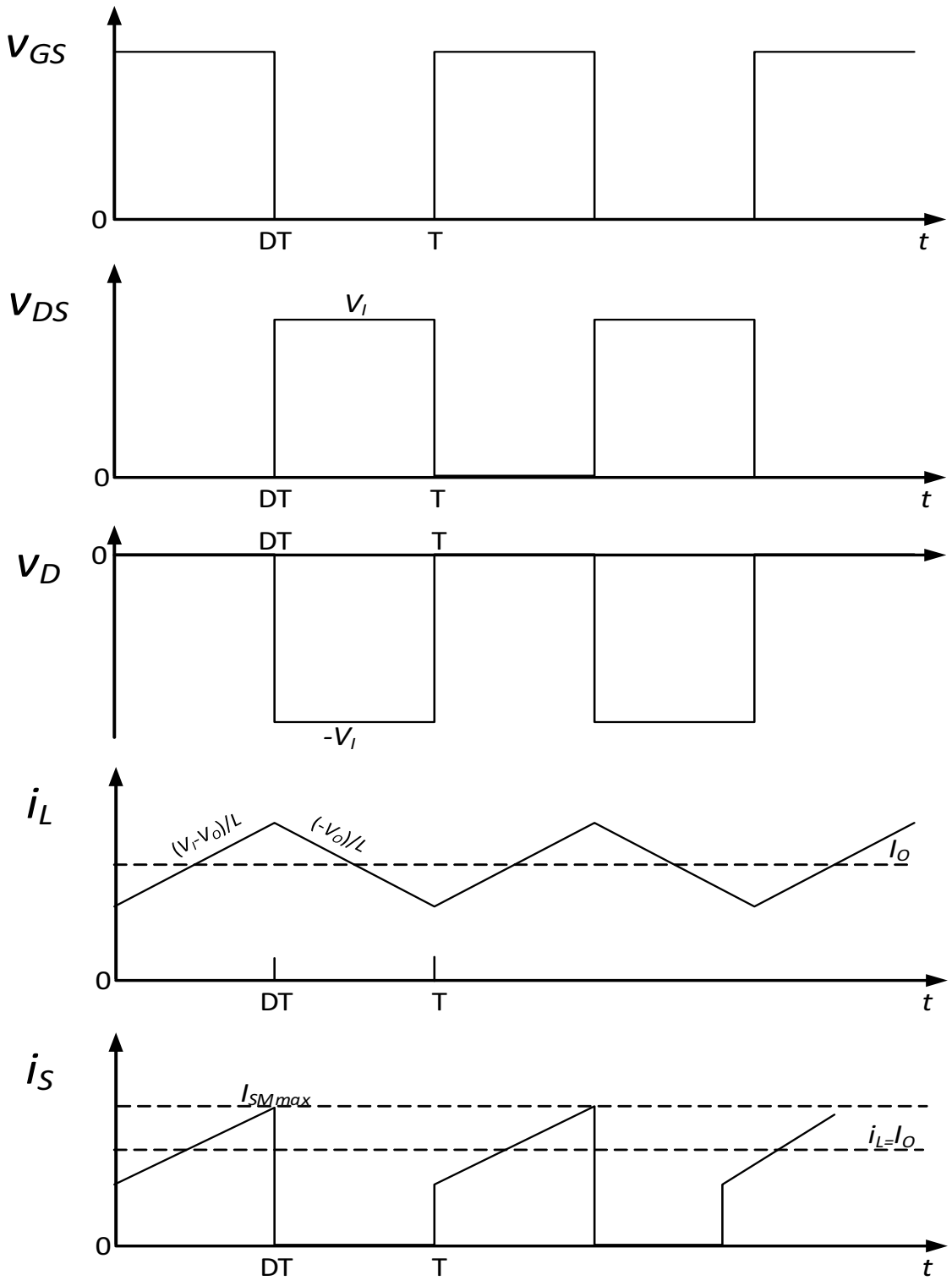

Figure 3.2: Key switching waveforms of the dc-dc buck converter in CCM [1].

3.2 Design Consideration for Buck Converter in CCM

The design equations used here is for buck converter in CCM derived from literature [1] for $V_I = 28$ V, $V_O = 12$ V, $I_{Omin} = 1$ A, $I_{Omax} = 10$ A, $V_r/V_O \leq 1\%$.

$$P_{Omax} = V_O I_{Omax} = 12 \times 10 = 120\,\text{W}. \tag{3.4}$$

$$P_{Omin} = V_O I_{Omin} = 12 \times 1 = 12\,\text{W}. \tag{3.5}$$

$$R_{Lmin} = \frac{V_O}{I_{Omax}} = \frac{12}{10} = 1.2\,\Omega. \tag{3.6}$$

$$R_{Lmax} = \frac{V_O}{I_{Omin}} = \frac{12}{1} = 12\,\Omega. \tag{3.7}$$

The voltage transfer function is given by

$$M_{VDC} = \frac{V_O}{V_I} = \frac{12}{28} = 0.43. \tag{3.8}$$

Assuming the converter efficiency to be 90%, the duty cycle D is given by

$$D = \frac{M_{VDC}}{\eta} = \frac{0.43}{0.9} = 0.48. \tag{3.9}$$

Starting with 100 kHz switching frequency, we get the inductor L and capacitor C values to be:

$$L_{min} = \frac{R_{Lmax}(1-D)}{2f_s} = 31.2\,\mu\text{H}, \tag{3.10}$$

$$\Delta i_L = \frac{V_O(1-D)}{f_S L} = 20\,\text{A}. \tag{3.11}$$

The ripple voltage V_r is given by

$$V_r = \frac{V_O}{100} = 120\,\text{mV}. \tag{3.12}$$

The ESR of the capacitor C is given by

$$r_C = \frac{V_r}{\Delta i_L} = 60\,\text{m}\Omega. \tag{3.13}$$

The value of the capacitance C is given by

$$C = \frac{D}{2 f_s r_C} = 383\,\mu\text{F}. \tag{3.14}$$

The inductance L and the capacitance C are frequency dependent. They reduce in size as the frequency increases. Hence the values of the components are re-designed every time there is a change in the switching frequency f_s. The inductor L and capacitor C values designed for different switching frequency f_s are shown in Table 3.

Table 3: Values of inductance L and capacitance C for various switching frequencies f_s.

Switching frequency f_s	**Inductor** L	**Capacitor** C
100 kHz	4.05 μH	306.6 μF
500 kHz	0.8 μH	61.3 μF
1 MHz	0.4 μH	30.6 μF
2 MHz	0.205 μH	15 μF
3 MHz	0.135 μH	10 μF
5 MHz	81 nH	6.13 μF
10 MHz	0.04 μH	3 μF
20 MHz	0.02 μH	1.53 μF

3.3 Analysis of Buck Converter in CCM for switching Frequency f_s = 100 kHz to 500 kHz.

Let us consider 100 kHz switching frequency, which is considered low-frequency in this thesis. At this switching frequency, the buck converter, along with the MOSFET, works normally. The MOSFET, either Si or SiC or GaN, irrespective of which MOSFET is used, switches normally in line with the switching frequency f_s. The output of the buck converter V_O is as expected, along with the output power P_O and output current I_O. The values obtained from simulations, closely match the theoretical values calculated using the design equations.

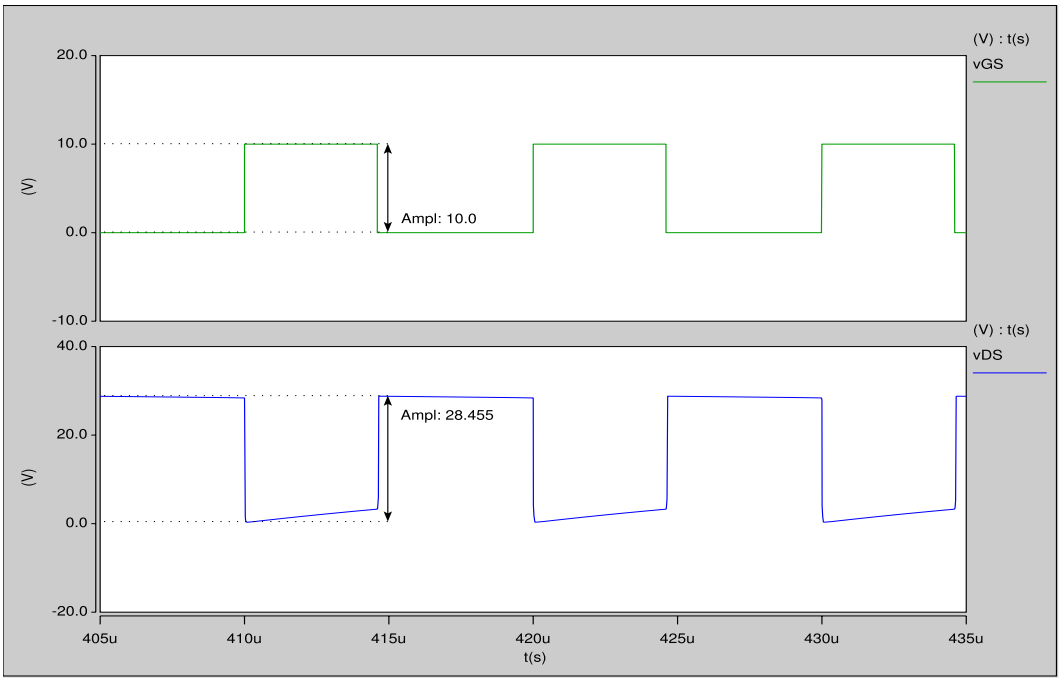

Figure 3.3: Drain-to-source voltage v_{DS} and gate-to-source voltage v_{GS} for silicon at $f_s = 100$ kHz.

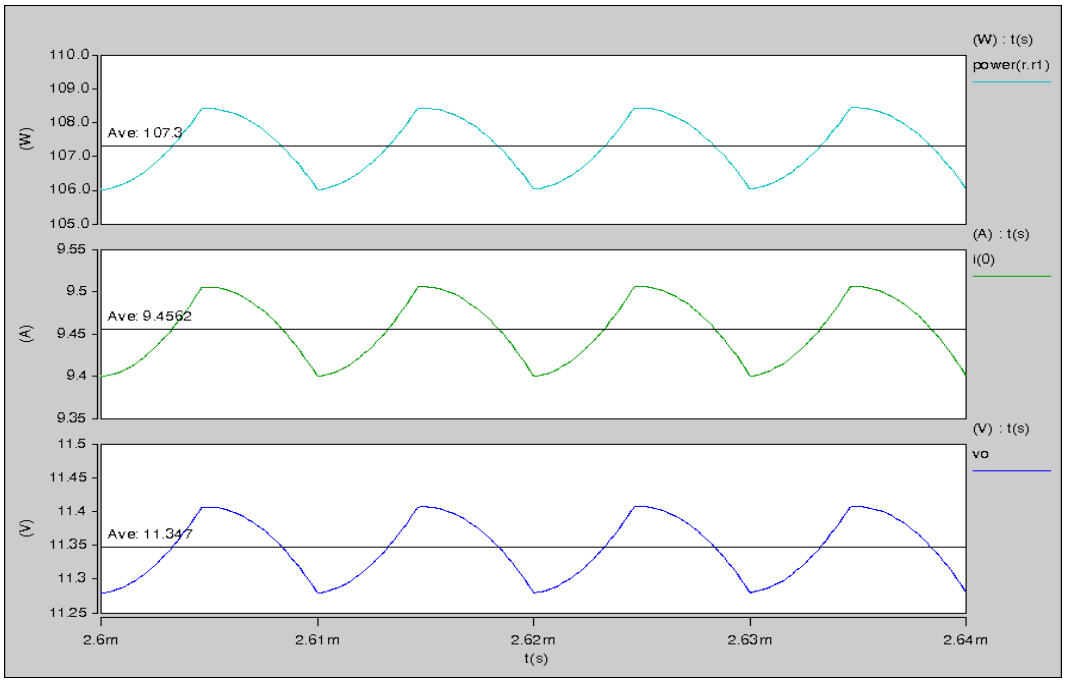

Figure 3.4: Output voltage V_O, output current I_O, and output power P_O for silicon at $f_s = 100$ kHz.

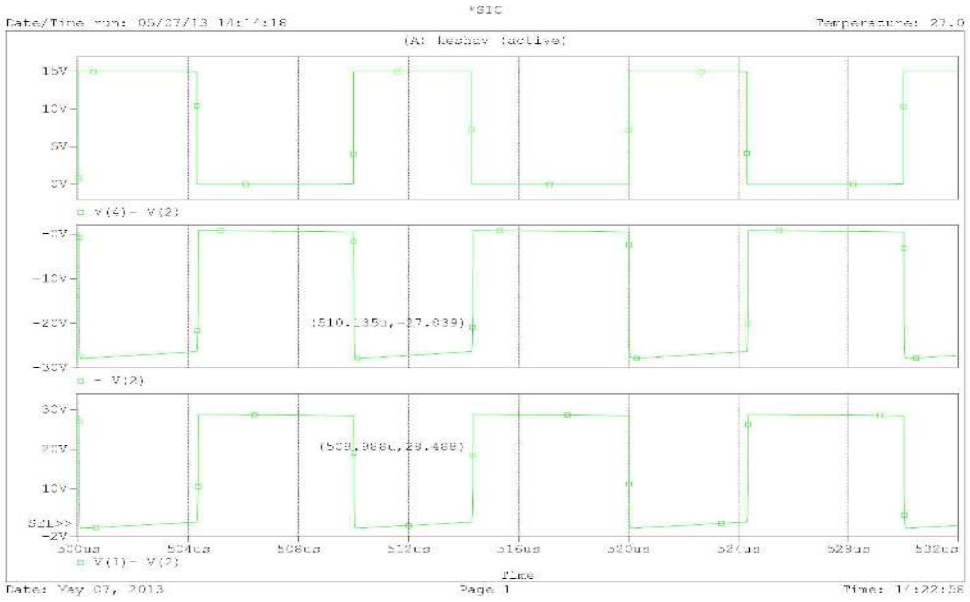

Figure 3.5: Drain-to-source voltage v_{DS} and gate-to-source voltage v_{GS} for silicon carbide at $f_s = 100$ kHz.

Simulation waveforms for switching frequency 100 kHz using Si, SiC, and GaN MOSFETs are shown in Figures 3.3, 3.4, 3.5, 3.6, 3.7, and 3.8. As the frequency is increased from 100 kHz to 500 kHz, the MOSFET power loss is expected to increase as it is directly proportional to the switching frequency f_s. This in turn results in a drop in the overall efficiency of the converter. The waveforms obtained do not differ much when compared to the waveforms obtained for f_s=100 kHz. This is because the switching frequency f_s is relatively low and all MOSFETs, i.e., Si, SiC, and GaN work normally and differ just in terms of their power loss. Simulation plots for switching frequency 500 kHz using Si, SiC, and GaN MOSFETs are shown in Figures 3.9, 3.10, 3.11, 3.12, 3.13, and 3.14.

The switching frequency f_s is within the low-frequency range and hence the MOSFETs response is fast enough for it to switch from zero to V_I. As the switching frequency is increased, the MOSFETs response time deteriorates. This response time gradually decreases and at a certain switching frequency f_s, the MOSFET starts to switch partially. This cut-off

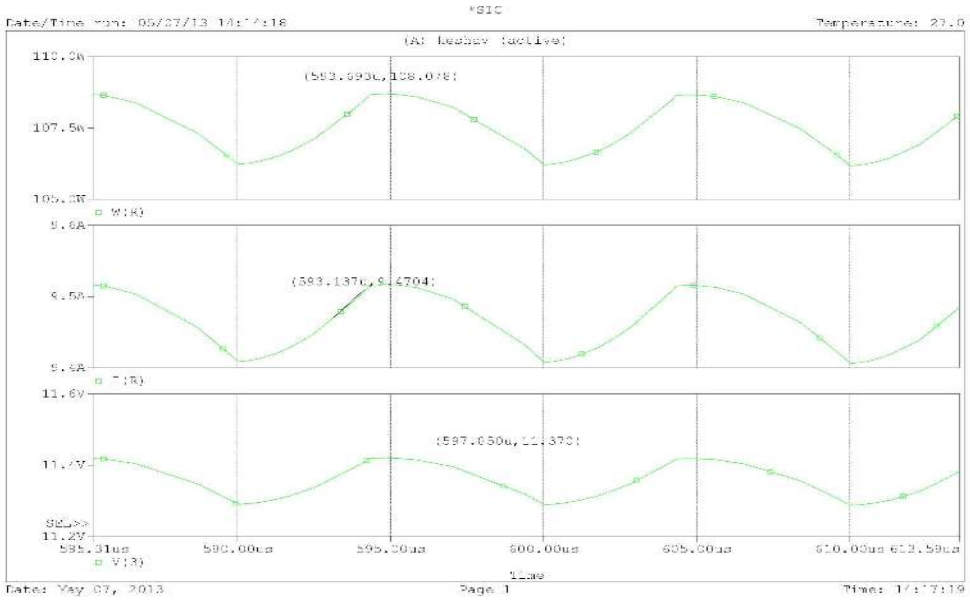

Figure 3.6: Output voltage V_O, output current I_O, and output power P_O for silicon carbide at $f_s = 100$ kHz.

switching frequency f_s can range anywhere from 500 kHz to 1 GHz depending on the type of MOSFET. Therefore, based on the waveforms obtained via simulations, it is clearly seen that all three MOSFETs, i.e., Si, SiC, and GaN MOSFETs work normally at low switching frequency f_s, i.e., 100 kHz to 500 kHz. Analysis beyond the low switching frequency range is made for Si, SiC, and GaN MOSFETs and is explained in the following chapter along with the waveforms obtained.

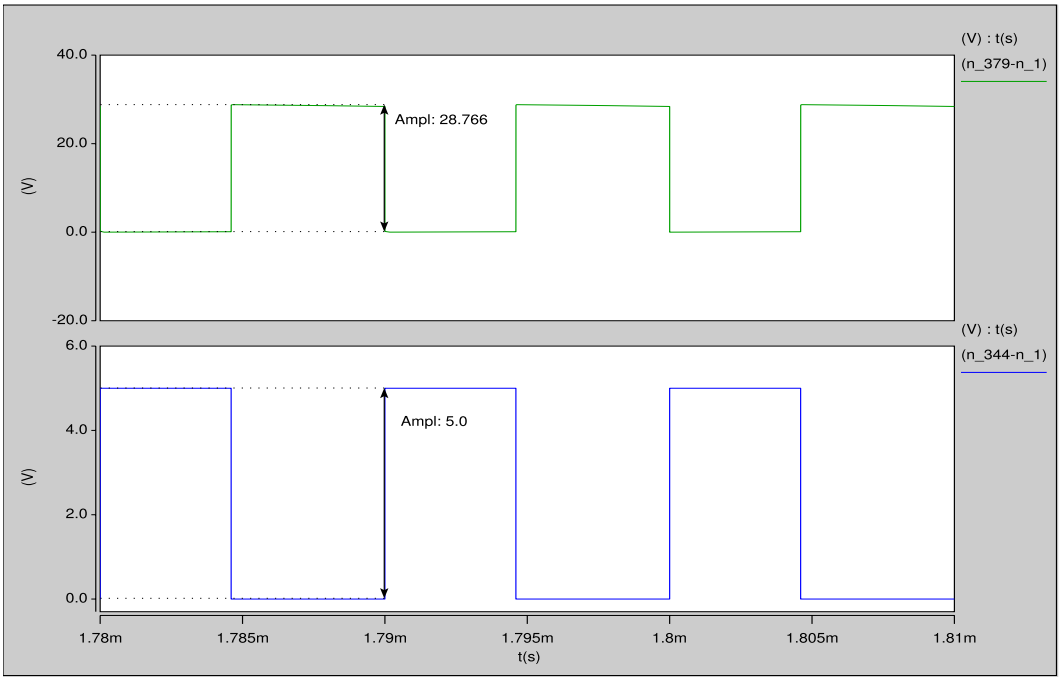

Figure 3.7: Drain-to-source voltage v_{DS} and gate-to-source voltage v_{GS} for gallium nitride at $f_s = 100$ kHz.

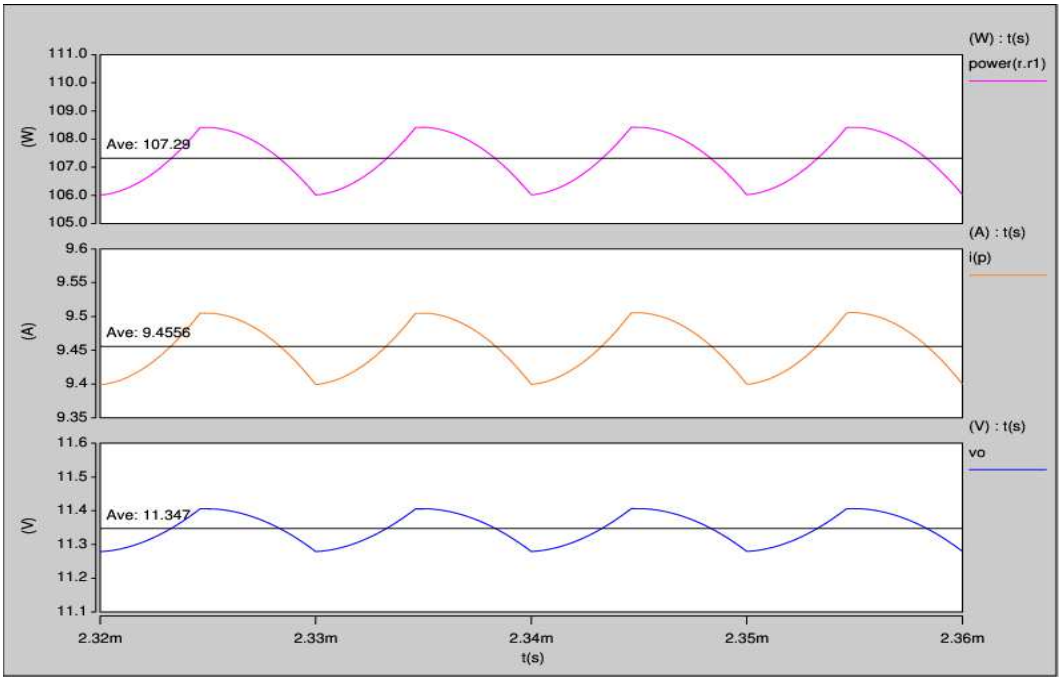

Figure 3.8: Output voltage V_O, output current I_O, and output power P_O for gallium nitride at $f_s = 100$ kHz.

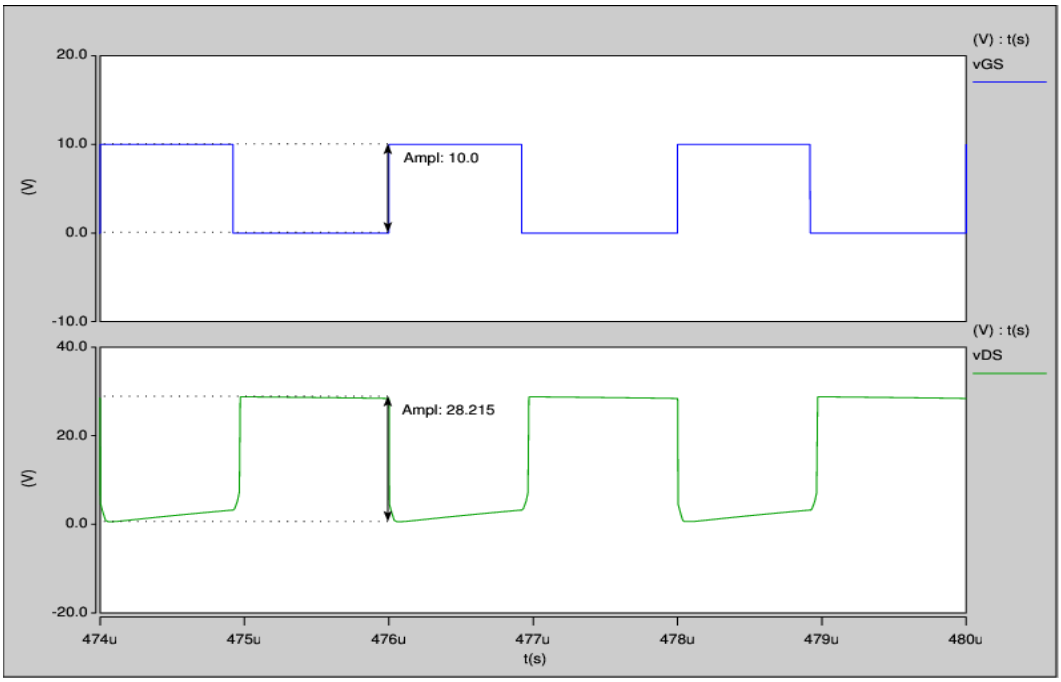

Figure 3.9: Drain-to-source voltage v_{DS} and gate-to-source voltage v_G for silicon at $f_s = 500$ kHz.

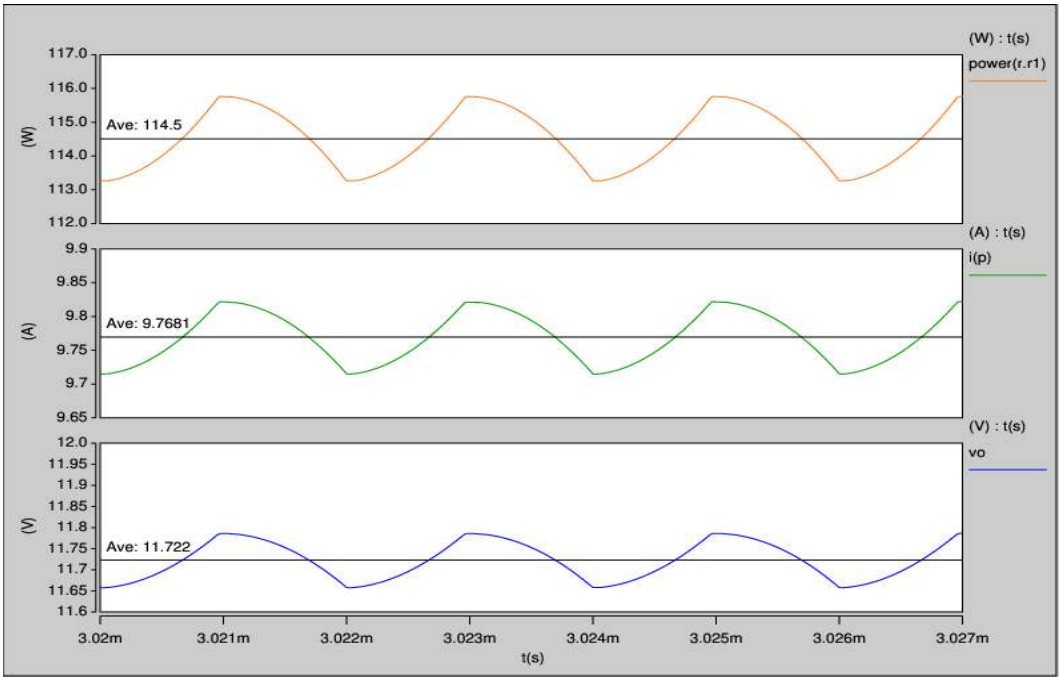

Figure 3.10: Output voltage V_O, output current I_O, and output power P_O for silicon at $f_s = 500$ kHz.

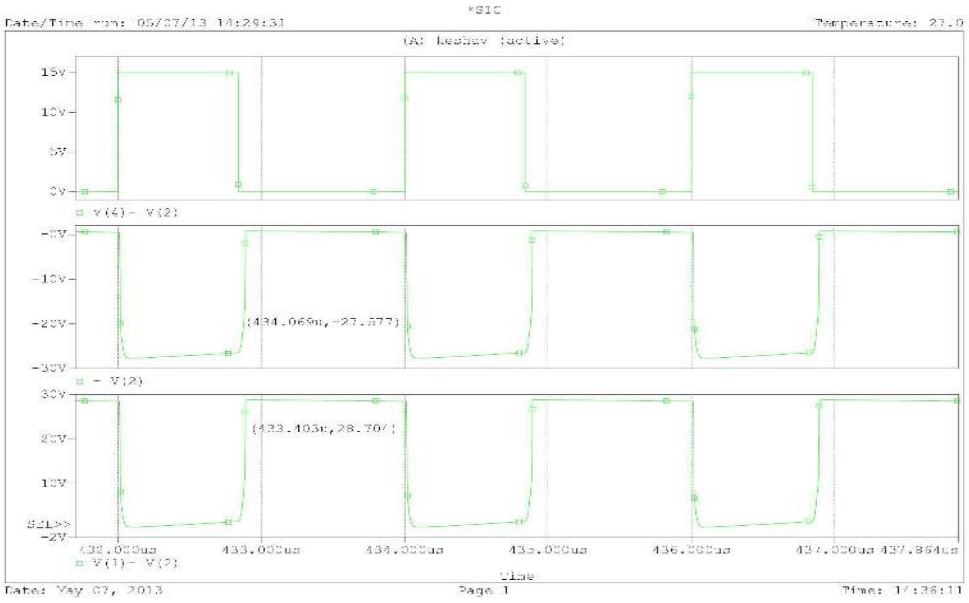

Figure 3.11: Drain-to-source voltage v_{DS} and gate-to-source voltage v_{GS} for silicon carbide at $f_s = 500$ kHz.

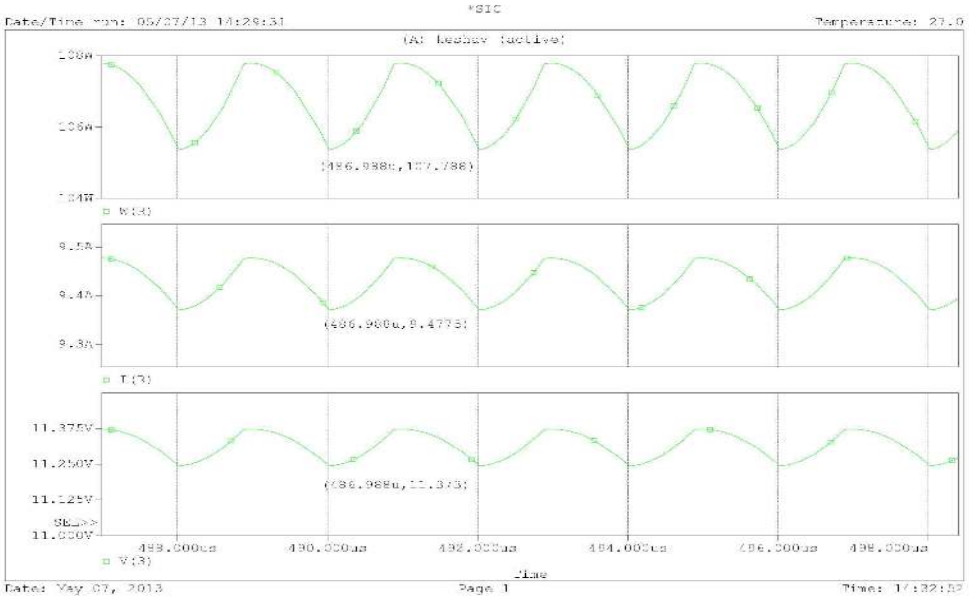

Figure 3.12: Output voltage V_O, output current I_O, and output power P_O for silicon carbide at $f_s = 500$ kHz.

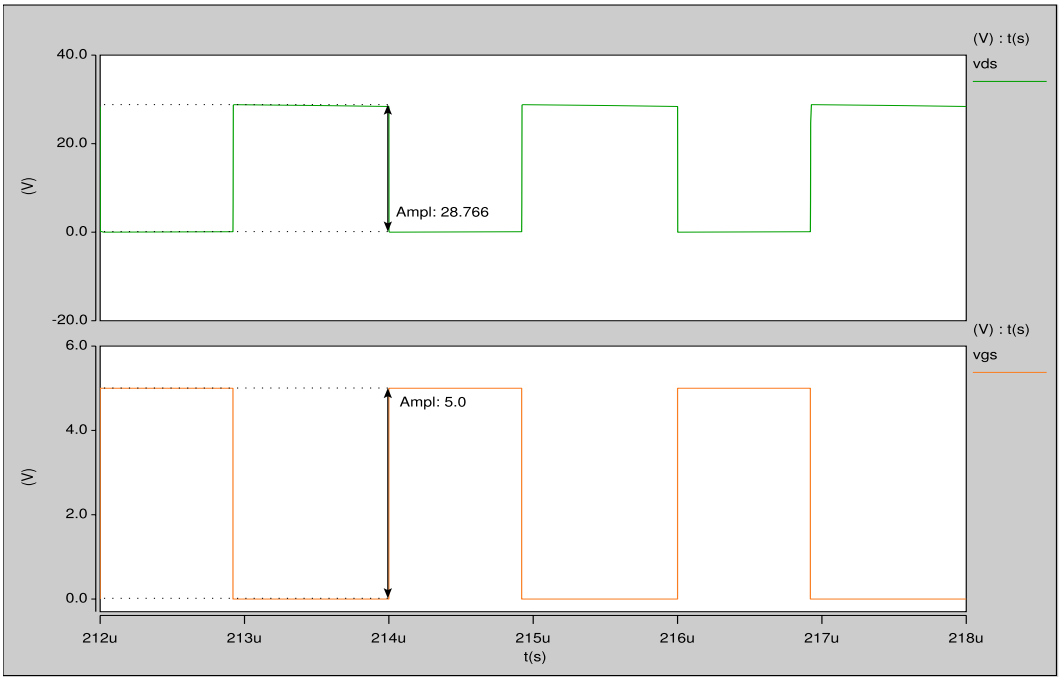

Figure 3.13: Drain-to-source voltage v_{DS} and gate-to-source voltage v_{GS} for gallium nitride at $f_s = 500$ kHz.

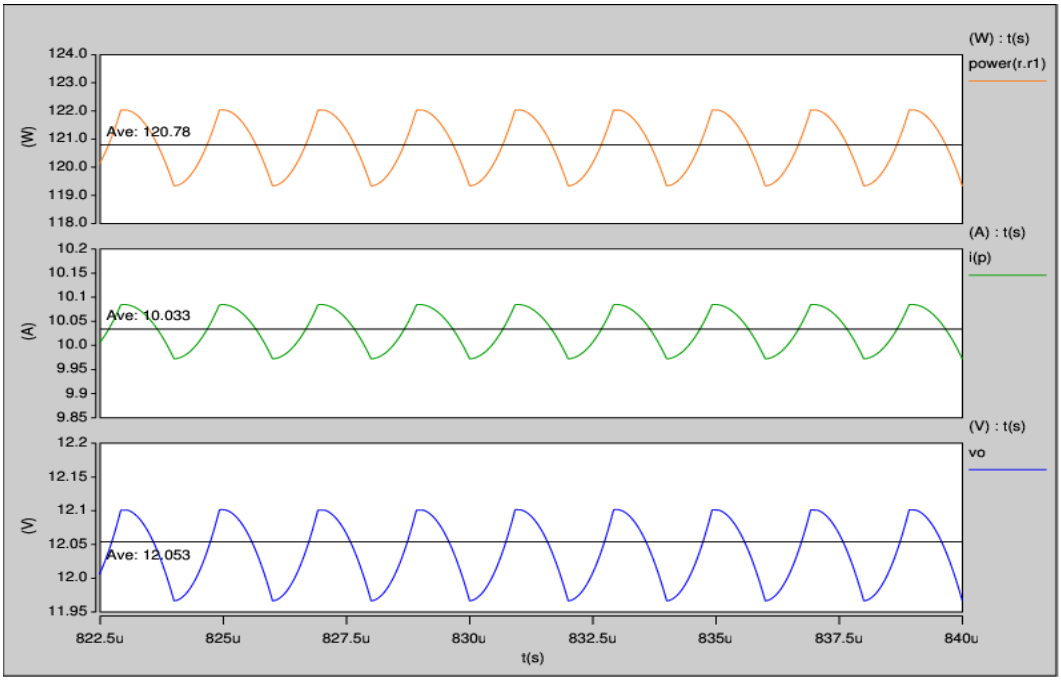

Figure 3.14: Output voltage V_O, output current I_O, and output power P_O for gallium nitirde at $f_s = 500$ kHz.

4 Analysis of Si, SiC, and GaN MOSFETs at Cut-Off Switching Frequency and at Very High Switching Frequency

Simulations were performed using SABER and PSpice simulation software. Due to the unavailability of suitable Silicon Carbide (SiC) MOSFET model, SiC MOSFET simulations were performed with PSpice. The obtained results via simulations show significant improvements in switching capabilities and their efficiencies based on the type of material used.

In this chapter, the cut-off switching frequency of each MOSFET is determined along with the analysis of each MOSFET at cut-off switching frequency. Once the cut-off frequency of each MOSFET is determined, evaluation is made at 4 to 5 times the cut-off switching frequency and this frequency is considered as high- frequency for each MOSFET in this thesis. The waveforms obtained via simulations is compared with theoretical assumptions made on each MOSFET for that frequency.

4.1 Exposition of Si, SiC, and GaN MOSFETs at Cut-off Switching Frequency

In this thesis, cut-off switching frequency is the frequency at which the MOSFET actually starts to gradually stop switching in-line with the switching frequency. A number of factors affect the efficient switching of the MOSFET like, Miller's plateau, parasitics of the MOSFET, and the resistances of the MOSFET. In integrated systems, capacitances of circuit nodes are due not only to the capacitance of gates to the nodes, but also include capacitances to ground of signal paths connected to nodes and other stray capacitances [2]. These are called parasitic capacitances. In high-frequency applications, the charging and discharging losses affect the systems efficiency. We cannot neglect the parasitic nature of the capacitances anymore as they play an important role in the switching times of the MOSFET. The charging and discharging losses are mainly due to the parasitic capacitances of the MOSFET, which are dynamic in nature and a non-linear function of switching frequency f_s. They usually tend to limit the frequency response. The MOSFET has parasitic capacitances between each of its terminals and are as shown in Figure 4.25 [7].

The output capacitance mainly includes the drain-to-source capacitance C_{ds} and gate-to-drain capacitance C_{gd}. These capacitances are strongly dependent on the voltage applied across them [7] and also depend on the geometry of the MOSFET. They vary with the drain-to-source voltage v_{DS}. Since the MOSFET's gate drive circuit is insulated from the rest, C_{ds} and C_{gd} are the only load to the MOSFET's gate drive circuit and influence switching times [7]. Hence, now we require time to supply charge to the parasitic capacitance too. Thus, its effect on the system is twice that of the parasitic capacitance to ground [3]. The gate resistance R_g presents an impedance like an RC network to its gate drive [31]. For this reason the RC network acts as a low-pass filter at high frequencies.

When voltage is applied to the gate, the rise in v_{GS} is brought about by charging C_{gs} and C_{gd}. At this time the drain-to-source voltage v_{DS} doesn't change much, C_{gd} and C_{ds}

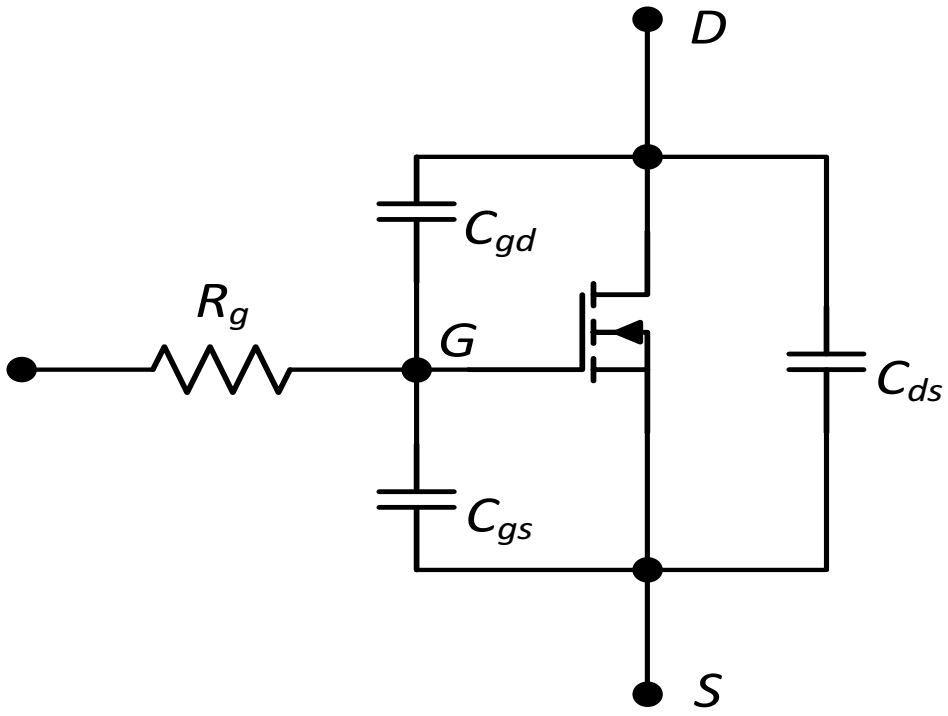

Figure 4.1: MOSFET model with parasitic capacitances and gate resistance.

remain constant as they are a function of v_{DS}. This is shown in Figure 4.2. The gate charge can be assumed to be Q_{gs} [31]. The Miller capacitance is a result of the overlap of the gate metallization and the n-minus region [5]. It is the point at which gate charge goes in to the plateau region and is in accordance with the peak value of current. We assume that the gate voltage at knee point is same as load current i_D. This is because current can reach its maximum value soon after left knee due to changes in values of i_D and output impedance. Generally, the miller plateau is to have a zero slope. If slope is non-zero, then the drive current flows into C_{gs}, else some current flows into C_{gd}. Q_{gd} is the charge injected into the gate. Once the plateau is finished, v_{DS} reaches it's ON state value. C_{gd} becomes constant again and entire current flows into C_{gs}. The slope is not as steep as before as C_{gd} is larger than C_{gs} [5].

The turn-off characteristics of the MOSFET is strongly influenced by the current

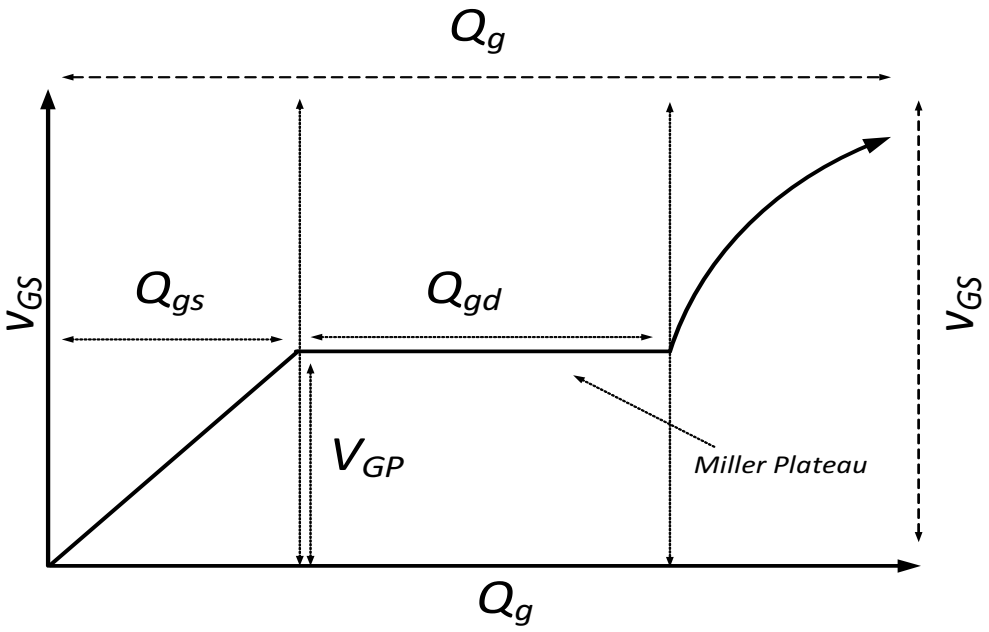

Figure 4.2: Detailed breakdown waveform of gate charge Q_g.

through the Miller capacitance. This situation is quite clear in the case of a MOSFET [5]. The gate driver issues concerned with the MOSFETs are not considered here as we are using an ideal driver for simulation purpose. On the whole, one can say that the parasitics of the MOSFET tend to limit the overall switching process at high frequencies. The MOSFET's maximum operating frequency can be determined by looking at the low-state and high-state time values, i.e., the turn-ON and turn-OFF values. Usually for a MOSFET to switch, the low-state value should be greater than the turn-OFF value and the high-state value should be greater than the turn-ON value. The turn-OFF and turn-ON values are calculated using the following equations where $t_{d(OFF)}$ and $t_{d(ON)}$ are the ON-time and OFF-time delays and t_f and t_r are the respective fall and rise times. For a MOSFET to switch normally, he low-state should be greater than the sum of $t_{d(OFF)}$ and t_f and the high-state should be greater than the sum of $t_{d(ON)}$ and t_r. This is the maximum operating limit of a MOSFET, but here we test the operating limit of a MOSFET in a DC-DC buck converter in CCM.

Hence, the MOSFET limit is expected to be well within the maximum operating limit and is evaluated.

$$T_{turn-OFF} = t_{d(off)} + t_f, \tag{4.1}$$

$$T_{turn-ON} = t_{d(on)} + t_r, \tag{4.2}$$

$$high - state > t_{d(on)} + t_r, \tag{4.3}$$

$$low - state > t_{d(off)} + t_f. \tag{4.4}$$

In power MOSFETs, there is basic trade-off between conductivity and the amount of charge required to turn the device ON and OFF. From this comes the figure-of-merit (FOM), which is also called RQ product. This is the device's on-resistance r_{DS} times the total charge supplied to the gate Q_g to turn the device ON and OFF at operating voltage and current. Better FOM leads to better switching efficiency at high frequencies in DC-DC converters [27].

The performance of a MOSFET is calculated using the figure-of-merit (FOM), which is given by

$$FOM = r_{DS} \times Q_g. \tag{4.5}$$

4.1.1 Silicon (Si) MOSFET

The silicon MOSFET's maximum operating limit was calculated using the equations (

$$t_{d(off)} = 150 \text{ ns}, \tag{4.6}$$

$$t_f = 75 \text{ ns}, \tag{4.7}$$

$$t_{d(off)} + t_f = 225 \text{ ns}, \tag{4.8}$$

$$low - state > 225 \text{ ns}, \tag{4.9}$$

$$t_{d(on)} = 35 \text{ ns}, \tag{4.10}$$

$$t_r = 65 \text{ ns}, \tag{4.11}$$

$$t_{d(on)} + t_r = 100 \text{ ns}, \tag{4.12}$$

$$high - state > 100 \text{ ns}. \tag{4.13}$$

Consider switching frequency of 800 kHz. Si MOSFET for this switching frequency, switches normally as it does at lower frequencies. The waveforms of drain-to-source voltage v_{DS}, gate-to-source voltage v_{GS}, output voltage V_O, output current I_O, and output power P_O for 800 kHz are shown in Figures 4.3 and 4.6. At this switching frequency, the drain-to-source voltage v_{DS} is perfectly in-line with the switching frequency f_s. The MOSFET works normally, and the buck converter steps down the input voltage V_I. As we increase the switching frequency f_s, the MOSFET abnormalities are seen. For 900 kHz switching frequency, it can be observed that the amplitude of the drain-to-source voltage v_{DS} is almost equal to input voltage V_I. This is shown in Figure 4.4. The output voltage current V_O and output power P_O are as expected and matches the theoretical design values. When the frequency is taken up to 1 MHz, the amplitude of the MOSFET's drain-to-source v_{DS} starts decreasing.

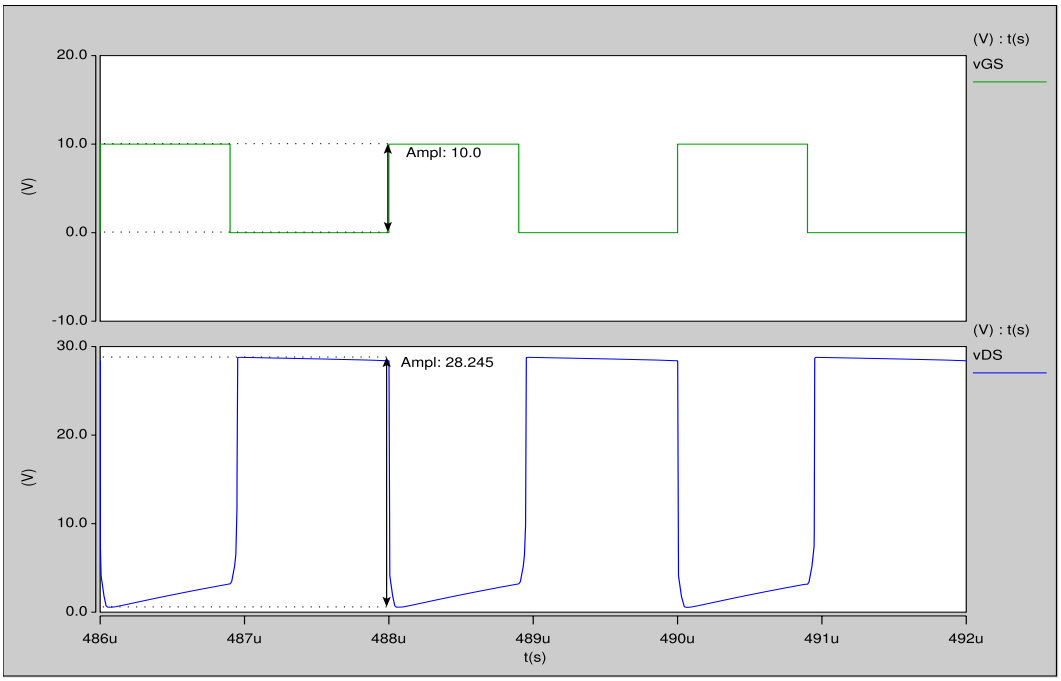

Figure 4.3: Drain-to-source voltage v_{DS} and gate-to-source voltage v_{GS} at $f_s = 800$ kHz.

$$f_s = 1 \text{ MHz}, \tag{4.14}$$

$$T = 1/f_s = 1\ \mu\text{s}, \tag{4.15}$$

$$D = 0.46, \tag{4.16}$$

$$t_{ON} = DT = 0.48 \times 1\ \mu\text{s} = 0.48\ \mu\text{s}, \tag{4.17}$$

$$t_{ON} = 0.48\ \mu\text{s} > 100 \text{ ns}. \tag{4.18}$$

The ON time of the MOSFET, i.e., the high-state value is much greater than 100 ns, which is well under the maximum operating limit of Si MOSFET. This data is obtained from SABER simulations and the waveforms are as shown in Figures 4.5 and 4.8. At the cut-off switching frequency, the MOSFET drain-to-source voltage v_{DS} peak does not exactly reach the maximum value of V_I. The perfect square switching waveform tends to curve slightly towards the falling and the rising edges. This is due to the MOSFET parasitics and the

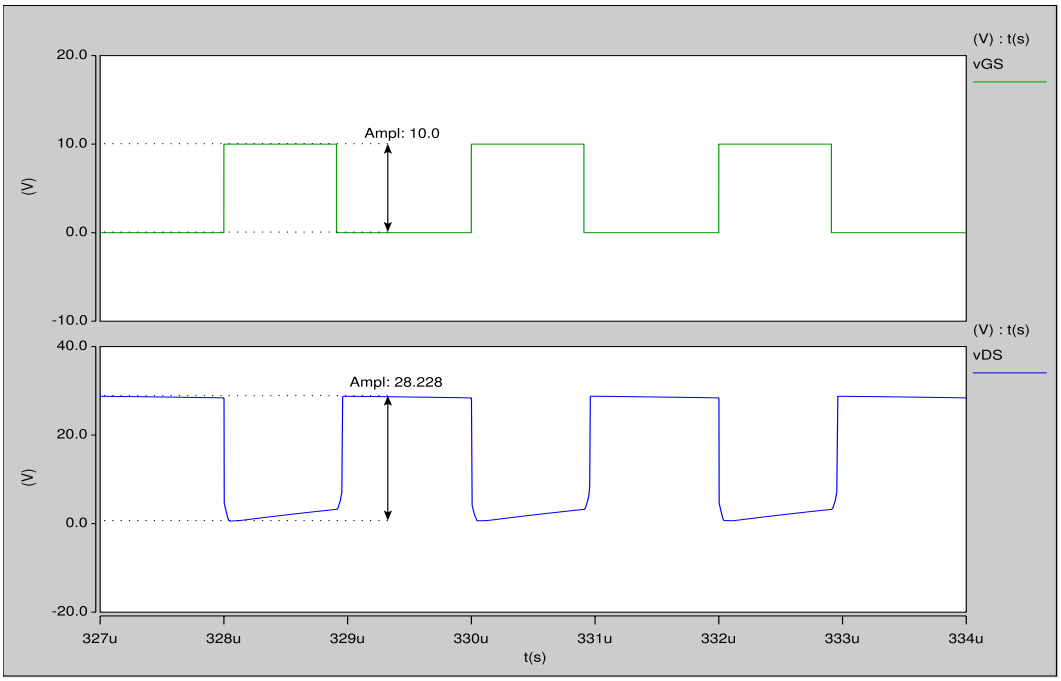

Figure 4.4: Drain-to-source voltage v_{DS} and gate-to-source voltage v_{GS} at $f_s = 900$ kHz.

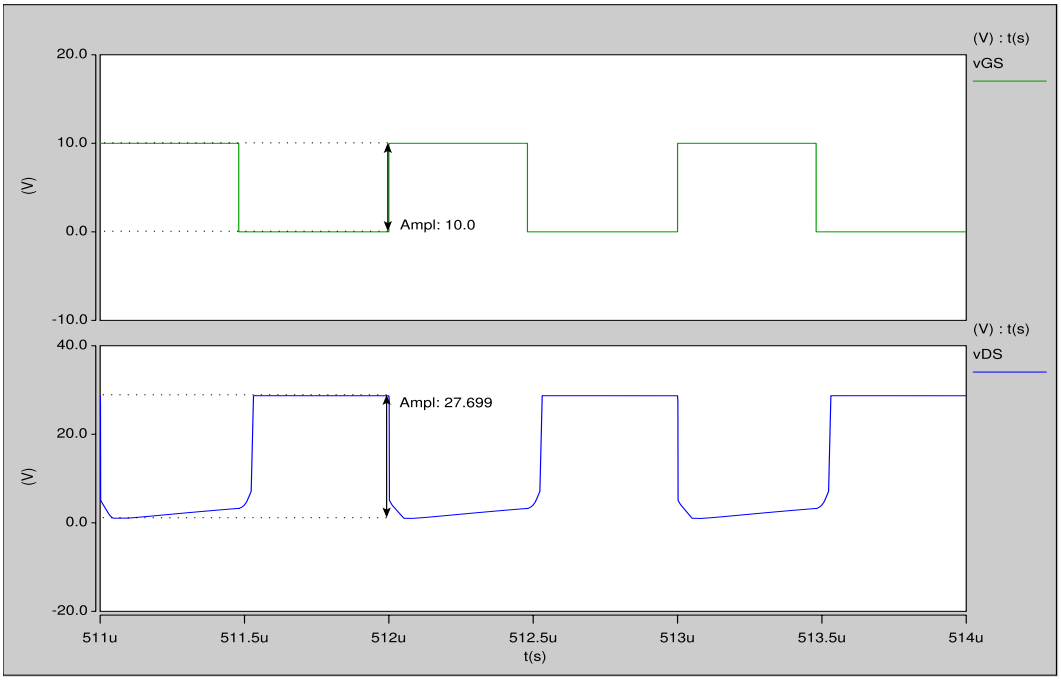

Figure 4.5: Drain-to-source voltage v_{DS} and gate-to-source voltage v_{GS} at $f_s = 1$ MHz.

RC network as explained above. The MOSFET v_{DS} doesnt switch in-line with the gate drive signal anymore. This is due to the high switching frequency f_s. Hence, the MOSFET starts to stop switching normally and gradually stops to work as a switch. This frequency is considered as breakdown frequency or cut-off switching frequency of the MOSFET in this thesis. The drain-to-source voltage v_{DS} amplitude starts decreasing gradually. As the switching frequency is high, the MOSFET's parasitics affect the MOSFET's response to switch normally. The MOSFET's drain-to-source voltage v_{DS} and gate-to-source voltage v_{GS} for 1 MHz is shown in Figure 4.5. As explained earlier, the MOSFET's parasitics are a non-linear function of switching frequency and hence, at high frequencies they play an important role in the response time of the MOSFET. The MOSFET has very limited time to turn ON and OFF perfectly. The effects of frequency beyond this breakdown frequency are discussed in the following section. Si MOSFETs figure-of-merit is calculated as follows (4.19).

$$FOM_{(Si)} = r_{DS} \times Q_g = 0.3 \times 110 \times 10^{-9} = 33 \times 10^{-9} \quad \text{V/s.} \tag{4.19}$$

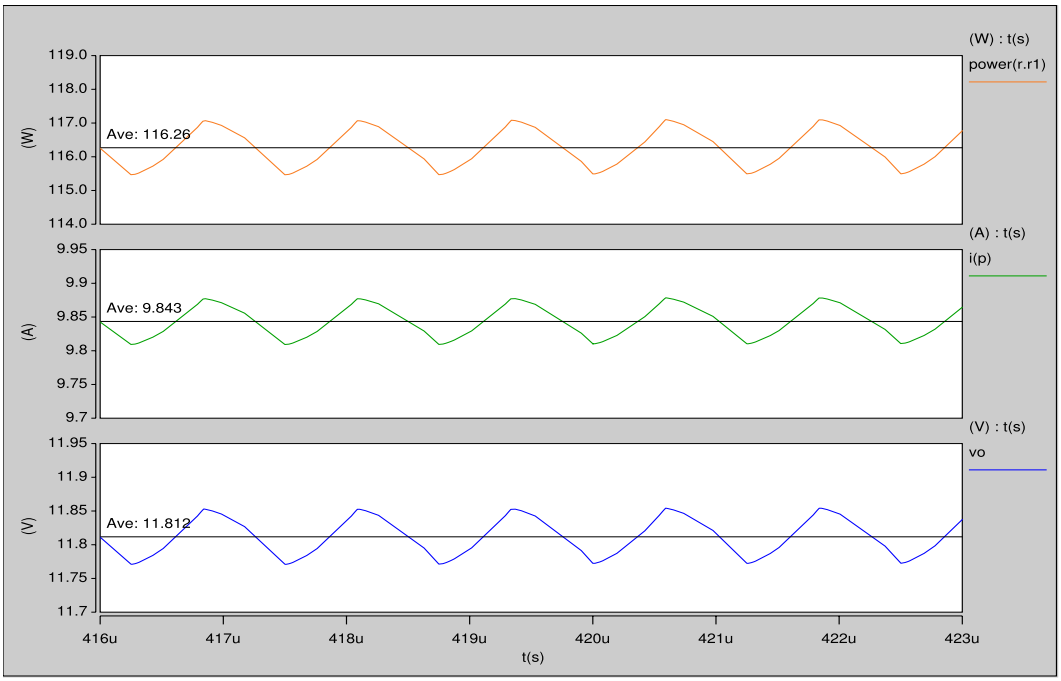

Figure 4.6: Output voltage V_O, output current I_O, and output power P_O at $f_s = 800$ kHz.

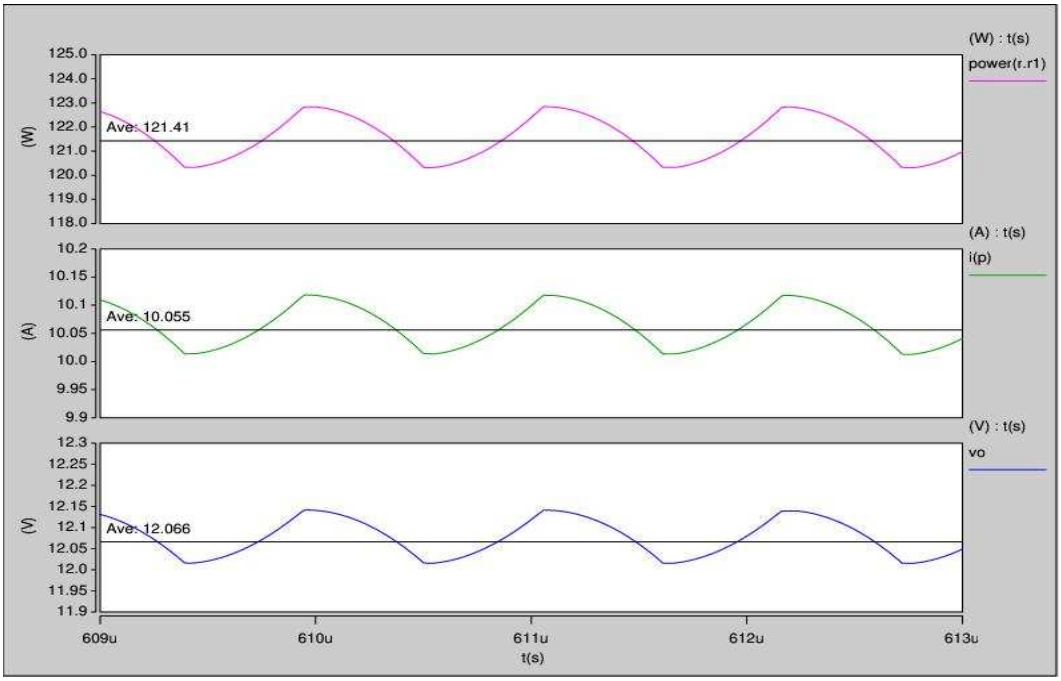

Figure 4.7: Output voltage V_O, output current I_O, and output power P_O at $f_s = 900$ kHz.

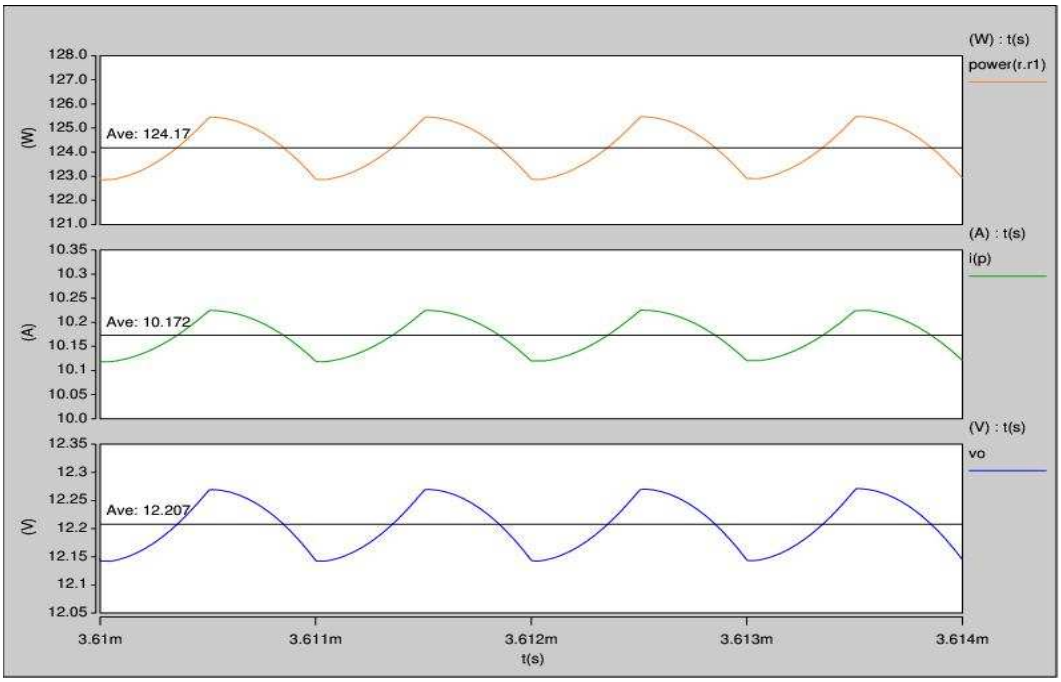

Figure 4.8: Output voltage V_O, output current I_O, and output power P_O at $f_s = 1$ MHz.

4.1.2 Silicon Carbide (SiC) MOSFET.

Based on the literature study, the SiC MOSFET operates efficiently at high temperatures and at high frequencies when compared to Si MOSFETs. One of the advantages over Si MOSFETs is, the Miller plateau is not as flat as observed in Si MOSFETs [33]. The SiC MOSFET, in theory, is more efficient and is capable of switching at frequencies greater than that of Si MOSFET. The SiC MOSFET used here is SCT2080KE from ROHM semiconductors. The specifications are as shown in the data sheet [35]. Due to the nature of the PSpice model used, the simulations of SiC MOSFET were carried out using PSpice simulation software. The maximum operating limit of silicon carbide (SiC) MOSFET was calculated and is shown in equations (4.29)-(4.33). Silicon carbides FOM and K_C is shown in equation (4.28).

$$t_{d(OFF)} = 76 \text{ ns}, \tag{4.20}$$

$$t_f = 22 \text{ ns}, \tag{4.21}$$

$$t_{d(off)} + t_f = 98 \text{ ns}, \tag{4.22}$$

$$low - state > 98 \text{ ns}, \tag{4.23}$$

$$t_{d(on)} = 35 \text{ ns}, \tag{4.24}$$

$$t_r = 36 \text{ ns}, \tag{4.25}$$

$$t_{d(on)} + t_r = 71 \text{ ns}, \tag{4.26}$$

$$high - state > 71 \text{ ns}. \tag{4.27}$$

$$FOM_{(SiC)} = r_{DS} \times Q_g = 80 \times 10^{-3} \times 106 \times 10^{-9} = 8.48 \times 10^{-9} \quad \text{V/s}. \tag{4.28}$$

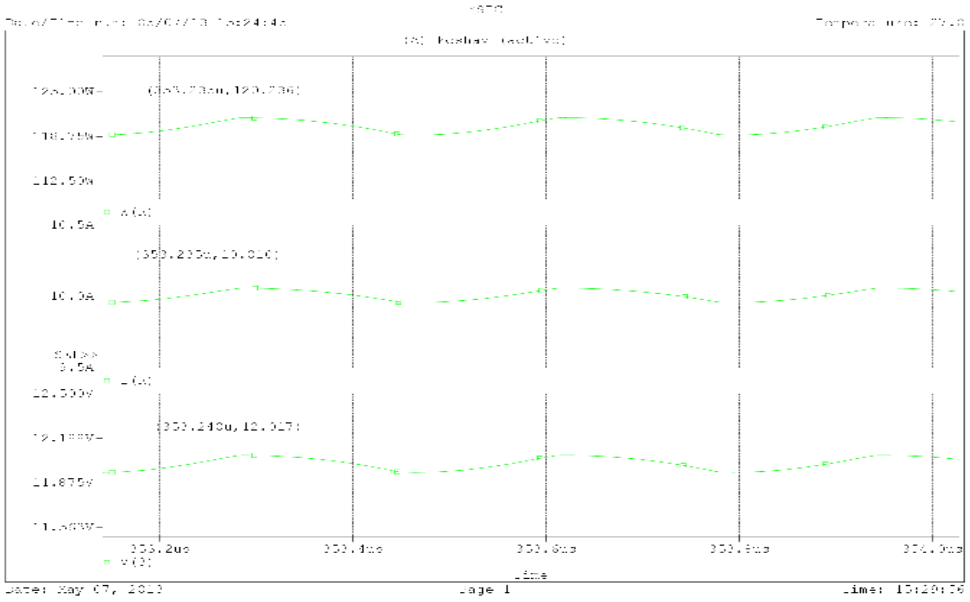

Figure 4.9: Drain-to-source voltage v_{DS} and gate-to-source voltage v_{GS} at $f_s = 1$ MHz.

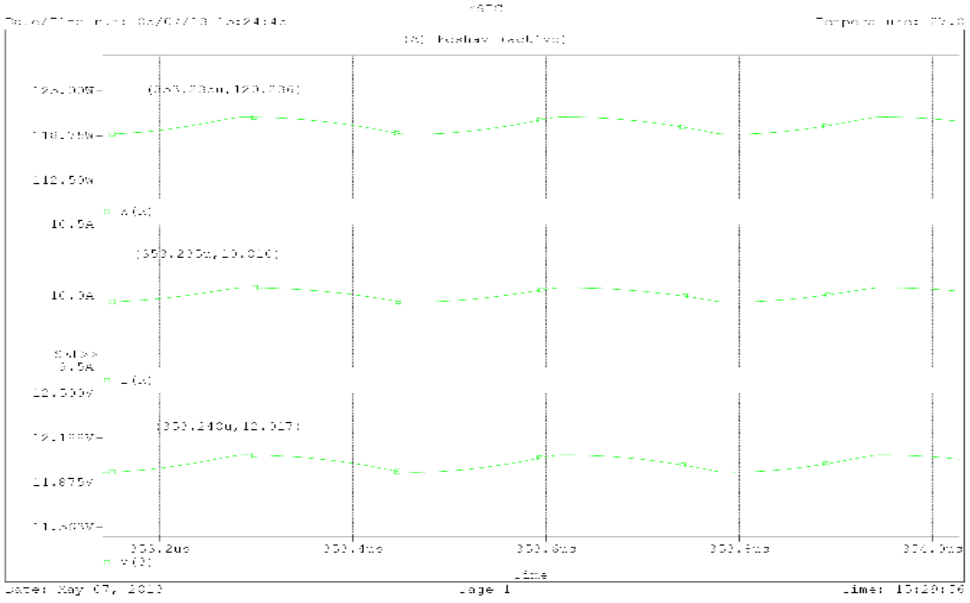

Figure 4.10: Output voltage V_O, output current I_O, and output power P_O at $f_s = 1$ MHz.

SiC MOSFET has its own advantages and disadvantages based on frequency, temperature, size, etc. Based on SiC material properties, SiC MOSFET is expected to switch faster and has low switching power loss when compared to Si MOSFET. SiC MOSFET was tested for the same frequency as that of Si MOSFET's cut-off frequency, i.e., for 1 MHz. The MOSFET works normally responding as quickly as it does at lower frequencies. The output voltage V_O and output power P_O of the converter matches the designed values. This is shown in Figures 4.9 and 4.10. Simulations were carried out for increase in switching frequency starting at 1 MHz. Taking three times this frequency, the circuit was simulated for 3 MHz switching frequency. The MOSFET showed very little delay in its response for 3 MHz switching frequency. Plots of drain-to-source voltage v_{DS} and gate-to-source voltage v_{GS} for 3 MHz is shown in Figures 4.12 and 4.11. Comparing the SiC device FOM with of Si, SiC MOSFET has a better device performance than that of Si MOSFET. This is given in equation (4.34)

$$f_s = 3\ \text{MHz}, \tag{4.29}$$

$$T = 1/f_s = 0.33\ \mu\text{s}, \tag{4.30}$$

$$D = 0.46, \tag{4.31}$$

$$t_{ON} = DT = 0.48 \times 0.33\ \mu\text{s} = 0.158\ \mu\text{s}, \tag{4.32}$$

$$t_{ON} = 0.158\ \mu\text{s} > 71\ \text{ns}. \tag{4.33}$$

$$\frac{FOM_{(Si)}}{FOM_{(SiC)}} = \frac{33}{8.48} = 4. \tag{4.34}$$

At 3.5 MHz switching frequency, we inferred that the MOSFET has reached its cut-off frequency limit. This is due to the response of the MOSFET that was observed in the waveforms generated. In reference to Figure 4.11, it is clearly seen that the MOSFETs drain-to-source voltage v_{DS} has a delay to respond quickly to the switching frequency f_s.

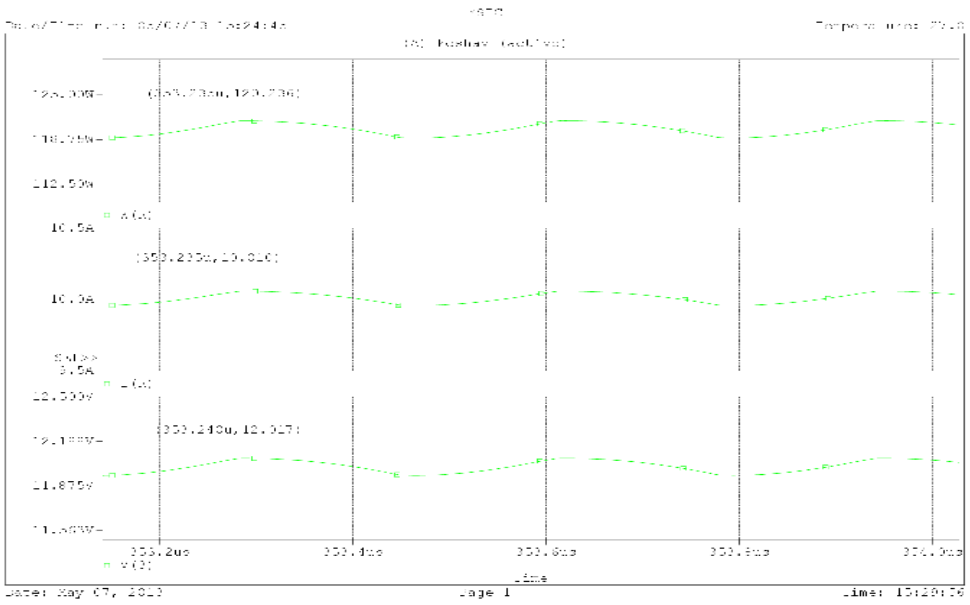

Figure 4.11: Output voltage V_O, output current I_O, and output power P_O at $f_s = 3$ MHz.

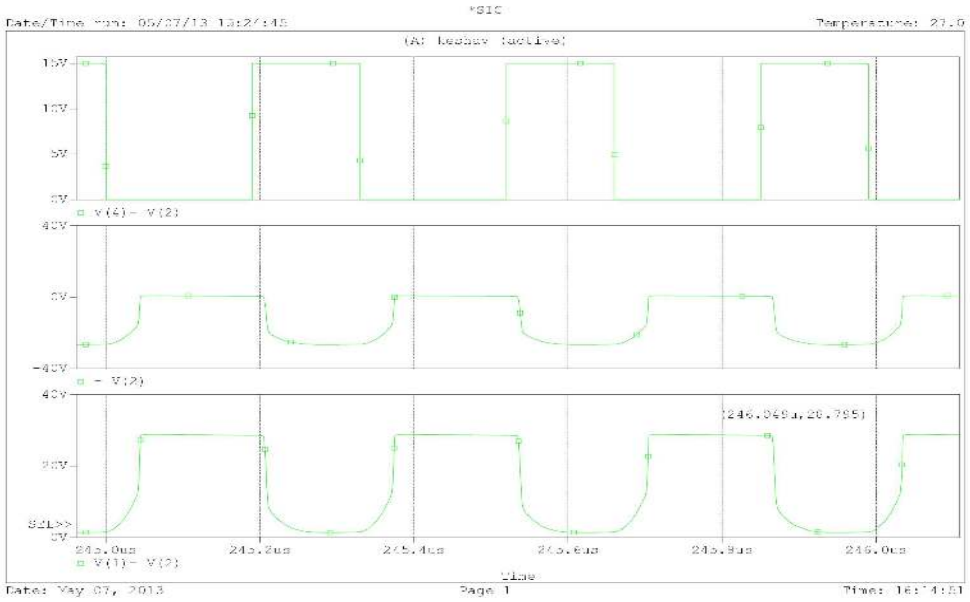

Figure 4.12: Drain-to-source voltage v_{DS} and gate-to-source voltage v_{GS} at $f_s = 3$ MHz.

The response time of the SiC MOSFET starts decreasing beyond this frequency. So, for a SiC MOSFET the cut-off frequency was determined to be 3.5 MHz based on the simulation results obtained. When the amplitude starts decreasing, the MOSFET starts to stop behaving like a normal switch as the drain-to-source voltage v_{DS} does not swing from zero to V_I completely. This in turn results in the rise in the output current I_O and output voltage V_O. We determined the cut-off frequency based on the drain-to-source voltage v_{DS}, output voltage V_O, output power P_O, and the output current I_O as mentioned. The output voltage V_O starts to increase beyond 12 V after 3.5 MHz. The MOSFET stops to switch normally and hence gradually stops to turn OFF or ON completely as shown in Figure 4.14. The MOSFET tries to remain ON all the time and hence the buck converter doesn't step down the input voltage V_I anymore. Plots of drain-to-source voltage v_{DS}, gate-to-source voltage v_{GS}, and inductor current i_L are shown in Figures 4.15 and 4.16.

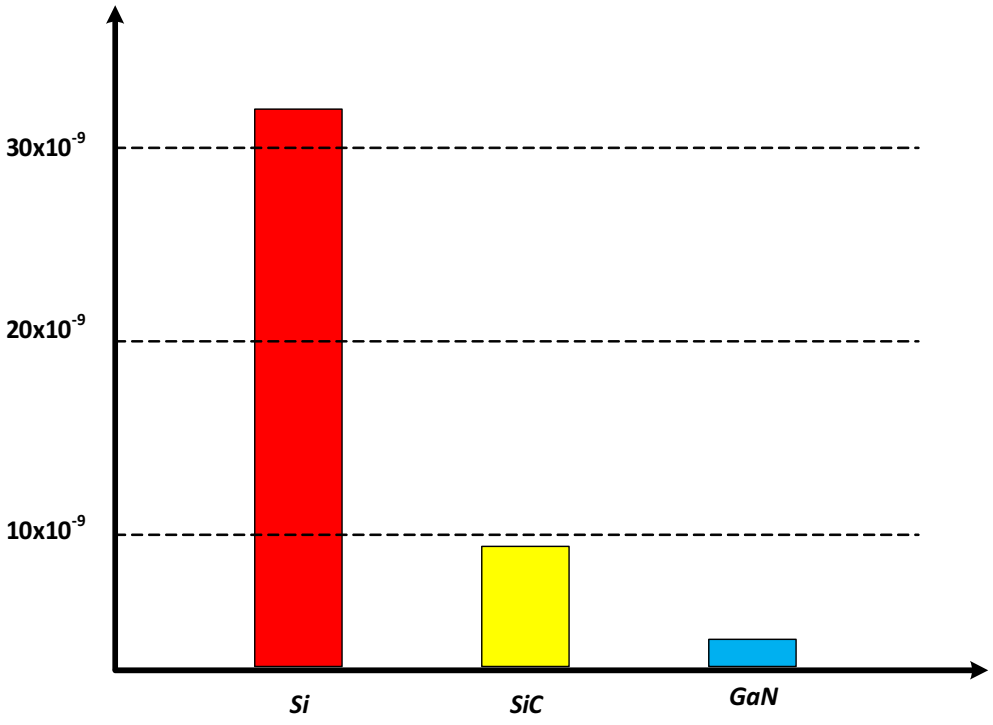

Figure 4.13: Comparison of figure-of-merit (FOM) of Si, SiC, and GaN semiconductor MOSFETs.

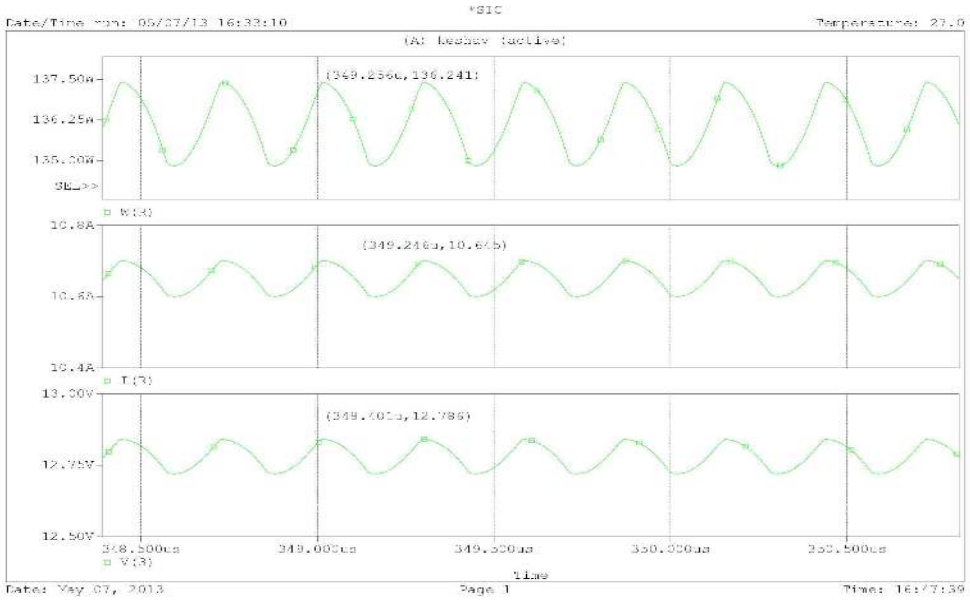

Figure 4.14: Output voltage V_O, output power P_O, and output current I_O at $f_s = 3.5$ MHz.

Even for 3.5 MHz switching frequency, the MOSFET's performance could be sufficient for today's industries, but efficiency is application dependent. More results on efficiency and power loss and covered in chapter 5.

The problem accompanying with faster switching speeds is the more severe ringing during transitions due to the MOSFET parasitics, which is not observed in simulation because, the parasitic inductances are not considered and an ideal driver is used. The ringing deteriorates the device stresses, which in turn offsets the reduced switching loss of the MOSFET [12]. The SiC MOSFET on-state resistance $r_{DS(ON)}$ value changes with temperature. The value initially decreases with increase in temperature at lower temperatures and then increases at higher temperatures [10]. The SiC MOSFET's bigger channel length modulation coefficient leads to the fact that it does not have a very obvious plateau region [10]. The capacitances C_{ISS} ,C_{RSS}, and C_{OSS} are of major importance to the MOSFET as they play an important role and determine the dynamic behavior of the MOSFET during switching

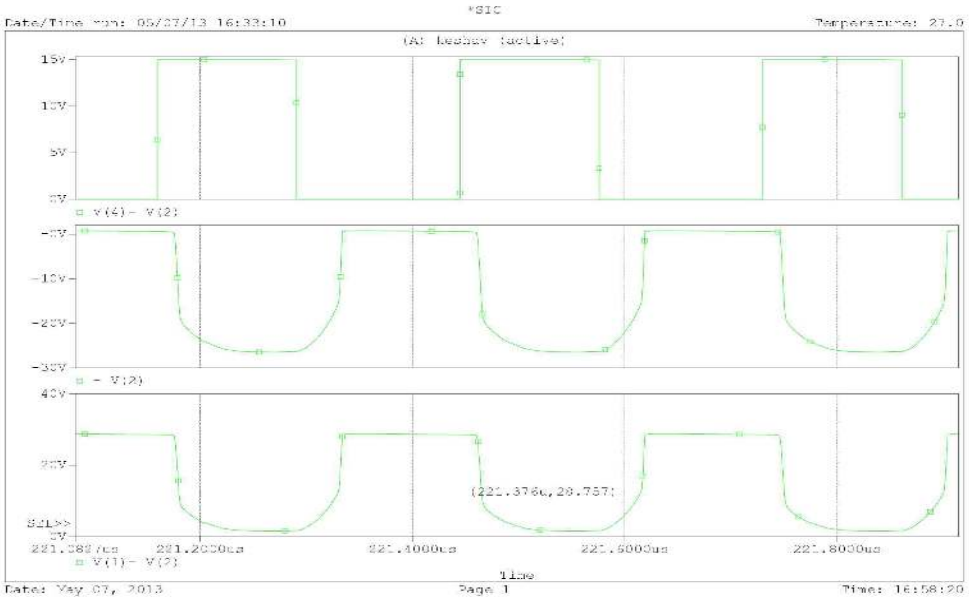

Figure 4.15: Drain-to-source voltage v_{DS} and gate-to-source voltage v_{GS} at $f_s = 3.5$ MHz.

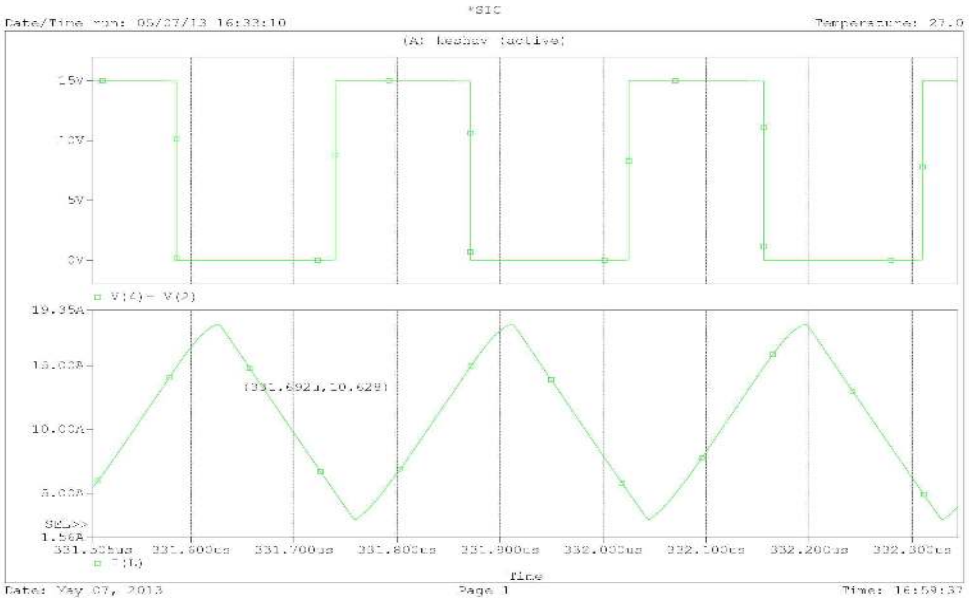

Figure 4.16: Gate-to-source voltage v_{GS} and inductor current i_L at $f_s = 3.5$ MHz.

transients. They are all parasitic and non-linear functions of v_{DS}. Apart from this there are the parasitic inductances L_G,L_D, and L_S, which are in series with gate, drain, and source of the MOSFET respectively, which are not taken into consideration as the model used is of order 1 [10].

4.1.3 Gallium Nitride (GaN) MOSFET

Gallium Nitride (GaN) MOSFETs have an advantage over Si and SiC due to the enhanced mobility of electrons. The device properties of GaN can be found in literature [30]. As explained earlier, better FOM leads to better switching efficiency at high frequencies in DC-DC converters. GaN MOSFET has the highest performance according to the figure-of-merit when compared to Si and SiC as seen in equation (4.35). This is shown in Figure 4.13. The FOM which considers the r_{DS} and Q_g gives the performance of a semiconductor material based on the least value obtained. The lesser the value, higher is the performance. These new GaN devices cover the current and voltage range for today's power electronic applications [27]. When compared to a Si MOSFET, GaN devices offer better performance (4.36). This is shown in Figure 4.19.

$$FOM_{(GaN)} = r_{DS} \times Q_g = 5.6 \times 10^{-3} \times 8 \times 10^{-9} = 0.0448 \times 10^{-9} \quad \text{V/s.} \tag{4.35}$$

$$\frac{FOM_{(Si)}}{FOM_{(GaN)}} = \frac{33}{0.0448} = 736. \tag{4.36}$$

GaN devices are at the beginning stages of replacing its silicon counterparts. The MOSFET used here is EPC2001 from Efficient Power Conversion (EPC). The specifications are shown in the data sheet [36]. The output power P_O of the converter was designed for 120 W with output voltage $V_O = 12$ V. Hence, output current I_O of 10 A. With reference to the literature survey carried out, we understand that the GaN MOSFETs switch at frequencies 4 to 5 times the maximum switching frequency of Si MOSFET. Based on this, a frequency of 4 MHz switching frequency was used and the circuit and was simulated. As explained earlier, irrespective of the type of MOSFET used, at lower frequencies the response of the MOSFET remains normal and the waveforms obtained matches the theoretical waveforms. For 4 MHz switching frequency, the GAN MOSFET switches normally as it does at lower

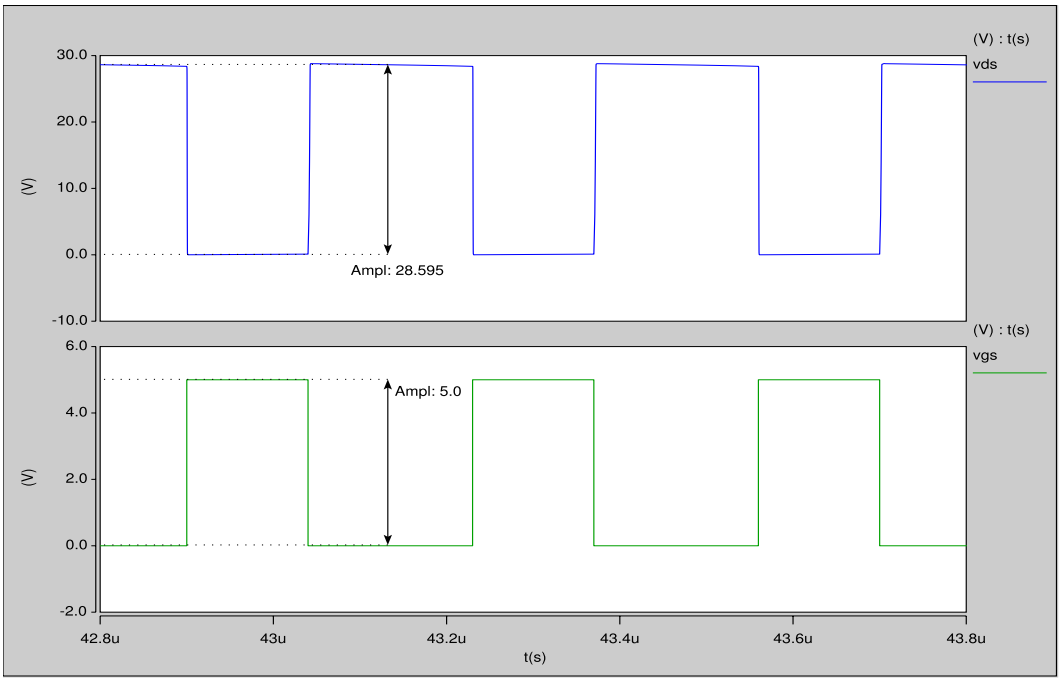

Figure 4.17: Drain-to-source voltage v_{DS} and gate-to-source voltage v_{GS} at $f_s = 4$ MHz.

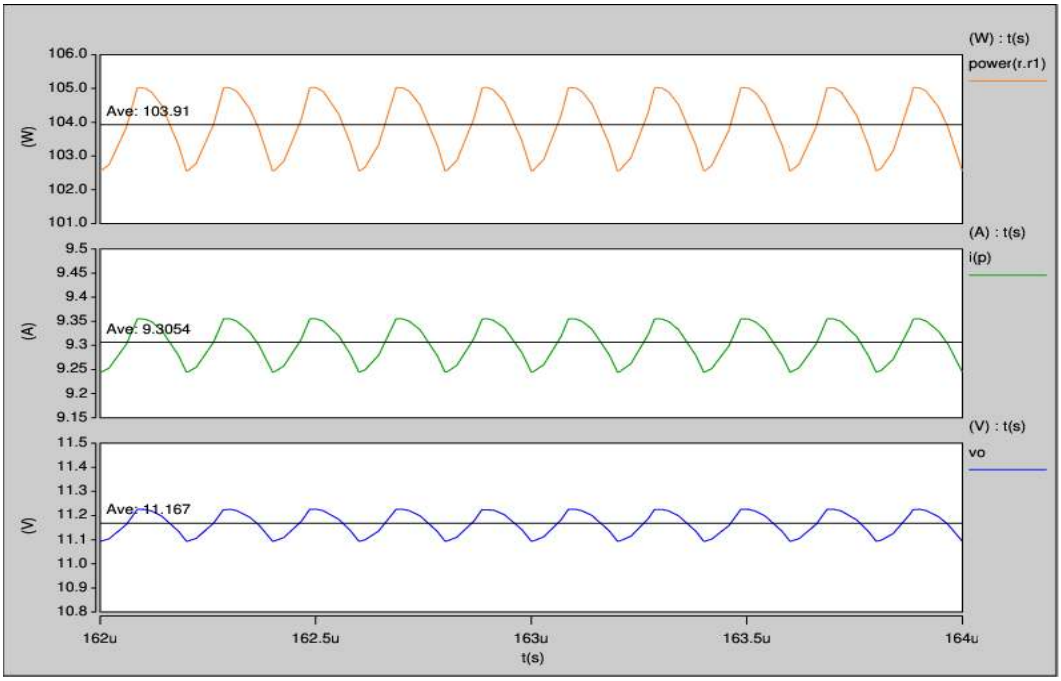

Figure 4.18: Output voltage V_O, output current I_O, and output power P_O at $f_s = 4$ MHz.

frequencies as shown in Figures 4.17 and 4.18. As the switching frequency f_s was increased to 5 MHz, notable changes were observed in the waveforms generated.

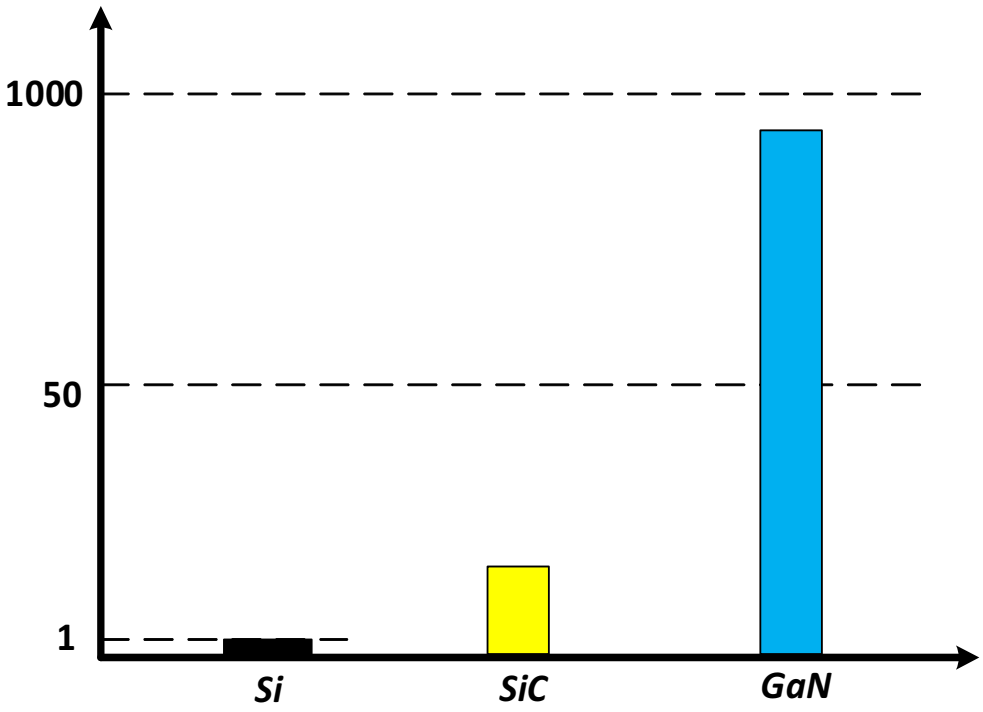

Figure 4.19: Comparison of normalized figure-of-merit (FOM) of Si, SiC, and GaN semiconductor MOSFETs.

Unlike Si and SiC MOSFETs, where the amplitude of the drain-to-source voltage v_{DS} starts decreasing and the output current I_O, output voltage V_O, and output power P_O rise at the cut-off frequency. In the case of a GaN MOSFET, the output voltage V_O, output current I_O, and output power P_O starts increasing for 5 MHz, but the amplitude of the drain-to-source voltage v_{DS} remains the same varying from zero to V_I. Plots of drain-to-source voltage v_{DS} and output current I_O, and gate-to-source voltage v_{GS} at 5 MHz are as shown in Figures 4.20 and 4.22. As a result of this high switching frequency, the average drain current i_D keeps rising, which in turn results in increase in the inductor current i_L, and hence a total rise in the output current I_O (Figure 4.22). This is presumed to be due to the anti-parallel diode of the MOSFET. Plots of drain current i_D and drain-to-source voltage

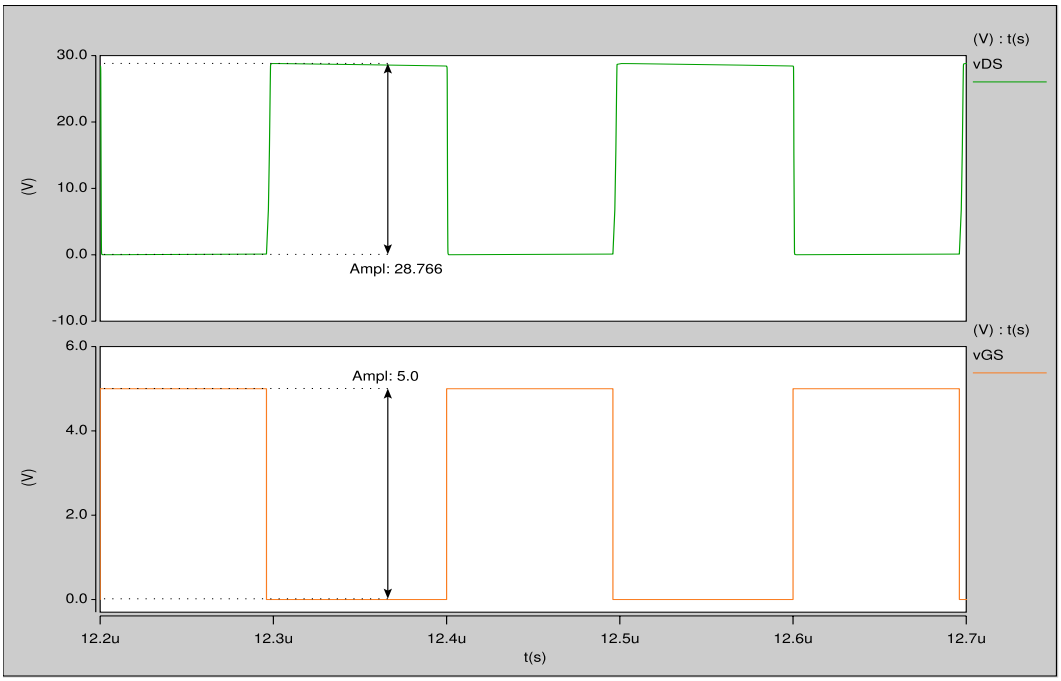

Figure 4.20: Drain-to-source voltage v_{DS} and gate-to-source voltage v_{GS} at $f_s = 5$ MHz.

v_{DS} are as shown in Figure 4.21.

From the results obtained via simulations, a number of advantages were noted. One of the main advantages was the efficient switching ability of the GaN MOSFET. Even with the output of the converter crossing designed values resulting in severe decrease in efficiency, the MOSFET switches normally in-line with the switching frequency f_s. After several simulations at various switching frequencies, the cut-off frequency of the MOSFET was presumed to be around 5 MHz. But choosing the right switching frequency is all dependent on the application and the required efficiency as there is always a trade-off between switching frequency f_s and efficiency η. A plot showing drain-to-source voltage v_{DS} at 50 MHz is shown in Figure 4.24.

It is clearly seen that the drain current i_D starts rising as shown in Figure 4.21. Hence, the output power P_O keeps rising. As observed earlier in the case of Si and SiC MOSFETs, the drain-to-source voltage v_{DS} does not completely fall back to zero once it

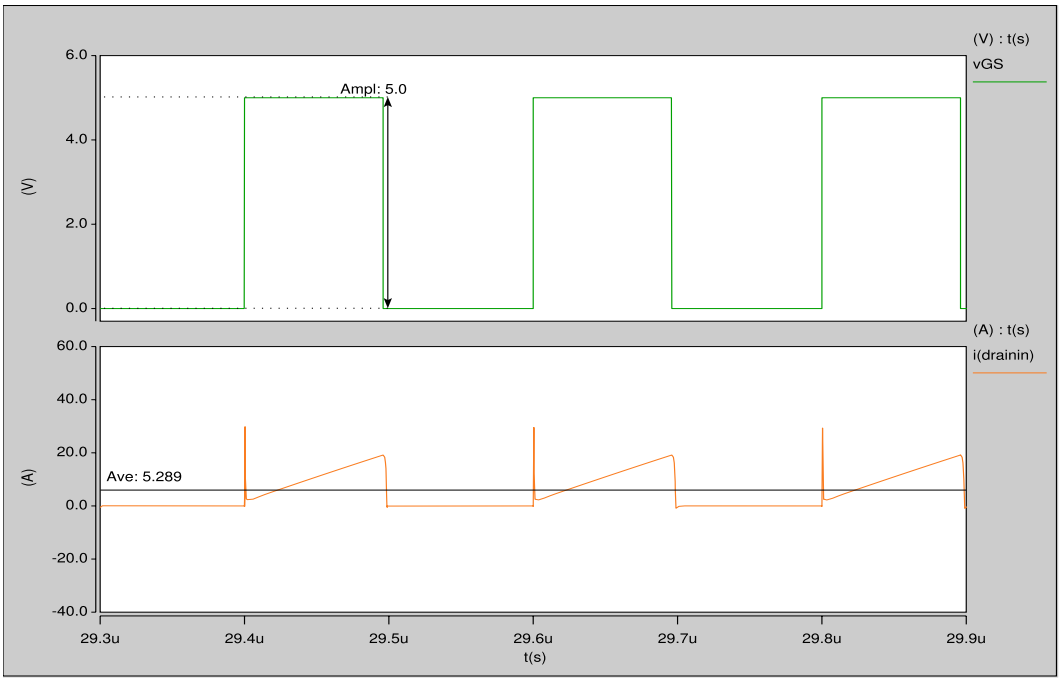

Figure 4.21: Drain current i_D and drain-to-source voltage v_{DS} at $f_s = 5$ MHz.

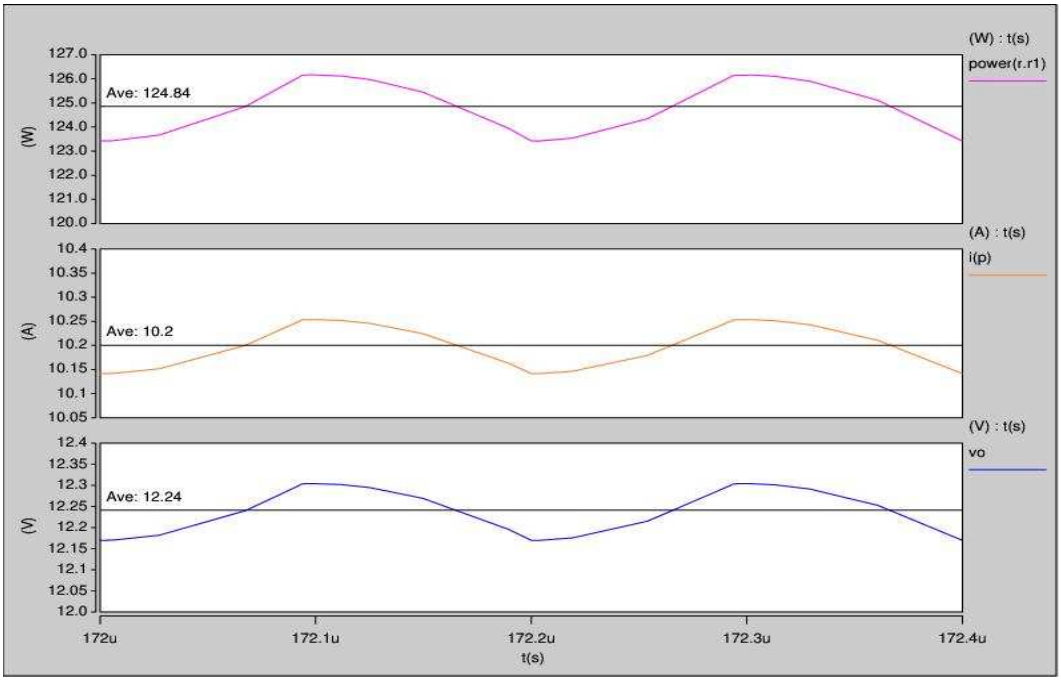

Figure 4.22: Output voltage V_O, output current I_O, and output power P_O at $f_s = 5$ MHz.

turns ON. It starts to gradually turn ON and OFF rather than switching normally. In the case of GaN MOSFET, the rise time starts increasing with increase in frequency, whereas there is very little effect on the fall time. Even at high frequencies, only the rise time gets affected the most. In the case of Si and SiC, both rising and falling edges are affected by the high switching frequency. The GaN MOSFETs fall time is less affected. The rise time slew rate is very high when compared to that of Si and SiC MOSFETs and starts increasing with increase in switching frequency f_s. The smaller terminal capacitance of GaN MOSFET may become an issue at higher frequencies due to the increased dv/dt during switching [8].

Table 4: Cutoff frequency of Si, SiC and GaN MOSFETs

MOSFET type	**Cutoff frequency**
Si	1 MHz
SiC	3.5 MHz
GaN	5 MHz

The reason for the superior performance of the GaN MOSFET is the basic semiconductor material properties of GaN. In the case of hardware, the parasitic common source inductance L_S is very important as it directly influences the driving speed of the devices. It is mainly controlled by the package inductance and varies from package to package. The loop inductance L_{loop} influences the switching time and the drain-to-source voltage v_{DS} spikes [29]. When it comes to GaN FET, the parasitics were considered of high importance and was packaged in such a way that the parasitics were reduced to minimum. As a result, the package inductance was reduced to minimum in terms of 10^{-12}H, which resulted in efficient switching at high frequencies [29]. A table consisting of the cut-off frequencies of Si, SiC and GaN MOSFETs is shown in Table 4.1.3.

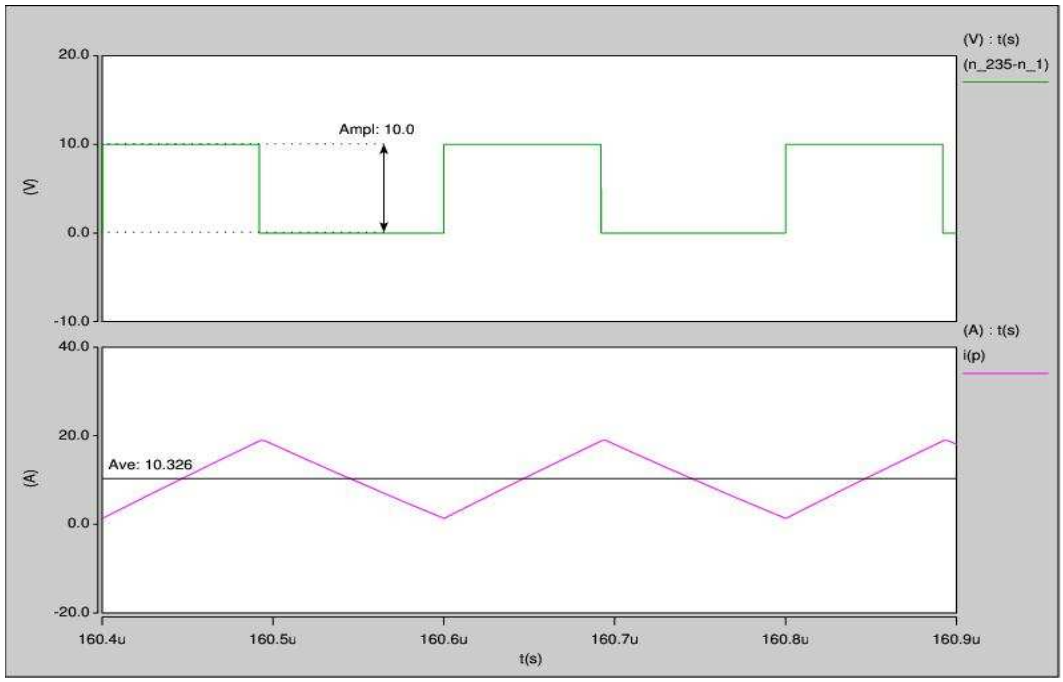

Figure 4.23: Inductor current i_L for switching frequency $f_s = 5$ MHz.

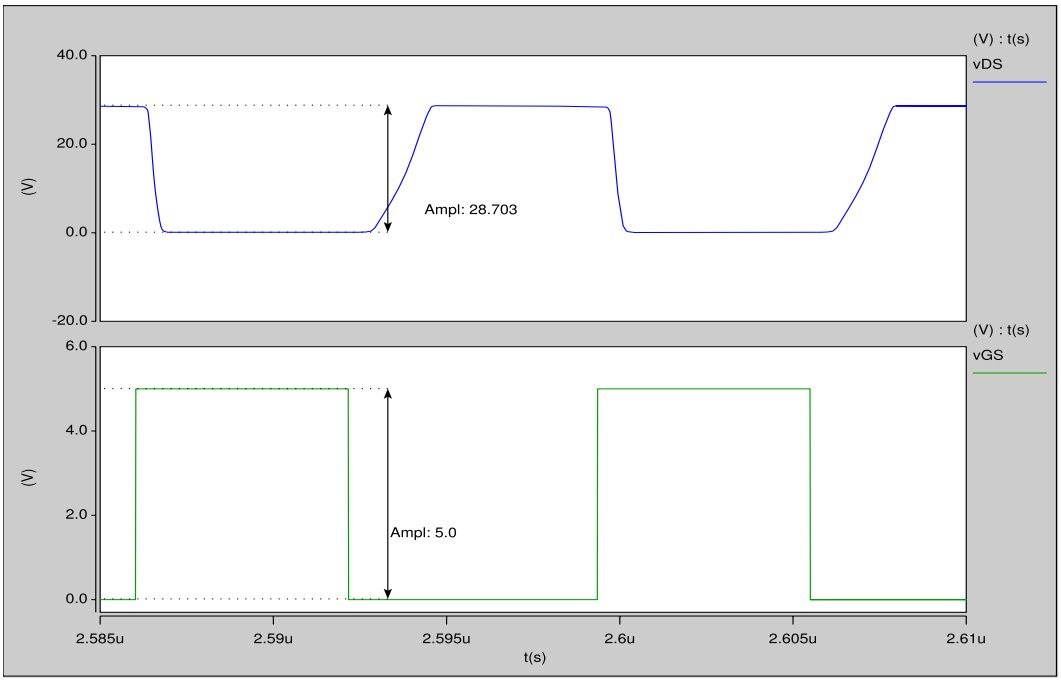

Figure 4.24: Drain-to-source voltage v_{DS} and gate-to-source voltage v_{GS} at $f_s = 50$ MHz.

4.2 Evaluation of Si, SiC, and GaN MOSFETs at Very High Switching Frequency

Power MOSFETs, or any other power device has operational frequency limit, which we have seen in the above section. Beyond this cut-off frequency, a MOSFET starts to perform abruptly. When we say cut-off frequency, we stress that it is in the case of a DC-DC buck converter and not the maximum operating limit of a MOSFET as we have seen MOSFETs working at GHz frequencies in the case of power amplifiers. In this thesis, four to five times the cut-off frequency determined for each MOSFET in the previous section is considered as very high frequency and this remains to be true as it is well beyond the cut-off switching frequency.

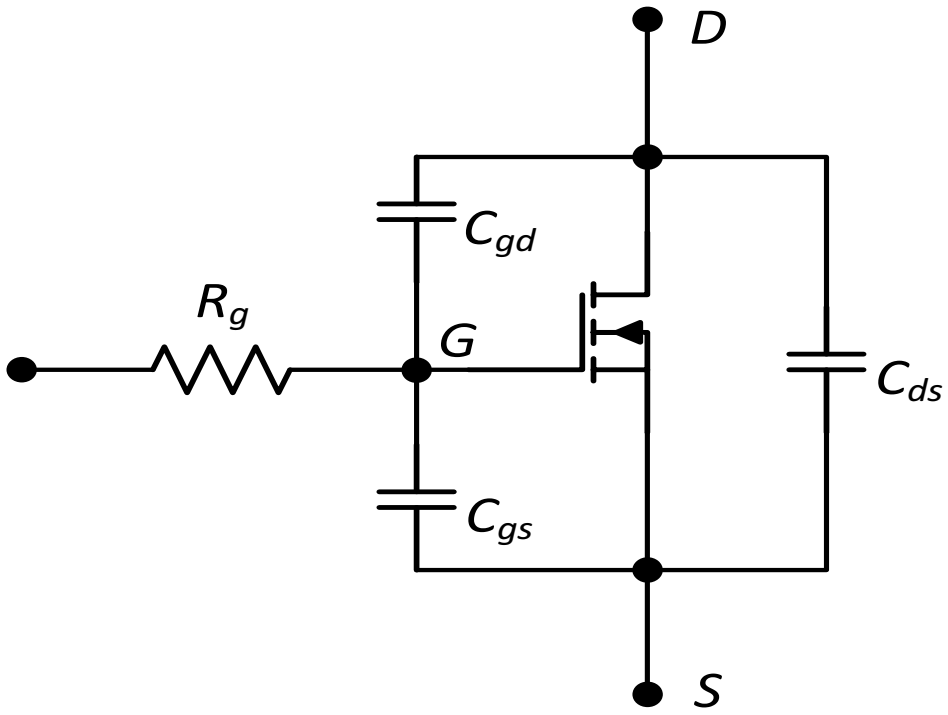

Figure 4.25: MOSFET model with parasitic capacitances and gate resistance.

We know that the MOSFET has parasitic capacitances and the gate resistance R_g as depicted in Figure 4.25. The MOSFET also has parasitic inductances L_G, L_D, L_S, and

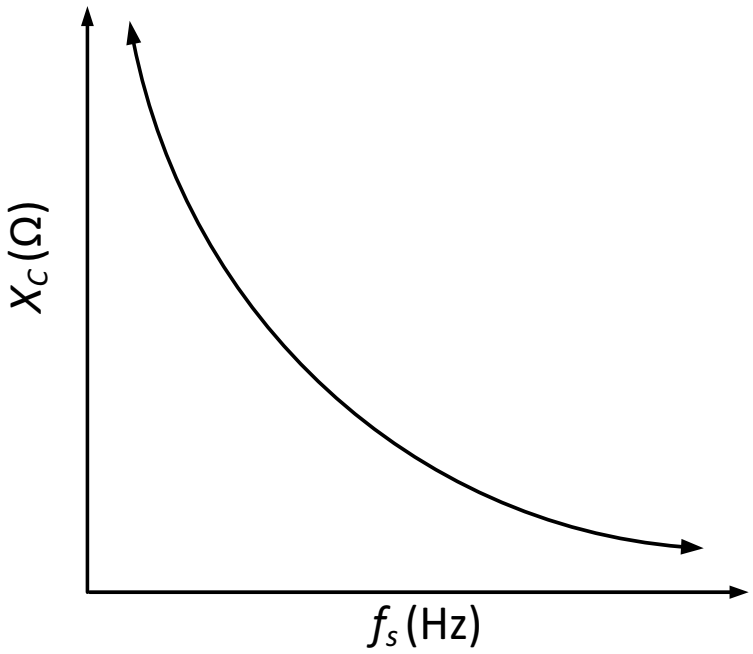

Figure 4.26: RC filter's capacitive reactance X_C versus switching frequency f_s.

resistances R_D and R_S, which also contribute to the high-frequency effects of the MOSFET. Since the the MOSFET model used here is of order 1, the parasitic inductances and resistances are not taken into consideration. The combination of the gate resistance R_g and the MOSFET capacitance acts as a basic RC filter. A basic RC filter consists of a resistor and a capacitor with the output taken at the junction of these two components. When a continuously changing voltage is applied to a capacitor, the capacitor gets charged and discharged at the rate of change, which is controlled by the frequency. Thus a current flows, which is restricted by the internal resistance of the capacitor. The capacitive reactance X_C is a function of frequency. It is the built-up electric field which resists the change of voltage and is given by equation (4.2). This capacitive reactance X_C is inversely proportional to the frequency. A plot of capacitive reactance X_C versus frequency f is as shown in Figure 4.26.

$$X_C = \frac{1}{2\pi f C}, \tag{4.37}$$

A low-pass filter is a circuit which allows frequencies to pass through it only below its cut-off frequency f_c. Each filter has it's own cut-off frequency and beyond this frequency, there is no unity gain anymore and the resistance is equal to the capacitive reactance. The output voltage is 70 % of the input voltage. The combination of R and C produces a charging and discharging effect on the capacitor and this is known as time constant denoted by τ.

$$\tau = RC, \tag{4.38}$$

$$f_c = \frac{1}{2\pi\tau}. \tag{4.39}$$

An integrator is nothing but a low-pass filter with a pulse voltage applied to the input instead of sine. At high frequencies, the output is not a pulse anymore as the frequency is well beyond the cut-off frequency f_c, where $\omega > 1/RC$. An integrator along with its input and output waveforms is shown in Figure 4.27.

$$V_{in} = IR, \tag{4.40}$$

$$V_{out} = \frac{1}{RC}\int V_{in}\, dt.$$

.

If the RC time constant is long compared to the input waveform, the output will become more and more triangular in shape and the amplitude starts decreasing with increase in the input frequency.

In the case of a MOSFET, we see that the R_g and the capacitances C_{gs} and C_{gd} start acting like a low-pass filter. This is shown in figure 4.28. Redrawing this figure, we combine

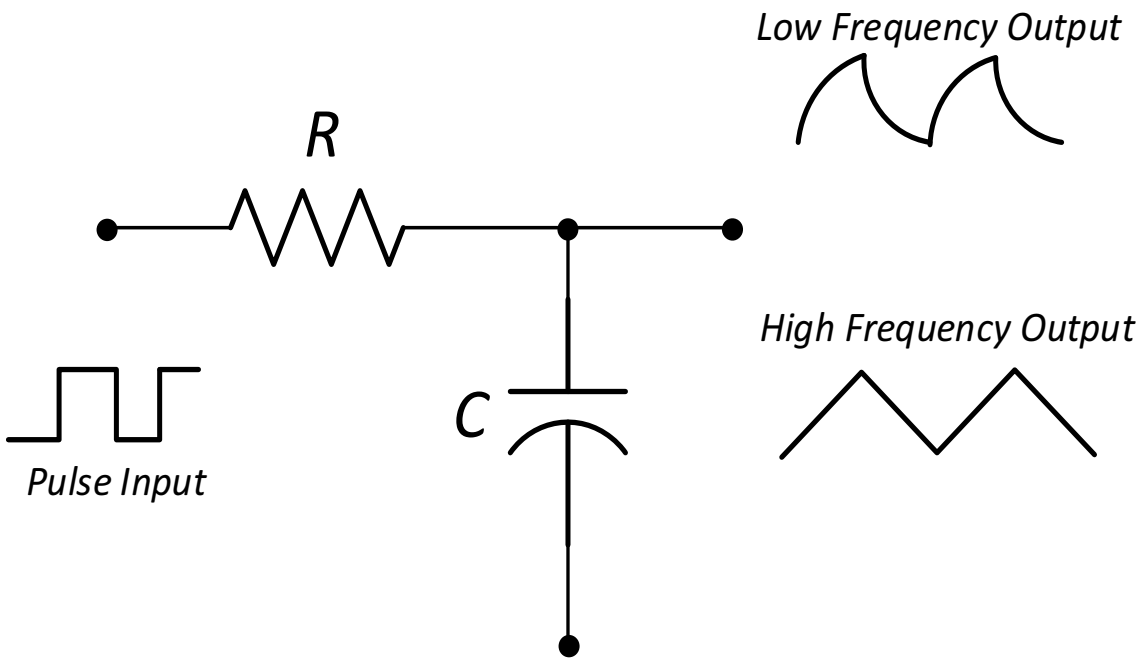

Figure 4.27: Circuit diagram of a basic RC low-pass filter.

the two capacitances to get a combined capacitance and call it C_g. And hence this R_g along with C_g start behaving like a RC low-pass filter.

This C_g includes the gain A_m which is given by

$$A_m = \frac{\Delta V_{DS}}{\Delta V_{GS}}, \tag{4.42}$$

and

$$C_g = C_{gd}(1 - A_m) + C_{gs}. \tag{4.43}$$

For a Silicon MOSFET, the cut-off frequency was determined to be 1 MHz. Consider 5 MHz, which is five times the cut-off frequency of Si MOSFET. The drain-to-source voltage v_{DS}, gate-to-source voltage v_{GS}, etc. waveforms obtained for this switching frequency are shown in Figures 4.29,4.30, and 4.31.

The gate resistance R_g is an equivalent value of a distributed resistor network

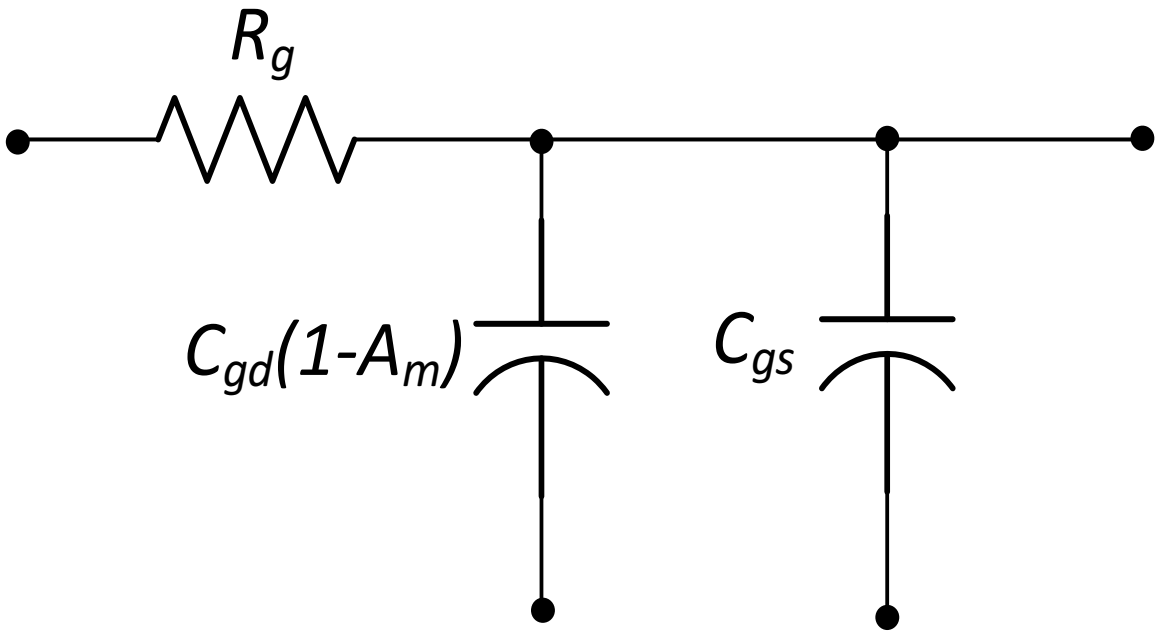

Figure 4.28: MOSFET's gate resistance R_g along with it's parasitic capacitances C_{gs} and C_{gd}.

connecting the gates of the individual MOSFET transistor cells in the device. This the gate signal distribution within a device behaves like that of a transmission line, which leads to different switching times of the individual MOSFET cells within a device, also depending on the cells distance from the bound pad of the gate connection [24]. The most accurate method to determine the gate resistance is to use an impedance bridge.

Choosing the right value of R_g is always important. An incorrect value does not hold good for high frequencies, because the capacitances value change with frequency, i.e., the parasitic capacitances are a non-linear function of the switching frequency f_s.

Using the value of R_g and the total value of C_g of the MOSFET, the cut-off frequency f_c can be determined using

$$f_c = \frac{1}{2\pi R_g C_g}. \tag{4.44}$$

The cut-off frequency of the RC filter in the case of a MOSFET cannot be accurately

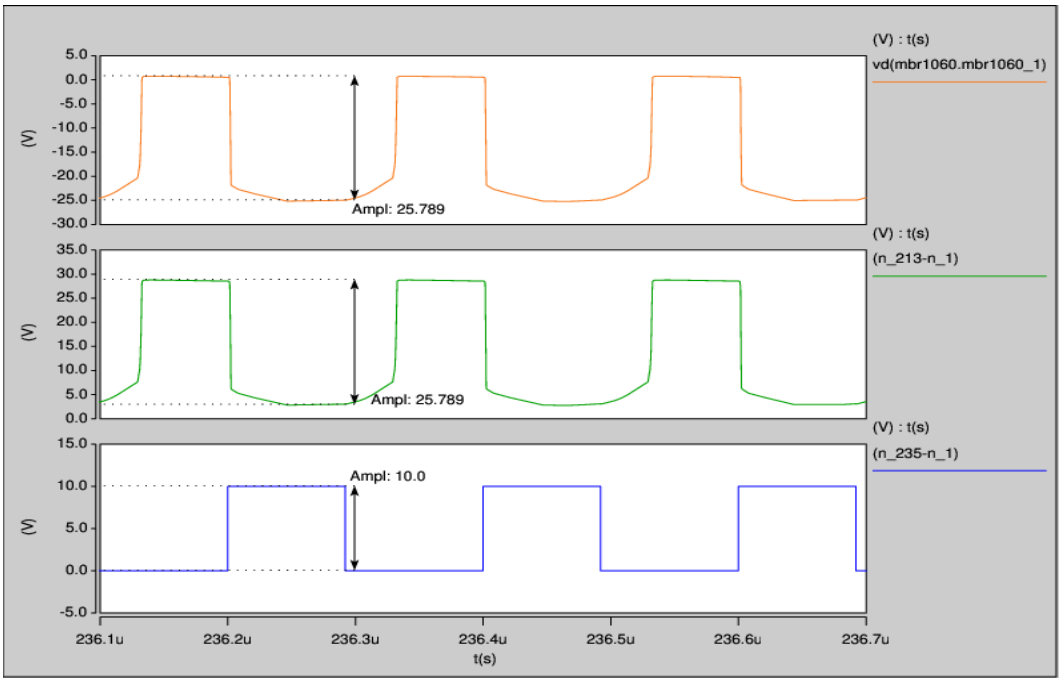

Figure 4.29: Drain-to-source voltage v_{DS} and gate-to-source voltage v_{GS} of silicon MOSFET at $f_s = 5$ MHz.

measured due to the parasitic nature of capacitances. Beyond the cut-off frequency, i.e., at very high frequency, the waveform is not a pulse anymore. Due to insufficient response time as explained earlier, the waveform turns triangular and the MOSFET starts to continuously turn itself ON and OFF over and over again. We see that the MOSFET has very little time or almost no time at higher frequencies to turn itself ON and OFF in-line with the gate drive signal. By the time the MOSFET completely turns OFF, it is turned ON and vice versa. This incomplete turn-ON and turn-OFF of the MOSFET brings about abnormalities in the circuit.

The cut-off frequency for SiC MOSFET was determined to be around 3.5 MHz and that of GaN to be around 50 MHz. The waveforms are as shown in the previous section. At higher frequencies, the MOSFET has no time at all to turn itself OFF. We say turn-OFF because, in this thesis the gate drive signal of the MOSFET has a high-state at the beginning of the signal. Hence, the MOSFET is turned ON by the gate drive signal at the

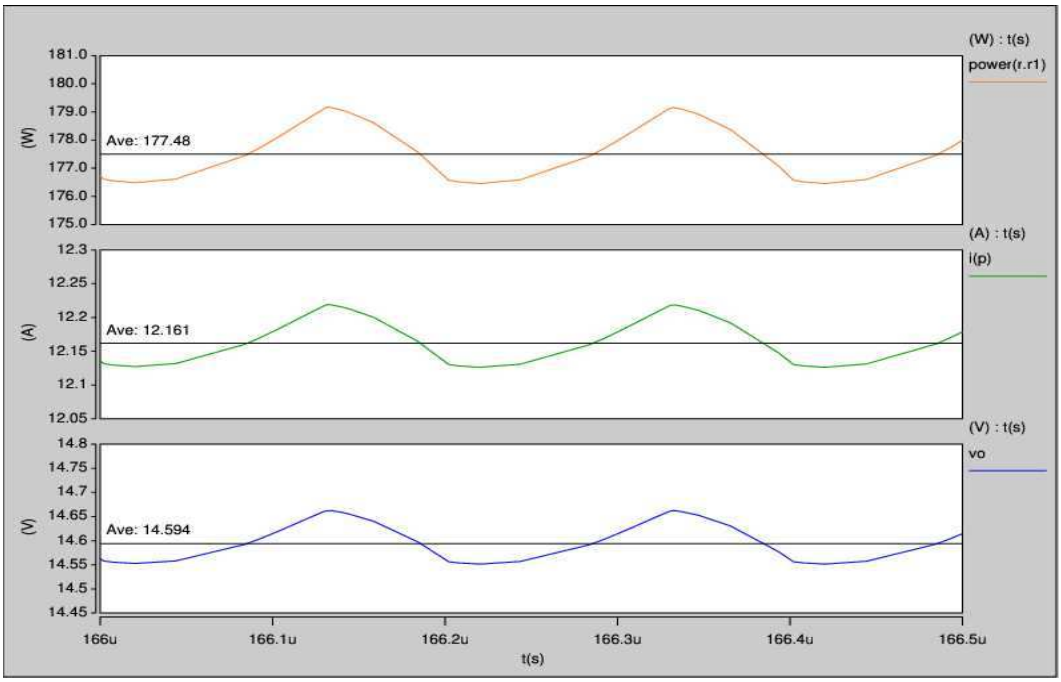

Figure 4.30: Output voltage V_O, output current I_O, and output power P_O of silicon MOSFET at $f_s = 5$ MHz.

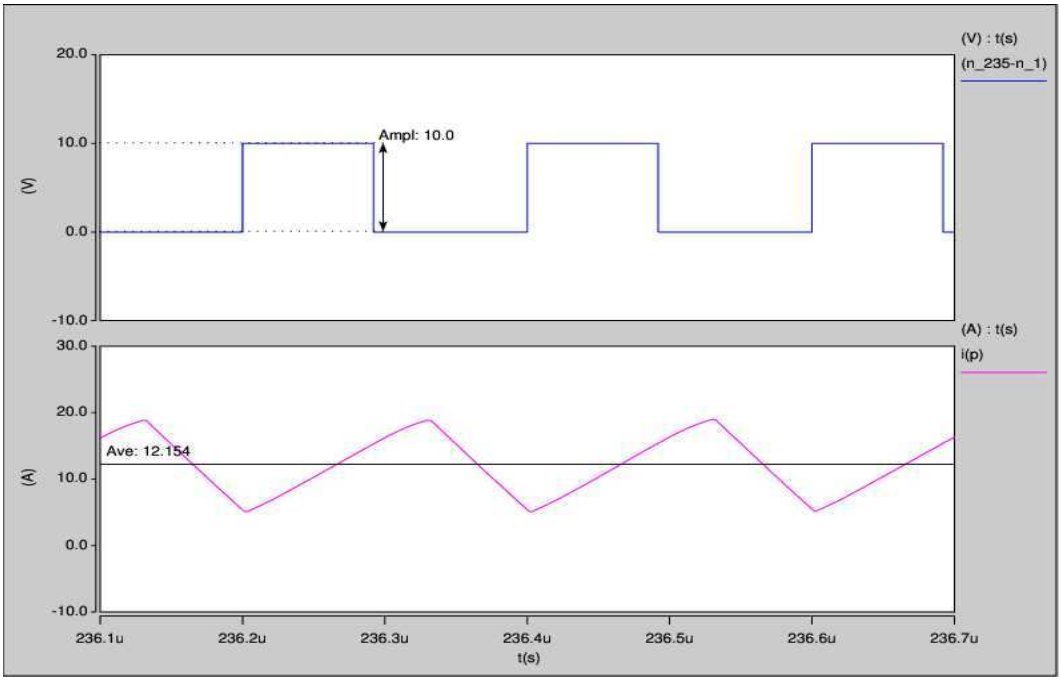

Figure 4.31: Inductor current i_L of silicon MOSFET at $f_s = 5$ MHz.

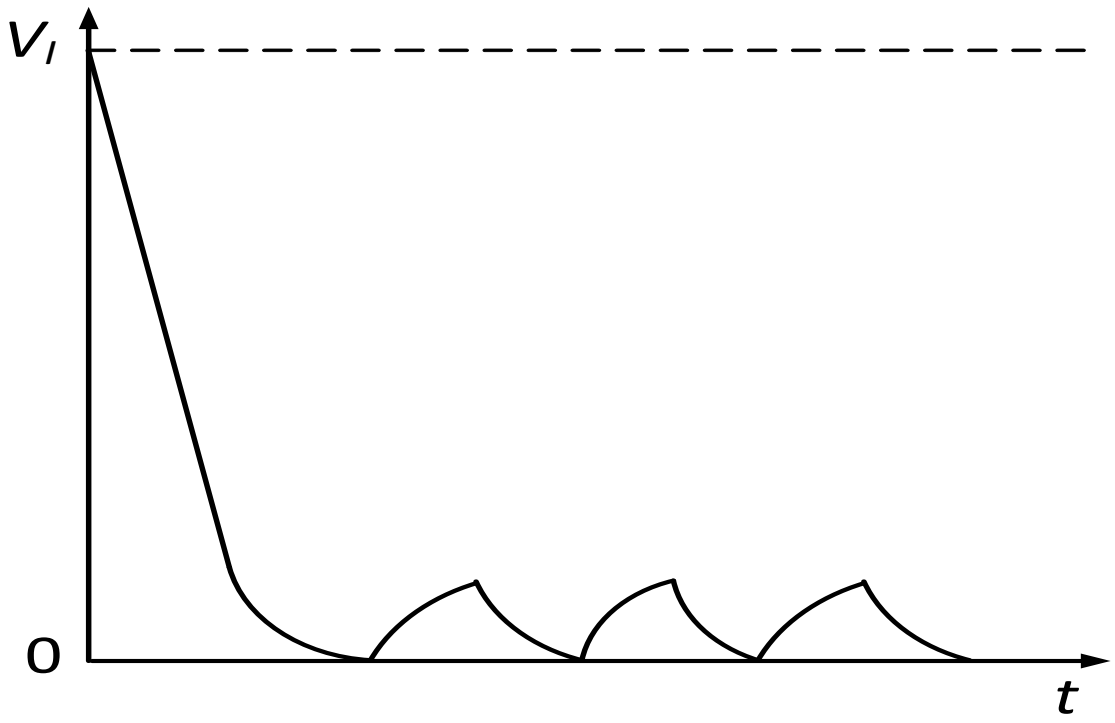

Figure 4.32: Expected plot of drain-to-source voltage v_{DS} at very high frequency f_s.

beginning of the signal. Since the switching frequency f_s is so high, the MOSFET has no time at all to turn itself OFF and remains ON almost all the time. This is shown in Figure 4.32. The output voltage V_O is almost equal to the input voltage V_I applied. The average inductor current i_L (output current) starts rising. The energy gets continuously stored in the inductor. The diode D is never turned ON and hence the switching network fails to perform it's switching operation, and in turn the buck converter fails to operate as a step down converter. The output power P_O of the converter starts increasing at a very high rate, that when calculated in terms of efficiency turns out to be a 10% efficient, which is very well less than the acceptable range of efficiency. Detailed evaluation of power loss and efficiency is covered in chapter 5.

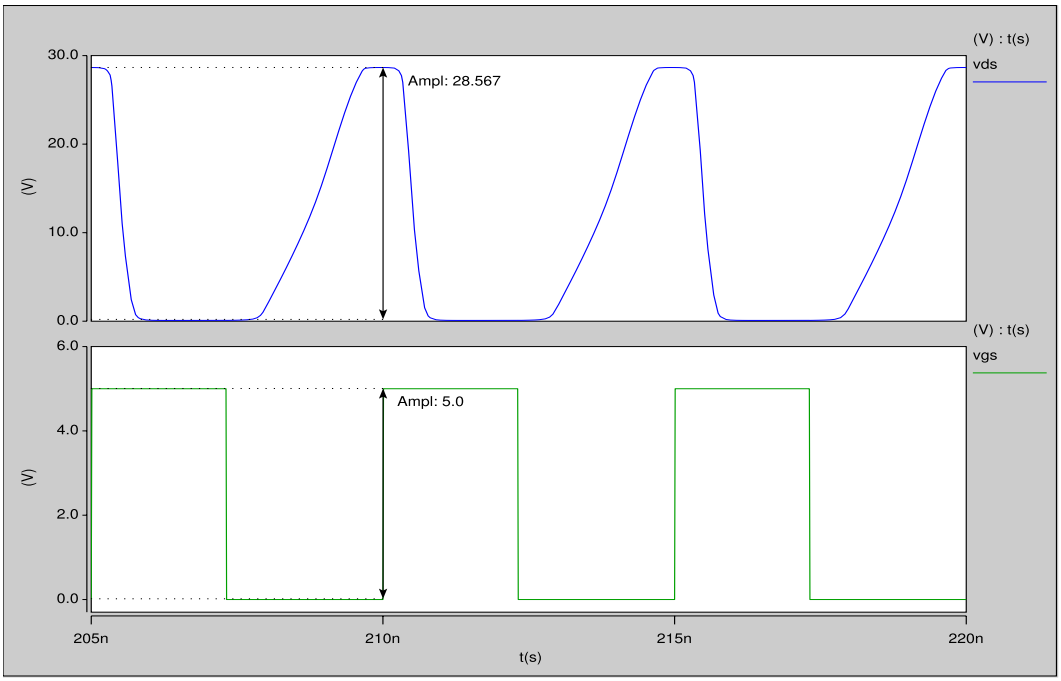

Figure 4.33: Drain-to-source voltage v_{DS} of gallium nitride MOSFET at $f_s = 250$ MHz.

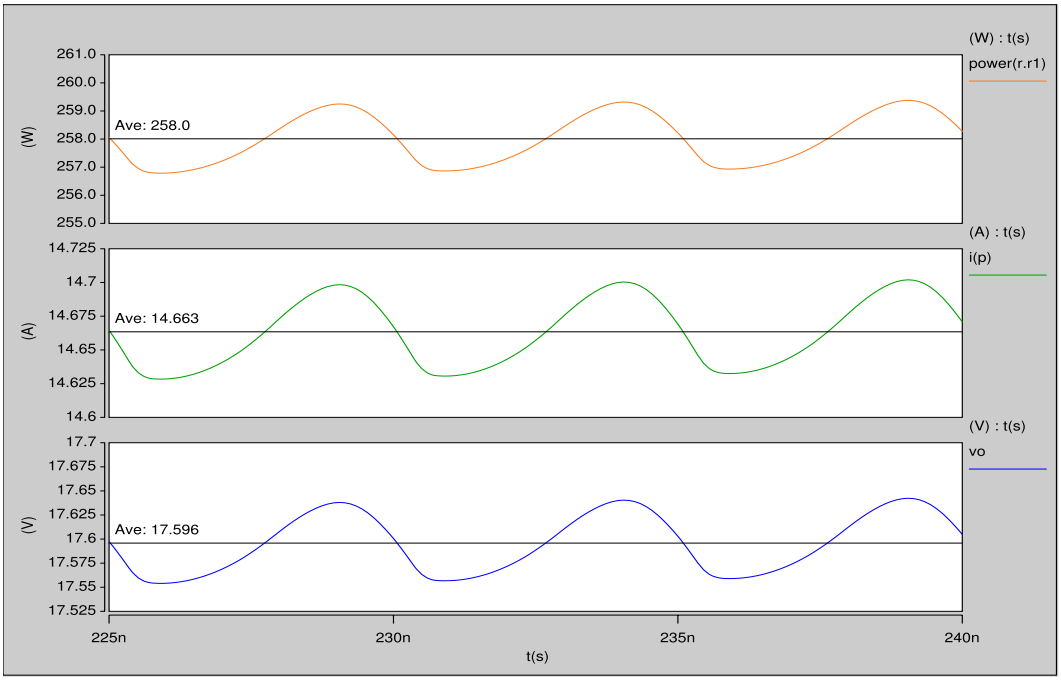

Figure 4.34: Output voltage V_O, output current I_O, and output power P_O of gallium nitride MOSFET at $f_s = 250$ MHz.

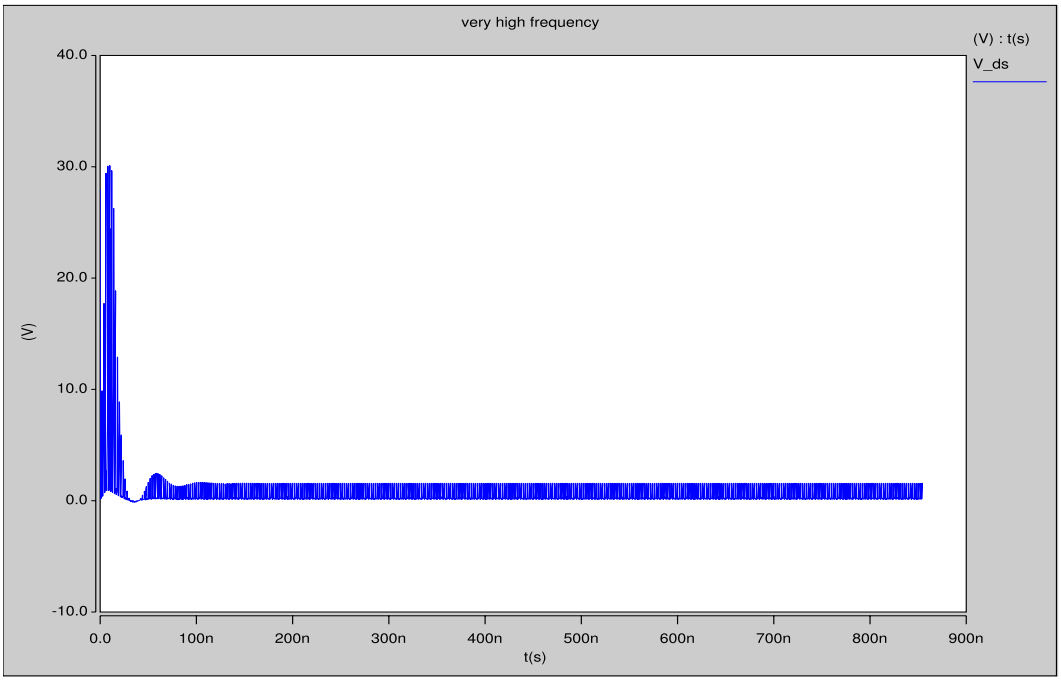

Figure 4.35: Drain-to-source voltage v_{DS} of gallium nitride MOSFET at very high switching frequency.

5 MOSFET Power Loss and Efficiency of DC-DC Buck Converter

Power loss and efficiency are the two most important factors that determine the credibility of any converter. As the switching frequency increases, the size of the reactive components decrease, which is one of the advantages of increasing the switching frequency. But as the switching frequency increases, so do the losses in the circuit and are inversely proportional to each other. The total power loss of the buck converter is given by P_{LS}. The buck converter has two types of losses mainly, the switching loss and the conduction loss. As this thesis is mainly focused on the analysis of MOSFET at high switching frequencies, the components, diode D, inductor L and capacitor C are considered ideal and their power loss P_D, P_{rL}, and P_{rC} have very little contribution to the total power loss P_{LS}. This includes the gate power loss P_G as well, as the driver used is ideal. The following sections compares the MOSFET power loss P_{FET} and efficiency η of the Si, SiC, and GaN MOSFETs at various switching frequencies.

5.1 MOSFET Power Loss P_{FET}

The MOSFET has mainly two types of losses, i.e. the gate loss P_G, which is a function of f_S and the power loss in the MOSFET P_{FET}, which includes the MOSFET conduction loss P_{rDS} and the switching loss P_{SW}. The switching loss P_{SW} is due to the switch output capacitance C_O. It occurs during switching transitions, which is due to the switch current i_S and the switch voltage v_S. The conduction power loss of the MOSFET is the loss due to the on-state resistance $r_{DS(ON)}$ given by P_{rDS}. The gate loss P_G is not considered as we are using an ideal driver for simulation purpose as mentioned earlier. Consider the turn-off transition of the MOSFET. During this turn-off phase, the drain-to-source voltage v_{DS} increases from zero to V_I and the output capacitance C_O is charged. This charge is then transferred from the input voltage V_I to the capacitance C_O. Thus the energy lost in the capacitor charging path results turn-off switching loss given by [1],

$$P_{turn-off} = \frac{1}{2} f_s C_O {V_I}^2, \tag{5.1}$$

When the MOSFET is turned ON, the capacitance is shorted out through the on-state resistance $R_{DS(ON)}$ and the capacitor discharges decreasing the drain-to-source voltage v_{DS} from V_I to zero. This turn-ON energy loss results in turn-ON switching loss given by [1]

$$P_{turn-on} = \frac{1}{2} f_s C_O {V_I}^2, \tag{5.2}$$

The total MOSFET switching loss of the MOSFET P_{SW} is given by

$$P_{SW} = f_s C_O {V_I}^2. \tag{5.3}$$

The total MOSFET power loss P_{SW} mentioned above considers the output capacitance C_O as a linear capacitance. But the MOSFETs drain-to-source capacitance C_{ds} is non-linear

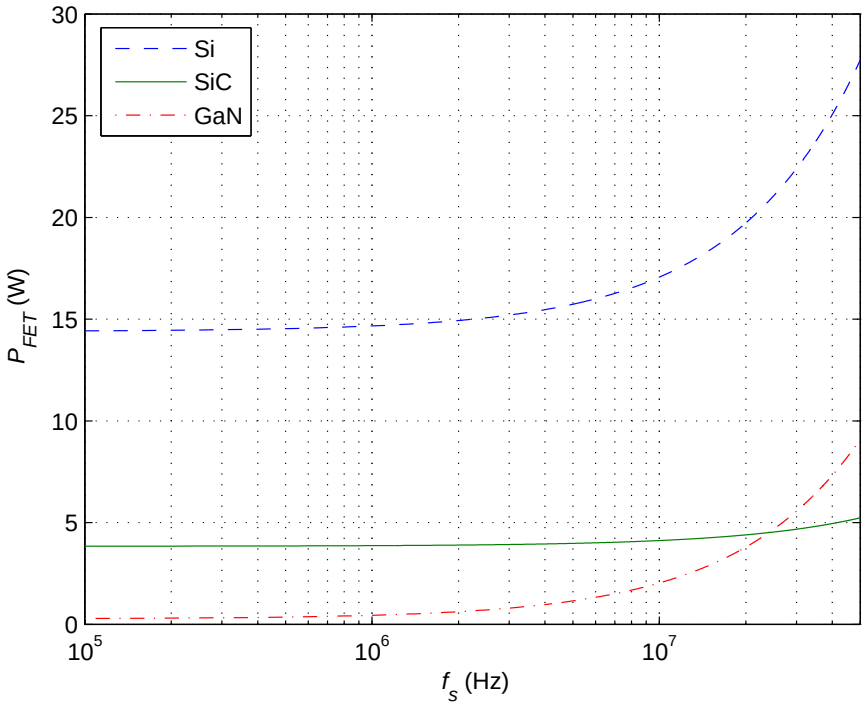

Figure 5.1: MOSFET power loss P_{FET} versus switching frequency f_s for Si, SiC, and GaN MOSFETs considering C_{ds} as linear.

and depends on the drain-to-source voltage v_{DS} [1]. A plot of MOSFET power loss P_{FET} versus switching frequency f_S considering C_O as linear capacitance is shown in Figure5.1.

Since the drain-to-source capacitance C_{ds} is non-linear, the above equations do not hold good when comparison is made with the obtained data via simulations. A new set of equations obtained from literature [1] provides more accurate results considering C_{ds} as non-linear [1]. C_{ds} is given by the equation

$$C_{ds} = C_{oss} - C_{rss}. \tag{5.4}$$

The switching power loss during turn-OFF transition is given by

$$P_{turn-off} = \frac{20}{3} f_s C_{ds} \sqrt{V_I{}^3}, \tag{5.5}$$

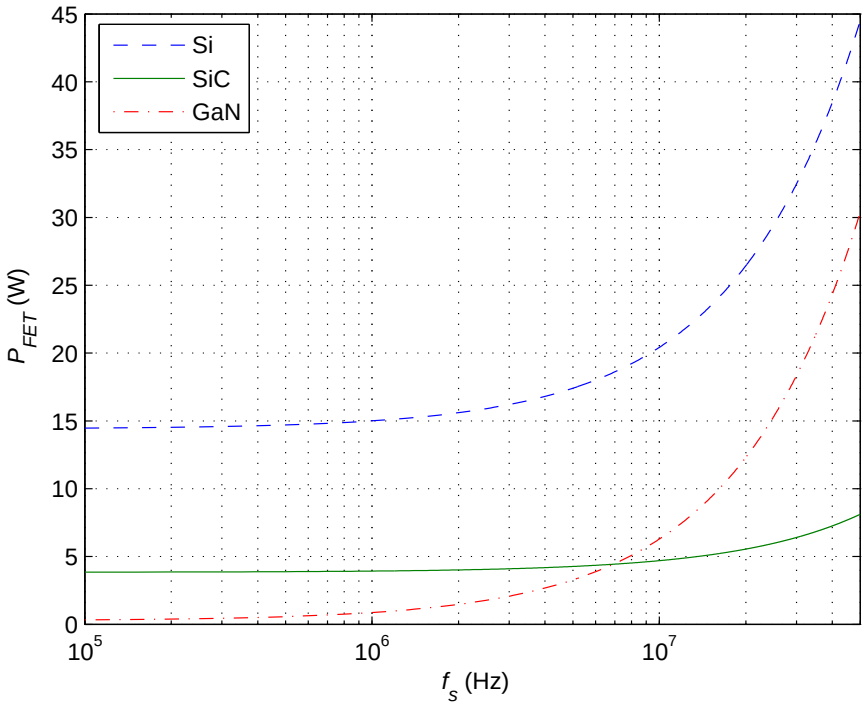

Figure 5.2: MOSFET power loss P_{FET} versus switching frequency f_s for Si, SiC, and GaN MOSFETs considering C_{ds} as non-linear.

The switching power loss during turn-ON transition is given by

$$P_{turn-on} = \frac{10}{3} f_s C_{ds} \sqrt{V_I{}^3}, \tag{5.6}$$

The total switching power loss of the MOSFET is,

$$P_{SW} = 10 f_s C_{ds} \sqrt{V_I{}^3}. \tag{5.7}$$

Therefore the equivalent capacitance which results in the same amount of switching loss as the non-linear one is given by[1]

$$C_{eq} = \frac{10 C_{ds}}{\sqrt{V_I}}. \tag{5.8}$$

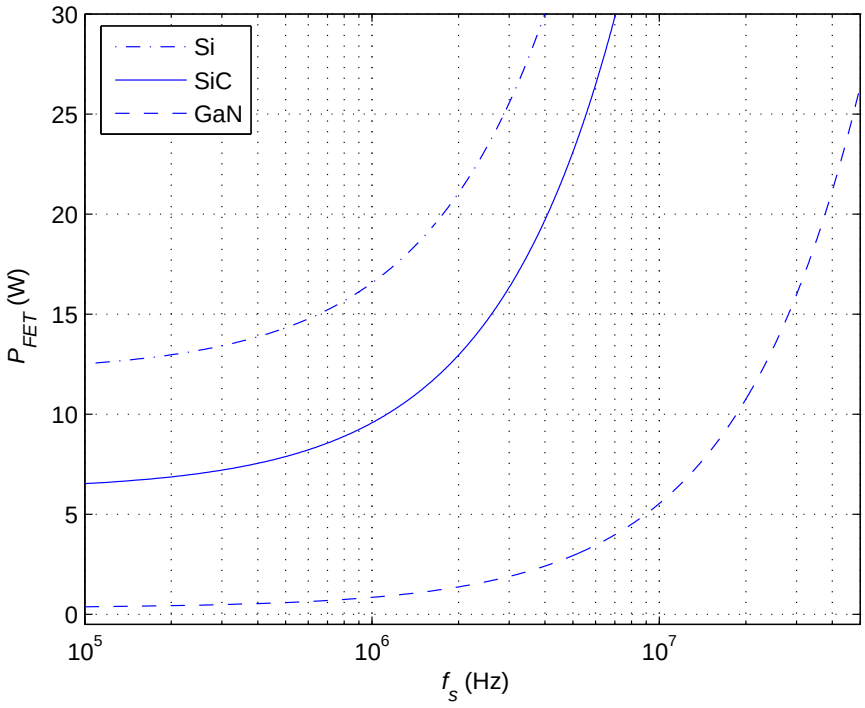

Figure 5.3: Simulated MOSFET power loss P_{FET} versus switching frequency f_s for Si, SiC, and GaN MOSFETs.

Table 5: Drain-to-source capacitance C_{ds} and the on-state resistance r_{DS} of Si, SiC, and GaN at room temperature.

Property	**S**i	**S**iC	**G**aN
$C_{ds}(pF)$	430	61	430
$r_{DS}(m\Omega)$	300	80	5.6

The total power loss of the MOSFET is given by the equation,

$$P_{FET} = P_{rDS} + \frac{P_{SW}}{2}. \tag{5.9}$$

A plot of MOSFET power loss P_{FET} versus switching frequency f_S based on the equations for non-linear capacitance is shown in Figure 5.2. The power loss of each MOSFET using non-linear capacitance equations differs by a high value when compared to the MOSFET power loss obtained when the capacitance is considered linear. A table comparing MOSFET drain-to-source capacitance C_{ds} and the on-state resistance r_{DS} of Si, SiC, and

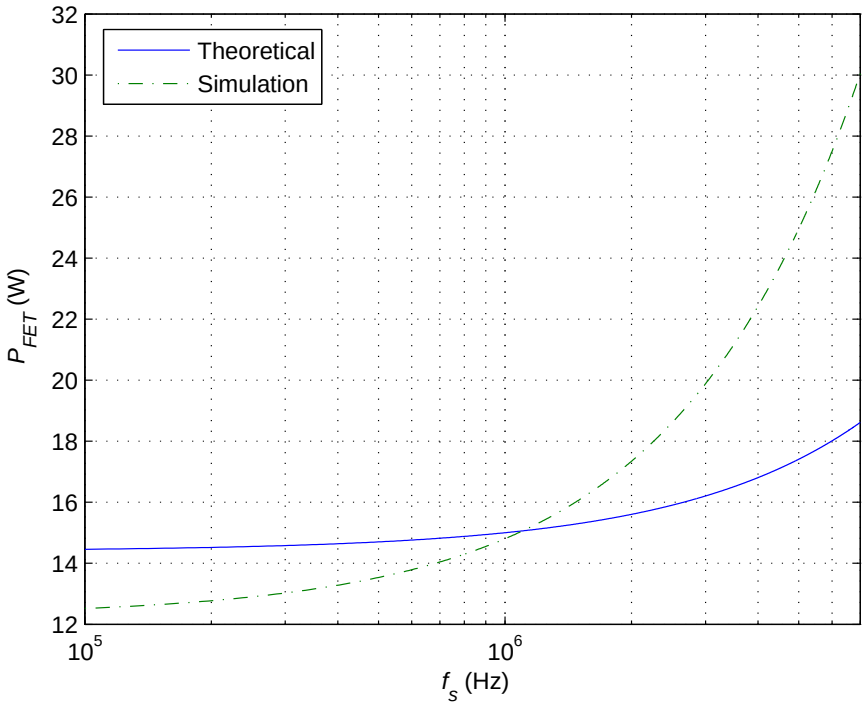

Figure 5.4: Theoretical and simulated MOSFET power loss P_{FET} versus switching frequency f_s for Si MOSFET.

GaN MOSFETs is as shown in Table 5

Considering Table 5, one can say that Si MOSFET has very high power loss when compared to SiC and GaN MOSFETs. This is because Si MOSFET has very high r_{DS} value relatively. Though the drain-to-source capacitance C_{ds} is the same as that of GaN MOSFET, Si MOSFET has very high r_{DS}. The power loss resulting from these, which make up for the total power loss of the MOSFET is high. In Figure 5.2, we can see that SiC has the least MOSFET power loss when compared to Si and GaN. This is due the low C_{ds} and low r_{DS} of the device and the plot obtained is based on theoretical values generated using non-linear capacitance equations. The P_{FET} data obtained from simulation shows exactly how the MOSFET power loss varies with f_S. The P_{FET} of all the three MOSFETs used for analysis increases rapidly after a certain frequency as shown in Figure 5.3

Plots of theoretical MOSFET power loss and power loss obtained via simulations

versus switching frequency f_s for Si, SiC, and GaN are shown in Figures 5.4, 5.5, and 5.6.

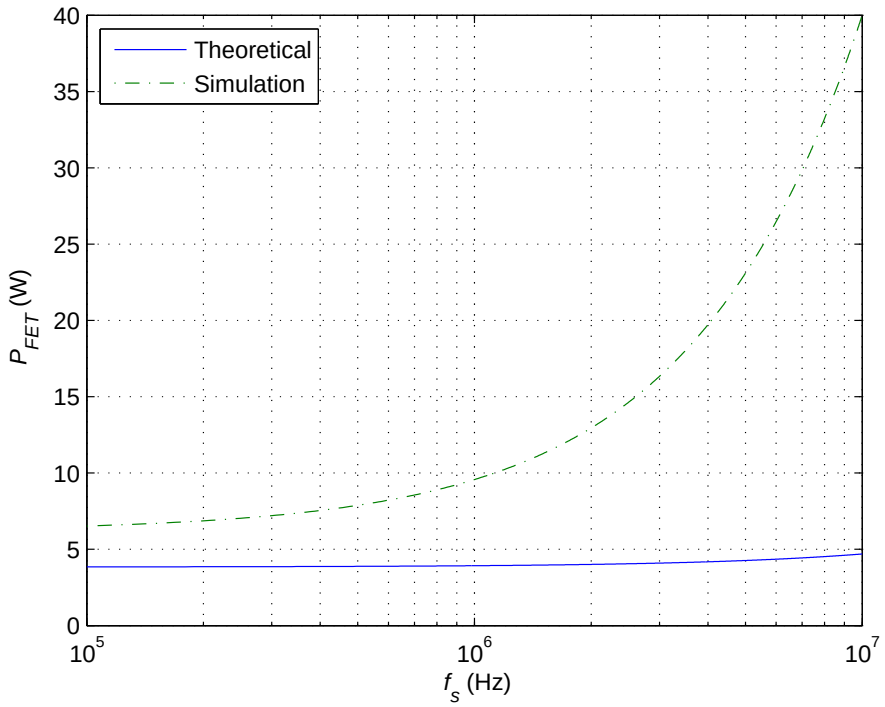

Figure 5.5: Theoretical and simulated MOSFET power loss P_{FET} versus switching frequency f_s for SiC MOSFET.

In Figures 5.4, 5.5, and 5.6, at low frequencies, the theoretical P_{FET} curve matches with the simulated P_{FET} curve. After a certain frequency f_s, the simulated power loss P_{FET} does not exactly match with the theoretical data. This is because, each MOSFET has its own operational frequency limit as explained in earlier chapters. Though the non-linear theoretical equations were used, it does not take into account the parsitic effects of the MOSFET and as a result, the theoretical P_{FET} curve does not match up to the simulated P_{FET} curve. The MOSFET power loss P_{FET} increases more rapidly than the theoretical values obtained. This is clearly seen in Figures 5.4, 5.5, and 5.6. The SiC MOSFETs low r_{DS} has an obvious advantage when it comes to conduction loss, but still suffers from high switching loss when compared to GaN MOSFET. The power loss of GaN MOSFET is very less compared to SiC, which in turn, is less when compared to Si. From the figures above, it

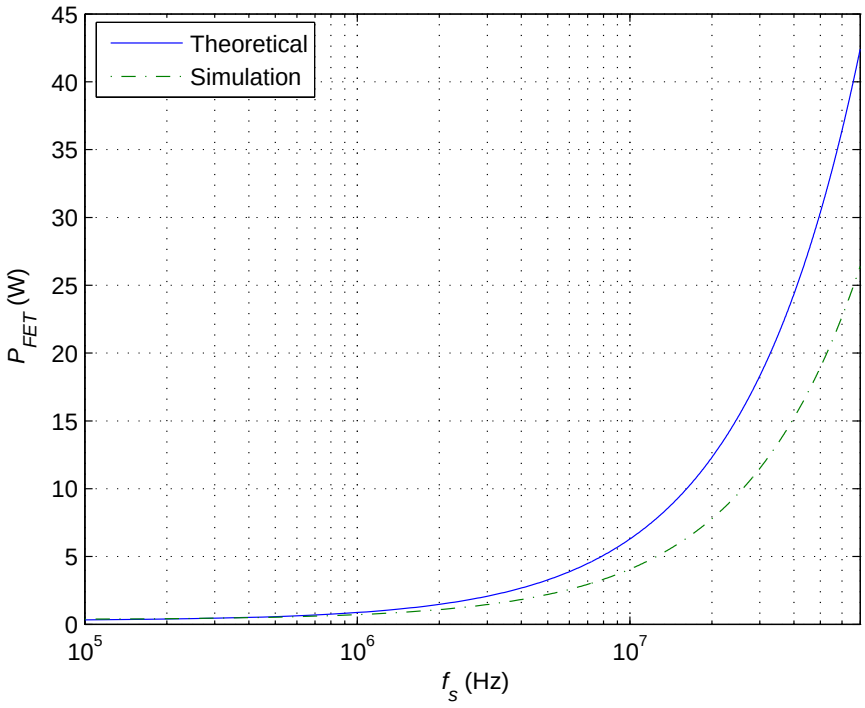

Figure 5.6: Theoretical and simulated MOSFET power loss P_{FET} versus switching frequency f_s for GaN MOSFET.

is seen that the Si MOSFET has the highest power loss at any given frequency and the GaN MOSFET has the least. This low power loss gives rise to high efficiency which is explained in the following section.

The MOSFET conduction loss P_{rDS} is proportional to the duty cycle D at an output current I_O. Maximum conduction takes place when $D = 1$ as the switch is ON all the time. The maximum MOSFET conduction power is given by [1]

$$P_{rDS} = Dr_{DS}{I_O}^2, \tag{5.10}$$

Therefore the total power loss of the MOSFET is given by

$$P_{FET} = P_{rDS} + \frac{P_{SW}}{2}. \tag{5.11}$$

The diode and the inductor power losses are as follows.

$$P_D = (1 - D)(\frac{V_F}{V_O} + \frac{R_F}{R_{Lmin}}), \tag{5.12}$$

$$P_{rL} = r_L {I_O}^2, \tag{5.13}$$

The power loss in the filter capacitor is given by

$$P_{rC} = \frac{r_C {\Delta i_L}^2}{12}, \tag{5.14}$$

Therefore the overall power loss of a buck converter is given by

$$P_{LS} = P_{rDS} + P_{SW} + P_D + P_{rL} + P_{rC}. \tag{5.15}$$

Though the components diode D, inductor L, and capacitor C used are ideal, their losses cannot be neglected at high frequencies and are assumed to be 10% of the output power P_O of the buck converter. This gives rise to the equation

$$P_{LS} = P_{FET} + 10\%(P_O). \tag{5.16}$$

Using the equation above the total power loss P_{LS} of the converter is calculated for the three MOSFETs. Figures 5.7 and 5.8 shows a theoretical plot of overall power loss of the converter P_{LS} versus switching frequency f_s and a plot of simulated total power loss P_{LS} versus switching frequency f_s for Si, SiC, and GaN MOSFETs.

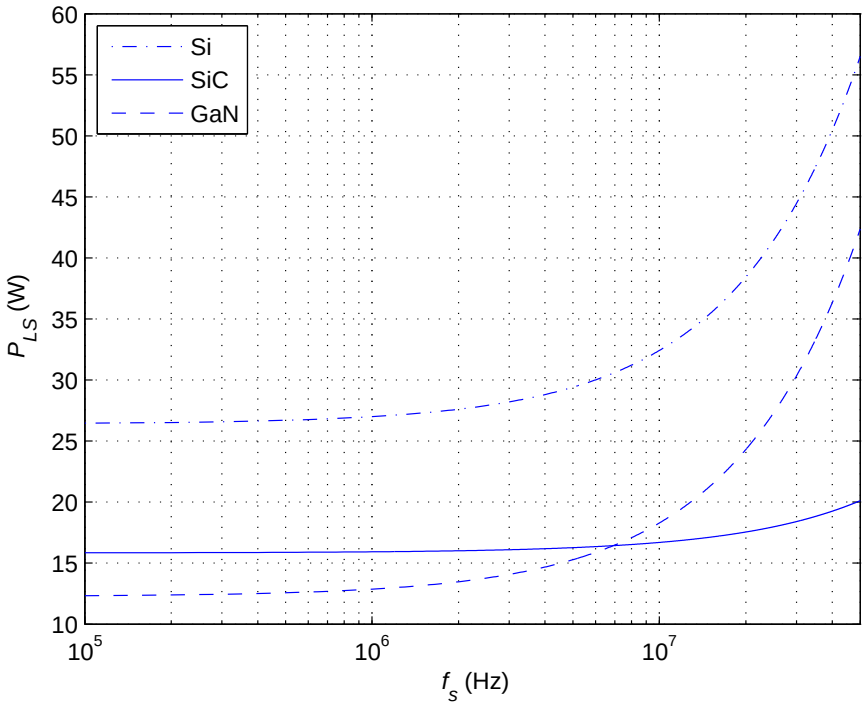

Figure 5.7: Theoretical total power loss of the converter P_{LS} versus switching frequency f_s for Si, SiC, and GaN MOSFET.

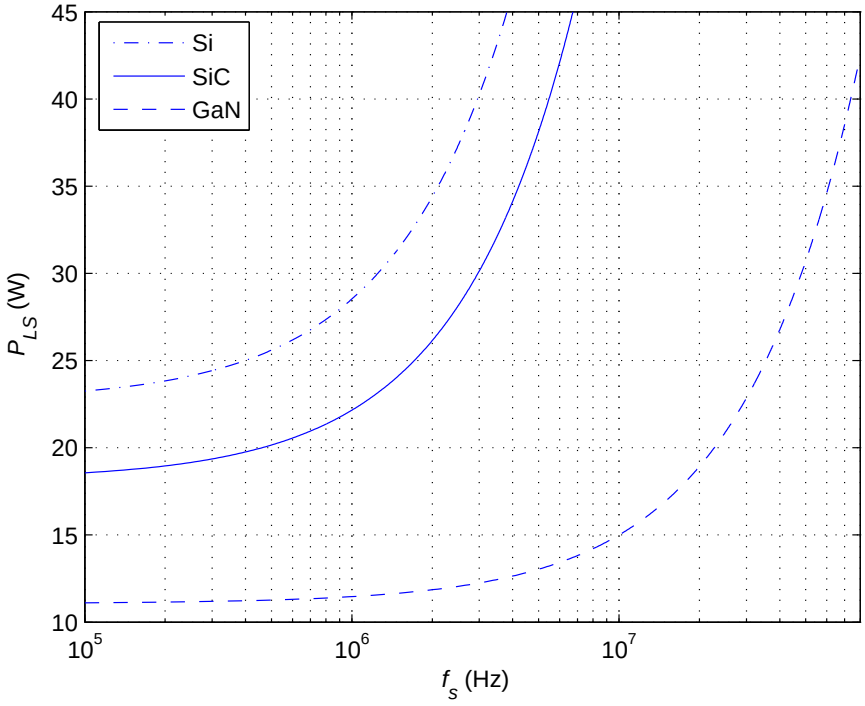

Figure 5.8: Simulated total power loss of the converter P_{LS} versus switching frequency f_s for Si, SiC, and GaN MOSFET.

5.2 Efficiency η

Efficiency, in general describes the capability or the effort of an application to provide a good outcome with very little effort or loss. It is described by the term η and measured in terms of %. The efficiency of a buck converter is given by the equation,

$$\eta = \frac{P_O}{P_O + P_{LS}}. \tag{5.17}$$

Where P_O is the output power of the converter and P_{LS} is the power loss of the converter.

$$P_{LS} = P_{rDS} + P_{SW} + P_D + P_{rL} + P_{rC}. \tag{5.18}$$

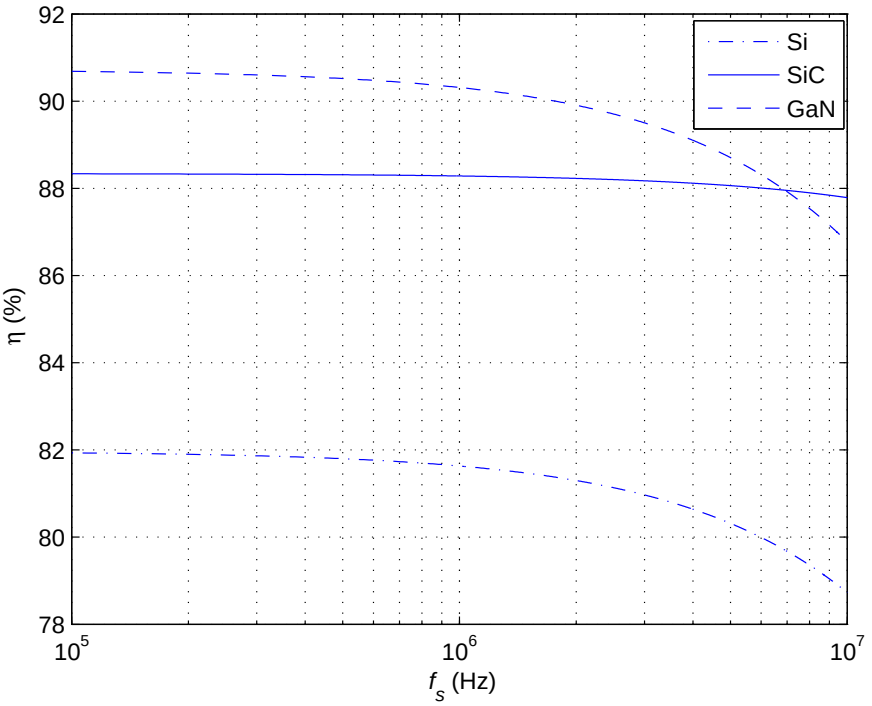

Figure 5.9: Theoretical efficiency η versus switching frequency f_s for Si, SiC, and GaN MOSFET.

As shown in Figures 5.7 and 5.8, the power loss of the converter is highest when Si MOSFET is used for any given frequency and is the least when GaN MOSFET is used.

A plot of efficiency η versus switching frequency f_s for Si, SiC, and GaN MOSFETs based on theoretical values is shown in Figure 5.9. With reference to Figure 5.9, GaN MOSFET has the highest efficiency when compared to Si and SiC due to its low r_{DS} and C_{ds}. SiC MOSFET has better efficiency when compared to Si. At high frequencies, the efficiency of the converter when using GaN MOSFET falls below the efficiency of that of when SiC is used. This is the result of very low C_{ds} and r_{DS} of the SiC MOSFET.

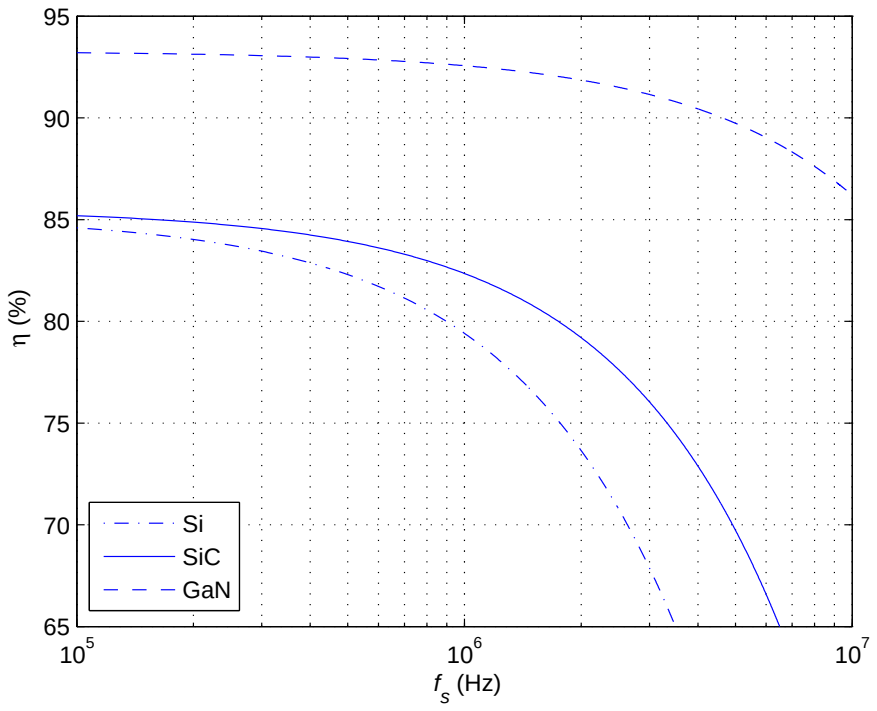

Figure 5.10: Simulated efficiency η versus switching frequency f_s for Si, SiC, and GaN MOSFET.

This is in contradiction with the simulated results. The efficiency of the converter is much higher when GaN MOSFET is used than that of when SiC or Si is used for any given frequency. Figure 5.10 shows a plot of efficiency η versus switching frequency f_s for data obtained through simulations. The efficiency differs by almost 5% when compared to that of when SiC MOSFET is used and differs by at least 10% when compared to when Si MOSFET is used. This is because of the high MOSFET power loss P_{FET} of Si and SiC MOSFETs

when compared to GaN MOSFET. This is possible only due to the basic semiconductor material properties. On the whole one can say that GaN MOSFET is the obvious choice for buck converters as efficiency η and switching frequency f_s are the most important factors that play a major role that determine the credibility of any power electronic system.

6 Conclusion and Future Work

6.1 Conclusion

A systematic study about silicon (Si), silicon carbide (SiC), and gallium nitride (GaN) MOSFETs with reference to their basic semiconductor material properties, switching frequency f_s, power loss P_{FET}, and efficiency η has been carried out in this thesis. Classification of these MOSFETs based on the previous experiments conducted and analysis made has been explained and discussed. The design considerations for the buck converter used have been discussed in detail along with the operation in continuous conduction mode (CCM). Analysis was made based on the simulations performed for various switching frequencies to estimate the power loss and efficiency. Based on the methodology proposed in this thesis, simulations were performed and the cut-off frequency of Si, SiC, and GaN MOSFETs was determined. Detailed study of the same has been made and explained.

Systematically studies the MOSFETs operation beyond their cut-off frequency, i.e., at frequencies much higher than the MOSFETs maximum operating frequency. The parasitic effects of the MOSFET have been explained. A detailed study of the MOSFET power loss P_{FET} and the efficiency η of the buck converter for different frequencies is made. The results and waveforms obtained is verified with the theoretical waveforms and results. On the whole, choosing the right MOSFET always depends on the type of application. A few guidelines based on this thesis have been established and is as follows [20].

1) Never choose a MOSFET with high Miller capacitance C_{gd} as the switching loss goes higher with higher Miller capacitance.

2) Based on the study made, choose a MOSFET with lower drain-to-source capacitance as it is non-linear and is a function of drain-to-source voltage v_{DS}.

3) Always choose a MOSFET with lower r_{DS} as it plays an important role in the charging time of the MOSFET capacitance which in turn affects the switching transients.

6.2 Future Work

Based on the study and results, a cut-off frequency limit for Si, SiC, and GaN MOSFETs has been determined. The MOSFET models used in this thesis for analysis are of order 1. Hence, the results obtained may not be as accurate compared to the results obtained when a higher order model is used. This is because, it does not take into account the effects of the parasitic inductances of the MOSFET. A much accurate result can be obtained using a MOSFET model of higher order.

The MOSFET models used are n-channel MOSFETs. These require a positive voltage to turn ON. Future work can include analysis of p-channel MOSFETs using a suitable gate driver. Characterization was made at room temperature and for a particular low voltage of 28 V. Characterization at higher voltages and higher temperature may provide more detailed information about these MOSFETs, because MOSFETs like SiC are expected to be more efficient at higher temperatures and at higher voltages.

The cut-off switching frequencies determined in this thesis fall in the range of MHz frequency. In order to implement these MOSFETs at such high-frequency, a suitable/efficient gate driver is to be used as the MOSFET is difficult to drive in a buck converter. Gate drivers capable of operating at such high frequencies are not commercially available yet. Developing such a high-frequency driver can lead to hardware experimentation of these MOSFETs. These experiments can lead to further advanced investigation of the MOSFETs. A characterization based on switching frequency was carried out using buck converter in CCM as an application and the advantages and dis-advantages of each type of MOSFET was specified. The high frequency characteristics of these MOSFETs in many different applications and their qualities are yet to be known and can provide much needed information for the further development of MOSFETs in the field of power electronics.

7 Bibliography

References

[1] M. K. Kazimierczuk, *Pulse-width Modulated DC-DC Power Converters*, United Kingdom: John Wiley & Sons, Inc., 2008.

[2] C.-In. H. Chen and A. Kumar, *Bicmos Logic Circuits*, United Kingdom: Kluwer Academic Publishers., 2002.

[3] N. A. Sherwani , *Algorithms for VLSI Physical Design Automation*, United States: John Wiley & Sons, Inc., 1999.

[4] N. Ting, Q. Haihong, B. Zhao, and N. Xin, " Evaluation of SiC MOSFET in buck converter," *IEEE Industrial Electronics and Applications (ICIEA)*, pp. 1213-1216, June 2013.

[5] J. Boehmer, J. Schumann, and H.-G. Eckel, "Effect of the miller-capacitance during switching transients of IGBT and MOSFET," *IEEE Power Electronics and Motion Control Conference (EPE/PEMC), 2012 15th International*, pp. LS6d.3-1 - LS6d.3-5, September 2012.

[6] M. Lazarczyk, N. Barry, T. O'Donnell, and Boguslaw Grzesik, "Design considerations for high frequency buck converter," *IEEE Universities Power Engineering Conference.*, pp. 701-706, September 2007.

[7] K. Gauen, "The effects of MOSFET output capacitance in high-frequency applications," *IEEE Industry Applications Society Annual Meeting.*, vol. 2, pp. 1227-1234, October. 1989.

[8] K. Shah and K. Shenai, "Simple and accurate circuit simulation model for gallium nitride power transistors," *IEEE Trans. Electron Devices.*, vol. 59, no. 10 pp. 2735-2741, October 2012.

[9] B. J. Baliga, "Power semicondcutor device figure of merit for high-frequency applications," *IEEE Trans. Electron Devices.*, vol. 10, no. 10 pp. 455-457, October 1989.

[10] Z. Chen, D. Boroyevich, R. Burgos, and F. Wang, "Characterization and modeling of 1.2 kV, 20 A SiC MOSFETs," *IEEE Energy Conversion Congress and Exposition, (ECCE).*, pp. 1480-1487, September 2009.

[11] J. A.Cooper, JR. and A. Agarwal, "SiC power-switching devices - The second electronics revolution," *Proceedings of the IEEE.*, vol. 90, no. 6 pp. 956-968, June 2002.

[12] Z. Chen and D. Boroyevich, "Modeling and simulation of SiC MOSFET fast switching behavior under circuit parasitics," *Proceedings of the 2010 Conference on Grand Challenges in Modeling Simulation.*, pp. 352-359, 2010.

[13] J. Hornberger, A. B. Lostetter, K. J. Olejniczak T. McNutt, S. Magan Lal, and A. Mantooth, "Silicon-carbide (SiC) semiconductor power electronics for extreme-high temperature environments," *IEEE Aerospace Conference.*, vol. 4, pp. 2538-2555, March 2004.

[14] A. Ong, J. Carr, J. Balda, and A. Mantooth, "A comparison of silicon and silicon carbide MOSFET switching characteristics," *IEEE Region 5 Technical Conference.*, pp. 273-277, April 2007.

[15] R. Chu, A. Corrion, M. Chen, R. Li, D. Wong, D. Zehnder, B. Hughes, and K. Boutros, "1200 V normally off GaN-on-Si field-effect transistors with low dynamic on-resistance," *IEEE Trans. Electron Device Letters.*, pp. 632-634, March 2011.

[16] J. W. Chung, K. Ryu, B. Lu, and T. Palacios, "GaN-on-Si technology, a new approach for advanced devices in energy and communications," *IEEE Solid-State Device Research Conference (ESSDERC).*, pp. 52-56, September 2010.

[17] D. Mistele, T. Rotter, K.S. Rover, S. Paprotta, M. Seyboth, V. Schwegler, F. Fedler, H. Klausing, O.K. Semchinova, J. Stemmer, J. Aderhold, and J. Graul, "First AlGaN/-GaN MOSFET with photoanodic gate dielectric," *ELSEVIER Materials Science and Engineering.*, 2002.

[18] Y. Cai, Y. Zhou, K. M. Lau, and K. J. Chen, "Control of threshold voltage of AlGaN/-GaN HEMTs by fluoride-based plasma treatment: from depletion mode to enhancement mode," *IEEE Trans. Electron Devices.*, vol. 53, no. 9, pp. 2207-2215, September 2006.

[19] J. Delaine, P.-O. Jeannin, and D. Frey, "High frequency DC-DC converter using GaN device," *IEEE Applied Power Electronics Conference and Exposition (APEC).*, pp. 1754-1761, February 2012.

[20] Z. Chen, "Characteristics and modeling of high-switching speed behavior of SiC active devices," Virgina Polytechnic Institute and State University, December 2009.

[21] B. K. Bose, "Advances in power electronics-its impact on the environment," *IEEE Proceedings Industrial Electronics ISIE.*, vol. 1, pp. 28-30, July 1998.

[22] "Gallium nitride (GaN) versus silicon carbide (SiC) in the high frequency (HF) and power switching applications," Microsemi Corp.

[23] "SiC MOSFET module replaces up to 3 times higher current Si IGBT modules in voltage source inverter application," Bodos Power Systems.

[24] "Estimating MOSFET parameters from the data sheet," *Appendix A.*, pp. 2.41-2.45, Texas Instruments.

[25] "SiC power devices and modules," ROHM Semiconductors, June 2013.

[26] "AN002: Fundamentals of gallium nitride power transistors," Efficient Power Conversion.

[27] "AN001: Is it the end of the road for silicon in power conversion?," Efficient Power Conversion.

[28] "AN007: High frequency 24 V to 1 V DC-DC converters using EPC's gallium nitride (GaN) power transistors," Efficient Power Conversion.

[29] "White paper 09: Impact of parasitics on performance," Efficient Power Conversion.

[30] "White paper 01: Gallium nitride (GaN) technology overview," Efficient Power Conversion.

[31] "AN608: Power MOSFET basics: understanding gate charge and using it to assess switching performance," Vishay Siliconix.

[32] "AN: Can gallium nitride replace silicon?," Efficient Power Conversion.

[33] "AN: Application considerations for silicon carbide MOSFETs," CREE Inc.

[34] International Rectifiers, IRF350 n-channel Si MOSFET datasheet, www.datasheetcatalog.com.

[35] ROHM Semiconductors, SCT2080KE n-channel SiC MOSFET datasheet, www.rohm.com.

[36] Efficient Power Conversion, EPC2001 n-channel GaN HEMT datasheet, www.epc-co.com.

8 Appendix

8.1 PSpice Model of Silicon n-channel MOSFET (IRF350)

```
.SUBCKT irfru3504z 1 2 3
* SPICE3 MODEL WITH THERMAL RC NETWORK
* Model generated on Jul 20, 04
* MODEL FORMAT: SPICE3
* Symmetry POWER MOS Model (Version 1.0)
* External Node Designations
* Node 1 -> Drain
* Node 2 -> Gate
* Node 3 -> Source
M1 9 7 8 8 MM L=100u W=100u
.MODEL MM NMOS LEVEL=7 IS=1e-32
+VTO=4.33685 LAMBDA=0 KP=35.0031
+CGSO=1.27558e-05 CGDO=3.85542e-08
RS 8 3 0.00315494
D1 3 1 MD
.MODEL MD D IS=3.33604e-15 RS=0.00431783 N=0.832107 BV=40
+IBV=0.00025 EG=1 XTI=1 TT=1e-07
+CJO=5.9213e-10 VJ=0.5 M=0.358745 FC=0.5
RDS 3 1 1e+07
RD 9 1 0.0001
RG 2 7 4.2907
D2 4 5 MD1
* Default values used in MD1:
*   RS=0 EG=1.11 XTI=3.0 TT=0
*   BV=infinite IBV=1mA
.MODEL MD1 D IS=1e-32 N=50
+CJO=1.14152e-09 VJ=0.5 M=0.457207 FC=1e-08
D3 0 5 MD2
* Default values used in MD2:
*   EG=1.11 XTI=3.0 TT=0 CJO=0
*   BV=infinite IBV=1mA
.MODEL MD2 D IS=1e-10 N=0.52542 RS=3e-06
RL 5 10 1
FI2 7 9 VFI2 -1
VFI2 4 0 0
EV16 10 0 9 7 1
CAP 11 10 1.14152e-09
FI1 7 9 VFI1 -1
VFI1 11 6 0
RCAP 6 10 1
D4 0 6 MD3
* Default values used in MD3:
*   EG=1.11 XTI=3.0 TT=0 CJO=0
```

```
*   RS=0 BV=infinite IBV=1mA
.MODEL MD3 D IS=1e-10 N=0.52542
.ENDS irfru3504z

*SPICE 2-Layer Thermal Model Subcircuit
.SUBCKT irfru3504zt 2 0

R_RTHERM1         2 1  1.117722
C_CTHERM1         2 0  0.00048
R_RTHERM2         1 0  0.542278
C_CTHERM2         1 0  0.008166

.ENDS irfru3504zt
```

8.2 PSpice Model of Silicon Carbide n-channel MOSFET (SCT2080KE)

```
*$
* SCT2080KE SiC NMOSFET model
* Model Generated by ROHM
* All Rights Reserved
* Commercial Use or Resale Restricted
* Date: 2013/08/23
******************D G S
.SUBCKT SCT2080KE 1 2 3
.PARAM T0=25
.FUNC R1(I)   {59.56m*I*(1+0.5563*(EXP((TEMP-T0)/128.7)-1))+
+              4.300u*I*ABS(I)**(1.898/(1+0.5341*(EXP((TEMP-T0)/-17.66)-1)))*
+             (1+0.9978*(EXP((TEMP-T0)/-6.998)-1))}
.FUNC V1(V,W) {V-87.01m*W/(1+0.2299*(EXP((TEMP-T0)/-71.48)-1))-
+              395.5m*ASINH(W/0.3073/(1+0.1881*(EXP((TEMP-T0)/-47.01)-1)))}
.FUNC V2(V)   {IF(V>0,2.053u*V**7.933/(1+0.9745*(EXP((TEMP-T0)/-32.48)-1)),0)}
.FUNC I1(V,W) {V*(ABS(W)+1000)/1010*1.2*W/(ABS(W)+2)}
.FUNC C1(V)   {IF(V>-1.891,1526+193.0*V,1905*(1-V/1.119)**-0.5006)}
.FUNC C2(V)   {C1(V)*(0.4187*TANH((V+1.426)*1.264)+0.5813)-5.147m*V}
V1  1 11 0
E1 11 12 VALUE={R1(LIMIT(I(V1),-1MEG,1MEG))}
V2  2 21 0
E2 21 22 VALUE={I(V2)*11.5}
V3  3 31 0
E3 31 32 VALUE={I(V3)*0.00}
E4 41  0 VALUE={LIMIT(V(22,32),0,22)}
E5 42  0 VALUE={V1(V(41),LIMIT(V(43),0,200))}
E6 43  0 VALUE={V2(LIMIT(V(42),0,20))}
G1 12 32 VALUE={I1(V(43),V(12,32))}
C1 12 32 1p
R1 12 32 1E15
E7 51  0 VALUE={V(22,1)}
E8 52  0 VALUE={V(22,1)}
V4 52 53
C2 53  0 1p
G2 22  1 VALUE={I(V4)*C2(V(51))}
C3 22 32 2.064n
R2 22 32 1G
********* ********* ********* ********* *********
.FUNC R101(I) {1.395*ASINH(I/6.151)*EXP((TEMP-T0)/1035)+404.5u*I*ABS(I)}
.FUNC I101(V) {IF(V>0,309.4u*V**(10.21*EXP((TEMP-T0)/2494))*EXP((TEMP-T0)/43.22),0)}
.FUNC I102(V) {IF(V<0,1.528n*(EXP(V/10)-1)*EXP(-V/969.2)*EXP((TEMP-T0)/267.4)*
+             (EXP((-V-1720*EXP((TEMP-T0)/1250))/10)+1),0)}
.FUNC C101(V) {IF(V>0.5735,896.6+988.5*V,1119*(1-V/1.147)**-0.3874)-50.20-29.23m*V}
V101   3 103 0
E101 103 104 VALUE={R101(LIMIT(I(V101),-1MEG,1MEG))}
E102 111   0 VALUE={V(104,1)}
```

```
E103 112   0 VALUE={V(104,1)}
V102 112 113 0
C101 113   0 1p
G101 104   1 VALUE={I101(LIMIT(V(111),0,20))+I102(LIMIT(V(111),-3k,0))+
+                  I(V102)*C101(LIMIT(V(111),-3k,20))}
.ENDS SCT2080KE
*$
```

8.3 PSpice Model of Gallium Nitride n-channel MOSFET (EPC2001)

```
* source EPC2001DEV1
.subckt EPC2001 gatein drainin sourcein
.param aWg=1077 A1=41.7998 k2=2.259866e+000 k3=1.2e-001 rpara=4.463059e-003
+   aITc=5.486028e-003 arTc=-4.699671e-003 ax0Tc=0.75E-4 x0_0=-0.75 x0_1=1.10
+   dgs1=4.3e-7 dgs2=2.6e-13 dgs3=.8 dgs4=.23
+   ags1=8.6952e-010 ags2=5.3168e-010 ags3=1.9975e+000 ags4=2.8377e-001
+   ags5=-1.4751e-010 ags6=-7.5163e+000 ags7=7.2121e+000
+   agd1=1.4182e-011 agd2=2.1475e-010 agd3=-3.8030e+000 agd4=5.9551e+000
+   asd1=3.3621e-010 asd2=6.3080e-010 asd3=-1.2803e+001 asd4=2.2690e+000
+   asd5=2.5818e-010 asd6=-4.0599e+001 asd7=2.0638e+001

rd drainin drain {(0.75*rpara*(1-arTc*(Temp-25)))}
rs sourcein source {(0.25*rpara*(1-arTc*(Temp-25)))}
rg gatein gate {(.6)}

*Large resistors to aid convergence
Rcsdconv drain source {100000Meg/aWg}
Rcgsconv gate source {100000Meg/aWg}
Rcgdconv gate drain {100000Meg/aWg}


gswitch drain source Value {if( v(drain,source)>0.0,
+   (A1*(1-aITc*(Temp-25))*log(1.0+exp((v(gate,source)-k2)/k3))*
+   v(drain,source)/(1 + max((x0_0+x0_1*v(gate,source))/
+(1+ax0Tc*(Temp-25)*(Temp-25)),0.5)*v(drain,source)) ),
+   (-A1*(1-aITc*(Temp-25))*log(1.0+exp((v(gate,drain)-k2)/k3))*
+   v(source,drain)/(1 + max((x0_0+x0_1*v(gate,drain))/
+(1+ax0Tc*(Temp-25)*(Temp-25)),0.5)*v(source,drain)) ) ) }


ggsdiode gate source VALUE {if( v(gate,source) < 10,
+   0.5*aWg/1077*(dgs1*(exp((v(gate,source))/dgs3)-1)
+dgs2*(exp((v(gate,source))/dgs4)-1)),
+   0.5*aWg/1077*(dgs1*(exp((10)/dgs3)-1)+dgs2*(exp((10)/dgs4)-1)) ) }


ggddiode gate drain Value {if( v(gate,drain) < 10,
+   0.5*aWg/1077*(dgs1*(exp((v(gate,drain))/dgs3)-1)
+dgs2*(exp((v(gate,drain))/dgs4)-1)),
+   0.5*aWg/1077*(dgs1*(exp((10)/dgs3)-1)+dgs2*(exp((10)/dgs4)-1)) ) }



*Parasitic gate-source capacitance
*C_GS         gate source  {ags1}
*Model for voltage dependent gate-source capacitance
```

```
E_IGS tl_gs bl_gs value = {0.5*ags2*ags4*log(1+exp((v(gate,source)-ags3)/ags4))+
+   ags5*ags7*log(1+exp((v(source,drain)-ags6)/ags7))+
+   ags1*v(gate,source) }
V_INGS br_gs bl_gs 0.0
C_IGS br_gs tr_gs {1.0e-6}
R_IGS tr_gs tl_gs {1.0e-4}
F_IGS gate source V_INGS 1e6
R_IGS2 bl_gs source 100Meg

*Parasitic gate-drain capacitance
*C_GD         gate drain  {agd1}
*Model for voltage dependent gate-drain capacitance
E_IGD tl_gd bl_gd value = {0.5*ags2*ags4*log(1+exp((v(gate,drain)-ags3)/ags4))+
+   agd2*agd4*log(1+exp((v(gate,drain)-agd3)/agd4))+
+   agd1*v(gate,drain) }
V_INGD br_gd bl_gd 0.0
C_IGD br_gd tr_gd {1.0e-6}
R_IGD tr_gd tl_gd {1.0e-4}
F_IGD gate drain V_INGD 1e6
R_IGD2 bl_gd drain 100Meg

*Parasitic source-drain capacitance
*C_SD         source drain  {asd1}
*Model for voltage dependent source-drain capacitance
E_ISD tl_sd bl_sd value = {asd2*asd4*log(1+exp((v(source,drain)-asd3)/asd4))+
+   asd5*asd7*log(1+exp((v(source,drain)-asd6)/asd7))+
+   asd1*v(source,drain) }
V_INSD br_sd bl_sd 0.0
C_ISD br_sd tr_sd {1.0E-6}
R_ISD tr_sd tl_sd {1.0e-4}
F_ISD source drain V_INSD 1e6
R_ISD2 bl_sd drain 100Meg

.ends
```