

Frequency dispersion reduction and bond conversion on *n*-type GaAs by *in situ* surface oxide removal and passivation

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The method of surface preparation on *n*-type GaAs, even with the presence of an amorphous-Si interfacial passivation layer, is shown to be a critical step in the removal of accumulation capacitance frequency dispersion. *In situ* deposition and analysis techniques were used to study different surface preparations, including NH₄OH, Si-flux, and atomic hydrogen exposures, as well as Si passivation depositions prior to *in situ* atomic layer deposition of Al₂O₃. As–O bonding was removed and a bond conversion process with Si deposition is observed. The accumulation capacitance frequency dispersion was removed only when a Si interlayer and a specific surface clean were combined. © 2007 American Institute of Physics. [DOI: 10.1063/1.2801512]

GaAs has once again attracted attention as an alternative substrate for metal oxide semiconductor (MOS) technologies. The advantages of GaAs over silicon are well-known, mainly having a higher electron mobility and breakdown voltage as well as a direct band gap suggesting GaAs for a wide range of devices. The elimination of anomalous frequency dispersion of the accumulation capacitance of GaAs MOS devices is a major motivation behind surface and interface treatment studies. Previous reports have attributed this dispersion, *viz.*, the reduction of maximum capacitance with increasing measurement frequency, to a high density of interface states which results in Fermi-level pinning. Recent studies have indicated that the disruption of As–O bonding at the dielectric/GaAs interface results in an unpinned interface.¹ Revisiting earlier works on Si passivation of GaAs surfaces (see, for example, Refs. 2 and 3), recent reports of Si deposition on GaAs for surface passivation in conjunction with high-*k* dielectrics (for example, Refs. 4 and 5), have stimulated this study using *in situ* deposition and analysis methods. In this letter, *in situ* analysis techniques are used to correlate differences in electrical characteristics caused by different surface treatments employed on the technologically relevant *n*-type GaAs surface for use in enhancement mode transistors.

The samples used in this work were *n*-type Si-doped GaAs wafers with a doping concentration of $5 \times 10^{17} \text{ cm}^{-3}$. One set of samples was degreased in acetone, methanol, and isopropyl alcohol for 1 min each, followed by a 3 min etch in 29% NH₄OH,⁶ and dried with N₂, while another set was prepared, *in situ* with no chemical treatment, using a hydrogen cracker source (cell temperature of 1400 °C, $P_{\text{H}_2} = 1 \times 10^{-6} \text{ mbar}$) producing atomic H with a substrate temperature of 430 °C for 30 min.^{7,8} Silicon of various thicknesses was deposited at room temperature on treated GaAs by

e-beam evaporation (deposition rate = 18–132 Å/min in a multitechnique deposition/characterization system (base pressure = $2 \times 10^{-11} \text{ mbar}$).⁹ MOS capacitors were made using such treated surfaces followed by atomic layer deposition (ALD) of 10 nm of Al₂O₃ using trimethylaluminum (TMA) and H₂O at 300 °C in an adjacent chamber and *ex situ*, rf sputtered TaN as the gate metal using shadow masks. An *ex situ* electron-beam evaporated Ni/Au/Ge alloy annealed at 425 °C was used as an Ohmic back contact.¹⁰

The two types of surface cleans produce widely disparate surfaces with respect to bonding. The native oxide of GaAs exhibits As⁺⁵ and As⁺³ oxidation states in addition to Ga–O formation.¹¹ Exposure of the native oxide to the NH₄OH etch reduces the As–O bond concentration, as seen in photoelectron spectroscopy.¹² As–O bonding is further reduced by a post-etch, *in situ* anneal in vacuum up to 325 °C, as seen by monochromatic (Al K $\alpha_{1,2}$, 1486.7 eV) x-ray photoelectron spectroscopy (XPS) in Fig. 1(a). Analysis of the corresponding O 1s region for the annealed surface [Fig. 1(c)] reveals that the O concentrations for the etched surface and the annealed surface are comparable, indicating no significant loss of oxygen and suggesting that the bond conversion from As–O to Ga–O bonding is favored with such treatments.^{13,14}

Atomic hydrogen exposure removes As–O and Ga–O bonds by producing water and unstable As and Ga oxides that desorb at the 430 °C substrate temperature used here.⁷ Figures 1(a) and 1(b) show the striking difference in the concentrations of As–O and Ga–O bondings, respectively, for each of the two treatments with both peaks being below the detection limit after H exposure. Figure 1(c) illustrates the reduction in the total amount of oxygen after exposure to the atomic hydrogen.

Exposure of the NH₄OH-etched surface to a Si flux¹⁵ also results in the reduction of As–O bonding [Fig. 2(a)] in favor of Si–O bond formation without the loss of surface oxygen. As seen in the Ga 3d region [Fig. 2(b)], the presence of Ga–O is detected as a shoulder in the photoelectron spectra. The feature is seen to shift toward the bulk Ga peak as a

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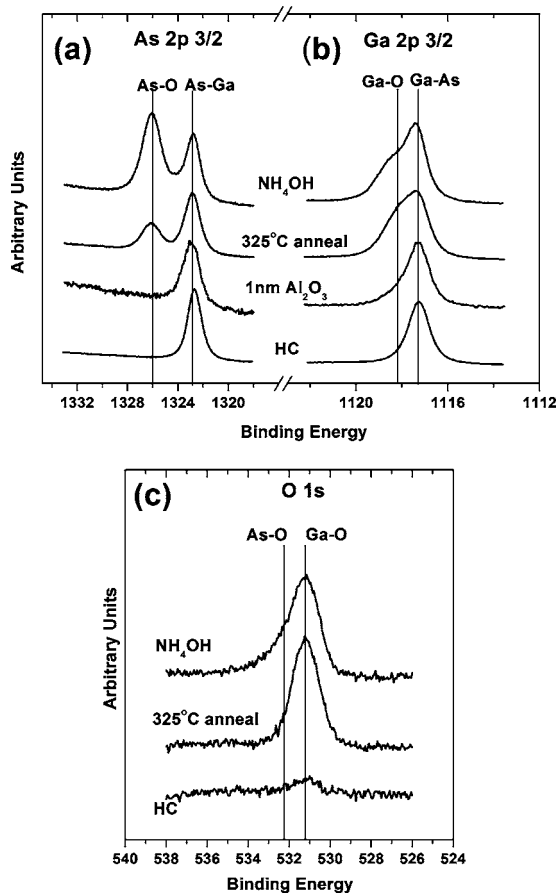


FIG. 1. (a) As $2p_{3/2}$, (b) Ga $2p_{3/2}$, and (c) O $1s$ spectra showing marked difference in surface oxygen between NH_4OH clean, 325°C anneal, ALD Al_2O_3 deposition, and atomic hydrogen exposure.

function of Si-flux exposure, suggesting that the Si exposure gradually results in Ga–O–Si bonding over Ga–O–As bonding. The ratio of the Ga–O peak area to the bulk Ga peak area indicates that there is no detectable loss of Ga–O bonds, consistent with a bond conversion process. We note that under the *in situ* deposition techniques employed here, no As–O–Si bonding is detected in contrast to previous reports.⁴

The amount of SiO_x that arises as the Si is deposited on the differently prepared surfaces as calculated using Si $2p$ XPS spectra also differs (not shown). On an NH_4OH treated surface exposed to a Si deposition of ~ 1.1 nm, 40% of the Si $2p$ signal is from some form of SiO_x rather than Si–Si bonds. The H-treated surface, with a substantially lower amount of oxygen, has a significantly lower percentage of its Si $2p$ signal due to an oxide after Si deposition. This SiO_x layer could be a direct cause of Fermi-level pinning, as reported recently.¹⁶

The capacitance-voltage (C - V) characteristics of samples with Al_2O_3 deposited directly on the NH_4OH and hydrogen-treated n -type GaAs (100) surfaces show the same amount of accumulation capacitance (C_{acc}) frequency dispersion for both types of surface preparations (not shown). These similarities, despite the different starting surfaces, are probably due to the comparable number of interfacial oxide bonds after dielectric deposition due to the subsequent exposure to oxygen from H_2O in the ALD cycles. We note that the As–O peak of the NH_4OH treated surface is reduced below detection limit after ALD deposition [Fig. 1(a)], as seen by previous groups.^{17,18} There is also detectable Ga–O bond forma-

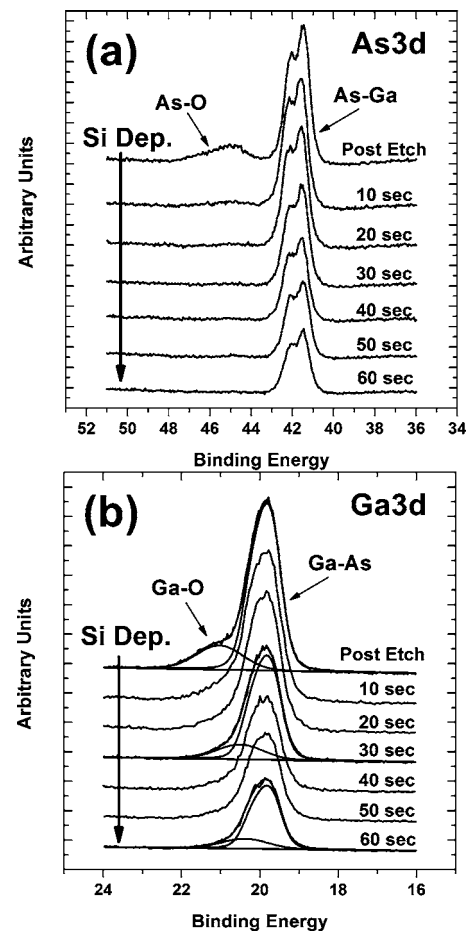


FIG. 2. (a) As $3d$ XPS results showing As–O removal as a function of Si deposition and (b) Ga $3d$ XPS results showing bond conversion after Si-flux exposure to the NH_4OH treated GaAs surface.

tion for the atomic hydrogen–treated sample after Al_2O_3 deposition, in contrast to the H-cleaned surface prior to Al_2O_3 deposition. As a result, As–O and Ga–O species are similar in concentration for these two post-ALD surfaces (not shown).

Figure 3 shows the changes in the dispersion observed from a device consisting of a Si interlayer deposited on the prepared GaAs surface followed by Al_2O_3 deposition. Figure 3(a) shows the C - V response of 1.1 nm e-beam deposited Si with 10 nm Al_2O_3 on an NH_4OH cleaned surface. The frequency dispersion is still prevalent suggesting that simply depositing a Si interlayer without further surface treatment will not reduce the dispersion. Figure 3(b) shows the significant reduction in C_{acc} frequency dispersion for the identical Si and Al_2O_3 depositions on a H-treated substrate. The shift in the voltage transition region as a function of frequency is a behavior generally attributed to the presence of unpassivated interface states.¹⁹ This occurs when the capacitance due to interface traps is larger than the oxide capacitance. The amount of oxygen at the starting surface appears to be of utmost importance for the reduction of this dispersion. Furthermore, each of the stacks which produced the C - V curves shown has interfaces that show As–O below the detection limit of XPS. Due to the different accumulation capacitance responses, it is unlikely that As–O is the root of the dispersion.

The frequency dispersion of the voltage transition observed in the capacitors with reduced accumulation disper-

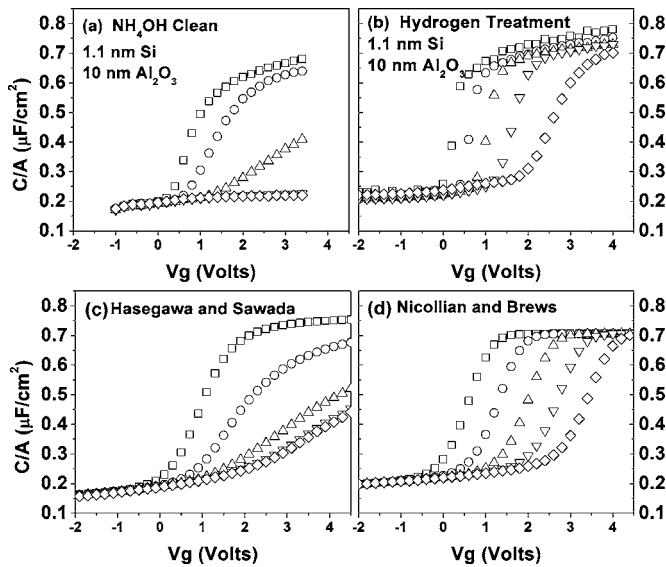


FIG. 3. C - V curves of (a) NH_4OH cleaned GaAs surface and (b) atomic H-treated GaAs surface, each with 1.1 nm Si interlayer and 10 nm ALD deposited Al_2O_3 , and simulated data using the (c) Hasegawa-Sawada model and (d) Nicollian-Brews model. Symbols correspond to different frequencies: \square , 100 Hz; \circ , 1 kHz; \triangle , 10 kHz; ∇ , 100 kHz; and \diamond , 1 MHz.

sion [Fig. 3(b)] can be modeled using the Nicollian-Brews (NB) interface state model.¹⁹ Figure 3(d) shows a simulation of this model using an interface state density (D_{it}) of approximately $5 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$. The NB model cannot, however, simulate the C_{acc} dispersion characteristics of Fig. 3(a). Hasegawa and Sawada (HS) proposed a structurally different model to explain the C_{acc} dispersion phenomenon using a “disordered” GaAs layer at the interface of the crystalline substrate and the dielectric.²⁰ Following this model, we assume that trap states in the bulk of the dielectric can be occupied by tunneling due to a postulated lower band gap of a disordered dielectric/interface region. Using the same value of D_{it} used in the NB model as a parameter for the HS model produces the C - V curves shown in Fig. 3(c), exhibiting a behavior reminiscent of the experimental curves [Fig. 3(a)]. The C - V models, therefore, suggest that the interfacial defect density may not be the reason for reduced accumulation capacitance frequency dispersion. These models, while using the same interface state density, produce different C - V characteristics due to the disordered layer in the HS model.

In summary, the starting surface of GaAs must be prepared so that the atomic concentrations of surface As and Ga oxide species are below the XPS detectable limits, less than ~ 1 at. % ($< 10^{13} \text{ cm}^{-2}$), to reduce the C_{acc} frequency dispersion seen in GaAs MOS capacitors. However, while the surface cleans examined do not appear to be sufficient to reduce the dispersion due to oxide formation from subsequent dielectric deposition, Si deposition on a starting surface that

has residual oxide species is not in itself sufficient to reduce the dispersion. These results suggest that an interlayer on an oxide-free surface is required to reduce the dispersion, as shown by a Si interlayer on a hydrogen cleaned surface. We also observe the removal of As–O bonds with a Si-flux exposure, ALD Al_2O_3 deposition, as well as hydrogen exposure. We also note that As–O bonds are below XPS detectable limits in a number of devices examined here; however, some show reduced dispersion while others do not. This strongly suggests that the As–O bonding is not the primary species responsible for the frequency dispersion of accumulation capacitance.

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