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# Frequency response masking based FIR filter using approximate multiplier for bio-medical applications

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**Abstract.** The advancements in medical healthcare networks and bio-medical sensor technologies enabled the use of wearable and body implantable intelligent devices for healthcare monitoring. These battery-operated devices must be capable of very low power operation for ensuring long battery life and also to prevent intense radiations. The major power consuming part of these devices are the multipliers built into the digital filters for performing signal processing operations. This paper proposes a low power signed approximate multiplier architecture for bio-medical signal processing applications. The circuit characteristics and error metrics of the proposed multiplier are estimated to verify its performance advantage over other approximate multipliers. In order to validate the efficacy of the approximate multiplier in real time signal processing applications, a band pass finite impulse response filter (FIR) filter is designed using frequency response masking technique and used in the Pan Tompkins method for the extraction of QRS complex from raw ECG data. The sensitivity, positive predictivity, and detection error rate of the QRS detection method are estimated and the results show that the approximate filtering method implemented gives a comparable performance as that of exact methods.

**Keywords.** Approximate multiplier; ECG; FRM; QRS detection; Wordlength reduction.

## 1. Introduction

The technological advancements in the field of wireless sensor networks, medical sensors, and microelectronic devices enabled the development of Wireless Body Area Networks (WBAN) and Wireless Body Sensor Networks (WBSN). These technologies can provide continuous monitoring of various health parameters of critically ill patients. The intelligent sensors and devices can be used as wearables or implantable in the human body without any positive hindrance to daily life and with connectivity to the healthcare network. Such a constraint demands very low power operations and high-speed data communication capabilities for these intelligent agents or interfaces to maintain connectivity and real time data processing. In this context, bio-medical signal processing constitutes an active area of research and development as it offers great potential to improve the healthcare delivery, diagnostic monitoring, disease tracking and sports medicine applications. Strategically placed wireless sensors with associated interfaces consistently monitor the patient's health parameters by continuously measuring and processing the electrocardiogram (ECG), electroencephalogram (EEG) and blood pressure, etc. Remote monitoring of ECG and other vital physiological signals continuously is becoming increasingly important as it can significantly reduce the costs and risks involved in personal healthcare. The ECG monitoring is a vital area of WBAN application attributed to the increasing number of cardiac patients especially among the aged. Cardiotocography is another important area of ECG application in which the fetal heart rate is calculated from the fetal ECG. The important signal that is decisive in determining the health of the heart is the QRS complex. The separation of QRS complex from the raw ECG is the first step in the ECG processing because the shape and occurrence time of the QRS complex decides the heart rate and the health of the heart.

The major power consuming part of these wearable bio-medical devices are the digital filters built into the circuit for signal processing purpose. The digital filters are generally categorized into two groups as Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) filters. Because of the advantages like phase-linearity, low coefficient sensitivity and bounded input bounded output stability, etc., the FIR filters are preferred over IIR filters in many applications. They are inherently stable and free of limit cycle oscillations caused by using finite wordlength. They can be easily designed to be linear phase and hence achieve constant group delay, which helps in preserving the integrity of the information-carrying signals and is crucial

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in communication signals [1]. However, FIR filters suffer from a major disadvantage as they require a higher-order to achieve narrow transition bands as compared to IIR filters. Since the order of an FIR filter is inversely proportional to the transition bandwidth, any decrease in bandwidth increases the length of FIR filter significantly [2]. The hardware complexity of the FIR filters can be reduced to a certain extent by using the Frequency Response Masking (FRM) approach [3–5]. The FRM approach produces FIR filters with sparse coefficients, which gives lower hardware complexity.

The major arithmetic block in digital FIR filters is the Multiply and Accumulate (MAC) unit. The multiplier unit decides the speed, area and power dissipation of the MAC unit and in turn of the filter module. High speed exact multipliers such as Wallace, Booth, and Baugh Wooley multipliers have been widely used but they have reached saturation in terms of area and power optimization. The replacement of an exact multiplier with an approximate multiplier is a possible alternative for reducing power consumption in error resilient signal processing applications. Several approximate multipliers have been proposed in the literature [6–10]. Approximate Multipliers reduces area, power, and delay at the cost of computational error. By sacrificing some accuracy, the error-tolerant multiplier circuits can attain a large reduction in both the power consumption and area. Also, they may generate satisfactory results rather than accurate results sufficient to meet the specifications.

This paper proposes an area and power efficient approximate signed integer multiplier architecture. A FIR bandpass filter is developed using the FRM technique. The computationally intensive MAC operation of FIR filtering is performed using the proposed approximate multiplier. The bandpass filter is then used to demonstrate the efficacy of the approximate multiplier in applications like ECG signal processing. The approximate multiplier architecture is modeled using Verilog HDL. The circuit characterization is done by evaluation of the area, power, and delay performance of the circuit. The error characterization of the proposed design is performed using standard error characterization techniques and compared with other similar approximate designs. The performance of the FRM-FIR approximate bandpass filter in QRS detection is evaluated by estimating the sensitivity, positive predictivity, and detection error rate of the QRS detection method.

The rest of the paper is organized as follows. The approximate signed multiplier architecture is described in Sect. 2. The error and circuit characteristics of the proposed multiplier are presented in Sect. 3. Section 4 gives a brief description of the FIR bandpass filter design using FRM technique. Section 5 describes the application of FRM-FIR bandpass filter using approximate multiplier in extracting the QRS complex from the raw ECG data collected from MIT/BIH Arrhythmia Database. Finally, the conclusions are presented in Sect. 6.

## 2. Proposed approximate multiplier

The power consumption of digital CMOS-VLSI circuits can be split into static power and dynamic power components, where the static power is primarily driven by leakage currents, which relates to the area and density of the chip, while the dynamic power is a function of the circuit's switching activity. Chandrakasan *et al* [11] showed that the data wordlength affects the design parameters like speed, area, and power in VLSI circuits. The dynamic power consumption in CMOS digital logic circuits is proportional to switching activity in logic gates and it can be reduced by reducing the precision of the multiplier. Truncation and wordlength reduction are the two major approaches in multiplier design that considerably reduces the amount of switching in the multiplication process [12, 13]. Wordlength reduction methods reduce the switching activity of CMOS circuits and thereby reduce the dynamic power consumption at the cost of reduced precision. The wordlength reduction technique offers better power- saving per reduced bit, but with reduced accuracy. By using appropriate correction logic, it is assumed that data word length reduction can offer good power reduction with acceptable accuracy. The data wordlength reduction can be applied to one or both the inputs of the multiplier and this greatly reduces the area and power consumption in the multiplier circuit. In this paper, a low power signed approximate multiplier architecture based on data wordlength reduction for ECG signal processing applications is proposed.

The basic block diagram of an approximate multiplier based on wordlength reduction can be represented by three sub-blocks as shown in figure 1. The first sub-block is the wordlength reduction logic which reduces the input operand wordlength. Second sub-block is an arithmetic unit which is an exact multiplier block of appropriate wordlength to match with the output of the wordlength reduction logic and the last sub-block is a correction logic block to compensate for the reduction of input operand wordlength. A simple wordlength reduction logic is derived and implemented using the right shifting method. In the proposed approximate multiplier, the wordlength of the N-bit input operands are reduced to N/2-bits and multiplication is done with an N/2-bit multiplier instead of N-bit multiplier in the arithmetic unit. The correction logic

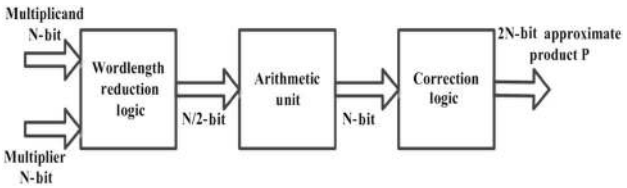


**Figure 1.** Block diagram of approximate multiplier.

expands the truncated product of N-bit wordlength to an approximate 2N-bit product.

The proposed multiplier is a signed approximate multiplier capable of performing signed multiplication. In order to process signed numbers, an additional sign-processing block must be added to the block diagram shown in figure 1. The detailed architecture of the proposed signed approximate multiplier is shown in figure 2.

The signed multiplier comprises of a sign-detect and two's complement block at the input, N/2-bit sign-extension encoder, inverter-based control logic, right barrel shifter, unsigned exact multiplier block of N/2-bit wordlength, left barrel shifter, and sign-set block at the output. The N/2-bit sign-extension encoder, inverter-based control logic, and right barrel shifter constitutes the wordlength reduction logic. The proposed wordlength reduction logic avoids the use of complex N-bit Leading-One-Detector (LOD), N-bit encoder and N-bit multiplexer as proposed in earlier designs such as DRUM multiplier [10]. The N/2-bit sign-extension encoder and a simple inverter-based control logic used for wordlength reduction in the proposed multiplier which gives more area and power savings than using an N-bit LOD, and N-bit encoder based circuit.

The signed multiplier receives the inputs in signed two's complement format. The sign-detect stage checks the sign of each of the input operand and if the sign bit is set, the two's complement block determines the absolute value of the negative operand. The N/2-bit sign-extension encoder receives the higher-order N/2-bit positive operands obtained from the sign-detect and two's complement block as the inputs. The sign-extension encoder calculates the effective size of the positive operands. A modified priority encoder is used for this purpose. The effective size of the positive operands is computed by finding the number of sign-extension bits (zeros) immediately to the right of the most-significant bit. For an N-bit multiplier, N/2 to $\log_2(N/2)$ priority encoder is required since the multiplier block is of N/2-bit wordlength. An 8:3 sign-extension encoder is required for a 16-bit multiplier. The truth table and Boolean expression of an 8:3 sign-extension encoder for a 16-bit signed approximate multiplier is shown in figure 3. The higher-order N/2-bits obtained from sign-detect and two's complement block are designated as $D_7D_6D_5D_4D_3D_2D_1D_0$ and the encoded outputs are denoted as $Q_2$, $Q_1$ and $Q_0$ in the truth table in figure 3. The encoded output is passed to the control logic block, which is used to calculate the amount of shift needed to reduce the wordlength of the inputs. The control logic derives the shift amount by concatenating a **'0'** with the inverted output of the sign-extension encoder. If the size of the input operand is below N/2-bits, then shift operation need not be performed and input operands are not truncated. In case of operand wordlength above N/2-bits, the right barrel shifter right shifts the input operands to the required number of places as decided by the control logic to obtain the N/2-bit input operand. Now the effective size of the input operands are limited to wordlength of size N/2-bit instead of N-bits and the multiplication is performed as an N/2×N/2-bit multiplication and truncated product of N-bits is obtained. Unsigned exact Wallace-Tree multiplier is adopted for the multiplier block in the arithmetic unit. To compensate for the N/2-bit truncated multiplication, the correction logic is used. The correction logic is a left barrel shifter which left shifts the truncated product of N-bits as many times as the number of bits which were truncated

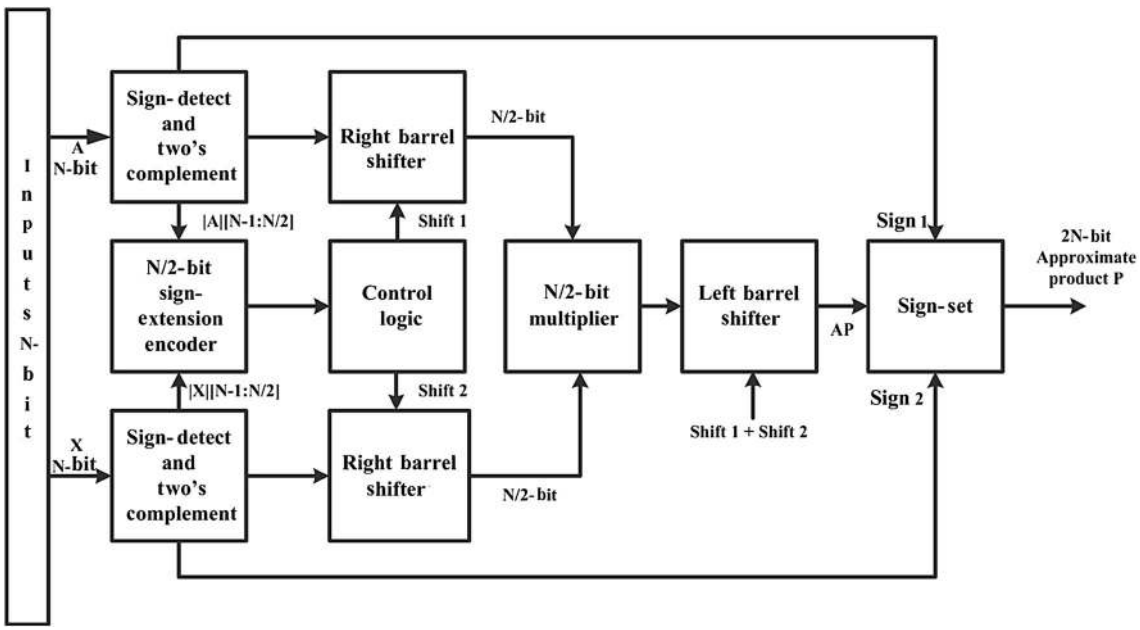


**Figure 2.** Signed Approximate Multiplier Architecture.

| Inputs | | | | | | | | Outputs | | |
|---|---|---|---|---|---|---|---|---|---|---|
| $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | $Q_2$ | $Q_1$ | $Q_0$ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | X | 1 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 1 | X | X | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | X | X | X | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | X | X | X | X | 0 | 1 | 0 |
| 0 | 0 | 1 | X | X | X | X | X | 0 | 0 | 1 |
| 0 | 1 | X | X | X | X | X | X | 0 | 0 | 0 |

X: Don't care

$Q_0 = \overline{D_7}.\overline{D_6}.D_5 + \overline{D_7}.\overline{D_6}.\overline{D_4}.D_3 + \overline{D_7}.\overline{D_6}.\overline{D_4}.\overline{D_2}.\overline{D_0} + \overline{D_4}.\overline{D_2}.D_1$

$Q_1 = \overline{D_7}.\overline{D_6}.\overline{D_5}.(D_3 + D_4 + \overline{D_2}.\overline{D_1})$ and $Q_2 = \overline{D_7}.\overline{D_6}.\overline{D_5}.\overline{D_4}.\overline{D_3}$

**Figure 3.** The truth table and Boolean expression of 8:3 Sign-Extension Encoder.

from both the input operands and 2N-bit approximate product (AP) is obtained. Depending on the sign of the input operands, the unsigned approximate product (AP) is negated in the sign-set block to obtain the final signed approximate product (P) as the output.

## 3. Simulation set-up and result analysis

This section gives an overview of the simulation set-up and the measurement approach used in the evaluation of error characteristics and circuit characteristics for approximate multipliers. In order to evaluate the error performance of the proposed multiplier, the proposed multiplier, and other approximate multipliers namely the Signed RoBA (S-RoBA) and Approximate Signed RoBA (AS-RoBA) multipliers are simulated in MATLAB.

Two sets of hundred thousand random numbers are generated with uniform probability as the inputs and the error metrics are calculated. To evaluate the circuit characteristics, all the 16-bit multiplier architectures are modeled using Verilog HDL and implemented in Cadence using generic PDK (gPDK) 90-nm CMOS technology with typical library settings. The functionality of the multipliers are verified using Cadence NCSIM and all the designs are synthesized using Cadence RTL compiler in 90-nm technology with proper timing constraints. The synthesized gate-level netlist is used to generate the layout using Cadence SoC Encounter tool.

### 3.1 *Error characteristics*

A detailed error analysis is done in MATLAB to compare the error performance of the proposed multiplier, with the existing approximate signed multipliers [6]. A comparison of the error metrics is given in table 1. The error metrics such as Normalized Mean Error Distance (NMED), the absolute value of Mean Relative Error Distance (MRED) and percentage mean accuracy are used to evaluate the performance of approximate multipliers. The definitions of the various error metrics are given as follows [14, 15]:

1. Error distance (ED): ED is the absolute difference between the accurate product (M) and the approximated product (M′).

**Table 1.** Arithmetic accuracy comparison of proposed 16-bit multiplier with other approximate multipliers.

| Signed designs | NMED (%) | MRED (%) | Mean accuracy (%) |
|---|---|---|---|
| Proposed signed multiplier | 0.032 | 0.52 | 99.48 |
| S-RoBA [6] | 0.172 | 2.88 | 97.12 |
| AS-RoBA [6] | 0.173 | 2.89 | 97.11 |

$$ED = |M - M'| \quad (1)$$

2. Mean error distance (MED): It is computed by taking the average value of all possible EDs

$$MED = \frac{1}{N}\sum_{i=0}^{N} ED_i \quad (2)$$

where, N is the total number of samples, and $ED_i$ is the error distance in the $i^{th}$ value.

3. Normalized mean error distance (NMED): It is the normalization of the mean error distance by the maximum output of the accurate multiplier.

$$NMED = MED/M_{max} \quad (3)$$

where $M_{max}$ is the maximum accurate product.

4. Mean relative error distance (MRED): MRED is computed as the average value of all possible relative error distances and is defined as:

$$MRED = \frac{1}{N}\sum_{i=0}^{N} ED_i/M_i \quad (4)$$

where $ED_i$ and $M_i$ are the error distances and the accurate output of the $i^{th}$ input.

5. Mean accuracy: It is defined as:

$$\text{Mean Accuracy}\,(\%) = 100 - \text{MRED}\,(\%) \quad (5)$$

The results tabulated in table 1 show that the proposed design of the approximate multiplier gives better error performance than the S-RoBA and AS-RoBA designs.

### 3.2 *Circuit characteristics*

To evaluate the circuit characteristics, the approximate multipliers as well as exact multiplier are implemented in Verilog HDL and synthesized using Cadence RTL Compiler in generic Process Design Kit (gPDK) 90-nm standard cell library at the typical process corner, with a supply voltage of 1V. The clock period is set at 11 ns. The circuit characteristics of the proposed signed multiplier are compared against Baugh-Wooley multiplier (Exact signed) architecture and a certain state-of-the-art approximate signed multiplier architectures. The post-synthesis circuit characteristics such as power, area and delay of all the multipliers are measured with respect to the maximum achievable frequency of the exact multiplier as reference, and tabulated in table 2. Since leakage currents are also contributing to the total power, the better parameter for characterizing circuit performance is Energy or Power-Delay Product (PDP), hence PDP also computed and tabulated in table 2 for performance comparison. Table 2 illustrates the synthesis results of an exact multiplier, proposed multiplier, and other approximate designs in terms of power, delay, area, and power-delay product.

The results in table 2 show that the proposed signed multiplier has smaller values of area and power consumption than exact and existing signed approximate multipliers, due to hardware efficient wordlength reduction logic employed, thereby their PDPs are also small. The proposed 16-bit signed multiplier consumes 46% less power than exact signed Baugh-Wooley multiplier. The PDP or Energy, and area of the proposed multiplier are about 37% (22%) and 40% (29%), respectively, lower than those of Baugh Wooley (S- RoBA) architectures.

## 4. Design of FIR bandpass filter using FRM approach

The hardware complexity of the FIR filters can be drastically reduced by using the FRM method to design the FIR filters. The FRM technique [3, 16–18] is suitable for designing digital filters with sharp transition bands. The sharp transition bandwidth is achieved by the use of a combination of wide transition band filters generally called model filters and masking filters. The model filter is upsampled to generate the periodic model filters which compress the frequency response of the filter to form the desired frequency band with sharp transition band as a result of upsampling. Also, there are extra frequency components, called images in the spectrum due to the upsampling. Cascading of the model filter with masking filters removes these spectral images. The cascading of periodic filters with non-periodic filters to obtain sharp transition bands is called the technique of FRM, proposed in [3]. The general FRM structure allows the implementation of arbitrary-bandpass FIR filters with less hardware

**Table 2.** Circuit characteristics of exact and approximate multipliers.

| Signed designs | Power (μW) | Delay (ns) | PDP (pJ) | Area ($\mu m^2$) |
|---|---|---|---|---|
| Proposed signed approximate multiplier | 414.02 | 5.34 | 2.21 | 4012 |
| S-RoBA [6] | 541.17 | 5.24 | 2.83 | 5640 |
| AS-RoBA [6] | 537.40 | 5.15 | 2.76 | 5210 |
| Exact signed multiplier | 769.07 | 4.56 | 3.51 | 6679 |

complexity since many of the filter coefficients are zero. It utilizes a model filter, G(z) and masking filters $F_0(z)$ and $F_1(z)$. The periodic model filters $G(z^L)$ are generated from G(z) by upsampling by a factor L. Also the complement of the periodic model filter is given by

$$G_C(z^L) = z^{-K} - G(z^L) \quad (6)$$

where K= (N−1)/2, N is the length of the filter $G(z^L)$

The transfer function of the FIR filter thus designed is,

$$H(z) = G(z^L)F_0(z) + G_C(z^L)F_1(z) \quad (7)$$

where G(z) is termed the model filter and $G(z^L)$ the periodic model filter. One or several pass-bands of the periodic model filters are extracted by the two masking filters, $F_0$ (z) and $F_1$ (z). The structure of FRM technique is shown in figure 4.

In the proposed FIR bandpass filter design using FRM approach, both the model and masking filters are derived from low pass model filter G(z). This restricts the number of filter coefficients to the coefficients of G(z). The model filter is G(z) and the interpolator filters $G(z^2)$, $G(z^4)$, $G(z^8)$, $G(z^{16})$ and $G(z^{32})$ are the periodic model filters used in the current design. The basic idea is that the prototype model filter G(z) is interpolated by different values i.e., 2, 4, 8, 16 and 32 and by cascading these interpolated sub-filters with G(z) or $G_C(z)$ may generate the required bandpass filters. The different combination of model and masking filters are listed in table 3, where G(z) and $G_C(z)$ taken as the masking filters.

The prototype filter G(z) is designed using the least square method. The normalized transition bandwidth of the prototype G(z) is fixed as 0.2 and stop band attenuation of 60 dB. The frequency response of the prototype model filter G(z) is shown in figure 5. The required bandpass filter can be generated by combining the appropriate pair of sub-filters given in table 3. As an illustrative example, let us consider the sub-filters $P_2$ and $P_4$. They may be combined to generate a bandpass filter with transfer function H (z) which is given by the following Eq. (8)

$$H(z) = G(z^4)G(z^2)G(z) - G(z^{16})G(z^8)G(z^4)G(z^2)G(z) \quad (8)$$

The frequency responses of the sub-filters $P_2$, $P_4$, and that of the bandpass filter thus designed are shown in figure 6.

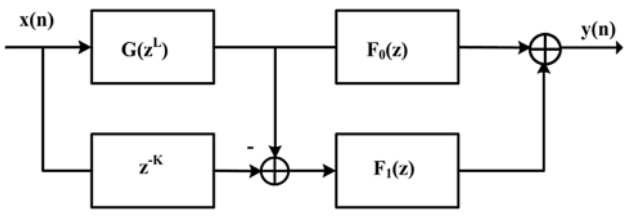


**Figure 4.** Basic structure of FRM technique.

**Table 3.** Transfer function of different sub-filters.

| Sub-filter | Transfer function |
|---|---|
| $P_1(z)$ | $G(z^{32})G(z^{16})G(z^8)G(z^4)G(z^2)G(z)$ |
| $P_2(z)$ | $G(z^{16})G(z^8)G(z^4)G(z^2)G(z)$ |
| $P_3(z)$ | $G(z^8)G(z^4)G(z^2)G(z)$ |
| $P_4(z)$ | $G(z^4)G(z^2)G(z)$ |
| $P_5(z)$ | $G(z^2)G(z)$ |
| $P_6(z)$ | $G(z)$ |
| $P_7(z)$ | $G_C(z)$ |
| $P_8(z)$ | $G(z^2)\ G_C(z)$ |
| $P_9(z)$ | $G(z^4)G(z^2)G_C(z)$ |
| $P_{10}(z)$ | $G(z^8)G(z^4)G(z^2)G_C(z)$ |
| $P_{11}(z)$ | $G(z^{16})G(z^8)G(z^4)G(z^2)G_C(z)$ |
| $P_{12}(z)$ | $G(z^{32})G(z^{16})G(z^8)G(z^4)G(z^2)G_C(z)$ |

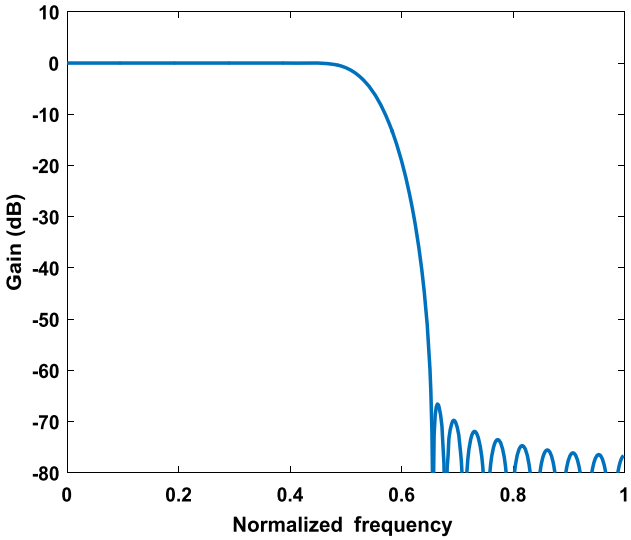


**Figure 5.** Frequency response of G(z).

## 5. Performance Evaluation of Approximate Multiplier in ECG Signal Processing

In real-time ECG measurements, the ECG signal gets corrupted by various disturbances such as base line wander noise, electrode contact noise, motion artifacts caused by changes in skin electrode impedance, instrumentation noise due to radio frequency interference from other equipment, electromyography (EMG) noise, and 50 or 60 Hz power line interference. Therefore, almost all QRS detection algorithms use a filter stage before the actual detection in order to attenuate unwanted signal components and artifacts, such as P-wave, T-wave, baseline drift, and in coupling noise. Experimental results show that a bandpass filter with a pass band of 8-20 Hz optimizes the QRS detection [19, 20]. Another study suggests a preferable center frequency for the pass band as 17 Hz [21].

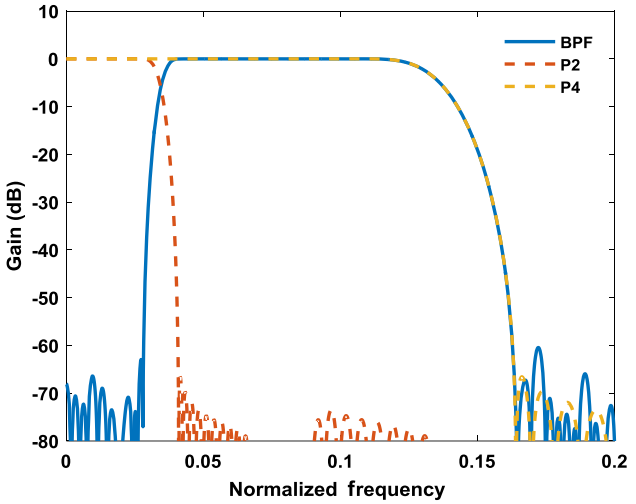


**Figure 6.** Illustration of the FRM technique for the generation of the bandpass filter (BPF).

The Pan Tompkins algorithm [22] is the most widely used QRS detection algorithm for the extraction of QRS complex from ECG waveforms. In the first step of the algorithm, the signal is passed through a digital bandpass filter (or a cascade of low-pass and high-pass filters) to attenuate the noise. The filtered signal is differentiated to get the QRS complex slope information. This step is followed by squaring to make the entire data points positive and emphasizing the ECG frequencies. In the final step, moving window integration is performed to obtain the waveform feature information that contains the slope and width of QRS complex. Now, peak detection algorithms may be applied to the QRS data for marking locations of the QRS pulses and pulse intervals for calculating the heartbeat rate. The separation of QRS complex from ECG data using Pan Tompkins algorithm is illustrated in figure 7.

In the proposed system, the low-pass and high-pass filter stages of the Pan Tompkins algorithm are replaced by the FRM approach based bandpass filter with a center frequency of nearly 15 Hz with a 3 dB bandwidth of nearly 17 Hz to maximize the QRS complex filtering. The frequency response of the FRM-FIR bandpass filter using approximate multiplier is illustrated in figure 8.

In order to validate the efficacy of the approximate multiplier in real time signal processing applications, the Pan Tompkins QRS Detection algorithm is implemented. The algorithm suggested in [23, 24] is used for finding the location of the QRS complex. The output signals corresponding to various steps of the Pan Tompkins algorithm for ECG record number 105 is demonstrated in figures 9i(a)–9i(e), using exact multiplier and figures 9ii(a)–9ii(e) using approximate multiplier methods. Normalized amplitude scales were used for easy visualization. The bandpass filtering is done with approximate multiplier and

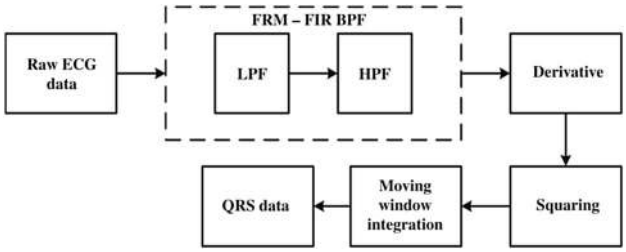


**Figure 7.** Steps involved in Pan Tompkins algorithm.

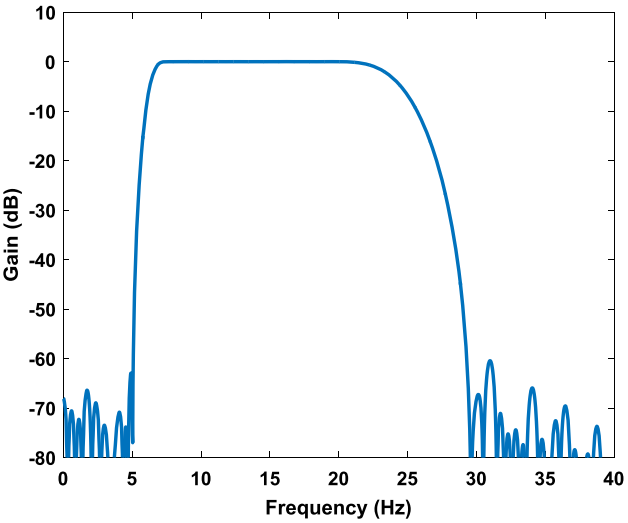


**Figure 8.** Frequency response of proposed FRM bandpass filter.

the rest of the steps in Pan Tompkins algorithm involved follow exact computing.

## 5.1 *Performance evaluation*

The QRS detection algorithm presented uses an FRM bandpass filter and a squaring stage to improve the signal-to-noise ratio for an adaptive threshold decision stage. The performance of the FRM band pass filter implemented using approximate multiplier is evaluated using real ECG records from MIT-BIH Arrhythmia Database [25] to extract the QRS complex. The database contains half an hour recordings from two channels of ECG data with sampling frequency of 360 Hz. In order to quantify the efficacy of the approximate method, the sensitivity (Se), positive predictivity (+P), and Detection Error Rate (DER) of the proposed method are calculated and tabulated in table 4. The performance indices are defined as follows:

$$\mathrm{Se}(\%) = \mathrm{TP}/(\mathrm{TP} + \mathrm{FN})\ \% \tag{9}$$

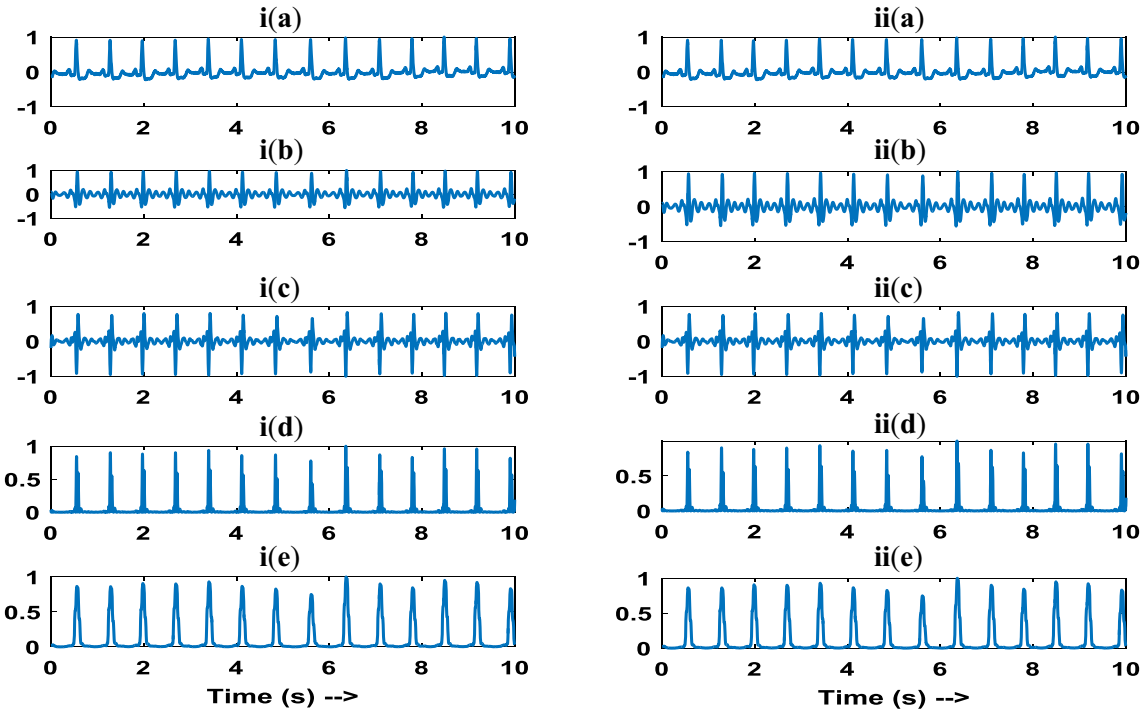


**Figure 9.** (i) Various steps of QRS Detection Pan Tompkins algorithm for ECG record 105 using exact multiplier (**a**) Original ECG signal, (**b**) Output of FRM-FIR BPF, (**c**) Output of differentiator, (**d**) Output of squarer, (**e**) Output of moving window integration. (ii) Same steps followed as in (i), but with using approximate multiplier.

**Table 4.** Experimental results of the proposed method using the MIT/BIH Arrhythmia Database.

| Record no. | Total beats | TP | FP | FN | Se (%) | +P (%) | DER(%) |
|---|---|---|---|---|---|---|---|
| 100 | 2273 | 2273 | 0 | 0 | 100 | 100 | 0 |
| 101 | 1865 | 1865 | 4 | 0 | 100 | 99.78 | 0.21 |
| 102 | 2187 | 2187 | 0 | 0 | 100 | 100 | 0 |
| 103 | 2084 | 2083 | 0 | 1 | 99.95 | 100 | 0.05 |
| 104 | 2229 | 2227 | 26 | 2 | 99.91 | 98.84 | 1.25 |
| 105 | 2572 | 2569 | 30 | 3 | 99.88 | 98.84 | 1.28 |
| 106 | 2027 | 2015 | 3 | 12 | 99.41 | 99.85 | 0.74 |
| 107 | 2137 | 2135 | 0 | 2 | 99.90 | 100 | 0.09 |
| 108 | 1763 | 1758 | 11 | 5 | 99.71 | 99.37 | 0.91 |
| 109 | 2532 | 2526 | 1 | 6 | 99.76 | 99.96 | 0.28 |
| 111 | 2124 | 2123 | 0 | 1 | 99.95 | 100 | 0.05 |
| 112 | 2539 | 2539 | 0 | 0 | 100 | 100 | 0 |
| 113 | 1795 | 1795 | 0 | 0 | 100 | 100 | 0 |
| 114 | 1879 | 1876 | 1 | 3 | 99.84 | 99.95 | 0.21 |
| 115 | 1953 | 1953 | 0 | 0 | 100 | 100 | 0 |
| 116 | 2412 | 2391 | 1 | 21 | 99.12 | 99.95 | 0.91 |
| 117 | 1535 | 1535 | 0 | 0 | 100 | 100 | 0 |
| 118 | 2278 | 2278 | 1 | 0 | 100 | 99.96 | 0.04 |
| 119 | 1987 | 1987 | 0 | 0 | 100 | 100 | 0 |
| 121 | 1863 | 1862 | 0 | 1 | 99.94 | 100 | 0.05 |
| 122 | 2476 | 2476 | 0 | 0 | 100 | 100 | 0 |
| 123 | 1518 | 1515 | 0 | 3 | 99.80 | 100 | 0.19 |
| 124 | 1619 | 1611 | 0 | 8 | 99.50 | 100 | 0.49 |
| **Total** | **47647** | **47579** | **78** | **68** | **99.85** | **99.83** | **0.31** |

**Table 5.** Performance comparison of the proposed method with other detectors for noisy MIT-BIH record 105.

| Method | FP | FN | Failed Detection (FP+FN) | DER (%) | Reference |
|---|---|---|---|---|---|
| Proposed Method | 30 | 3 | 33 | 1.28 | |
| Hilbert Transform | 6 | 3 | 9 | 0.35 | [19] |
| PT-Band Pass Filtering | 67 | 22 | 89 | 3.46 | [22] |
| Wavelet Transform | 15 | 13 | 28 | 1.09 | [26] |
| S-Transform | 10 | 22 | 32 | 1.24 | [27] |
| Level Crossing | 41 | 63 | 104 | 4.04 | [28] |
| Uniform Filter Banks* | 53 | 16 | 69 | 3.22 | [29] |
| Non-Uniform Filter Bank* | 16 | 13 | 29 | 1.36 | [30] |

*This result reported over 2139 beats only.

$$+\mathrm{P}(\%) = \mathrm{TP}/(\mathrm{TP}+\mathrm{FP})\ \% \quad (10)$$

$$\mathrm{DER}(\%) = \mathrm{FP}+\mathrm{FN}/\mathrm{Total\ number\ of\ beats}\ \% \quad (11)$$

where TP is the true positive, FN is the false negative and FP is the false positive. True positive is the total number of QRS complex correctly located by the detector, false positive (FP) denotes the false beat detection, and a false negative occurs when the algorithm fails to detect a true beat mentioned in the annotation file of MIT-BIH record.

The QRS detector based on the proposed approximate method produces a total of 68 FNs, and 78 FPs out of 47647 beats. The overall sensitivity, positive predictivity, and detection error rate are 99.85%, 99.83%, and 0.31%, respectively. The individual ECG record detection sensitivity varies from 99.12% to 100%, and positive predictivity varies from 98.84% to 100%. The sensitivity and predictivity of the algorithm is nearly 100% for records with less noise and practically detects all the QRS complexes present in those records. But in few of the noisy records like record number 104, 105, etc., the DER has slightly larger value like any other detection algorithm. Record number 104 is characterized by the occurrence of several bursts of muscle noise, and in record number 105, both the channels contain high-grade noise and artifacts. Table 5 gives the performance comparison of the proposed method with other QRS detectors for the noisy MIT-BIH record number 105, which contains 2572 QRS beats.

The QRS complex detection depends primarily on the performance of the filtering stage and the decision stage. Most of the QRS detection algorithms use appropriate filters to remove the baseline wander, power line interference, electromyography noise and motion artifacts. The wavelet transform, S-transform and the Hilbert transform methods uses transform domain techniques and hence expected to show better accuracy in the decision stage. The performance of other QRS detection algorithms mainly depends on the decision as to whether a pulse corresponds to an R-peak and is performed with a thresholding operation with adaptive techniques or other decision methods. The performance results obtained for the proposed approximate system is comparable with all other QRS detection algorithms with detection error well within the acceptable limits.

The purpose of this study is to show that QRS complex detection can be performed with approximate filters that are computationally efficient and offer a low power solution for applications in wearable and implantable bio-medical devices. The advantage of FRM-based FIR filter for detecting QRS complex is to reduce the overall filter complexity in hardware and gives significant power and area savings in comparison with a traditional FIR filter implementation. The FRM-FIR filter implementation using approximate multiplier gives additional power savings in comparison with an exact multiplier implementation. The proposed system offers high sensitivity, positive predictivity, and lower false detection even in the presence of significant noise and motion artifacts.

The FIR filters using the approximate method are a good option for bio-medical signal processing applications in personalized low power health care devices in the future.

## 6. Conclusions

In this paper, an area and power efficient approximate multiplier architecture is proposed. The proposed signed multiplier requires low area and power compared with exact and other approximate multiplier designs. The accuracy of computing is also evaluated and shows better performance compared to similar designs. By adopting frequency response masking approach, a FIR bandpass filter is developed using an approximate multiplier to extract the QRS complex from the raw ECG signal. The performance of the approximate multiplier in QRS filtering has been evaluated using the MIT-BIH Arrhythmia Database. The comparable performance of the approximate arithmetic in QRS detection with that of exact methods shows the efficacy of the proposed multiplier in applications like low power wearable or implantable intelligent bio-medical sensors which can do real time health monitoring and able to ensure connectivity with health care networks. The approximate arithmetic architectures designed using the

proposed multiplier architecture are strong contenders for error tolerant low power bio-medical applications where low power and reconfigurability are mandated.

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