Zhiyu Ru

Frequency Translation Techniques for Interference-Robust Software-Defined Radio Receivers

Frequency Translation Techniques for Interference-Robust Software-Defined Radio Receivers

Zhiyu Ru

Invitation

On Thursday,
November 12th 2009
at 16:45
in Collegezaal 2
of the Spiegel building,
I will be defending
my thesis.

Frequency Translation Techniques for Interference-Robust Software-Defined Radio Receivers

At 16:30,
I will give
a short introduction
to my thesis.

You are most welcome
to attend
the introduction,
the defense,
and the reception
afterwards.

Zhiyu Ru

FREQUENCY TRANSLATION TECHNIQUES FOR INTERFERENCE-ROBUST SOFTWARE-DEFINED RADIO RECEIVERS

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Author: Zhiyu Ru
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FREQUENCY TRANSLATION TECHNIQUES FOR INTERFERENCE-ROBUST SOFTWARE-DEFINED RADIO RECEIVERS

DISSERTATION

to obtain
the degree of doctor at the University of Twente,
on the authority of the rector magnificus,
prof.dr. H. Brinksma,
on account of the decision of the graduation committee,
to be publicly defended
on Thursday 12 November 2009 at 16:45

by

Zhiyu Ru

born on 8 February 1981
in Nanjing, China

This dissertation is approved by

the promotor,
prof.dr.ir. Bram Nauta

and the assistant promotor,
dr.ing. Eric A. M. Klumperink

Thank you

Committee:

Chairman:		
	prof.dr.ir. J.H.A. de Smit	Universiteit Twente
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	prof.dr.ir. A.J. Mouthaan	Universiteit Twente
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Abstract

There has been a growing demand for wireless communications and diverse communication standards have been developed over time, e.g. GSM, Bluetooth, Wi-Fi, etc. For convenience of use, people desire a universal radio to be able to communicate anywhere using any standard. A software-defined radio (SDR) which aims at greater programmability can meet such a demand. However, there are a number of technical challenges to make a SDR receiver practical.

This thesis focuses on frequency translation (FT) techniques and addresses two key SDR challenges: the robustness to out-of-band interference (OBI) and the compatibility with CMOS scaling and system-on-chip (SoC) integration. The thesis studies the principles and the performance limitations of existing FT techniques and proposes new circuit-and-system techniques to improve SDR receivers.

Fundamental differences between various FT techniques are highlighted by means of a classification and comparison of mixing and sampling. This leads to the definition of a new discrete-time (DT) mixing technique. The suitability of RF-mixing and RF-sampling receivers to SDR is evaluated. RF sampling seems to be more compatible with CMOS scaling and SoC integration. However, existing RF-sampling techniques are narrowband and are not directly suitable for a wideband SDR receiver.

To address this issue, a DT-mixing technique is proposed which performs a mixing operation in the DT domain after RF sampling. It can make RF sampling more suitable to wideband SDR receivers because it has two properties: wideband phase shifting and wideband harmonic rejection (HR). DT mixing can be realized using de-multiplexing of samples. To verify the concept, a 200-to-900MHz DT-mixing downconverter with 8-times oversampling and 2^{nd}-to-6^{th} HR is implemented in 65nm CMOS. To construct a complete RF-sampling receiver, a tunable LC filter and a linearized low-noise amplifier (LNA) are applied as pre-stages of the DT-

mixing downconverter. The LC filter employs an external coil and on-chip switchable capacitors. The LNA employs cascaded inverter stages linearized via an enhanced voltage mirror. The RF-sampling receiver achieves a minimum NF as low as 0.8dB and improves HR by 30dB compared to the downconverter alone.

To be more robust to OBI, two FT techniques are proposed: one to improve the out-of-band linearity and the other to make the HR robust to mismatch. A low-pass blocker filtering technique is proposed to avoid voltage gain at radio frequencies (RF) but make voltage gain only at baseband simultaneously with low-pass filtering to attenuate OBI. The low voltage gain at RF is realized by means of a low "mix-impedance", which is analyzed quantitatively. A 2-stage polyphase HR technique is proposed to perform HR in cascaded stages to dramatically improve the amplitude accuracy. To also achieve the high phase accuracy, a simple and accurate frequency divider is presented. The effects of random amplitude and phase errors to HR are analyzed. To demonstrate these concepts, a 65nm CMOS receiver based on RF mixing shows +3.5dBm in-band IIP3 and +16dBm out-of-band IIP3. More than 60dB HR ratio is measured over 40 randomly-selected chips. The multiphase clock generator works up to 0.9GHz while the -3dB RF bandwidth is measured up to 6GHz.

Contents

Chapter 1

Introduction

Wireless communications rely on radio. Future wireless communications rely on software-defined radio (SDR), which makes radio more flexible. However, a low-cost practical SDR still stays as a concept so far. This thesis addresses the main challenges of realizing practical SDR receivers, focusing on the analog front-end.

Section 1.1 describes the motivation behind the trend towards SDR and the actual origins of the concept of software radio and software-defined radio. From the concept to a practical SDR, a few major challenges exist. Section 1.2 discusses these challenges and Section 1.3 reviews the up-to-date solutions. After that, Section 1.4 defines the objectives of this work. Then Section 1.5 gives an overview on the organization of this thesis. Section 1.6 provides the references of the chapter.

1.1 Software(-Defined) Radio: Motivation and Origins

Communication is essential for people, and the modern society heavily relies on it. Assisted by wireless technologies, people can communicate over long distances, flexibly at different places, and even while moving. Today, radio communication not just exists but it is everywhere and keeps growing. As a typical example, by 2008, the global mobile phone penetration rate was already more than 50% and it is predicted to reach 75% by 2011 [1].

In the mean time, different communication standards have been developed to serve various applications in our daily life. To give a couple of examples, in the spectrum of 400MHz to 6GHz (Fig. 1.1) which is typically used for mobile applications, we

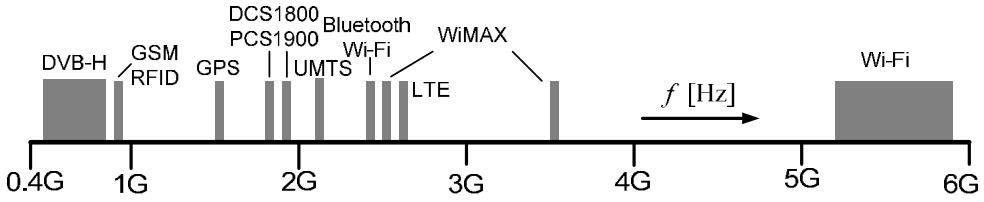

Figure 1.1 An example of spectrum allocation for mobile communications

have the cellular standards GSM, UMTS, and LTE, the wireless networking standards Wi-Fi and WiMAX, the mobile TV standard DVB-H, the navigation standard GPS, and the short-range communication standards Bluetooth and RFID, etc. The list is only getting longer as new standards are still emerging.

For convenience of use, it is a natural step to combine as many applications as possible into a single mobile radio device, i.e. to add more functionality. Compared to the approach of adding separate radio hardware for every application, the use of flexible hardware controlled by software can make the device smaller, lighter, more flexible, and at lower cost. This trend of *radio evolution*, i.e. moving functionality into software for a *flexible* multi-function radio device, leads to the emerging of the term "software radio" (SWR), coined in the early 90's by Mitola [2] [3]. Similar trends can be seen in many other electronic systems.

With radio functions mainly implemented in software, SWR refers to a universal radio platform being able to cope with *current and future* communication standards only by running and upgrading different software. The goal of SWR is to make a radio as flexible as a computer: the software defines the application.

However, a SWR receiver has to first convert an analog radio signal into a digital representation before the signal can be handled by software. Consequently, an analog-to-digital converter (ADC) is indispensible. As shown in Fig. 1.2, an *ideal* SWR receiver [4] [5] moves the ADC towards the antenna, through an anti-aliasing filter. Such a radio concept can be very flexible because it minimizes the analog hardware and maximizes the usage of digital hardware which provides the platform to run software.

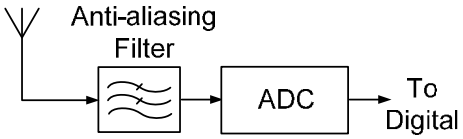

Figure 1.2 Ideal software-radio (SWR) receiver but impractical yet

The dominant technology for digital circuits is CMOS which stands for Complementary Metal-Oxide Semiconductor. Moreover, commercially it is attractive to achieve a high level of integration for a low cost, and the trend is clear: system-on-chip (SoC), with both analog and digital implemented on the same chip. Therefore, SWR hardware is preferably implemented in CMOS.

As mentioned, an ideal SWR receiver requires a high-performance ADC to directly digitize RF signal. However, without downconversion and filtering ahead, the required ADC performance such as speed and dynamic range is usually impractical in CMOS. For example, assuming at least 10GS/s speed and 16-bit resolution are required to receive RF signals up to 5GHz, and assuming 1pJ/conversion for the ADC lead to almost 1kW power consumption, if feasible at all [6].

While Mitola described the *ideal* SWR receiver has an ADC connected closely to antenna, he also suggested that a *practical* SWR receiver may have the ADC located at IF after frequency conversion [2]-[5].

Such a practical SWR is close to another term "software-defined radio" (SDR), which, according to Mitola [5, Section II-A], was defined by BellSouth [7] in 1995 "to describe an evolution towards greater programmability of a wireless infrastructure" [5].

The *implementation* of a SDR (can be but) does not have to be primarily in software like a SWR, but at least the *function* of a SDR can be defined, or reconfigured, by software for different communication standards, preferably also software-upgradable to deal with future standards. Please note that there is not necessarily to be a clear boundary between SDR and non-SDR; the more programmable the better. Today's industrial multi-band multi-mode radios can be seen as an intermediate step towards SDR.

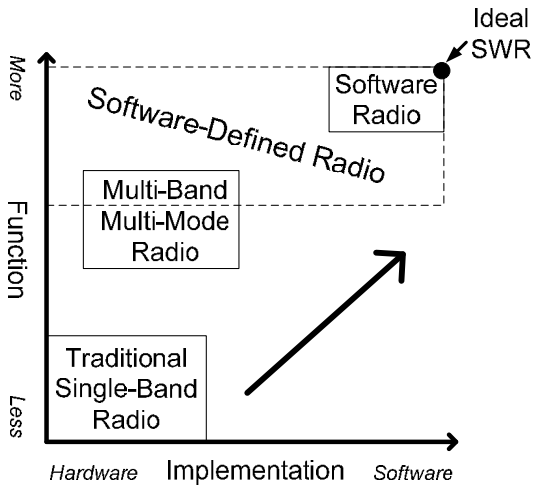

Figure 1.3 Conceived phase space of radio evolution towards greater programmability

Besides coping with multiple standards, SDR can also be an enabler for cognitive radio (CR) [8]. A CR can automatically adapt its parameters, such as carrier frequency, dynamic range, and power consumption, in response to the radio environment and user demands. The present cognitive radio application regulated by FCC [9] focuses on dynamic spectrum access in the unoccupied TV band below 1GHz, which is aimed to improve the efficiency of utilizing the scarce spectrum resources.

Till this end, we have presented the motivation of SWR and SDR as well as the actual origins of these two terms which were not always clear. However, the relationship between them can still be confusing and these two terms can be mixed up with each other. To further clarify the ambiguity between them as well as to clearly set our research scope, we summarize, in our view, their distinctions below.

Functionally, both are flexible radios but SWR also restricts the way of implementation to be primarily in software, i.e. *SWR = software-intensive SDR*. In our view, the scope of SDR is broader and includes SWR, while SWR represents the highest degree of flexibility in SDR. Our research targets at SDR, which is broader and more feasible for now.

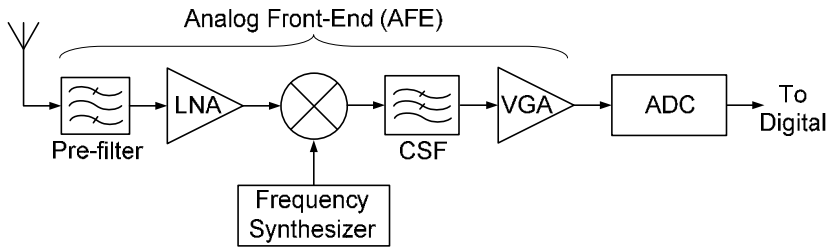

Figure 1.4 A typical block diagram of a traditional receiver

Fig. 1.3 represents, in our view, a conceived phase space of radio evolution towards greater programmability. It also indicates the scope of traditional radio, multi-band radio, SWR, and SDR, concerning the diversity of radio function and the way to implement radio function. Note that software has to run on hardware, but a SWR uses less hardware and more software, in percentage of the construction of a radio function, than traditional single-band radio and today's multi-band radio.

SDR is a wide research topic, which can range from analog to digital and from transmitter to receiver. As for SWR, the preferred technology for SDR is also CMOS, for the sake of SoC integration. For the feasibility of A/D conversion in CMOS, till this age we still need functions such as amplification, downconversion, and filtering in the analog front-end (AFE) of a radio receiver before A/D conversion.

This thesis focuses on the *analog front-end for SDR receivers* in CMOS, aiming at low power consumption to target mobile applications. There are several main challenges to realize such an AFE, which will be discussed in the next section.

1.2 Challenges

Fig. 1.4 shows the typical block diagram of a traditional receiver, which is often dedicated to one band for one standard. The analog front-end (AFE) consists of an RF band-selection filter (pre-filter), low-noise amplifier (LNA), mixer, baseband channel-selection filter (CSF), and variable-gain amplifier (VGA). The challenges we talk about here will be focused on the AFE, while the synthesizer and ADC are

outside the scope of this thesis. We may also want to receive more than one standard at the same time, which can be challenging too but not in the scope of this thesis.

The key difference of a SDR receiver compared to a traditional receiver is the enhanced flexibility, i.e. it is *functionally* more flexible. To turn a traditional radio receiver into a flexible SDR receiver, considering the two main purposes of SDR, i.e. multi-standard and cognitive radio applications, we face at least the following challenges in the AFE:

a) To deliver "good enough" NF and in-band linearity to satisfy each targeted standard in a *continuously*-covered wide frequency range;
b) To provide "good enough" linearity or selectivity tunable over a wide frequency range, against strong out-of-band interference;
c) To realize channel-selection filtering which can cover variable channel bandwidth, e.g. in small steps, with reconfigurable filter order;
d) To be compatible with CMOS scaling and SoC integration.

Generally, all the above goals should better be achieved with low cost, small size, and low power consumption for large-volume (consumer) mobile applications.

To clarify their meanings, we will discuss each point of the listed challenges.

Points a) and b)

Points a) and b) deal with NF and linearity, which are key performance to radio receivers, and for SDR receivers, the considerations for noise and linearity are quite different from traditional radios.

For a specific band of one standard, we may classify the received RF signal into three categories: *desired signal, in-band interference (IBI), and out-of-band interference (OBI)*. The desired signal is often a single channel in a band and IBI refers to signals in other channels than the desired in the same band while OBI refers to signals in any other bands. As an example, Fig. 1.5 shows a typical interference scenario for the GSM standard in the 900MHz band [11], indicating a

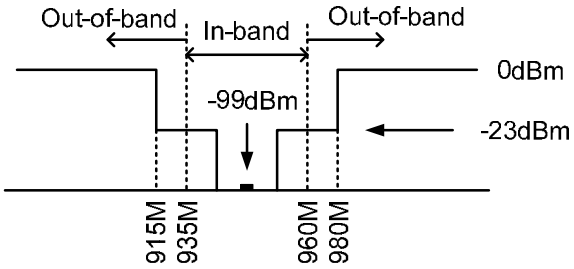

Figure 1.5 A typical blocking scenario for GSM 900MHz standard

weak desired signal at -99dBm (3dB above the sensitivity level), IBI as strong as -23dBm and OBI as strong as 0dBm.

First let's look at the *desired signal*.

For each standard, there is a sensitivity level to define the minimum available power of the desired signal received at antenna. For instance, the required sensitivity for GSM is -102dBm over a 200kHz channel while that number for DVB-H is -98dBm over a 5MHz channel. A traditional receiver should be able to provide good enough NF in a specific frequency band to satisfy the minimum signal-to-noise ratio (SNR) for successful demodulation when antenna signal is at the sensitivity level. Since a SDR receiver should cover multiple standards, it should be able to meet the required sensitivity for each *individual* standard in different bands. Furthermore, to accommodate future standards and for CR applications, it is preferred that SDR can cover a wide bandwidth *continuously*. As most mobile communication standards up to now use a band between 400MHz and 6GHz (Fig. 1.1), our focus will be on this frequency range. Typically, a $NF < 6dB$ should be "good enough" for most standards in this RF range [12].

Now let's look at *interference*.

Traditional wireless standards use dedicated radio bands, so that in-band interference (IBI) can be distinguished from out-of-band interference (OBI). For a SDR aiming at covering arbitrary frequencies, the definition of IBI and OBI may become fuzzy. Still, we will use the terms IBI and OBI in this thesis as: 1) current SDR receivers often aim at covering multiple traditional radio standards which

have clear band definitions; 2) even if this is not the case, e.g. for cognitive radios, a SDR still aims at implementing selectivity, i.e. receive a signal for which the baseband bandwidth is much smaller than the RF carrier frequency. In the latter case OBI can be interpreted as "out-of-baseband interference".

For mobile communications, the IBI can be as strong as -30 to -20dBm while the OBI can be as strong as -10 to 0dBm [13]. An RF pre-filter is often employed to suppress the OBI to no larger than the IBI level. Since a desired band is often a small ratio of its carrier frequency and strong interference can be close to the desired signal frequency, the RF pre-filters often require high quality factor (Q) and sharp roll-off. Such filters are difficult to integrate on chip and are typically dedicated to one specific band, e.g. SAW band filters. As the RF pre-filters often do not suppress the IBI, the linearity of the receiver should be good enough to tolerate IBI. A receiver *in-band IIP3 > -10dBm* would be "good enough" for most standards [12] [26]. As shown in Fig. 1.4, assisted by a *dedicated* RF pre-filter, a traditional receiver should be able to provide good enough linearity to counter the IBI and the suppressed OBI.

However, for SDR receivers, using a dedicated filter for each band would dramatically increase the size and cost. Therefore we prefer a *flexible* RF pre-filter, which can adjust its center frequency, bandwidth, and order for different standards. Such a filter can attenuate the OBI for each standard so that the required linearity of the SDR receiver is relaxed. However, to build such a filter at low cost is very challenging, since it usually requires multiple poles and zeros simultaneously tunable over a broadband, on top of the requirements of a traditional dedicated RF pre-filter such as high Q, sharp roll-off, and low insertion loss. Research on flexible RF pre-filters is actively ongoing, e.g. exploring the use of MEMS technology [14].

In this thesis, we look at solutions from the CMOS receiver perspective. In parallel to enhance the filter flexibility to relax the receiver linearity, we can also try to enhance the linearity of the receiver so that the requirements on the filter can be relaxed. After all, what matters is that the combined efforts from both sides, filter and receiver, meet the required system specification. Since pre-filters mainly suppress OBI, to relax those filters, the robustness of the SDR receiver to OBI is critical, while the required in-band linearity is similar to traditional receivers for each standard.

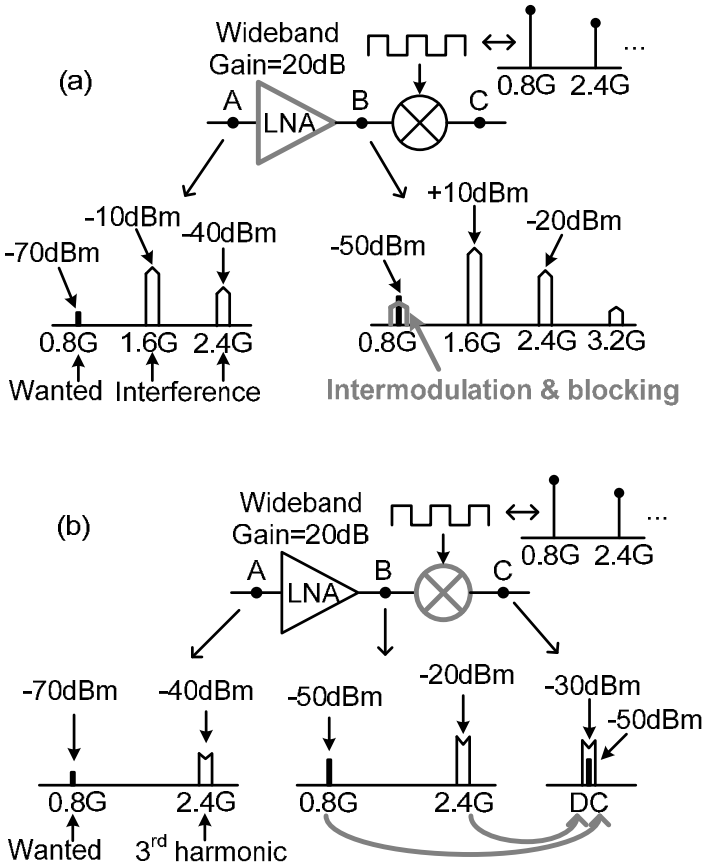

Figure 1.6 Wideband interfering mechanisms:
(a) out-of-band nonlinearity; (b) harmonic mixing

At least two mechanisms generate *in-band* distortion due to OBI: 1) nonlinearity related mixing of strong out-of-band interferers via, e.g., intermodulation or cross-modulation; 2) harmonic mixing of interferers with LO harmonics due to hard-switching mixers or the use of digital LO waveforms. To clarify, we will explain these two mechanisms briefly below.

1) *Out-of-band nonlinearity*: Nonlinearity may generate intermodulation and harmonic distortion falling on top of the desired signal, or may desensitize a receiver due to blockers and produce cross modulation [15]. Fig. 1.6 (a)

shows an example, where a wideband LNA amplifies the desired signal at 0.8GHz and the undesired wideband interference at 1.6GHz and 2.4GHz with an equal gain of 20dB[1]. At the output of the LNA, the amplified interference challenges the nonlinear output impedance of the LNA and the linearity of a next-stage mixer, which can severely degrade the signal-to-noise-and-distortion ratio. Without sufficient RF pre-filtering, the out-of-band linearity can become the bottleneck since OBI is much stronger than IBI. For example, if OBI is 20dB stronger than IBI, without any attenuation of OBI, the required out-of-band IIP3 can be derived as *30dB* higher than the required in-band IIP3, if aiming at that OBI generates the same distortion level as IBI.

2) *Harmonic mixing*: Linear time-variant behavior in a hard-switching mixer, or equivalently multiplication with a square wave, down-converts not only the desired signal but also interference around LO harmonics. Fig. 1.6 (b) shows an example, where both the desired signal at 0.8GHz and the interference at 2.4GHz pass through the wideband LNA with equal gain. Even if the LNA is perfectly linear, the interference may directly fall on top of the desired signal after the mixer via the 3rd-order harmonic mixing. A quick calculation shows that large rejection ratio is wanted: if we want to bring harmonic responses down to the noise floor (e.g. -100dBm in 10MHz for NF=4dB), and cope with interferers between -40 and 0dBm, a harmonic rejection ratio of 60 to 100dB is needed.

Both out-of-band nonlinearity and harmonic mixing can severely degrade signal-to-distortion ratio[2] which directly affects the demodulation of desired signal. Therefore, in our view, a SDR receiver is not just a wideband receiver with "good enough" NF and in-band linearity, but it should also have enhanced out-of-band linearity and harmonic rejection (HR).

[1] The gain might be lower for a clipping signal.
[2] Signal-to-Distortion Ratio is so important to software-defined radio that it can be viewed as another interpretation of "SDR".

Point c)

Channel selection is used to select the desired channel and so to reduce the required dynamic range for the ADC. It is often done at baseband where high selectivity can be achieved more easily than at RF. For a traditional receiver, a fixed baseband filter to meet one dedicated standard is good enough. But for a SDR receiver, the channel-selection filter should be able to vary its characteristics, e.g. bandwidth and order, to fit the requirements of different standards. For a true SDR receiver, the filter is expected to cover a range of channel bandwidth in a certain resolution, suitable for both current and future standards. Later we will see through a couple of examples that some promising solutions have been proposed for SDR channel-selection filters.

Point d)

The achievable system performance can directly depend on the adopted technology platform. For example, it might be easier for technologies such as superconductor or GaAs than CMOS to achieve wider bandwidth and higher dynamic range, which are key parameters to realize the AFE of a SDR receiver. However, as described in Section 1.1, we prefer to implement SDR in CMOS as an ideal technology platform for software, and integrate analog and digital systems on one chip. Unfortunately, CMOS downscaling mainly benefits digital circuits but can put extra-ordinary challenges for analog circuits [10]. Although SoC integration may bring the opportunity of digitally-assisted calibration for analog blocks, it is challenging to integrate analog with digital on the same chip due to, e.g., simultaneous switching noise generated from millions of digital gates. Therefore, it is challenging to make SDR compatible with CMOS scaling and suitable for SoC integration.

Now we may summarize the major challenges of the analog front-end (AFE) of a SDR receiver, compared to a traditional receiver, as:

SDR Receiver AFE = Wideband Receiver AFE +
Robustness to Out-of-band Interference +
Flexible Channel-Selection Filtering +
Compatibility with CMOS Scaling and SoC Integration.

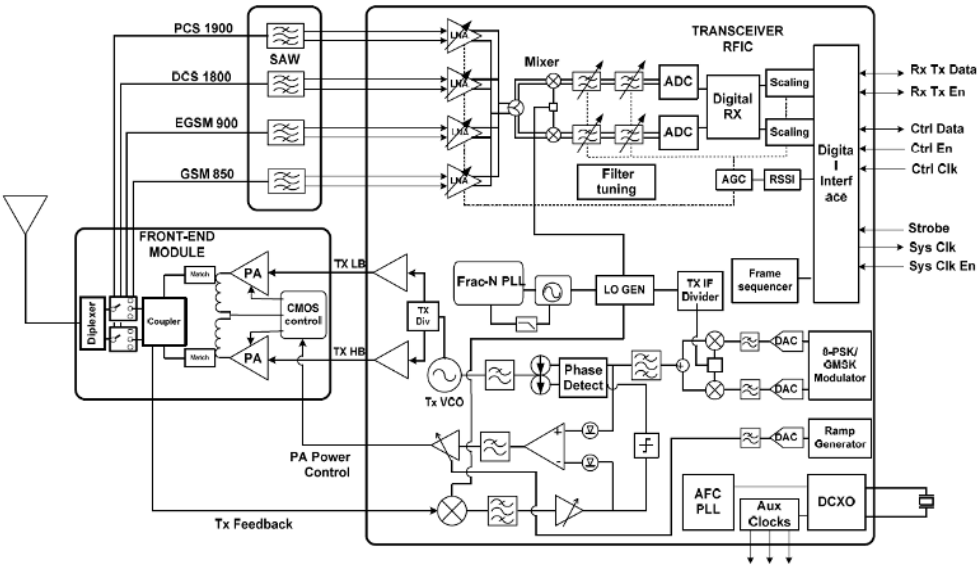

Figure 1.7 An integrated quad-band GPRS/EDGE transceiver [16]

1.3 State of the Art

This section presents state-of-the-art work[3] related to SDR receivers, as a brief literature overview. The aims are: a) to show how the challenges pointed out in the previous section have been addressed so far by other researchers; b) to show the differences and the added values of our work (Chapter 2 to 5) compared to others'.

A traditional multi-standard receiver basically puts multiple dedicated receivers in parallel with each for one band. It is effective now for product development aiming at a quick time to market and low risk. However, this approach significantly increases system size and cost for every band that is added, for both on-chip and off-chip components. It is becoming increasingly impractical as there are already a large number of radio communication standards, while new ones are continuously being developed.

[3] Please note that most work mentioned in this section is *not* "previous" work but developed in parallel to this Ph.D. project which got started in 2005. Of course, they are only valid to be "state-of-the-art" till 2009 when the thesis is written.

To be able to move towards SDR, it might make sense to re-think the way of designing radios. Instead of putting hardware radios in parallel for each band, we aim at sharing the same hardware for different bands. This trend of sharing hardware is evident from the multi-band multi-mode radio transceivers in today's industry, which can be considered as an intermediate step towards SDR (Fig. 1.3). A practical example is shown in Fig. 1.7 [16], which is a quad-band GSM transceiver. If we focus on the receiver side, the mixers and the baseband circuits are shared for all bands. However, in this particular example, all the targeted bands have a similar protocol (channel) bandwidth, around 200 kHz, which makes sharing the baseband hardware relatively easier. Furthermore, the LNAs and the off-chip band-filters are still dedicated for each band. The parallel LNA configuration actually can allow the freedom to select which band in use by enabling an LNA and avoid a lossy switch on the signal path. The off-chip components such as band-filters are a key bottleneck towards the SDR. Also these LNAs and band-filters cannot continuously cover a broadband.

To achieve the goal of SDR, we have recognized four major challenges in the previous section. Next we review some solutions in literature for each challenge.

1.3.1 Wideband Receivers

Relevant characteristics of a wideband receiver include the input reflection coefficient (S_{11}), gain, and NF versus frequency. A key enabling block is a wideband low-noise amplifier (LNA), which is usually the first block of a receiver chip and therefore can largely affect the S_{11}, gain, and NF of the whole receiver. For a wideband LNA, to simultaneously achieve good impedance matching, e.g. $S_{11} < -10$dB, and low noise, e.g. NF < 3dB, is challenging. Some techniques have been proposed for wideband LNAs, mainly based on noise cancelling [17] [18] or negative feedback [19] [20]. Besides, another bottleneck of wideband operation may come from the interface between LNA and mixer where the capacitive loading from mixer can limit the bandwidth of LNA.

With CMOS downscaling, the unity current-gain frequency (f_T) of MOS transistor keeps increasing, which exceeds 100GHz for CMOS beyond the 100nm node [21]. This makes it feasible to realize receivers with a few GHz bandwidth using no or

very few inductors which cost area. In recent years, many wideband receivers have come up, partly enabled by the process advancement. They can continuously cover a wide bandwidth, say at least an octave, and therefore largely share the receiver components. These features differentiate them from the current industrial multi-band multi-mode radios (Fig. 1.7).

One of the first CMOS wideband receivers was published in 2004 [22], showing a -3dB bandwidth of 200MHz to 2.2GHz and implemented in 0.18μm technology. It is a zero-IF receiver employing noise-cancelling LNA and passive mixer. By an extensive use of high effective gate-source voltages (V_{GS}-V_{TH}) and resistive degeneration, it achieves +1dBm IIP3 at a conversion gain of around 25dB. However, this comes at the cost of a relatively high NF of 7dB and a power consumption of 200mW.

The UCLA SDR receiver [23] published in 2006 is a zero-IF receiver aming at the 800MHz to 5GHz range in 90nm CMOS, including baseband filters and an LO generator. The noise-cancelling LNA exploits inductive peaking to extend the bandwidth at the input and the interface with mixer and a passive mixer is adopted for low 1/*f* noise and high IIP2. The LNA and the mixer operate at a 2.5V supply for high dynamic range, consuming 45mW. At a full-gain setting, the LNA and mixer achieves 30dB gain, 5dB NF, and -15dBm IIP3 up to 2.4GHz, while at a medium-gain setting, it achieves 21dB gain, 9dB NF, and -3.5dBm IIP3. However, the performance of the whole receiver is only presented for two frequencies: 900MHz and 2.4GHz. No measurement data are shown beyond 2.4GHz.

The IMEC SDR transceiver [24] [25] published in 2007 consists of a zero-IF wideband receiver in 0.13μm CMOS. The publications stress on extensive programmability aiming at an adaptive power/performance trade-off. To resolve the conflict of low 1/*f* noise required below 500MHz RF and fast transistors required for 5GHz, two separate LNAs are used: a noise-cancelling LNA for 100MHz to 2.5GHz and an inductive-degeneration LNA for 2.5GHz to 6GHz. Its second generation [26] published in 2009 is a 0.1-to-5GHz zero-IF receiver implemented in 45nm CMOS, including baseband filter and frequency synthesizer. A passive mixer follows two LNAs, an active-feedback LNA for 0.1GHz to 1.5GHz and a resistive-feedback LNA for 1.5GHz to 5GHz. The dual-band LNAs use switchable low-Q inductive peaking to cover the whole wide band in four sub-

bands. The receiver sensitivity is verified for 6 different standards, from DVB-H at 600MHz to 802.11n at 5GHz, achieving an NF from 2.3dB to 6.5dB.

In parallel to [24-26], a similar approach of realizing a SDR transceiver aiming at a power/performance trade-off has also been developed in industry. As an example, the Bitwave "Softransceiver" [27] is configurable from 700MHz to 3.8GHz and is compliant with cellular, WLAN, and broadcast standards. Each element of the transceiver's single-component transmit and receive chain can be software-optimized for a given standard. The receiver integrates an analog front-end, ADCs and frequency synthesizers, in 0.13μm CMOS. However, detailed performance data such as NF and linearity are not available.

Besides, many wideband receivers have been developed for ultra-wideband (UWB) applications [28] [29]. Some of their techniques can also be useful to SDR. The "Blixer" [30] published in 2008 is a wideband zero-IF receiver using a combined balun-LNA-I/Q-mixer topology. It stacks an I/Q current-commutating mixer on top of a noise-canceling balun-LNA, thus reusing the bias current. The real part of the impedance of all RF nodes is kept low, and the voltage gain is not created at RF but at baseband where capacitive loading is no problem. Thus the bandwidth limitation is relaxed at the interface between the LNA and the mixer in a conventional receiver employing a voltage-gain LNA. A large RF bandwidth is thereby achieved without using inductors for bandwidth extension. This feature will also be exploited in one of our designs (Chapter 5). Implemented in 65nm CMOS, it achieves an 18dB gain, a flat NF of 5.5dB from 500MHz to 7GHz, and a -3dBm IIP3 while consuming only 16mW from a 1.2V supply. However, $1/f$ noise from the mixer which conducts DC current is a challenge for SDR applications.

In summary, most published wideband receivers use a zero-IF architecture for high-level integration and adopt a passive mixer for low $1/f$ noise. Both noise-cancelling [22] [23] [25] [30] and negative-feedback [26] [28] [29] LNAs have found applications. As demonstrated [23] [26] [30], using CMOS technology beyond 100nm node, a receiver RF bandwidth from a few hundred MHz to more than 5 GHz can be achieved with an NF < 6dB at a low power consumption, say a few tens of mW, suitable for mobile applications. Besides, some of the presented receivers can satisfy the in-band IIP3 > -10dBm [22] [28-30], simultaneously with NF < 6dB.

However, these wideband receivers mainly focus on realizing a wideband operation with good enough NF and in-band linearity for each band, more or less assuming an RF pre-filter will take care of strong out-of-band interference. Therefore, although these receivers can share the on-chip components for multiple bands, a dedicated narrowband RF pre-filter is still needed for each band thus adding size and cost. There is clearly room for improvement to make wideband receivers robust to out-of-band interference.

1.3.2 Robustness to Out-of-Band Interference

CMOS scaling is beneficial for wide bandwidth, but not for linearity because: a) more short-channel effects, e.g. channel-length modulation and mobility reduction, bring larger distortion related to transistor output impedance [31]; b) lowered supply voltage sets tighter constraints for handling large interference.

The linearity challenge in scaling CMOS is especially problematic for OBI, which can be much stronger than IBI. In a wideband receiver, out-of-band interference can generates in-band distortion via nonlinearity or harmonic mixing, as described in Section 1.2. Some wideband receivers, e.g. [23], claim to be able to completely get rid of the RF pre-filter however the achieved performance is not convincing. For example, the reported IIP3 of -3.5dBm is for a medium-gain setting, which cannot simultaneously guarantee the required sensitivity level while the derived IIP3 for the full-gain setting is around -15dBm. On the other hand, without any RF pre-filtering, the required IIP3 can be as high as, e.g., +30dBm for a Bluetooth radio [32].

To counter the extra-ordinary challenge due to OBI, there are a few measures reported in literature to relax the pre-filtering requirements, as discussed below one by one.

a) Out-of-Band Nonlinearity

One potential solution is to integrate some band-selectivity on chip. However, high-performance LC filtering is still difficult to realize in digital CMOS due to, for instance, large size and low Q of monolithic inductors. Q-enhanced band-pass

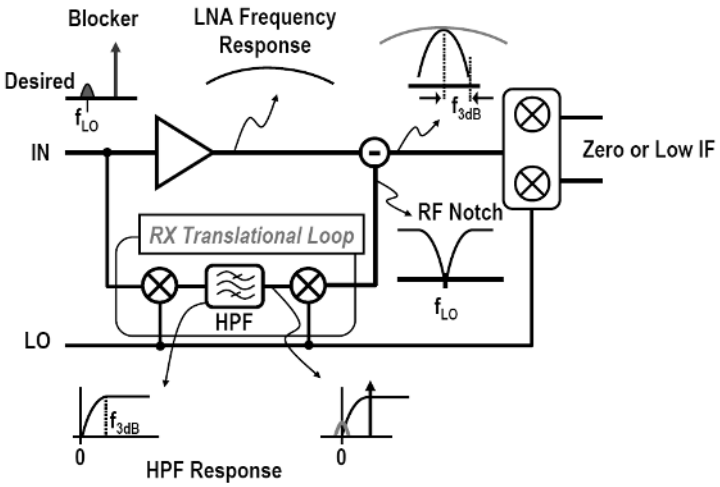

Figure 1.8 Feedforward blocker filtering concept [41]

filters [33] [34] have been proposed to improve the inductor *Q* using active components as negative resistance. However, this often comes at the cost of noise and linearity degradation. Also, the frequency tuning range is still limited by the LC tank, typically tuned via controlled capacitors. As shown by the benchmark in [33], the achieved tuning range so far is less than 25%, which means that more than a few filters are needed to cover a broad band for SDR applications. On the other hand, smaller filter size and larger tuning range (e.g. 100%) can be achieved using pure active band-pass filters without passive inductors [35] but at the cost of degraded dynamic range. Notch filters with a band-stop characteristic using a Q-enhanced LC-tank have been applied in some wideband receivers to suppress specific interference, e.g. for UWB applications [36] [37]. However, the limitation is that the interference should be predictable and concentrated in a small frequency range.

LNA linearization techniques have been proposed to achieve an IIP3 in excess of +15dBm via, for instance, derivative superposition methods [38] [39]. Some drawbacks of these techniques are [40]: 1) they often rely on two nonlinearity mechanisms that compensate each other but don't automatically match, so that some kind of fine tuning is needed, compromising the robustness to process spread; 2) they mostly rely on modeling of the weakly nonlinear region so that high IIP3 is

only achieved for low input interference power while there is only limited or even no benefit for strong interference.

Recently, a flexible blocker filtering technique has been presented to cancel blockers at the output of the LNA [41], as shown in Fig. 1.8. Blocker reduction is achieved by means of an auxiliary feedforward path, using two mixers with a high-pass filter (HPF) in between. This auxiliary path conducts the undesired interferers and suppresses them by subtracting them from the main signal path at the output of the LNA. However, it comes at significant cost in terms of noise and power consumption due to the additional feedforward signal path and its performance relies on the matching between the main path and the auxiliary path. We will see later in Chapter 5 that an equivalent functionality can be achieved with much simpler hardware.

b) Harmonic Mixing

Harmonic-rejection (HR) mixers using multi-phase square-wave LOs driving parallel operating mixers have been proposed [42]. Fig. 1.9 (a) shows an example, where the weighted current outputs add up to approximate mixing with a sine-wave LO. All even-order harmonics can be suppressed by a balanced LO. The combination of an amplitude ratio of 1:√2:1 and an 8-phase LO (equidistant 45°) can reject the 3rd and 5th harmonics, as shown in the vector diagram of Fig. 1.9 (b). The 7th harmonic is not rejected and still needs to be removed by filtering, but the filter requirement is strongly relaxed compared to the case of a normal double-balanced I/Q mixer whose first un-rejected harmonic is the 3rd order. However, the achievable HR ratio is typically limited to 30-to-40dB [23] [43] [44] by the accuracy of the LO phases and the amplitude ratios, e.g. the irrational amplitude ratio of 1:√2:1.

To improve the limited HR ratio in a mixer, the state-of-the-art wideband TV tuners rely on RF-tracking filters together with HR mixers [43] [44] to guarantee more than 65dB HR ratio. However, these tracking filters cost power, take area, and introduce extra noise and distortion. For example, the 4th-order band-pass Gm-C tracking filter in [43] achieves a 7dB gain, a 17dB NF, and a +7dBm IIP3 while consuming 72mW power.

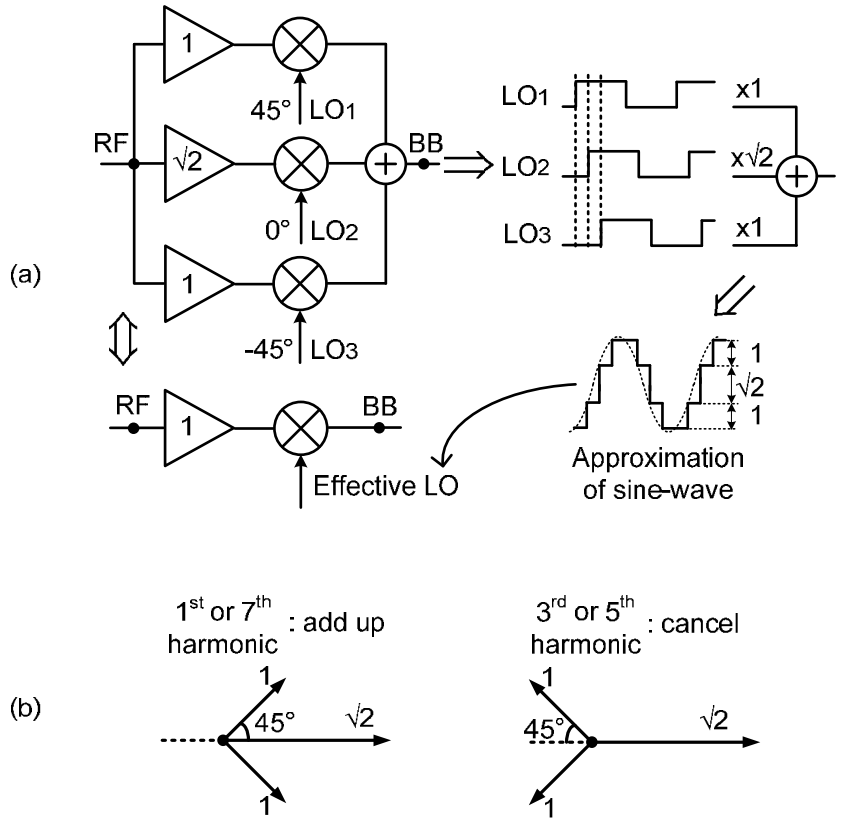

Figure 1.9 (a) Block diagram of a traditional HR mixer; (b) its vector diagram

As a summary, we see some measures have been taken in both areas, i.e. out-of-band nonlinearity and harmonic mixing. However, either they are not yet suitable for SDR applications due to insufficient flexibility, e.g. integrated LC filters, or they may significantly compromise other performance such as power and noise, e.g. tracking filters for TV tuners and blocker filtering via an auxiliary path. Some other techniques can be flexible and do not degrade other performance much, but are sensitive to mismatch and process spread, e.g. LNA linearization and HR mixers. Besides, of all the aforementioned techniques, their selectivity cannot yet match off-chip RF pre-filters such as SAW filters. To this end, we may conclude that there is a lot of room for improvement with respect to SDR receiver's robustness to out-of-band interference.

1.3.3 Flexible Baseband Channel Selection

Generally for the baseband-filter design, there exists a trade-off between bandwidth, noise, and filter order versus power consumption. Two classes of filters have been proposed for flexible SDR receivers: continuous-time (CT) and discrete-time (DT) filters. Both have shown promising results.

The IMEC SDR transceiver [24] applies CT baseband filters constructed via a cascade of two active-G_m-RC biquads and a Rauch biquad. It may continuously cover a bandwidth of 0.35MHz to 23.5MHz with a programmable 2^{nd}, 4^{th} or 6^{th} order. It can achieve a 12-bit frequency-tuning resolution via a combination of a 5-bit coarse tuning using a resistor array and a 7-bit fine tuning using a capacitor array [45]. Their second-generation SDR receiver also employs CT baseband filtering [26].

Flexible baseband DT filters have also been developed. The UCLA SDR receiver [23] uses a passive switched–capacitor filter demonstrated for the GSM and the 802.11g standards, tunable via changing sampling rate and decimation ratios. However, continuous frequency tunability was not shown. The active-G_m switched-capacitor filter from NEC [46] can cover 0.4MHz to 30MHz continuously tunable via a DT transconductor controlled by clock duty cycle, with a 2^{nd} or 4^{th} order characteristic. The frequency-tuning resolution was not mentioned but depends on the resolution of the clock duty cycle.

The baseband filter in the Bitwave "Softransceiver" [27] can continuously cover the bandwidth of 25kHz to 20MHz in more than 1000 steps and can support all major cellular, WLAN, and broadcast standards. It is unclear whether the filter is in CT or DT implementation.

From the above examples, we can see that many promising solutions have been demonstrated for the flexible baseband filtering and basically can satisfy the SDR applications. Especially, some have been built into products such as [27].

1.3.4 Compatibility with CMOS Scaling and SoC Integration

As shown in Section 1.3.1, using new design techniques, many wideband radio receivers have been demonstrated in advanced CMOS technology, e.g. 90nm [23], 65nm [30], and 45nm [26]. However, it is another degree of challenge to integrate radio transceivers and digital (de)modulators on the same chip, due to, e.g. digital switching noise.

Direct RF-sampling receivers seem to be a good candidate, both for better compatibility with CMOS scaling [47]-[49] and SoC integration [50] [51]. They sample the signal early in the receiver chain *before or simultaneously with* downconversion, instead of *after* downconversion which is done in RF-mixing receivers. A few RF-sampling receivers for commercial products have been presented [48]-[51], including what is claimed to be the first published [51] commercial SoC for quad-band GSM in 90nm baseline digital CMOS with no analog extension.

However, all of these RF-sampling receivers are dedicated to one narrowband standard and all the aforementioned wideband receivers in Section 1.3.1 are based on RF mixing. Further research is needed to evaluate the suitability of RF sampling for SDR applications, and we will address this subject in Chapter 2.

Till this point, we have discussed the challenges of realizing a SDR receiver and some state-of-the-art solutions in literature. The next section will discuss our research objectives and the challenges we are going to address, while also clarifying the added value to other work.

1.4 Research Objectives

After summarizing the previous section, we may conclude that lots of solutions have been proposed for wideband receivers and flexible baseband filtering, showing promising results. However, the other two challenges, of handling OBI in a wideband receiver and of realizing a SDR in a downscaled CMOS with SoC integration, still have a long way to go.

This thesis aims at finding: 1) techniques to improve the robustness of wideband receivers to OBI; 2) techniques for wideband receivers compatible with CMOS scaling and SoC integration.

To address the challenge due to OBI, we should look at both mechanisms: out-of-band nonlinearity and harmonic mixing. After amplification by an LNA, the burden of the nonlinearity is mainly on the mixer while harmonic mixing also happens in the mixer. Therefore, this thesis will focus on *frequency translation* related innovations to improve the receivers' robustness to OBI. The work aims at removing RF pre-filters or at least drastically relaxing their requirements.

As described in the previous section, RF-sampling receivers can bring two advantages: compatibility with CMOS scaling and SoC integration. However, as will be discussed in Chapter 2, current RF-sampling techniques do not directly fit wideband SDR applications. To our knowledge, all the wideband receivers shown by other researchers so far are based on RF mixing but not RF sampling. We will explore new RF-sampling techniques more suitable for wideband SDR receivers, which also involve new *frequency translation* techniques.

The title of the thesis refers to the above mentioned goals. This thesis mainly explores "frequency translation techniques" to improve the "interference-robust" characteristic of "software-defined radio receivers" and to make them compatible with CMOS scaling and SoC integration. Moreover, the thesis also describes some filter and amplifier techniques which support interference-robustness.

Based on the foregoing discussions, now we set our concrete research objectives:

- Develop new RF-sampling receivers for wideband applications
- Enhance the out-of-band linearity of wideband receivers
- Improve the robustness of harmonic rejection to mismatch

1.5 Thesis Organization

The rest of the thesis is organized as follows:

Chapter 2 discusses fundamental differences of frequency translation (FT) techniques for radio receivers, via a classification and comparison for FT techniques based on mixing and sampling principles [52]. This also leads to the definition of a discrete-time (DT) mixing technique. Moreover, we will evaluate the suitability of RF-mixing and RF-sampling receivers to SDR and analyze the challenges of applying RF sampling to wideband receivers [53].

Chapter 3 elaborates the DT mixing technique [52] [54], which can make RF sampling more suitable to SDR receivers by achieving two wideband features: wideband quadrature demodulation and wideband harmonic rejection. To verify the concept, a 200-to-900MHz DT-mixing downconverter with 8-times oversampling and 2^{nd}-to-6^{th} HR is implemented in 65nm CMOS. Chapter 4 describes a tunable LC filter and a linearized LNA [55] [56], applied as pre-stages of the DT-mixing downconverter to construct a complete RF-sampling receiver achieving a minimum NF as low as 0.8dB. To make the receiver more robust to interference, the tunable LC filter improves the HR ratio flexibly and the LNA exploits a new linearity enhancement technique.

Furthermore, Chapter 5 proposes two frequency translation techniques for an interference-robust SDR receiver [57] [58], one to improve the out-of-band linearity and the other to make the HR robust to mismatch. To demonstrate these two concepts, a 65nm CMOS receiver based on RF mixing shows that +3.5dBm in-band IIP3 and +16dBm out-of-band IIP3 can be achieved. More than 60dB HR ratio is measured over 40 randomly-selected chips while more than 80dB becomes possible with digitally-enhanced HR. The proposed accurate multi-phase LO generator works up to 0.9GHz while the RF bandwidth is measured up to 6GHz.

Chapter 6 draws conclusions, summarizes the main contributions of this work, and suggests some future research directions.

The appendix contains two important analyses. Appendix *A* derives the wideband transfer function of baseband impedance to RF through mixer switches (Chapter 5), namely “mix-impedance”. Appendix *B* performs a statistical analysis for HR considering random amplitude and phase errors, to quantify the required accuracy to achieve a certain HR ratio (Chapter 5).

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Chapter 2

Frequency Translation Fundamentals

From Section 1.4, we know that frequency translation (FT) techniques will be a focus of this thesis. This chapter discusses fundamental differences among various FT techniques for radio receivers, with an emphasis on downconversion. It serves as a theoretical base for the follow-up chapters (Chapter 3 to 5) which will present circuits and systems around various types of FT techniques.

Chapter 2 starts with a brief introduction on the main reasons for applying FT in radios in Section 2.1. To clarify different downconversion techniques, in Section 2.2 we present a classification of them [1]. This also leads to the definition of a discrete-time (DT) mixing technique which is the subject of the next two chapters. To further clarify the classification criteria, Section 2.3 compares mixing and sampling principles, stressing on their fundamental distinctions. Based on the classification, Section 2.4 comes up with three receiver architectures and discusses their suitability to SDR applications. Among these architectures, RF-sampling receivers show some advantages on the compatibility with CMOS scaling and SoC integration. However, traditional RF-sampling techniques also present some drawbacks for wideband SDR applications. Therefore, in Section 2.5, we analyze the challenges of applying RF sampling to wideband receivers [2]. These challenges can be solved via techniques presented in the next chapter. Chapter 2 ends with conclusions (Section 2.6) and references (Section 2.7).

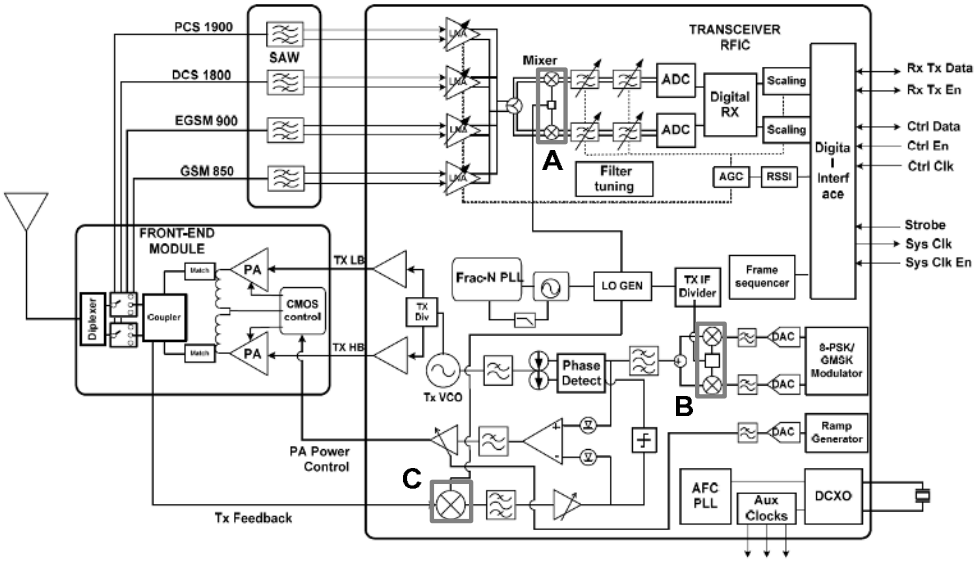

Figure 2.1 An integrated quad-band GPRS/EDGE transceiver [3]

2.1 Why Frequency Translation

Frequency translation (FT) includes frequency upconversion and downconversion. It can be found in many radios, e.g. as a *bridge* between baseband and RF parts, to process data at baseband while transmitting and receiving antenna signals at radio frequency, typically in the range of hundreds of MHz to a few GHz.

Fig. 2.1 shows an example of a quad-band GSM radio transceiver [3], indicating the blocks with FT functions in both receivers and transmitters. In the receiver, an RF quadrature mixer A is used between the LNA and the baseband filter, to down-convert the RF signal received at the antenna to baseband for the analog-to-digital converter (ADC). In the transmitter, an IF quadrature mixer B is used between baseband filter and IF filter, to up-convert the baseband signal from digital-to-analog converter (DAC) to be an input of the phase detector in the transmitter translational loop. Another mixer C is applied as a part of the translational loop to down-convert the transmitter feedback signal to be the other input of the phase detector.

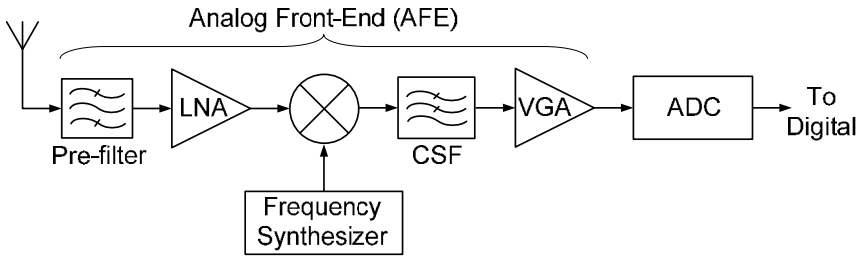

Figure 2.2 Block diagram of a typical radio receiver indicating AFE

There are two main reasons why we want FT in a radio: *feasibility and power consumption*. To explain this further, we first look at the receiver side.

In fact, a major function of an analog front-end (Fig. 2.2) is to assist in the conversion of an antenna signal into the digital domain[1], for advanced signal processing. Simply put, the analog front-end makes the job of the ADC easier with respect to the required speed and dynamic range (DR). The down-mixer is responsible for reducing the speed, from RF to baseband. Two other important blocks are the channel-selection filter (CSF), which suppresses interferers to reduce the required DR of an ADC, and the variable-gain amplifier (VGA), which controls the gain to reduce the DR of the desired signal and the unsuppressed interferers.

Without downconversion, the ADC in a radio receiver is often *unfeasible*, due to a higher speed required at a high DR. For instance, a GSM receiver can require an ADC resolution as high as 14 bits [4], even with the assistance of a VGA and a channel filter. Without downconversion, reception of a GSM signal at 1.9GHz asks for a 14-bit ADC running at a speed of at least 3.8GS/s (Nyquist rate). However, the reported state-of-the-art CMOS ADCs can only achieve 34dB (5.5-bit) signal-to-noise-and-distortion ratio (SNDR) at 2.5GS/s with 1.1GHz bandwidth [5] or 56dB (9-bit) SNDR at 1GS/s with 500MHz bandwidth [6]. An overview of the top ADCs published in recent years can be found in [7] but none is even close to the desired performance of about 4GS/s and 14 bits.

[1] Otherwise pure analog demodulation is also possible.

Please note that the actual required ADC resolution, without downconversoin ahead, is likely to be higher than what is typically required today for an ADC after downconversion. A key reason is that a band-pass (BP) channel-selection filter used in case of no downconversion is more challenging to make than a low-pass (LP) one. In the end, such a BP channel filter may be even not feasible or achieved with lower order and Q-factor. This can require a higher-resolution ADC due to a higher DR caused by stronger in-band interference since the BP channel selection is less effective. Moreover, if including out-of-band interference into consideration, e.g. for SDR applications, the requirement on the ADC will be even more stringent.

One step back. Even if such an ADC (and BP channel filter) can be feasible in the future, the *power consumption* of the whole radio is likely to be unnecessarily high. Without downconversion, it is not just the ADC to run at RF speed, e.g. in the GHz range, but also the channel filter, the VGA, and the digital front-end. However, the desired signal protocol (channel) bandwidth is often on the order of 1000 times smaller, e.g. in the MHz range. A lower operating speed means a lower overall power consumption, both for active analog circuits such as amplifiers and filters (static power) and for switching circuits such as quantizers and digital gates (dynamic power). Without downconversion early in the receiver chain, the required power of the whole radio would be dramatically increased.

For mobile applications, the reduced power consumption is a key advantage of applying downconversion early in a receiver, although the resulted architecture might not be as flexible as the ideal software-radio receiver (see Section 1.1).

Other than in receivers, frequency translation blocks are also widely applied in transmitters (Fig. 2.1), for either downconversion or upconversion. They usually share a similar motivation as for receivers, i.e. to make functions such as AD/DA conversion and phase detection feasible and to reduce the power consumption of the entire system.

This thesis mainly focuses on the receiver side, mostly involving frequency downconversion which is also the main subject of the rest of this chapter. Nevertheless, upconversion can be regarded as a counterpart, sharing most of the discussed principles.

Input / Principle	Analog-CT (CT CA)	Analog-DT (DT CA)	Digital (DT DA)
Mixing	CT Mixing[1]	**DT Mixing[2] (proposed)**	Digital Mixing[3]
Sampling	CT-to-DT Sampling[2]	DT Re-sampling[2]	Digital Re-sampling[3]

[1]RF-mixing receiver [2]RF-sampling receiver [3]Ideal SWR receiver

Table 2.1 Classification of frequency downconversion techniques based on the type of input signal and the downconversion principle

Different frequency downconversion techniques have been proposed for radio receivers, most notably mixing and sampling. We would like to compare them and answer questions such as: what are the fundamental distinctions among them, is it really more flexible to sample as early as possible in a receiver chain, and does sampling suffer more from clock jitter compared to mixing?

In order to clarify the differences among downconversion techniques, we first propose a classification of them.

2.2 Classification of Downconversion Techniques

Table 2.1 classifies various downconversion techniques based on two aspects. The columns are defined by the input signal domain, i.e. continuous-time (CT) versus discrete-time and continuous-amplitude versus discrete-amplitude[2]. The rows distinguish in downconversion principle, i.e. mixing or sampling[3].

[2] A column for continuous-time discrete-amplitude signal can also be added, but we omitted it because we are not aware of any practical radio examples yet operating in this domain, although some work [8] [9] tried to explore the potential benefits of CT DSP systems. Such type of signal often appears at the output of a digital-to-analog converter before applying a reconstruction filter.

[3] Please note that sampling always provides a DT output, and hence it provides CT to DT conversion in case of a CT input, while under certain conditions as will be described in Section 2.3.2, it can also provide frequency translation.

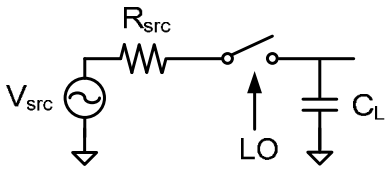

Figure 2.3 A general switching system for mixer or sampler

There are two techniques to achieve downconversion for each type of input signal:

1) For an analog-CT input signal, which is continuous in both time and amplitude, the downconversion can be realized via either CT mixing or CT-to-DT sampling.

2) For an analog-DT input signal, which is discrete in time but continuous in amplitude, DT mixing is possible. Alternatively, DT re-sampling can realize frequency conversion, also called decimation for down-sampling which reduces the sample rate.

3) For a digital input signal, which is discrete in both time and amplitude, downconversion can be done by digital mixing or digital re-sampling.

In Table 2.1, while all the other five techniques have been discussed in literature, to the authors' knowledge, we were the first to propose and implement the concept of DT mixing [10].

Different input signal domains can be easily distinguished, as done above for the three points. However, the other classification criterion, i.e. the mixing or the sampling principle, can still be vague. For instance, one circuit may have both functions, such as the circuit in Fig. 2.3: it has been presented as a passive mixer [11] [12] but also as a sampler [13] [14]. As another example, a sampler may have multiple functions: it is generally used for CT-to-DT conversion before an ADC but *sometimes* also for frequency translation as in [13]-[18]. To better distinguish the different classes in Table 2.1, we will explain more on the downconversion principles in the following section.

2.3 Fundamental Distinctions between Mixing and Sampling Principles

We will now try to find fundamental distinctions between the mixing and the sampling principles, from both a time-domain and a frequency-domain point of view.

2.3.1 Time Domain: Information Rate Changes or Not?

It is well known that mixing can be modeled as a multiplication in the time domain, while sampling can also be described via multiplication. For instance, CT-to-DT sampling can be modeled as multiplying a CT input signal $x(t)$ with a Dirac comb $\delta_T(t)=\Sigma\delta(t-n\cdot T_{LO})$, $n=-\infty\ldots+\infty$, and the sampled signal $x_s(t)$ is then:

$$\begin{gathered} x_s(t) = x(t)\cdot\delta_T(t) \overset{Fourier}{\leftrightarrow} \\ X_s(f) = X(f)\otimes\frac{1}{T_{LO}}\sum_{n=-\infty}^{+\infty}\delta(f-nf_{LO}) = \frac{1}{T_{LO}}\sum_{n=-\infty}^{+\infty}X(f-nf_{LO}) \end{gathered} . \tag{2.1}$$

$X(f)$ and $X_s(f)$ are Fourier transforms of $x(t)$ and $x_s(t)$ respectively. Equation (2.1) is commonly used to describe ideal sampling; however, the scaling factor $1/T_{LO}$ is often neglected. On might wonder whether this means that the "gain" of sampling is $1/T_{LO}$, with a unit of "Hz".

Analysis leads to the conclusion that this is not the case. In fact, sampling is more than just multiplication. There is an important step after (2.1), i.e. CT-to-DT conversion. The signals $x(t)$, $\delta_T(t)$, and $x_s(t)$ are all defined in the CT domain. If we convert $x_s(t)$ into the DT domain as $x_s(k)$ and apply DT Fourier transform, we will get a frequency-domain (FD) representation with continuous but normalized frequency axis, i.e. f/f_{LO}. Such a ratio can be defined as "r": $r=f/f_{LO}$. We can also obtain the r-axis FD representation by substituting $f=r\cdot f_{LO}$ into (2.1):

$$X_s(r\cdot f_{LO}) = X(r\cdot f_{LO})\otimes\frac{1}{T_{LO}}\sum_{n=-\infty}^{+\infty}\delta(r\cdot f_{LO}-nf_{LO}) = X(r\cdot f_{LO})\otimes\sum_{n=-\infty}^{+\infty}\delta(r-n)\,. \tag{2.2}$$

Note that the factor $1/T_{LO}$ goes away in (2.2), due to the scaling property of δ-function. If we define $Y_s(r)=X_s(r\cdot f_{LO})$ and $Y(r)=X(r\cdot f_{LO})$, then (2.2) can be written as

$$Y_s(r) = Y(r)\otimes\sum_{n=-\infty}^{+\infty}\delta(r-n) = \sum_{n=-\infty}^{+\infty}Y(r-n)\,. \tag{2.3}$$

$Y_s(r)$ is the FD representation for $x_s(k)$. Note that "r" is a continuous real number. Comparing (2.3) to (2.1), we can see that after converting the sampled signal $x_s(t)$ into the DT domain, the scaling factor $1/T_{LO}$ disappears and the gain of ideal sampling is 1, as normally expected. Therefore the step of CT-to-DT conversion is vital for a sampling operation.

We might look at this step as a way to reduce the *information rate* from infinite (CT information) to finite (DT data). Thus CT-to-DT sampling nicely fits in one row with DT re-sampling or digital re-sampling, all in the second row of Table 2.1, sharing the property of decreased information rate, i.e. decimation for downconversion. In contrast, all the mixing techniques do *not* change the information rate from input to output, neither for CT mixing and DT mixing nor for digital mixing.

This time-domain property can serve as an important distinction between mixing and sampling. For example, although a CT mixer and a CT-to-DT sampler have a similar implementation as shown in Fig. 2.3, there is a simple distinction between them: how the output signal is used. If the output signal is used as CT information, i.e. CT signal processing follows, then it is a CT mixer, but if it is used as DT information, i.e. DT signal processing follows, then it is a CT-to-DT sampler. Thus the distinction is *not in the circuit itself but in the way of interpreting the output*, i.e. whether the information rate changes from input to output or not.

With this distinction in mind, we see that a CT-to-DT sampler does *not* present a "hold effect"[4] in contrast to a sample-and-hold (S/H) with a CT output. Therefore, in this thesis, we will use the letter "S" in the symbol for sampler but not "S/H", as shown later in figures.

2.3.2 Frequency Domain: Frequency Translation Happens or Not?

Another distinction between mixing and sampling is visible in the frequency

[4] On the other hand, a "hold effect" can provide DT-to-CT conversion, e.g. following a digital-to-analog converter. Effectively a hold can increase information rate from finite (DT) to infinite (CT), like interpolation. In fact, applying a "hold effect" introduces a coefficient proportional to the holding time, and the factor of $1/T_{LO}$ in (2.1) can be cancelled. Therefore we can view (2.1) as an intermediate step, and the next step can be either CT-to-DT conversion (CT-to-DT sampler) or a hold (sample-and-hold).

domain. Simply put: mixing *always* does frequency translation while sampling *may or may not*. The main purpose of a mixer is mixing, i.e. "frequency translation", while a sampler has two possible functions: it always does "information-rate conversion" in the time domain, but *sometimes* it also does "frequency translation".

To be concrete, let's first look at CT mixing and CT-to-DT sampling, and then generalize the comparison to other cases in Table 2.1. Assume the input frequency is f_{in}, and the LO frequency is f_{LO} for mixing and the sampling frequency is f_s for sampling.

Using a CT mixer, the resulted spectrum is valid up to infinity due to the output's CT nature, and the input signal will always be translated by f_{LO} (unless f_{LO}=0) and its existing harmonics. If the desired signal at the output is at $f_{IF}=|f_{in}-f_{LO}|$, for downconversion $f_{IF}<f_{in}$ is required, i.e. $0<f_{LO}<2f_{in}$. Of course, the output of a CT mixer may contain spectrum not being translated, e.g. RF feed-through. However, that is often unwanted. Otherwise the mixer can be skipped.

On the other hand, using a CT-to-DT sampler, due to the output's DT nature, the resulted spectrum is valid from DC up to $f_s/2$, while the rest contains repetitive images. Focusing on the spectrum from DC to $f_s/2$, there are two cases:

1) If $f_s<2f_{in}$, the signal frequency will be translated (aliased) from f_{in} to $f_{IF}=|f_{in}-n\cdot f_s|$ (n=1,2…), where $n\cdot f_s$ is the closest sampling tone to f_{in}. Such a sampler is sometimes called a sampling mixer [19], as frequency translation does happen. This case is listed in Table 2.1 as CT-to-DT sampling.

2) If $f_s\geq 2f_{in}$ (Nyquist rate), the "closest sampling tone" is DC and *no* frequency translation happens, so the output signal remains at f_{in}, i.e. $f_{IF}=|f_{in}-n\cdot f_s|=f_{in}$ with n=0. Such a sampler corresponds to what is often used at baseband before an ADC. However, it may also be used at RF to generate an analog-DT signal or digital signal (after quantization) as the inputs for the second and the third columns in Table 2.1. However, this case is not considered in Table 2.1 which is only aimed to classify *downconversion* techniques.

Accordingly, DT mixing or digital mixing *always* results in frequency translation like CT mixing, while DT re-sampling or digital re-sampling always renders

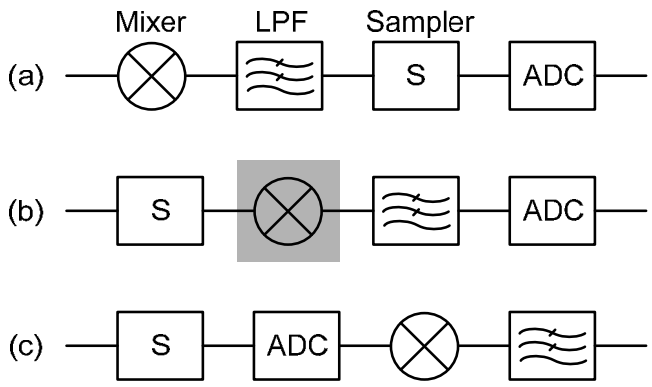

Figure 2.4 Three receiver architectures:
(a) RF-mixing receiver; (b) RF-sampling receiver; (c) Ideal SWR receiver

information-rate conversion as CT-to-DT sampling. But DT or digital re-sampling *sometimes* may also do frequency translation, depending on the relationship between the input signal frequency and the re-sampling frequency.

With a clear distinction among different downconversion techniques classified in Table 2.1, we can now conceive how to apply them to different receiver architectures and discuss the suitability of these architectures to SDR applications.

2.4 Receiver Architectures for SDR

As shown in Table 2.1, by their superscripts, the six classes of downconversion techniques are grouped into three receiver types. This section will discuss these receiver architectures, as illustrated in Fig. 2.4. To avoid confusion, we first clarify two points:

1) The way to group different downconversion techniques in a receiver architecture is based on necessary but insufficient conditions. For example, it is necessary to use either digital mixing or digital re-sampling for downconversion to define an ideal software-radio (SWR) receiver, but they can also be applied into other receiver architectures in combination with other downconversion techniques.

2) As explained in the previous section, a sampling operation may have multiple functions. Since Table 2.1 only targets at downconversion techniques, the word "sampling" used in the table only indicates the case with downconversion. However, since sampling operations can have different functions in a receiver, the word "sampling" used in this section is in a broad sense, which *may or may not* involve frequency translation.

2.4.1 Receiver Architectures

Fig. 2.4 (a) shows a simplified receiver architecture: mixer-LPF-sampler-ADC[5]. The "LPF" refers to low-pass filter. Other blocks such as amplifiers and LOs are also important but omitted here for figure clarity. The mixer is a CT mixer for downconversion and the sampler is a CT-to-DT sampler often without frequency translation. Since the input of the CT mixer is usually an RF signal, in Table 2.1 we group CT mixing as for "RF-mixing receiver", indicated by the superscript. This architecture is commonly used today for zero-IF or low-IF receivers.

Moving the sampler and the ADC towards the antenna renders other receiver architectures, as shown in Fig. 2.4 (b) and (c).

Fig. 2.4 (b) shows a sampler followed by a mixer. The (CT-to-DT) sampler receives RF signal and therefore this architecture is named "RF-sampling receiver". Please note that the sampler shown here may or may not do frequency translation. The follow-up mixer receives DT signal and therefore it is a DT mixer, for downconversion. In traditional RF-sampling receivers [13]-[18], the DT mixer (shaded block) was missing since the downconversion was realized using the sampler itself or a following DT re-sampler. In Table 2.1, we group these three techniques together as for "RF-sampling receiver" since they all use RF sampler, to directly do downconversion or to generate analog-DT signal for the follow-up blocks (DT mixer or DT re-sampler) to down-convert. This architecture does downconversion *before* ADC.

Fig. 2.4 (c) shows the ideal software-radio (SWR) receiver, which also uses RF

[5] Please note that in Fig. 2.4, the function of sampler (S) and ADC are separated, while in Fig. 2.2 they are represented as one block, i.e. ADC only.

sampler but with downconversion in the digital domain, using a digital mixer. In practice, the digital mixer can also be replaced by a digital re-sampler. In Table 2.1, we group these two items as for "ideal SWR receiver"[6], which also employs RF-sampling but it does downconversion *after* ADC.

2.4.2 Suitability to SDR

The ideal SWR receiver may offer the maximal flexibility, as it can select and process any band or channel in the digital domain which is more flexible than analog and it can process multiple bands or channels concurrently. But for that flexibility, the ADC has to convert the full RF spectrum of interests directly into the digital domain. The RF sampler in an ideal SWR receiver does not translate desired signals in frequency, but only does so after ADC. This is different from the RF-sampling receivers implemented in [13]-[18] which still down-convert and select the desired channel in the analog domain. Therefore the main asset of an ideal SWR receiver, i.e. flexibility, is *not* inherently shared by the RF-sampling receivers.

Although the ideal SWR receivers can be very flexible, without downconversion and filtering ahead, the required ADC performance, e.g. speed and dynamic range, is still too strict to be feasible (Section 1.1). So we will not discuss the ideal SWR receivers further in the chapter.

Both the RF-mixing and the RF-sampling receivers can be suitable for SDR applications, with similarities and differences. First we look at their similarities concerning some achievable performance, such as jitter-induced error and noise figure etc.

a) Similarities

A common concern for the RF-sampling receivers is the *clock jitter*. It can be shown [20] that for SDR receivers the jitter induced error using the RF-mixing receivers is proportional to the LO frequency f_{LO}, while for RF sampling it is

[6] To be precise, we may call Fig. 2.4 (b) as "RF-sampling analog-downconversion receiver" while call Fig. 2.4 (c) as "RF-sampling digital-downconversion receiver". However, for simplicity and compatibility with literature, we use the shorter names in this thesis.

proportional to the input signal frequency f_{in}. For zero-IF or low-IF receivers, f_{LO} and f_{in} are almost equal, and hence the difference in jitter requirement between the RF-mixing and the RF-sampling receivers is small. The feasibility of the RF-sampling receivers for practical use has been verified [15]-[18].

A serious consequence of jitter is the reciprocal mixing between the phase noise and the interference. For SDR receivers, the requirement on phase noise will be more stringent than for narrowband receivers since a selective RF pre-filter is not readily available. The actual jitter requirement depends on the interference scenario in different standards. In practice often the out-of-band interference is strong, so the frequency distance between the desired signal and the strong interference is large. If that is the case, the jitter-induced noise in the band of interest will be small [20] since the noise power induced by jitter is mainly concentrated around the strong interference due to reciprocal mixing.

Comparing the *RF flexibility*, there is little difference between RF mixing and RF sampling. They both require wideband RF front-end on the signal path. They both rely on changing LO frequency to vary the targeted band and hence require the same LO tuning range on the clock path. Actually there is a trade-off of flexibility between the signal path and the clock path. Sub-harmonic mixing or sub-sampling may lower the LO tuning range, i.e. more flexibility on the clock path. However, selective high-Q band-pass filtering is then likely needed to counter noise and interference folding. Such filters are difficult to implement on chip and will limit the flexibility of the signal path.

Another issue is the *baseband flexibility*, mainly the flexibility of the channel-selection filtering. For RF sampling, the baseband filtering can be implemented using DT filters such as switched-capacitor filters. For RF-mixing, the task can be done either using CT filters, such as G_m-C filters, or DT filters. As introduced in Section 1.3.3, both types of filters, i.e. CT [21] [22] and DT [4] [23], have been demonstrated for SDR applications.

For *gain and linearity*, which is mainly determined by active circuits such as amplifiers, we don't see a strong preference between RF sampling and RF mixing.

For *noise*, both approaches proved good NF in narrowband receivers. For GSM receivers, as an example, [17] based on RF sampling achieved an NF of 1.9dB and [24] based on RF mixing showed 2.5dB NF. However, for a wideband receiver such as SDR, noise folding will degrade the NF, i.e. the N^{th} harmonic of the LO will fold down noise (and interference) around $N{\cdot}f_{LO}$ to baseband during downconversion.

For RF mixing, the noise folding effect can degrade NF in a wideband receiver by 0.9dB for a 50% duty-cycle LO (Section 2.5.2). Note that the folding effect happens in the mixer stage and will fold down the noise from both antenna and LNA. Therefore the resulted NF degradation cannot be improved by extra LNA gain, if the LNA is wideband.

For RF sampling, aliasing results in noise folding. The effect here is more problematic than RF mixing, since all sampling harmonics ideally share the same magnitude, leading to an infinite NF if no any bandwidth limitation of the input noise. Traditional voltage sampling is known for its severe aliasing problem. Recently, charge sampling [4] [15]-[18] [25]-[27] has gained attention as it presents an embedded SINC function before the sampling action to reduce aliasing (Section 2.5.3). As a result, the effective LO harmonic magnitudes in charge sampling are similar to RF mixing, which means a similar noise folding effect.

From the discussions above, we see that concerning some achievable performance these two approaches can be close, but they do have different advantages and drawbacks concerning realization, such as compatibility with process technology and complexity of implementation.

b) Differences

Using RF sampling may offer *advantages* with respect to the *compatibility with advanced CMOS* processes because of the extensive use of switches, capacitors, and timing [18] [27] as explained in the following. The receiver baseband selectivity is digitally controlled by the clock frequency and the capacitance ratio, both of which can be very precise in deep-sub-micron CMOS [15]. Switching speed is a MOS device performance indicator that steadily improves with technology scaling [18]. Due to the process compatibility, such an architecture is

also amenable to migration from one process node to the next without significant re-work [16].

The main functions of passive switched-capacitor circuitry in DT receivers are filtering and decimation. Other tasks such as amplification still need active circuits that are less compatible with CMOS downscaling. However, if the baseband amplification can be shifted to somewhere after the switched-capacitor channel-selection filtering, linearity requirements can possibly be relaxed [28].

Furthermore, *system-on-chip (SoC) integration* of the RF transceiver and the digital baseband on the same chip is highly wanted for lower cost while also allowing for digitally-assisted calibration of analog blocks. However, it is a double-edged sword: the simultaneous switching noise generated from millions of digital transistors can ruin the analog performance. Using RF sampling naturally links the ADC sample rate to an integer division of the RF clock, via DT sample rate decimation. So the involved digital gates are clocked synchronously to the RF clock. This approach lessens the aggressor effects from digital activity, enabling what is claimed to be the first published commercial SoC for quad-band GSM in 90nm baseline digital CMOS with no analog extension [17].

A *disadvantage* of the RF-sampling approach in general is the *complexity of clock* generation and routing. It takes multiple different clock frequencies to decimate the RF sample rate to a lower rate operated by the ADC. Fortunately, these different clock frequencies have integer ratios, directly derivable via frequency dividers. But the routing of many clock signals to control lots of switches is still a challenge.

In another aspect, *RF-related baseband processing* can bring an extra degree of complexity especially for *wideband* SDR applications. Due to RF sampling with integer-times decimation, the baseband sample rate is directly related to the RF carrier frequency.

The bandwidth of DT filters, e.g. finite-impulse-response (FIR) or infinite-impulse-response (IIR) filters, intrinsically scales with its sample rate and hence the RF carrier frequency. Tuning to another channel thus changes the filter bandwidth! Instead, the baseband filter characteristic should be adapted to the protocol (channel) bandwidth, which is not necessarily related to the RF carrier. This

conflict can lead to an extra degree of *complexity* in baseband design, although it can be compensated by, e.g., digitally-programmable capacitor arrays to tune IIR filter bandwidth [16].

Moreover, for an accurate digital demodulation it is important to have the sample rate connected to the symbol rate. Since the whole analog-DT baseband including the ADC works at a sample rate connected to the RF carrier, a re-sampling block in digital baseband is desired for sample-rate conversion [15] [16], which means more *complexity* on the digital side as well as extra power consumption.

Therefore, the added complexity is a main disadvantage of RF sampling compared to traditional receivers based on RF mixing. But if the complexity is accomplished once, i.e. a DT receiver is implemented in a CMOS technology node, it might take less effort to move into next-generation processes than for traditional analog/RF circuits.

In summary, the RF-mixing and the RF-sampling receivers may offer similar performance in terms of gain, NF, linearity, RF and baseband flexibility, noise and interference folding, and jitter-induced errors. Compared to RF mixing, the RF-sampling receivers can require extra complexity, due to RF-related baseband-signal processing and extensive clock control for the switched-capacitor circuits used for DT operations. Furthermore, there are some extra challenges of applying traditional RF-sampling receivers to wideband applications which will be analyzed in Section 2.5, but these challenges can be solved via techniques proposed in Chapter 3. Nevertheless, RF sampling offers some advantages on the compatibility with advanced CMOS technology and SoC integration.

Anyhow, for both, we didn't find major roadblocks impeding the realization of a SDR. As CMOS continues scaling and the SoC trend goes on, it seems relevant to explore the potential of building a SDR receiver based on RF sampling. However, traditional RF-sampling techniques are not directly suitable to wideband receivers such as SDR, due to, e.g., some *frequency-dependent* properties that will be analyzed in the next section.

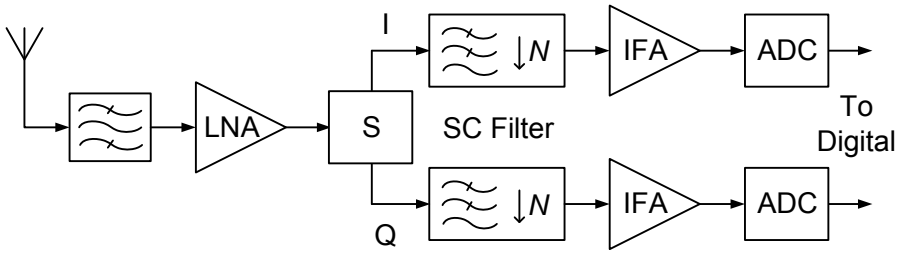

Figure 2.5 Block diagram of a traditional RF-sampling receiver

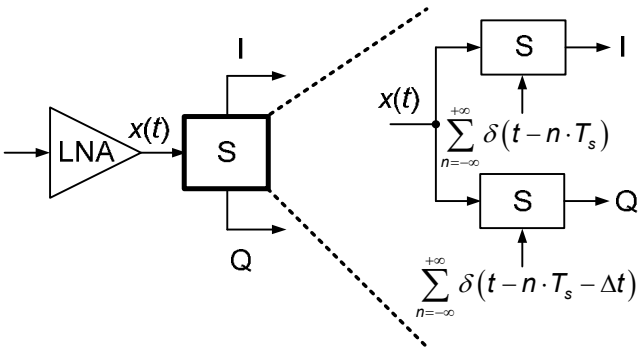

Figure 2.6 Traditional RF-sampling receiver using a time delay (Δt) for quadrature demodulation: pseudo-quadrature sampler

2.5 Challenges of RF Sampling for Wideband Receivers

Recently, the feasibility of CMOS RF-sampling receivers has been demonstrated for Bluetooth [15], GSM/GPRS [17] [28] and Wi-Fi/WiMAX [18] products. As shown in Fig. 2.5, the building blocks of a typical RF-sampling receiver include an RF pre-select filter, a low-noise amplifier (LNA), a sampler (S) producing I/Q outputs, a chain of switched-capacitor (SC) circuits for filtering and decimation, an IF amplifier (IFA), and an ADC.

We would like to discuss the challenges of applying traditional RF-sampling techniques for wideband radios such as SDR, which are not associated with RF mixing. *In addition to* the RF-related baseband processing that has been discussed in

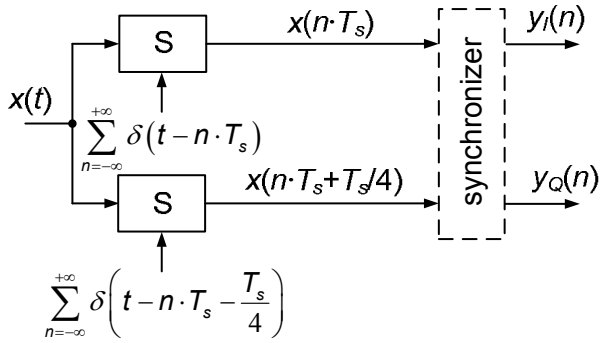

Figure 2.7 Modeling a pseudo-quadrature sampler with a synchronizer

Section 2.4.2, here we will analyze three other challenges. These three challenges serve as additional differences between RF mixing and RF sampling, but not fundamental. They can be solved via techniques proposed in Chapter 3.

2.5.1 Frequency-Dependent Phase Shift

As shown in Fig. 2.6, a *pseudo*-quadrature sampler, used in [13]-[18], multiplies the same input signal $x(t)$ with two different series of sampling impulses, with a delay of $\Delta t=T_s/4$ between each other, where T_s is the period of local oscillator (LO) signal. This procedure is also known as periodically nonuniform sampling of second order [29].

The sampled outputs are $x(n\cdot T_s)$ and $x(n\cdot T_s+T_s/4)$, as shown in Fig. 2.7. For the digital baseband demodulation of amplitude and phase information, a pair of I/Q samples will be treated as one complex sample. A complex sample can be written as

$$y_C(n) = y_I(n) + j \cdot y_Q(n). \tag{2.4}$$

A complex sample $y_C(n)$ consists of a pair of I/Q samples, $y_I(n)$ and $y_Q(n)$, which corresponds to $x(n\cdot T_s)$ and $x(n\cdot T_s+T_s/4)$ respectively. When combining an I sample and a Q sample together as a complex sample, the timing difference of $T_s/4$ is removed, which can be modeled as a synchronizer (Fig. 2.7). In fact, the synchronization can be viewed as a consequence of the sampling operation producing DT data. So the output signal is only valid at discrete time-points, e.g.

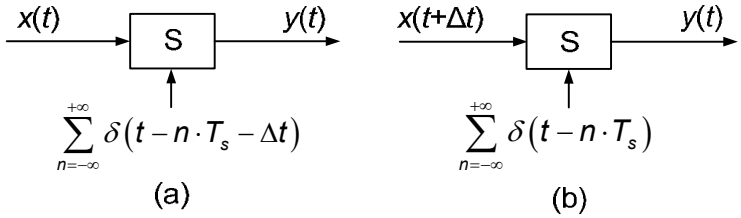

Figure 2.8 Two equivalent models of sampling with an arbitrary time delay: (a) delay on the clock path; (b) delay on the signal path

either n or n+1 but not in between, which means that $x(n\cdot T_s+T_s/4)$ should be defined as either $x(n)$ or $x(n+1)$ and thus gets "synchronized".

To generate an arbitrary-phase-shifted sample stream, a generalized analysis for a sampling system with a delay of Δt can be applied. If $0\le\Delta t<T_s$, we have the two equivalent sampling models in Fig. 2.8 (a) and (b). Due to the synchronization, the delay of Δt can be shifted from the sampling impulses $\Sigma\delta(t-n\cdot T_s-\Delta t)$ in Fig. 2.8 (a) to the input signal $x(t+\Delta t)$ in Fig. 2.8 (b), enabling the following analysis. Based on Fig. 2.8 (b), the output signal $y(t)$ can be written as

$$y(t)=x(t+\Delta t)\cdot\sum_{n=-\infty}^{+\infty}\delta(t-n\cdot T_s)\,. \tag{2.5}$$

Taking the Fourier transform of (2.5), we get

$$\begin{aligned} Y(f)&=\left[X(f)\cdot e^{j\cdot 2\pi\cdot f\cdot\Delta t}\right]\otimes\left[\frac{1}{T_s}\cdot\sum_{n=-\infty}^{+\infty}\delta(f-n\cdot f_s)\right]\\ &=\frac{1}{T_s}\cdot\sum_{n=-\infty}^{+\infty}\left[X(f-n\cdot f_s)\cdot e^{j\cdot 2\pi\cdot(f-n\cdot f_s)\cdot\Delta t}\right] \end{aligned}. \tag{2.6}$$

In (2.6), it should be noticed that the convolution in the frequency domain will fold the input spectrum $X(f)\cdot\exp(j\cdot 2\pi\cdot f\cdot\Delta t)$ but will not change its magnitude and phase. Therefore the phase shift of $y(t)$ is equal to that of $x(t+\Delta t)$, which can be written as

$$\Delta\varphi=2\pi\cdot f_{RF}\cdot\Delta t\,. \tag{2.7}$$

For illustration, (2.7) is also represented as Fig. 2.9 (a), from which we can clearly see that the phase shift of the sampled output is proportional to the RF input frequency (f_{RF}). On the other hand, if using a mixer to generate the phase shift, for the output signal that is downconverted by the fundamental harmonic of the LO,

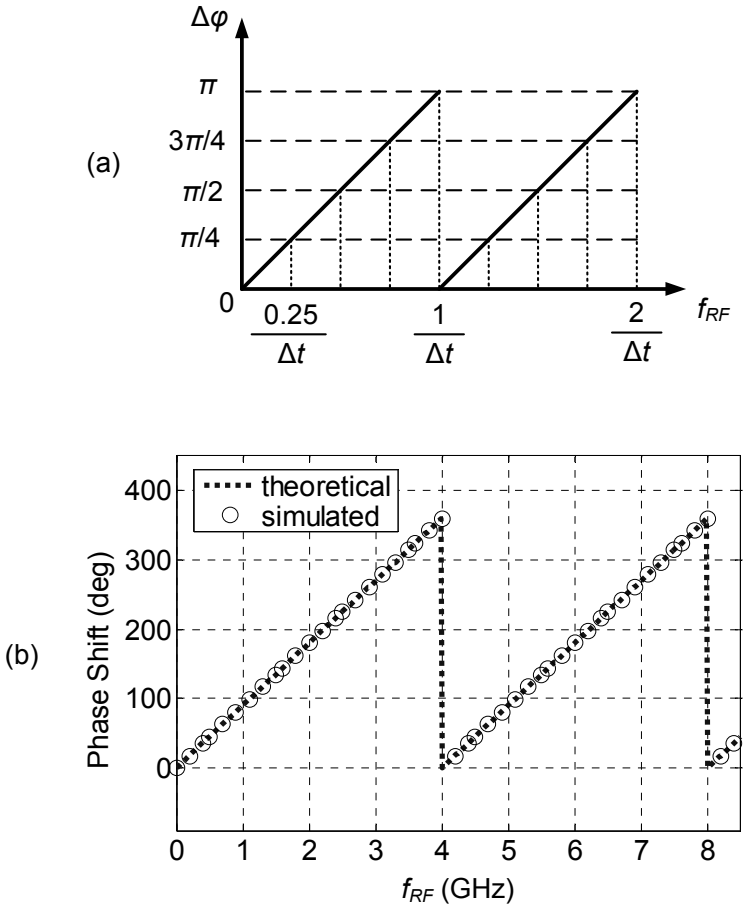

Figure 2.9 RF-dependent phase shift in a traditional RF-sampling receiver: (a) general theory; (b) a specific example comparing theory and simulation with f_s=1GHz and Δt=250ps (exactly 90° at f_{RF}=1GHz)

the resulted phase shift would be

$$\Delta\varphi_{mixer} = 2\pi \cdot f_{LO} \cdot \Delta t\,, \tag{2.8}$$

where f_{LO} is the LO frequency. Since Δt can be written as a fraction of the LO period (T_{LO}=1/f_{LO}), $\Delta\varphi_{mixer}$ is a constant. Note that the phase shift (2.8) generated by a mixer is not systematically dependent on the input RF frequency but the phase shift (2.7) generated by a sampler is!

Fig. 2.9 (b) compares the theoretical results based on (2.7) with the simulated results. Ideal components are used during the simulation to avoid parasitic effects and with the following settings: f_s=1GHz, and Δt=250ps. From the figure we can see the simulated results match with the theoretical results very well.

Suppose that we want to generate a phase shift of $\Delta\varphi$ using an LO signal with a delay of Δt. Via (2.7), it can be derived that the resulted phase shift will only be accurate at some specific input frequencies satisfying

$$f_k = \frac{\Delta\varphi}{2\pi \cdot \Delta t} + \frac{k}{\Delta t}, \tag{2.9}$$

where k is an integer ($\Delta\varphi=\Delta\varphi+k\cdot 2\pi$), and present frequency-dependent phase errors at other input frequencies.

Generally Δt can be chosen in such a way that the phase shift is exact for the center, or called carrier, frequency (f_c) of the desired input signal. Rearranging (2.7), we get $\Delta t=\Delta\varphi/(2\pi\cdot f_{RF})$. For a 90° phase shift, i.e. $\Delta\varphi=\pi/2+k\cdot 2\pi$, the following condition holds:

$$\Delta t = \frac{\pi/2 + k \cdot 2\pi}{2\pi f_c} = \frac{k + 0.25}{f_c}. \tag{2.10}$$

The absolute phase error at frequency f_{RF} can be described as

$$\left|\varphi_e\right| = \left|2\pi \cdot (f_{RF} - f_c) \cdot \Delta t\right| = \left|2\pi \cdot \Delta f \cdot \Delta t\right|. \tag{2.11}$$

From (2.11), we can see the phase error is proportional to the frequency offset Δf and the time delay Δt, which is inversely proportional to f_c according to (2.10). Please note that the sampling frequency (f_s) does not determine the phase error. For the smallest $|\varphi_e|$, we need the smallest time delay, i.e. k=0 so $\Delta t=0.25/f_c$.

Due to the presented systematic phase error, the sampler in Fig. 2.6 is called *pseudo*-quadrature sampler. At GHz frequencies (f_c) and a few MHz channel bandwidth, the error can still be acceptable without correction, but for lower f_c or larger channel bandwidth it easily becomes several degrees. For example, for ultra-wideband applications, a 528MHz-bandwidth channel around a 3.432GHz carrier in a zero-IF receiver leads to a maximum Δf=264MHz. According to (2.11) considering Δt=0.25/f_c, it means a maximum phase error of 7°. Larger phase error leads to less accurate quadrature demodulation and degraded image rejection.

This problem is especially serious for sub-sampling receivers. The aim of using sub-sampling is to use a low-frequency LO to receive an RF signal at a much higher frequency, e.g. to relax clock generation. That means, to generate quadrature outputs, $\Delta t=0.25/f_c$ is not suitable since it requires two LO signals with a time delay of a quarter of the RF-signal period. Although the LO frequency (f_s) can be many times lower than the RF-signal frequency (f_c), the effort to generate this small Δt can be significant. Based on (2.10), we can choose a larger $|k|$ for a larger $|\Delta t|$, easier for clock generation. However, the cost is the larger absolute phase error $|\varphi_e|$ as predicted in (2.11). For example, the time delay can be chosen as $\Delta t=1.25/f_c$ (k=1) instead of $\Delta t=0.25/f_c$ (k=0), but the phase error will be 5 times bigger for the same channel bandwidth.

The traditional RF-sampling receivers presented in [13]-[18], with downconversion based on CT-to-DT sampling or DT re-sampling, all have this frequency-dependent phase property. Since the error pattern is known as (2.11), it should be possible to compensate this error in the digital domain [30]. But this will add extra complexity and power, especially for compensation aiming at a high accuracy. Fortunately, combining RF sampling and DT mixing (Chapter 3), the systematic phase error can be avoided.

2.5.2 Aliasing of Noise and Interference

Another challenge to implement a wideband RF-sampling receiver is aliasing, e.g. noise and interference around harmonics of the LO are down-converted to baseband during the sampling operation. For narrowband applications, a dedicated RF pre-filter is often used (Fig. 2.5) so aliasing is less of a problem. However, for SDR applications, such a filter can limit the flexibility and therefore is undesired. Without such a filter, the folding effect can be overwhelming, since all "LO harmonics" of a Dirac comb used in ideal sampling have the same magnitude.

On the other hand, RF mixing also suffers from LO harmonic downconversion as hard-switching mixers are often used. As a comparison, it is useful to quantify the consequence of noise folding in RF-mixing receivers.

Consider a hard-switching mixer driven by a square-wave LO with a duty cycle "d". Assuming white noise over the spectrum of interest, we can quantify the ratio

of the total noise power around all LO harmonics to the noise power only around its fundamental tone, defined as a noise-folding factor F_{nf}:

$$F_{nf} = \frac{\sum_{N=1,2,3...} \left[\text{sinc}(\pi \cdot d \cdot \text{N})\right]^2}{\text{sinc}(\pi \cdot d)}. \tag{2.12}$$

The rectangular function in a square wave introduces the SINC function, and N is the order of the harmonic. The noise-folding factor described by (2.12) doesn't account for the image noise which can be solved by image rejection. Different d ($0<d<1$) can give a different folding factor. If d=0.5, we have

$$F_{nf} = \sum_{K=1}^{\infty}(\frac{1}{2K-1})^2 = \sum_{K=1}^{\infty}(\frac{1}{K})^2 - \frac{1}{4}\cdot\sum_{K=1}^{\infty}(\frac{1}{K})^2 = \frac{3}{4}\cdot\frac{\pi^2}{6} = \frac{\pi^2}{8}. \tag{2.13}$$

The folded noise will directly affect the NF of the receiver:

$$NF_{RX} = \frac{S_{n,FE}\cdot F_{nf} + S_{n,BB}}{S_{n,src}}. \tag{2.14}$$

The symbols $S_{n,FE}$, $S_{n,BB}$, and $S_{n,src}$ denote the noise power density (assuming a white spectrum) from the front-end (all noise before downconversion), baseband (all noise after downconversion), and signal source (part of the front-end noise $S_{n,FE}$) respectively. Normally with a sufficient front-end gain, the noise from the front-end will dominate. If $S_{n,FE}\cdot F_{nf} >> S_{n,BB}$, adding noise power around all harmonics and assuming no high-band attenuation as a worst case described by (2.13), the noise folding effect will degrade the system NF by $10\log(\pi^2/8)$=0.91dB.

For RF sampling, the NF degradation can be much more, approaching infinite NF in a worst case if with no bandwidth limitation. Practically, there is always a band limit, e.g. due to parasitic capacitance. Different sampler structures also have different transfer functions and therefore different folding effects.

RF-sampling receivers can be categorized based on their sampler structures as *voltage sampling* [13] [14] or *charge sampling* [15]-[18]. Briefly speaking, the main difference is that charge sampling integrates current and samples charge while voltage sampling samples voltage. As well known, voltage sampling often seriously suffers from aliasing of noise and interference, and the suppression of the alias bands heavily relies on an RF pre-filter or the circuit's intrinsic bandwidth limitation. On the other hand, due to the integration effect in charge sampling, there is a *SINC* transfer function filtering the input spectrum before the sampling action

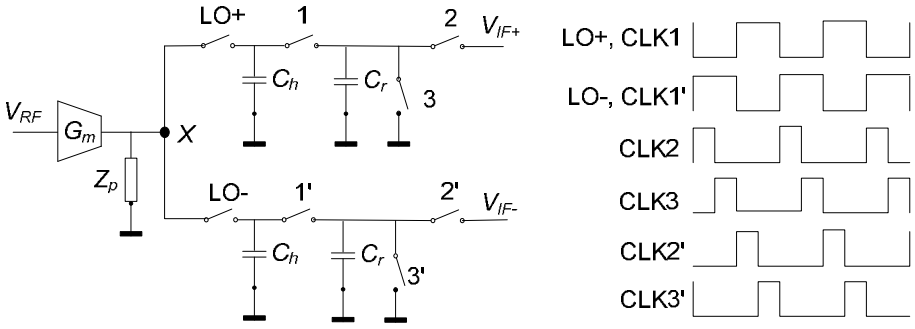

Figure 2.10 An RF charge sampler with an example of clock scheme

(see also (2.16)). This SINC function attenuates the aliasing images of RF sampling to the same level as RF mixing, like a 1st-order low-pass filtering.

The SINC function comes from the convolution in the time domain between the RF signal and a window function, due to the integration of signal current into charge (Section 2.5.3). In the frequency domain the convolution is equivalent to the multiplication between the RF signal and a SINC function. The characteristic of the SINC filter is tunable by the LO frequency and the LO duty cycle, which is generally more flexible than an RF pre-filter. Therefore, charge sampling attracted attentions recently and has already been applied in a few commercial products [15]-[18] [28].

However, this embedded SINC filtering due to integration does not come for free. Charge samplers can deliver a conversion gain which is proportional to the sampling frequency, also due to the integration feature in the time domain. A detailed analysis of this challenge and its potential solutions is going to be presented in the next section.

2.5.3 Frequency-Dependent Conversion Gain of Charge Sampling

This section will discuss a fundamental challenge if using a charge sampler as downconverter for a wideband receiver. A typical RF charge sampler is shown in

Fig. 2.10, consisting of transconductor (G_m), *pseudo*-differential[7] sampler with a pair of history capacitors (C_h) and rotating capacitors (C_r) [15]. C_h is used to integrate the current and store the charge, while C_r is used to read out the charge and to define the gain of the charge sampler. The history capacitance is normally much larger than the rotating capacitance to effectively implement an IIR filter. Impedance Z_p models the finite output impedance of G_m together with all the parasitic impedance at node X.

Switch 1/1' controls the signal path from C_h to C_r. Switch 2/2' controls the signal path from C_r to the next stage. Switch 3/3' controls the reset of C_r. The clock scheme is an example with no decimation, so all the switches are operating at the same frequency with LO, i.e. f_s. However, CLK 1/1', 2/2' and 3/3' can also involve decimation so to operate at an integer-times lower rate of LO+/LO- [15] [27].

In Fig. 2.10, the pseudo-differential sampling paths are driven by LO+ and LO- respectively. The pseudo-differential sampling paths work in an interleaved way, i.e. one path in track mode while the other path in hold mode. During the track mode, both C_h and C_r are connected to the output of G_m via the switches, to attract as much RF current as possible. Thus, G_m always sees a constant load impedance (Z_L) combined of C_h, C_r, and the switch-on resistance.

The following part of this section will focus on the analysis of the conversion gain (CG) of the RF charge sampler, for both ideal case and considering parasitics. The CG here refers specifically to the voltage-to-voltage conversion gain.

a) Conversion Gain of an Ideal Charge Sampler

As a first-order analysis, we assume Z_p is much larger than Z_L, so that Z_p can be neglected. Then the current delivered to C_h and C_r is

$$i_{RF} = G_m \cdot v_{RF} \tag{2.15}$$

In charge sampling, the current is integrated into charge followed by the sampling operation in each period. This integration in the time domain is equivalent to a convolution [31] with a pulse, whose pulse width is $d \cdot T_s$ and pulse height is 1, (T_s: sampling period; d: duty cycle). In the frequency domain, it effectively builds a

[7] We call it "pseudo-differential", due to the same reason as "pseudo-quadrature" introduced in Section 2.5.1, i.e. frequency-dependent phase shift.

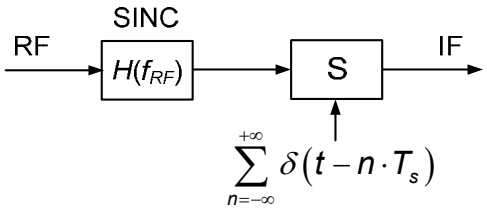

Figure 2.11 Modeling a charge sampler with SINC transfer function

SINC transfer function $H(f_{RF})$ filtering the RF input spectrum before the sampling action (see Fig. 2.11):

$$H\left(f_{RF}\right) = d \cdot T_s \cdot \mathrm{sinc}\left(\pi \cdot f_{RF} \cdot d \cdot T_s\right) = \frac{\sin\left(d \cdot \pi \cdot f_{RF} / f_s\right)}{\pi \cdot f_{RF}} \tag{2.16}$$

To reduce the noise-and-interference aliasing, the sampling frequency should be close to the RF of the wanted signal instead of suing sub-sampling. If using zero-IF sampling, where the sampling frequency $f_s=1/T_s=f_{RF}$, and using 50% duty-cycle LO (d=0.5), we can get

$$H\left(f_{RF} = f_s\right) = \frac{\sin\left(\pi/2\right)}{\pi \cdot f_s} = \frac{1}{\pi \cdot f_s}. \tag{2.17}$$

If we only focus on the desired signal, the sampling operation can be seen as folding signal from RF to IF without affecting its magnitude. Thus, by combining (2.15) and (2.17), the sampled charge data can be described by

$$Q_{in} = i_{RF} \cdot H\left(f_{RF}\right) = v_{RF} \cdot \frac{G_m}{\pi \cdot f_s}. \tag{2.18}$$

Charge samplers in the earlier age [31] didn't use the rotating capacitor C_r. Instead they reset C_h every LO cycle so to define the CG via C_h only[8]. On the other hand, in the modern charge sampler of Fig. 2.10 [15], the combination of C_h and C_r implements an IIR low-pass filter, which makes the overall CG more complicated.

[8] In that case, the down-converted voltage on C_h is well defined by the charge obtained from (2.18) divided by the value of C_h without seeing the memory effect from previous charge samples due to a reset in each LO cycle.

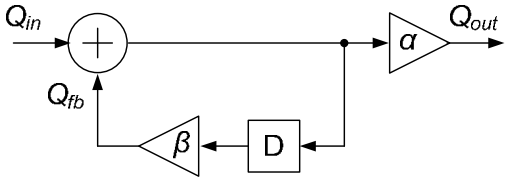

Figure 2.12 An ideal IIR filter model in charge domain

The IIR filtering effect can be understood in charge domain (Fig. 2.12). Q_{in} is the input charge got from (2.18). Q_{out} is the output charge carried by C_r, while Q_{fb} is the feedback charge reserved by C_h. The coefficients α and β can be written as

$$\alpha = \frac{C_r}{C_h + C_r}; \beta = \frac{C_h}{C_h + C_r}. \tag{2.19}$$

From (2.19) we know α=1-β. Then the charge transfer function of the IIR low-pass filter can be derived as

$$Q_{out} = Q_{in} \cdot \frac{\alpha}{1 - \beta \cdot Z^{-1}} = Q_{in} \cdot \frac{1-\beta}{1 - \beta \cdot Z^{-1}}. \tag{2.20}$$

Then the output voltage of IF signal can be written as

$$v_{IF} = \frac{Q_{out}}{C_r} = \frac{Q_{in}}{C_r} \cdot \frac{1-\beta}{1 - \beta \cdot Z^{-1}}. \tag{2.21}$$

Combining (2.18) and (2.21), we have

$$v_{IF} = v_{RF} \cdot \frac{G_m}{\pi \cdot f_s \cdot C_r} \cdot \frac{1-\beta}{1 - \beta \cdot Z^{-1}} \Rightarrow \frac{v_{IF}}{v_{RF}} = \frac{G_m}{\pi \cdot f_s \cdot C_r} \cdot \frac{1-\beta}{1 - \beta \cdot Z^{-1}}. \tag{2.22}$$

The Z-domain term in the above equations determines the response of the IIR filter. If we focus on the signal down-converted from RF to DC after zero-IF sampling, we only need to know the DC response of the IIR filter. Since

$$\frac{1-\beta}{1 - \beta \cdot Z^{-1}} = 1 @ DC, \tag{2.23}$$

we can write (2.22) into

$$\frac{v_{IF}}{v_{RF}} = \frac{1}{\pi} \cdot \frac{G_m}{f_s \cdot C_r}. \tag{2.24}$$

If we consider the pseudo-differential paths, the output signal voltage at DC will be doubled compared to the voltage of a single-ended path. Therefore, the conversion

gain of an ideal RF charge sampler driven by differential LO (LO+/LO-) is

$$CG_{id} = \frac{v_{IF,diff}}{v_{RF}} = \frac{2}{\pi} \cdot \frac{G_m}{f_s \cdot C_r}. \tag{2.25}$$

Equation (2.25) is based on two assumptions: 1) zero-IF sampling, i.e. an LO frequency (f_s) equal to the frequency of the input RF signal (f_{RF}); 2) 50% duty cycle for the LO. If the RF signal after downconversion is not at DC, then the CG should also consider the RF SINC and baseband IIR filtering effect. If the LO duty cycle is not 50%, then the CG coefficient should be different from $2/\pi$. Nevertheless, both effects can be considered via applying (2.16) for the SINC filtering and (2.20) for the IIR filtering characteristic.

It may be wondered, why the CG is only determined by C_r, but not related to C_h. The CG given by (2.25) is proportional to G_m multiplied with $1/(f_s \cdot C_r)$. From Fig. 2.10, we can see that if modeling switched-C_r as an equivalent resistance of $1/(f_s \cdot C_r)$, the CG is indeed determined by the multiplication of G_m and $1/(f_s \cdot C_r)$ while the product of C_h and $1/(f_s \cdot C_r)$ affects the baseband filtering bandwidth. Therefore C_r determines the CG while the ratio of C_h and C_r affects the filtering. The following example may give some insight as well: suppose if C_r=0, which means no charge is moved out from C_h, the signal charge downconverted to DC will always accumulate and the DC voltage at C_h approaches infinity. This trend can be clearly seen from (2.25).

From (2.25), it should be clear that the conversion gain is inversely proportional to f_s, which is equal to f_{RF} for zero-IF sampling. The frequency dependency of conversion gain is due to the integration feature of a charge sampler, so that *the amount of charge integrated in each period depends on the time of integration*. This systematic frequency dependence is undesired for a wideband receiver such as SDR, since both NF and linearity can be strongly dependent on the carrier frequency. As a comparison, for an active mixer[9] with a load resistance R_L, the conversion gain would be $(2/\pi) \cdot G_m \cdot R_L$, which is *not* systematically dependent on f_{RF}.

In [15] and [27], a technique called temporal moving averaging (MA) is introduced

[9] An interesting analogy can be found: an active down-mixer is often loaded by C_L and R_L to form a low-pass filter; while a charge down-sampler is loaded by C_h and an equivalent R emulated by switched-C_r which together form an IIR filter.

which might be a solution. The temporal MA is the temporal integration of N RF-samples, performing a FIR filtering with N all-one coefficients and an N-times decimation (N can be defined as the decimation ratio). The charge accumulation over N samples does result in a larger conversion gain. Ideally, the gain in case of accumulation of N samples is equal to N, so

$$CG_{id,N} = N \cdot \frac{2}{\pi} \cdot \frac{G_m}{f_s \cdot C_r}. \tag{2.26}$$

From (2.26), we can see an N-times increase of input frequency might be compensated by an N-times temporal MA to keep the conversion gain stable.

However, the temporal MA suffers from some problems. Due to the fact that the MA output is read out via C_r at an N-times lower rate, i.e. f_s/N, there is additional aliasing with a fold-over frequency at $f_s/(2N)$. Although the intrinsic FIR filter in a MA operation generates notches to suppress the aliasing of noise and interference, the notch width is limited by N, i.e. a larger N gives a smaller notch width [27]. A narrow notch corresponds to a narrow channel bandwidth that can be protected against aliasing images. Furthermore, circuit imperfections such as the parasitics at node X also limit the achievable notch depth [27]. A limited notch depth corresponds to a limited rejection ratio of aliasing images. Therefore, an RF pre-select filter is often needed to achieve sufficient aliasing suppression around the frequency points of $n\cdot(f_s/N)$ (n=0,1,2,3…, but $n\neq N$), which will limit the flexibility for a SDR receiver.

b) Conversion Gain with Finite Z_p

After some intuition developed via the first-order analysis in the previous part, we will include the effect of Z_p for a second-order analysis in this part. A finite Z_p causes a loss of gain as charge from C_h constantly leaks out through Z_p every LO cycle. Therefore, it is important to understand how a finite Z_p affects the conversion gain.

Z_p has two fundamental effects on the conversion gain of the direct RF charge sampler. One effect is *charge leakage*. Because of the finite impedance (Z_p) to ground at node X, part of the charge stored on C_h may leak away every cycle when switching on. The other effect is *current division*. With this effect, the current flowing onto C_h and C_r is smaller than what got from (2.15). Actually, the effect of

current division can be modeled in two steps. First, all the output current will be integrated to be a sample of charge on C_h. Second, part of this charge sample will leaks away from Z_p to ground.

Thus, both effects of Z_p can be explained with the leakage of charge. The leakage of the remained part of all the previous charge samples on C_h represents one effect. The leakage of the current charge sample represents the other effect. The actual impact of Z_p might be different depending on whether Z_p is capacitive or resistive. The following analysis will discuss these two cases respectively.

Capacitive

If Z_p is capacitive, it can be modeled as a capacitor C_p connected from node X to ground. Both C_p and C_r share the charge with C_h every LO cycle. If the charge on C_p is stored, there will be a charge *crosstalk* between the pseudo-differential paths: in an LO cycle when switching from the positive path driven by LO+ to the negative path driven by LO-, the charge from the positive path that has been stored on C_p will cancel one part of the charge on the negative path, after which another part of the charge from the negative path will be stored on C_p to cancel charge on the positive path in the next LO cycle. Therefore, if we focus on the signal downconverted from RF to DC, the amount of signal charge that is shared by C_p with the charge crosstalk effectively doubles the amount shared by C_p without the charge crosstalk. That means, due to this charge crosstalk, the effective value of C_p is doubled.

To quantify the effect, an IIR filter model including the charge leakage is shown in Fig. 2.13. Q_{in} is the input charge data got from (2.18). Q_{out} is the output charge carried by C_r, Q_{fb} is the feedback charge reserved by C_h, and Q_{leak} is the leakage charge taken by C_p. The coefficients α_1, α_2, and β can be written as

$$\alpha_1 = \frac{C_r}{C_h + C_r + 2C_p}; \alpha_2 = \frac{2C_p}{C_h + C_r + 2C_p}; \beta = \frac{C_h}{C_h + C_r + 2C_p}. \tag{2.27}$$

Note that the effect of C_p is doubled as in (2.27). The charge transfer function of the IIR low-pass filter can be written as

$$Q_{out} = Q_{in} \cdot \frac{\alpha_1}{1 - \beta \cdot Z^{-1}} = Q_{in} \cdot \frac{1-\beta}{1 - \beta \cdot Z^{-1}} \cdot \frac{\alpha_1}{1-\beta} = Q_{in} \cdot \frac{1-\beta}{1 - \beta \cdot Z^{-1}} \cdot \frac{C_r}{C_r + 2C_p}. \tag{2.28}$$

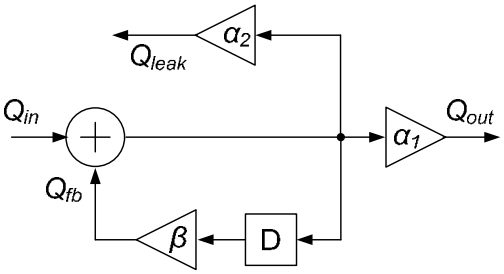

Figure 2.13 An IIR filter model including charge leakage

Therefore, the output voltage of IF signal can be written as

$$v_{IF} = \frac{Q_{out}}{C_r} = \frac{Q_{in}}{C_r + 2C_p} \cdot \frac{1-\beta}{1-\beta \cdot Z^{-1}}. \tag{2.29}$$

Combining (2.18) and (2.29), we have

$$\begin{aligned} v_{IF} &= v_{RF} \cdot \frac{G_m}{\pi \cdot f_s \cdot (C_r + 2C_p)} \cdot \frac{1-\beta}{1-\beta \cdot Z^{-1}} \\ \Rightarrow \frac{v_{IF}}{v_{RF}} &= \frac{G_m}{\pi \cdot f_s \cdot (C_r + 2C_p)} \cdot \frac{1-\beta}{1-\beta \cdot Z^{-1}} \end{aligned}. \tag{2.30}$$

Again, if we focus on the signal downconverted from RF to DC, we can write (2.30) as

$$\frac{v_{IF}}{v_{RF}} = \frac{1}{\pi} \cdot \frac{G_m}{f_s \cdot (C_r + 2C_p)}. \tag{2.31}$$

For the pseudo-differential output paths, the conversion gain will be

$$\frac{v_{IF,diff}}{v_{RF}} = \frac{2}{\pi} \cdot \frac{G_m}{f_s \cdot (C_r + 2C_p)}. \tag{2.32}$$

From (2.32), it should be clear that the conversion gain is, again, inversely proportional to the LO frequency f_s.

Resistive

If Z_p is resistive, it can be modeled as a resistor R_p connected from node X to ground. One step further, R_p can be modeled as an equivalent switched-capacitor resistor, with a capacitor C_{Rp} operating at the same frequency with LO, i.e. f_s. Since R_p only connects to C_h and C_r in either positive or negative path for half of the LO

period, the effective charge leakage is halved comparing to if connecting for a full period. So equivalently $2R_p$ should be counted if modeled as switched-C_{Rp}, and then we have the equivalent capacitor

$$C_{Rp} = \frac{1}{2R_p \cdot f_s}. \tag{2.33}$$

The same IIR model as in Fig. 2.13 can be used for the case of R_p. But different from a real capacitor, the equivalent capacitor C_{Rp} does not cause any charge crosstalk, because R_p can not store charge.

Therefore, the coefficients α_1, α_2, and β for the case of R_p should be written as

$$\alpha_1 = \frac{C_r}{C_h + C_r + C_{R_p}}; \alpha_2 = \frac{C_{R_p}}{C_h + C_r + C_{R_p}}; \beta = \frac{C_h}{C_h + C_r + C_{R_p}}. \tag{2.34}$$

The capacitor C_{Rp} is based on (2.33). Following the same derivation steps as for the case of capacitive Z_p, if we focus on the signal at DC, we can arrive at:

$$\frac{v_{IF}}{v_{RF}} = \frac{1}{\pi} \cdot \frac{G_m}{f_s \cdot (C_r + C_{R_p})} = \frac{1}{\pi} \cdot \frac{G_m}{f_s \cdot (C_r + 0.5/f_s R_p)} = \frac{1}{\pi} \cdot \frac{G_m}{(f_s \cdot C_r + 1/2R_p)}. \tag{2.35}$$

For the pseudo-differential output paths, the conversion gain will be

$$\frac{v_{IF,diff}}{v_{RF}} = \frac{2}{\pi} \cdot \frac{G_m}{(f_s \cdot C_r + 1/2R_p)}. \tag{2.36}$$

It is not directly inversely-proportional to f_s as (2.25) and (2.32) due to the "$1/2R_p$" term, but still can be strongly dependent on f_s.

Both Capacitive and Resistive

Combining (2.32) and (2.36), it can be proved that when both C_p and R_p are present, the non-ideal conversion gain is

$$CG_{nid} = \frac{2}{\pi} \cdot \frac{G_m}{f_s \cdot (C_r + 2C_p) + 1/2R_p}. \tag{2.37}$$

From (2.37), we can see that at low frequency R_p will dominate the parasitic effect and at high frequency C_p will dominate. It can also be seen that the conversion gain is just the same to an active mixer loaded with three equivalent resistors in parallel, i.e. $1/(f_s \cdot C_r)$, $1/(2f_s \cdot C_p)$, and $2R_p$.

With this intuition, for N-times temporal moving average, we can view the RF

charge sampler as a mixer loaded by $1/(f_s \cdot C_r/N)$, $1/(2f_s \cdot C_p)$, and $2R_p$ in parallel. Then the complete conversion gain, considering the parasitic effects and the decimation, can be written as

$$CG_{nid,N} = \frac{2}{\pi} \cdot \frac{G_m}{(f_s/N) \cdot C_r + f_s \cdot 2C_p + 1/(2R_p)}. \tag{2.38}$$

From (2.38), we can see that the conversion gain $CG_{nid,N}$ can be strongly dependent on the sampling frequency, which is equal to the input RF, in the case of zero-IF sampling.

If a charge leakage ratio is defined as

$$\alpha_N = \left(1 + \frac{C_r/N}{2C_p + 1/(2f_s \cdot R_p)}\right)^{-1}, \tag{2.39}$$

then (2.26) and (2.38) can be connected via this ratio:

$$CG_{nid,N} = CG_{id,N} \cdot (1 - \alpha_N). \tag{2.40}$$

Thus, to get closest to the ideal conversion gain, we need to minimize the charge leakage ratio α_N. Attention should also be paid to the decimation ratio N, because a larger N means a larger α_N.

c) Simulations

To verify the above analysis from (2.15) to (2.40), the circuit in Fig. 2.10 has been simulated for zero-IF downconversion, with the following settings: G_m=20mS, C_h=10pF, C_r=500fF. A buffer capacitor C_b=10pF is added at the output of each pseudo-differential path to store the charge, and it will not change the conversion gain at DC. Fig. 2.14 plots CG versus C_p and CG versus R_p with N=1 and f_s=1GHz, which shows the theoretical analysis (2.38) matches very well with the simulation.

From (2.38), we can see that, if we want parasitic impedance has little effect on the conversion gain, the conditions of $C_r >> 2C_p$ and $C_r >> 1/(2f_s \cdot R_p)$ have to be met simultaneously. To verify the parasitic effects versus the sampling frequency, Fig. 2.15 shows the conversion gain versus f_s, comparing the non-ideal case (R_p=10kΩ, C_p=10fF) with the ideal case for both at N=1, i.e. no decimation. From Fig. 2.15, we can see that at low frequency R_p will dominate the parasitic effect and the difference from ideal case can be big while at high frequency C_p tends to dominate but its effect is small since $C_r >> 2C_p$ in this specific example.

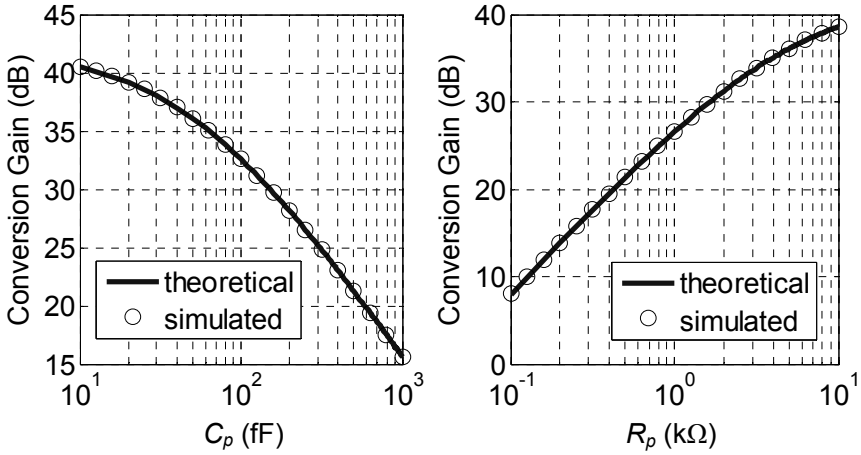

Figure 2.14 Conversion gain of an RF charge sampler with finite Z_p: (a) variable C_p and R_p=∞; (b) variable R_p and C_p=0

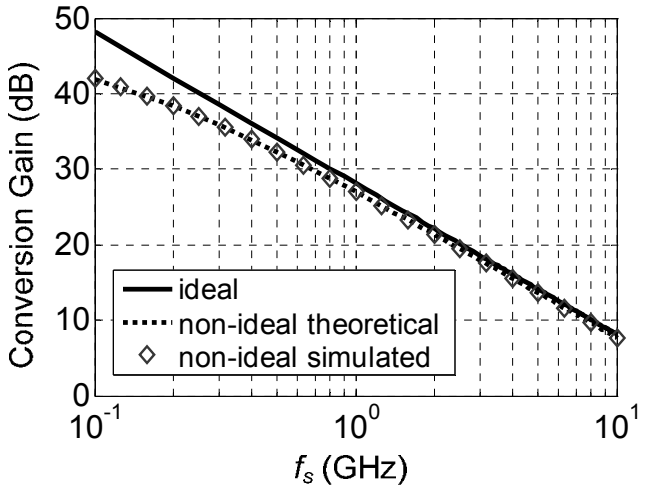

Figure 2.15 Conversion gain versus sampling frequency (f_s) of an RF charge sampler considering parasitics

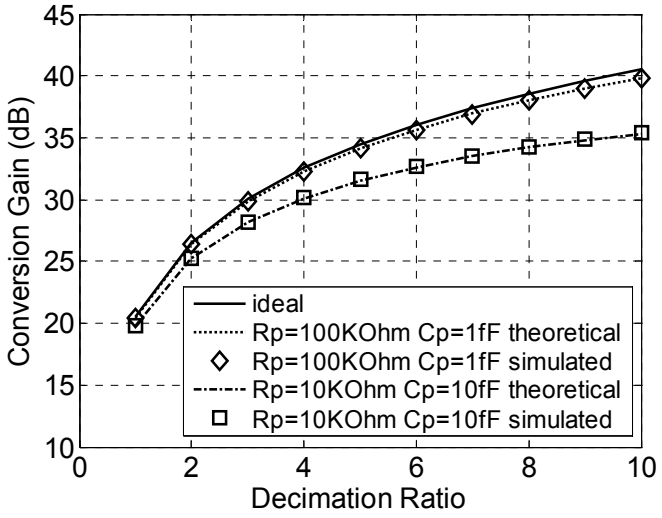

Figure 2.16 Conversion gain versus decimation ratio (N) of an RF charge sampler considering different parasitics

Fig. 2.16 shows the conversion gain versus the decimation ratio (N) at 2.4GHz, for an ideal and a non-ideal RF charge sampler based on (2.26) and (2.38) respectively. Two sets of non-ideal configuration have been simulated, one set is R_p=100kΩ and C_p=1fF, which corresponds to a charge leakage ratio of roughly 1% when N=1; the other set is R_p=10kΩ, and C_p=10fF, which corresponds to a charge leakage ratio of roughly 10% when N=1. Fig. 2.16 shows the simulated results match the theoretical results very well, and N can indeed control the CG.

d) Discussions

A major contributor of R_p can be the output resistance of G_m. For C_p, there might be several contributors, such as the output capacitor of G_m and the parasitic capacitor of switches. When AC coupling capacitor is used between the output of G_m and the sampling switches, its parasitic capacitance can be a major concern.

Consequences

Since the variation of conversion gain will change the NF contribution of later

stages, the finite impedance at node X, i.e. $Z_p=R_p//C_p$, has a direct impact on the receiver *sensitivity*. To achieve a maximum sensitivity, we should maximize Z_p, i.e. minimize C_p and maximize R_p. While for a smaller conversion gain, e.g. in the automatic-gain-control (AGC) application, we might sometimes want a smaller Z_p.

Other than the conversion gain, Z_p can also affect filter characteristics. For instance, if we look at (2.27), the feedback factor β will be lower when C_p is larger and similarly when R_p is smaller based on (2.34). A lower β means a larger -3dB bandwidth of the IIR filter. As another example, if the decimation is performed on the sampling stage, the charge leakage caused by C_p and R_p will reduce the notch depth introduced by the moving-average FIR filter [27]. Therefore, the performance of the aliasing rejection before decimation is degraded. Note that the effects on FIR and IIR filters reflect the impact of Z_p on the receiver *selectivity*.

Overall, the impedance Z_p at node X should be well controlled because of its critical effects on both sensitivity and selectivity.

Potential Solutions

Equation (2.38) shows the frequency dependency in a general sense. But more than that, it also suggests some potential solutions. For example, we can tune the parameters such as G_m, C_r, C_p, R_p, or N to compensate for the dependence of the CG on f_s.

From (2.38), we can see temporal moving average is possible to be used to tune the conversion gain by changing N. However, to make it effective, we have to minimize C_p, while the impact of R_p is not frequency dependent. In the mean time, as mentioned at the end of part a), the limited notch width due to the nature of FIR filter might block its application in some wide-channel communication standards. Therefore, for multi-stand RF-sampling receiver which should be able to accommodate any useful channel bandwidth, at least a selective IIR filter, together with the moving-average FIR filter, is preferred before any decimation.

The other solutions come by adding programmability to the receiver. For example, we can make a bank of transconductors which is programmable via switches for multi-band capability. The whole frequency range of input signal can be divided

into several sub-bands. The activated G_m can be tuned for different sub-bands to keep the conversion gain almost flat. Of course, the conversion gain will still have some variation within each sub-band, but this variation can be acceptable if the covering range of each sub-band has been chosen to be sufficiently small.

Similarly, programmable C_p or C_r can also be used. But programmability means added design complexity. It might also cost extra power and area. Fortunately, this programmability can also be used to play the role of an RF variable-gain amplifier (VGA). So the extra cost of complexity can be reduced, by merging the RF charge sampler and the RF VGA.

Interestingly, as shown by (2.38), since the CG's dependence on R_p is frequency-*independent*, if let R_p dominate the CG definition instead of C_r or C_p, the CG's frequency dependency can be negligible.

Anyhow, to solve the frequency-dependent CG property of charge sampling can take lots of efforts. On the other hand, voltage sampling does not have this undesired property and for this point it seems to be more compatible with wideband applications. More serious noise and interference folding associated with voltage sampling can be alleviated via DT mixing technique (Fig 2.4 (b)) with wideband harmonic rejection that will be introduced in Chapter 3.

2.6 Conclusions

For feasibility and lower power consumption, frequency translation (FT) is highly desired in radio transceivers. This chapter focuses on the fundamental differences among FT techniques for radio receivers, mainly for downconversion. The discussion is carried out in four parts.

1) We showed that downconversion techniques can be classified based on the type of input signal on the one hand, i.e. continuous versus discrete both in time and amplitude, and the downconversion principle on the other, i.e. mixing or sampling. Besides five techniques which are already known, the classification also leads to the definition of a DT-mixing technique that operates on continuous-amplitude but discrete-time samples which can be obtained from CT-to-DT sampling. This

technique will be extended in Chapter 3.

2) To clarify the classification, the fundamental distinctions between the mixing and the sampling principles are discussed in both time and frequency domain. Compared to mixing, sampling always changes the information rate in the time domain but not necessarily results in frequency translation in the frequency domain. It is mathematically shown that CT-to-DT conversion is important for sampling to achieve a well-defined gain.

3) Based on the classification, three receiver architectures are defined: an RF-mixing receiver, an RF-sampling receiver, and an ideal SWR receiver. The ideal SWR receiver is most flexible but not yet feasible for frequencies above a few hundred MHz. The suitability of RF-mixing and RF-sampling receivers for SDR is then discussed, arguing that both can be suitable. While RF sampling can have advantages with respect to the compatibility with the CMOS scaling and the SoC integration, it comes at the cost of extra complexity due to the clock generation/routing and the RF-related baseband processing. With the CMOS scaling and SoC trend, it can be relevant to explore the potential of RF-sampling receivers for SDR applications.

4) Compared to RF mixing, traditional RF-sampling techniques present extra challenges for wideband receivers. Therefore, we identified three challenges: frequency-dependent phase shift, aliasing of noise and interference, and frequency-dependent conversion gain of charge sampling. Their effects are analyzed quantitatively and verified via simulations. The frequency-dependent phase shift is due to the fact that sampling naturally uses delay to approximate phase shift. Voltage sampling seriously suffers from aliasing due to equal-magnitude harmonic sampling tones. Due to integration, charge sampling can have a reduced aliasing effect similar to CT mixing. However, also due to integration, charge sampling presents frequency-dependent conversion gain. A quantitative analysis for an RF charge sampler considering parasitic effects and a certain decimation ratio has been verified. In Chapter 3, we will show that these challenges can be addressed by applying voltage sampling followed by the proposed DT-mixing technique with wideband phase shift and wideband harmonic rejection.

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Chapter 3

Discrete-Time Mixing Receiver for RF-Sampling SDR

The previous chapter compared RF-mixing receivers and RF-sampling receivers, and concluded both can be suitable for software-defined radio but with different advantages and drawbacks. To benefit from RF sampling's advantages such as the compatibility with CMOS scaling and SoC integration, this chapter will explore the potential of RF sampling for SDR applications, by proposing a new frequency translation technique, i.e. discrete-time (DT) mixing [1] [2].

After the introduction in Section 3.1, Section 3.2 presents the DT-mixing concept which is defined after the classification of FT techniques in Section 2.2. It aims to solve the problems of traditional RF sampling for wideband receivers identified in Section 2.5 by its wideband features. To verify the concept, Section 3.3 presents an implementation of DT-mixing downconverter, with 8-times oversampling and 2^{nd}-to-6^{th} harmonic rejection for the 200-to-900MHz RF band. It is fabricated in 65nm CMOS with simulation and measurement results presented in Section 3.4. Conclusions are drawn in Section 3.5 and references are attached in Section 3.6.

3.1 Introduction

RF-sampling receivers have recently drawn both academic [3] [4] and industrial interests [5]-[8]. They sample the signal early in the receiver chain *before or simultaneously with* downconversion, instead of *after* downconversion, as done in conventional RF-mixing receivers. Direct RF sampling provides the potential to move A/D converters (ADC) closer to antenna aiming at an ideal software radio.

Several CMOS ICs have been published in recent years to demonstrate some features suitable for SDR receivers, e.g. [9] and [10], which use wideband front-ends based on RF mixing. On the other hand, traditional RF sampling [3]-[8] is not directly suitable for SDR, as it only provides *narrowband* quadrature demodulation due to the frequency-dependent phase shift and *narrowband*[1] harmonic rejection which can not protect aliasing for wideband applications. For a flexible SDR receiver, any useful channel bandwidth (BW) should be accommodated. Therefore wideband quadrature demodulation is desired to detect wideband signals and to provide wideband image rejection. Also, wideband harmonic rejection is highly desired to prevent aliasing of wideband interference or strong out-of-channel interference.

This chapter describes a discrete-time mixing architecture, featuring *wideband* quadrature demodulation and *wideband*[2] harmonic rejection. We will start with describing the DT-mixing concept and its wideband features. To verify the concept, we present a prototype downconverter in 65nm CMOS targeting at cognitive radio (CR) applications in TV bands [11]. The wideband features of DT mixing can be useful for the CR applications which might use non-contiguous segments of free spectrum distributed over a wide band.

3.2 Discrete-Time Mixing Receiver Concept

Modern CMOS technology offers excellent switches and digital gates whose switching speed is faster in each new process generation. This feature makes it feasible to realize RF sampling, as demonstrated by some narrowband RF-sampling receivers [3]-[8]. Fig. 3.1 (a) shows a traditional RF-sampling receiver, including RF pre-select filter, LNA, RF sampler, a chain of SC circuits for filtering and decimation, IF amplifier (IFA), and ADC. However, as identified in Section 2.5, the traditional RF-sampling receivers face a few challenges to apply to wideband receivers, including 1) the frequency-dependent phase shift, leading to a narrowband quadrature demodulation; 2) the noise and interference folding due to aliasing; 3) frequency-dependent conversion gain of charge sampling.

[1] Both “narrowband” here mean narrow channel bandwidth.
[2] Both “wideband” here mean wide channel bandwidth.

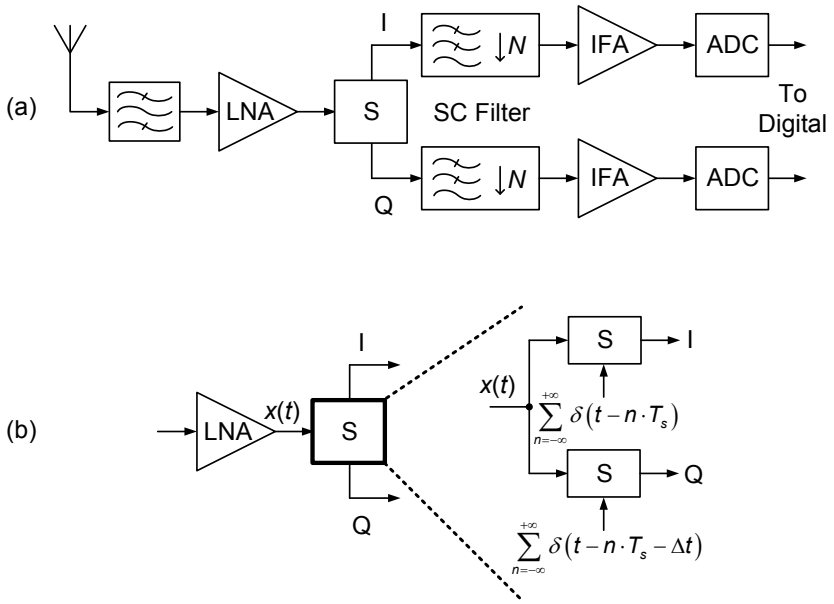

Figure 3.1 (a) Block diagram of a traditional RF-sampling receiver; (b) Traditional RF-sampling receiver using a time delay (Δt) for quadrature demodulation

The last point can be alleviated by applying voltage sampling whose voltage-to-voltage conversion gain is *not* systematically dependent on frequency. For the other two challenges, we will present an architecture-level solution, namely DT mixing, which allows both wideband quadrature demodulation and wideband harmonic rejection to reduce aliasing. Next, we will address these two problems one by one.

3.2.1 Wideband Quadrature Demodulation

A traditional RF-sampling receiver uses a time delay (shift) Δt between two sampling paths, which is also called second-order sampling [12], to approximate a desired phase shift such as 90°, as shown in Fig. 3.1 (b). The resulted phase shift between I and Q paths was given in Section 2.5.1:

$$\Delta\varphi = 2\pi \cdot f_{RF} \cdot \Delta t \,. \tag{3.1}$$

From (3.1) we can see for a fixed Δt, the phase shift $\Delta\varphi$ is dependent on f_{RF}, i.e. frequency-dependent phase shift. An exact $\Delta\varphi$ can only be obtained at specific

frequency points. For instance, an exact 90° is only achieved at frequencies of $\{(k+0.25)/\Delta t\}$ where k is an integer.

Generally Δt can be chosen in such a way that the phase shift is exact for the center frequency (f_c) of the desired RF signal. Rearranging (3.1), we get $\Delta t=\Delta\varphi/(2\pi\cdot f_{RF})$. For a 90° phase shift, i.e. $\Delta\varphi=\pi/2+k\cdot 2\pi$, the following condition holds:

$$\Delta t = \frac{\pi/2 + k\cdot 2\pi}{2\pi f_c} = \frac{k+0.25}{f_c}. \tag{3.2}$$

The absolute phase error at frequency f_{RF} can be described as

$$\left|\varphi_e\right| = \left|2\pi\cdot(f_{RF} - f_c)\cdot\Delta t\right|. \tag{3.3}$$

Larger phase error leads to less accurate quadrature demodulation and degraded image rejection. For SDR applications aimed to accommodate any standards, such a systematic phase error is clearly undesired.

Since the phase error can be predicted as (3.3), it can be corrected using digital compensation [13] at the cost of extra power and complexity. On the other hand, the *phase shift introduced by mixing is theoretically constant over frequency* since the multiplication operation conveys the phase from the LO to the IF signal. We propose to retain this favorable property of mixing in an RF-sampling receiver, via a discrete-time mixing architecture.

The basic DT-mixing downconverter is shown in Fig. 3.2. It consists of a sampler followed by a DT mixer. The sampler running at f_s converts the RF signal centered at f_c from CT to DT domain. In principle, there is no specific requirement on the ratio of f_s/f_c, i.e. subsampling, Nyquist sampling and oversampling are all possible. Assume the signal frequency after sampling is f_0, sampled at a rate of f_s. The relationship $f_0 \leq f_c$ holds, as a result of sampling. In the DT mixer the signal is mixed down from f_0 to f_{IF}, with a DT sine-wave of frequency f_1 and which is also sampled at f_s. The relationship $f_{IF}=|f_0-f_1|$ holds, as a result of down-mixing. Note that downconversion may happen in both the sampler and the DT mixer stages.

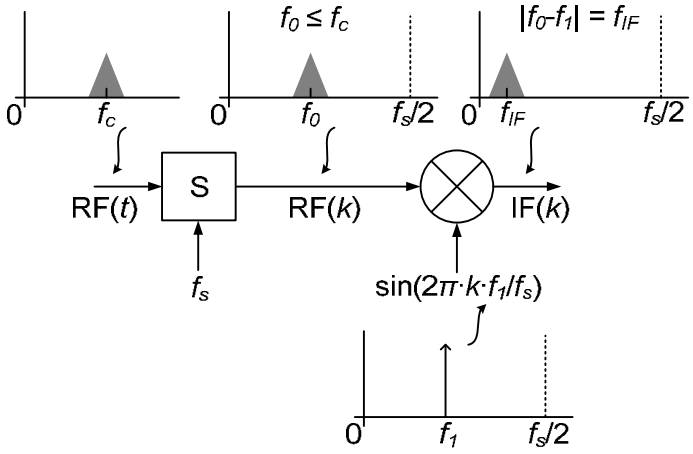

Figure 3.2 A basic discrete-time mixing downconverter

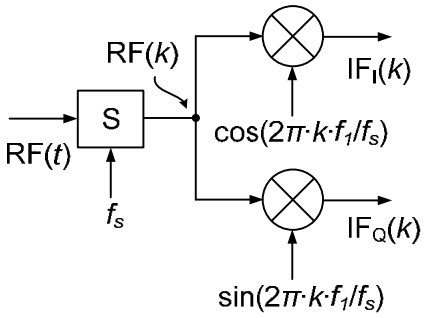

Figure 3.3 A discrete-time (DT) mixing downconverter using I/Q DT mixers

For I/Q DT mixing, as shown in Fig. 3.3, a single sampling stage converts a CT signal into the DT domain, followed by two DT mixers multiplying the sampled signal with a DT cosine-wave and a DT sine-wave respectively. For zero-IF downconversion, the DT cosine or sine frequency f_1 is the same as the signal center frequency f_0 after sampling, i.e. $f_1=f_0$. The DT cosine and sine waves have a 90° phase difference, transferred to IF via multiplication, similar to what a CT mixer does. In contrast to the traditional DT receivers generating a phase difference via a delay, the 90° phase shift by I/Q DT mixing is frequency independent, leading to a true wideband quadrature demodulation and wideband image rejection.

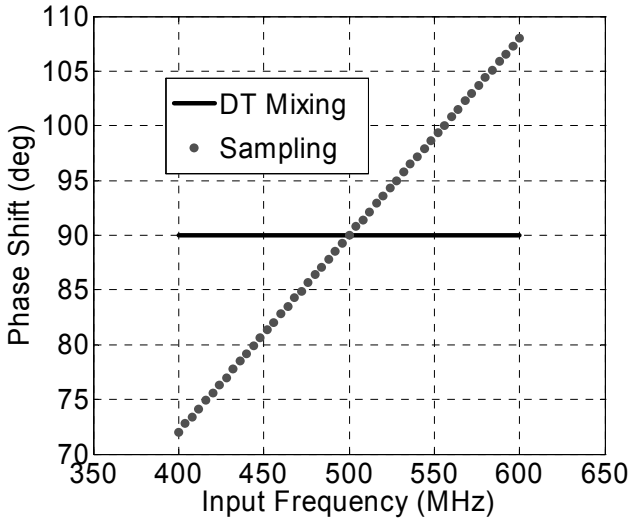

Figure 3.4 Phase shift over input RF at 500MHz LO, generated via quadrature demodulation of DT mixing and traditional RF sampling

We simulated a 500MHz RF signal down-converted to quadrature zero-IF by a traditional RF-sampling receiver and our proposed DT-mixing receiver. The phase shifts for the two approaches are compared in Fig. 3.4, for a 100MHz IF-span, showing almost a 20° error from the traditional approach while maintaining wideband flat 90° via our proposed approach.

3.2.2 Wideband Harmonic Rejection

Another challenge of an RF-sampling receiver is aliasing, e.g. noise and interference around harmonics of the LO are folded to baseband during the sampling process. For narrowband applications, a dedicated RF filter is often used (Fig. 3.1 (a)) so aliasing is not a problem. However, for SDR applications, such a filter may limit the flexibility and therefore undesired. We need to find other solutions to at least relax the requirement on the RF filter.

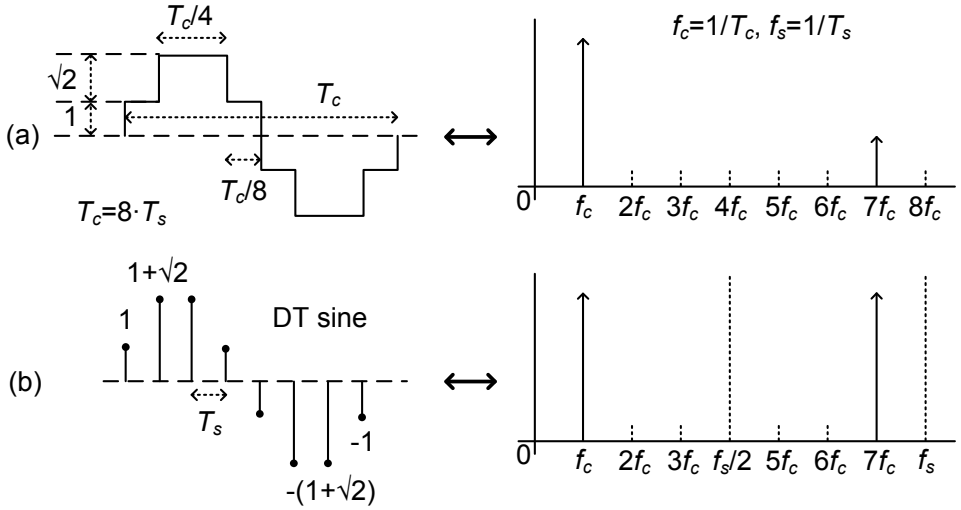

Figure 3.5 Effective LO waveform in one period for 2nd to 6th harmonic rejection and the corresponding spectrum: (a) continuous-time; (b) discrete-time

For CT mixer, it is well-known that all even-order harmonics can be rejected by applying a differential LO. Moreover, in [14], a harmonic-rejection (HR) technique for CT mixers in a transmitter was proposed to suppress some odd-order harmonics. The basic principle of HR is, using a sum of weighted square-wave signals, to build an effective LO that is closer to a sine-wave, so to reduce the amount of harmonics in the effective LO. For example, as shown in Fig. 3.5 (a), an effective LO summed from three time-shifted square-waves with an amplitude ratio of 1:√2:1 is free of the 2nd to 6th harmonics, and only contains the $(8n\pm1)^{th}$ harmonics (n=0, 1, 2…so only 1st, 7th, 9th…).

A similar idea can be applied to the DT mixer to reject sampling aliases. Since the DT sine-wave has the sampling alias located at ($n\cdot f_s\pm f_{IF}$), the higher the sample rate, the less the amount of in-band aliases, for a given RF-filter BW. So *oversampling* ($f_s>2f_{RF}$) is more effective. For zero-IF downconversion, we can choose $f_s=m\cdot f_c$ (m=1, 2, 3…). The remaining harmonics causing aliasing are the $(m\cdot n\pm1)^{th}$, and the first un-wanted harmonic is the $(m\text{-}1)^{th}$. The further-away the first unwanted harmonic, i.e. a larger m, the less requirements on the RF filter. Fig. 3.5 (b) shows an example of the DT sine-wave with m=8, corresponding to Fig. 3.5 (a).

A FIR filter on signal path can also be used to reject sampling aliases by positioning the filter notches at the targeted alias frequencies [15]. However, it is only effective for a limited channel BW due to the limited notch BW intrinsic to any FIR filters. For SDR applications, any useful channel BW should be accommodated, so a good HR ratio over a wide channel BW is important. Wideband HR is also important to reduce the distortion caused by strong out-of-channel interferers. Therefore, a FIR-filter based HR receiver does not suit SDR applications. In contrast, the DT-mixing based HR principle does not have intrinsic channel BW limitation, i.e. presenting wideband HR, just like the HR is also wideband in a CT mixer. The wideband HR will be verified later in Section 3.4.2.

Besides improving signal-to-interference ratio, oversampling and harmonic rejection in a sampling receiver will also improve signal-to-noise ratio (or equivalently NF) since the noise folding is also reduced, in the same way as rejecting interference.

As a summary of this section, we proposed an alternative receiver architecture using RF sampling followed by DT mixing with a sampled cosine or sine wave. It enables wideband quadrature demodulation and wideband harmonic rejection, making RF sampling more suitable for SDR receivers.

3.3 Proof-of-Concept Implementation

To prove the concept of DT mixing, we implemented a prototype receiver to cover 0.2 to 0.9GHz RF range, targeting at the cognitive radio application recently proposed in the TV band [11]. The wideband features of DT mixing can be useful for CR applications which might use non-contiguous segments of free spectrum distributed over a wide band.

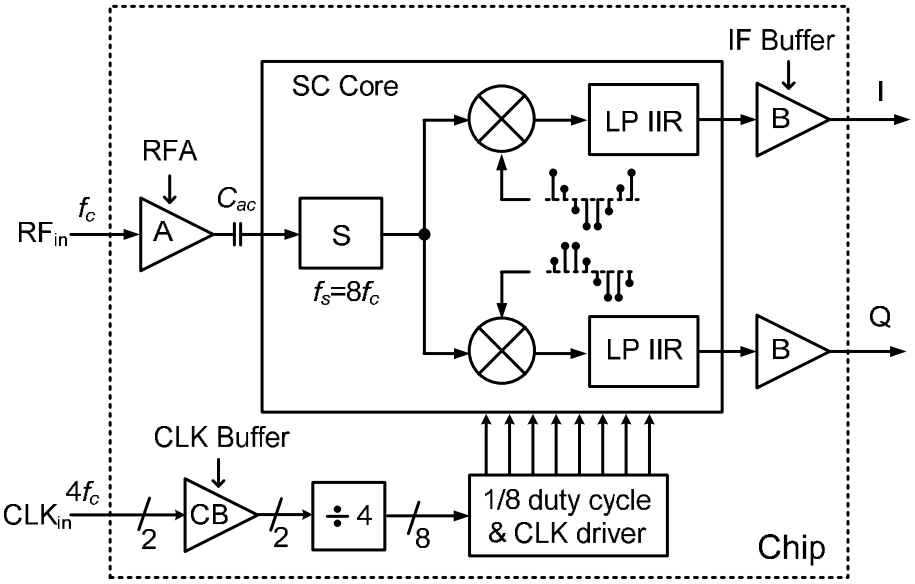

Figure 3.6 Block diagram of the implemented DT-mixing receiver with 8-times oversampling and 2nd-to-6th harmonic rejection

3.3.1 Receiver Architecture

Fig. 3.6 shows the architecture of the receiver. For simplicity it is shown single-ended, but in fact all circuits are implemented differentially. Please note that an LNA is not included in this work. An inverter-based RF voltage amplifier ("RFA") delivering 6dB gain drives a passive switched-capacitor (SC) core consisting of three stages. The first stage is effectively an oversampler ("S"), with a sample rate 8 times the input center frequency, i.e. f_s=8f_c, for 2nd to 6th harmonic rejection (Fig. 3.5 (b)). The second stage consists of I/Q DT mixers for downconversion to zero-IF. The third stage is a low-pass IIR filter ("LP IIR"), removing undesired interference and serving as an anti-aliasing filter before decimation to lower sample rate. For measurement purpose, the quadrature IF outputs are buffered via source-followers ("B") with a voltage gain of 1. An on-chip clock generator, consisting of clock buffer ("CB"), divide-by-4, and 1/8-duty-cycle driver, controls the SC core.

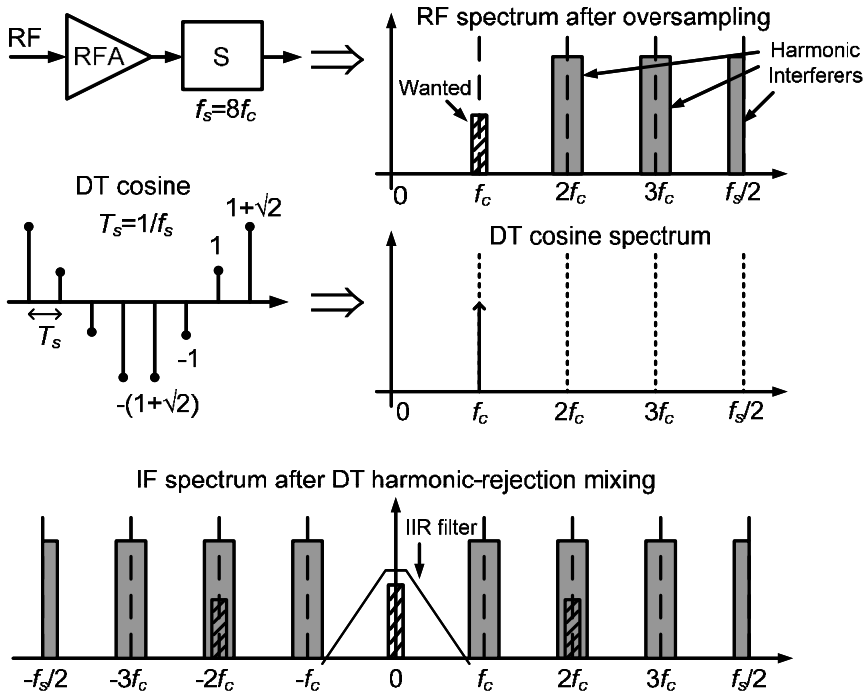

Figure 3.7 Mechanism of the discrete-time (DT) harmonic-rejection mixing

Fig. 3.7 illustrates how this DT HR mixer works. Two I/Q DT mixers shown in Fig. 3.6 multiply the incoming samples with a DT cosine and sine wave, i.e. weighting ratio of 1:(1+√2) if cosine and sine waves with frequency f_c are sampled at $8f_c$. Since the DT clock is periodic, its spectrum only contains an impulse at f_c within the DC to $f_s/2$ range. Multiplying the oversampled signal with the DT clock will down-convert the signal from f_c to DC without folding harmonics at $2f_c$, $3f_c$, and $4f_c$. However, the harmonics already folded to f_c during the sampling process cannot be differentiated from the wanted signal. Since $f_s=8f_c$, during sampling, the 7th harmonic folds to f_c, and the 5th harmonic folds to $3f_c$, etc. Therefore, the un-suppressed RF harmonics are the 7th, 9th, 15th, 17th etc, but the close-by 3rd and 5th and all even-order harmonics are removed. Mixing with the DT cosine and sine waves also leads to a true frequency-independent 90° phase shift for wideband quadrature demodulation.

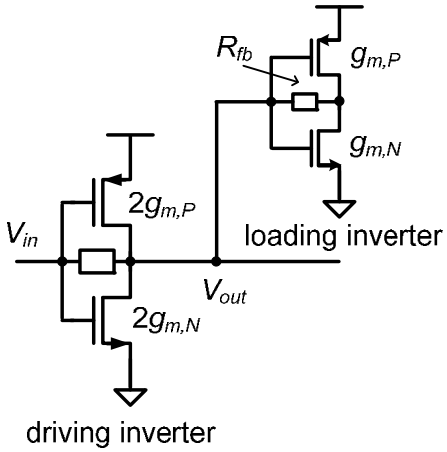

Figure 3.8 The schematic of RFA based on inverters

To better understand the implementation, a more detailed description for some of the key blocks will follow.

3.3.2 Circuit Implementation

1) RFA

The RFA is shown in Fig. 3.8, consisting of two inverters, and two such copies of RFA are employed for a differential operation. For a gain of two, the driving inverter, with a large feedback resistor for automatic DC bias, is twice the size of the loading inverter, with a small feedback resistor R_{fb} around $2/(g_{m,P}+g_{m,N})$ to partially compensate the 3rd-order nonlinearity, which will be analyzed in Chapter 4. Nominally, the driving inverter draws 1mA with a total g_m of 20mS and the loading inverter takes 0.5mA with 10mS. Please note that the RFA presented here is not a complete LNA and its input is not matched to 50Ω but targeted at high impedance. It mainly serves as a driver for the follow-up SC circuitry.

2) SC Core

Fig. 3.9 (a) shows the SC core circuitry. In total, there are 16 sampling units (SU) implemented, but for clarity only half of the differential system is shown. An AC

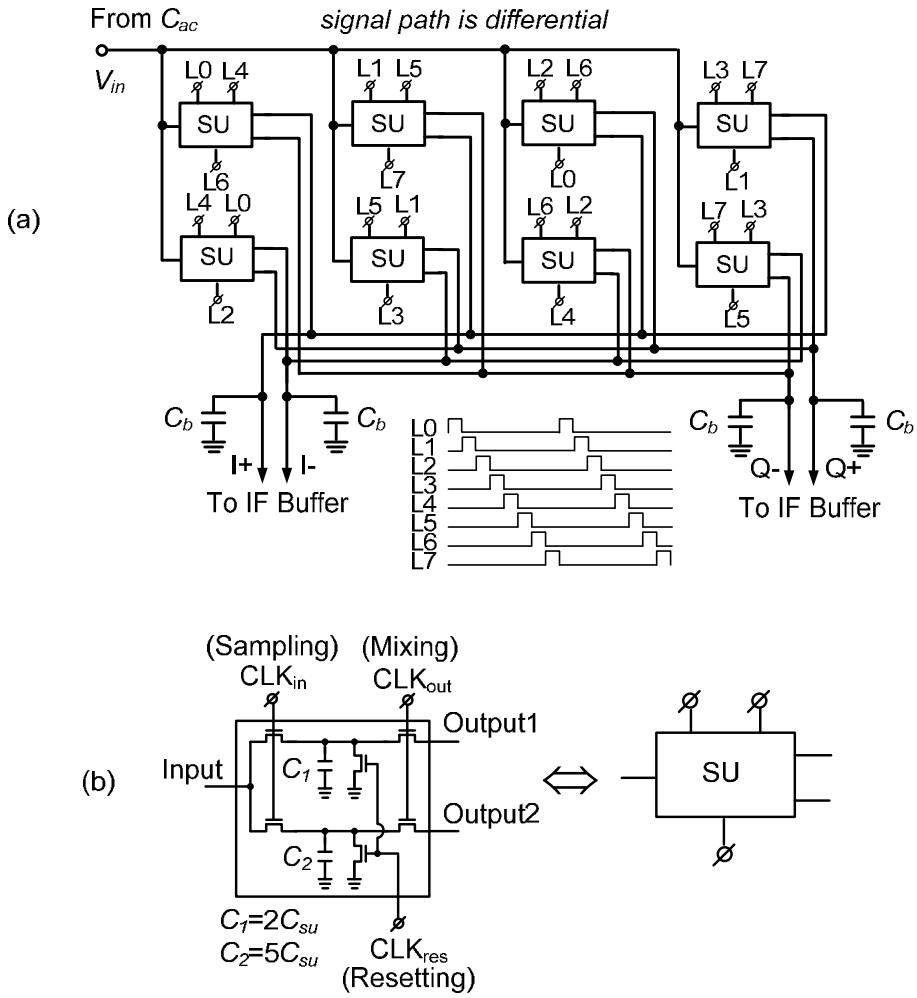

Figure 3.9 (a) Switched-capacitor (SC) core circuitry with 8-phase clock waveform; (b) Transistor-level construction of a sampling unit (SU)

coupling capacitor (C_{ac}=2.5pF) is used between RFA and the SC core input as shown in Fig. 3.6, so that the sampling units can work at a common-mode (CM) level close to ground (GND) while the clock (L0-L7) swings from GND to VDD to minimize the switch-on resistance of NMOS switches. Four buffer capacitors C_b (18pF each) are used to store the signal charge for quadrature outputs, built via NMOS accumulation capacitors.

Fig. 3.9 (b) shows a SU in detail. In each SU, there are two weighted sampling capacitors to map the 1:(1+√2) weighted pulse amplitudes needed for a DT cosine or sine wave. In previous work, weighted amplifiers were used [9] [14] [15]. We exploit weighted capacitors which can have superior matching properties. To make a non-integer 1:(1+√2) ratio reliable in layout is difficult. We used unit capacitors with value C_{su} in a 2:5 ratio as approximation (C_1=2C_{su}=160fF, C_2=5C_{su}=400fF), built via metal-oxide-metal (MOM) capacitors. In each sampling unit, there are three pairs of switches controlled by three different clock phases, and in each pair the two switches also share the same weighting factor as the two capacitors. The switch pair for sampling ("sampling switches") is controlled by CLK_{in}, and the switch pair for DT mixing ("mixing switches") is controlled by CLK_{out}. The third switch pair for reset ("reset switches") controlled by CLK_{res} defines the CM level of all switches to GND.

The working procedure of a sampling unit is as follows, taking the upper left unit in Fig. 3.9 (a) as an example:

1) at clock phase L0 (CLK_{in} high), the sampling switches take the same RF voltage to two sampling capacitors C_1 and C_2;

2) then the charge will be kept for three idle phases, and at phase L4 (CLK_{out} high) the two charge samples will be transferred via the "mixing switches" to two buffer capacitors C_b, one in I path (I+ side) and the other in Q path (Q- side);

3) waiting for another idle phase, in phase L6 (CLK_{res} high) the reset switches clean up the sampling capacitors C_1 and C_2;

4) and after one more idle phase, the whole procedure repeats from phase L0.

The other 7 units experience the same pattern of activity but shifted in time. By inserting some idle phases between each operation (sampling, mixing, or reset), we can guarantee the three switching operations do not disturb each other.

Next we will describe each functional blocks, i.e. the sampler, the DT mixer, and the IIR filter, in the SC core of Fig. 3.6.

a) Sampler

We aim for a voltage sampling downconverter, which suffers from severe noise

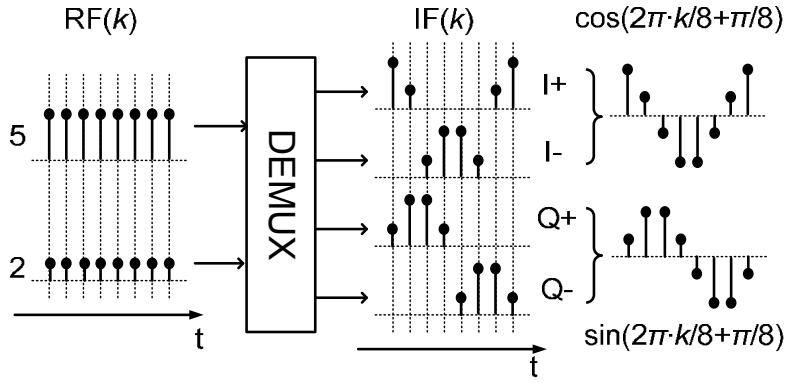

Figure 3.10 To implement discrete-time mixing via de-multiplexing

folding. Oversampling can reduce the noise folding and hence improve NF. The oversampling function is implemented via a time-interleaved sampling structure. Eight interleaved sampling units are controlled by 8-phase non-overlapping clocks with 1/8 duty cycle, as shown in Fig. 3.9 (a). Each of the 8-phase clocks gives a sample rate of f_c, and altogether an effective sample rate of $8f_c$ is achieved. Using time-interleaved sampling to achieve oversampling, there is no extra cost on clock speed compared to other HR systems [9] [14] [15], where multiphase clocks are also employed.

b) DT Mixer

The DT mixing is implemented in the charge domain, via a systematic combination of the mixing switches from all sampling units to transfer the charge samples from the sampling capacitors (C_1, C_2) to the buffer capacitors (C_b). Effectively the DT mixing is realized via de-multiplexing as shown in Fig. 3.10. The oversampled charge data stream RF(k) goes through the switching network controlled by CLK_{out} in Fig. 3.9 (b) and becomes IF(k). For illustration, Fig. 3.10 actually shows an example with a DC input RF(k) which is up-converted to become a quadrature DT sinusoidal output IF(k). But the same principle applies to downconversion.

Changing the initial phase of the DT cosine and sine, the resulting LO waveform can be different, leading to a different ratio among sampling capacitors. As shown

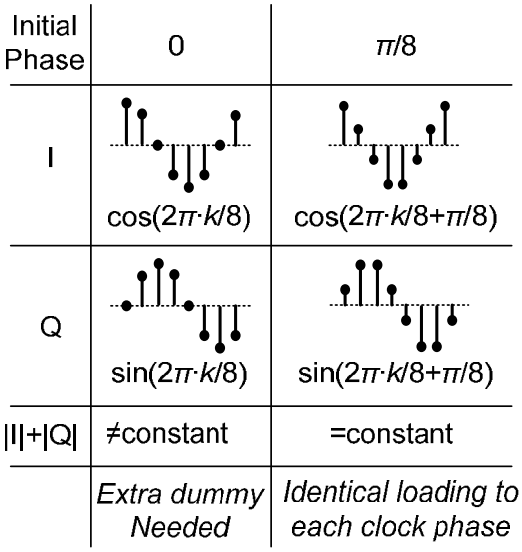

Figure 3.11 Choosing initial phases of DT cosine and sine: why π/8

in Fig. 3.11, by choosing the initial phase to be $\pi/8$, we have

$$\left|\cos(2\pi \cdot k/8+\pi/8)\right|+\left|\sin(2\pi \cdot k/8+\pi/8)\right| = \text{constant}. \tag{3.4}$$

This choice guarantees the identical loading for all clock phases without extra dummy needed.

Conversion gain (CG) is an important property of a mixer. A general DT mixer model for calculating the CG is given in Fig. 3.12, where the mixing is modeled in the charge domain. The figure shows the whole chain of the SC core, but we only derive CG of the DT mixer (in the dashed-line box) while the voltage gain of an ideal voltage sampler and an IIR filter is known to be 1.

An equivalent capacitor C_{in} at the input of the DT mixer converts voltage into charge, an equivalent capacitor C_{out} at the output converts charge back into voltage. The voltage gain is proportional to their ratio C_{in}/C_{out} due to charge conservation from input to output. Please note that the "resetting" operation in a sampling unit (Fig. 3.9 (b)) does not affect the charge conservation principle here since it occurs after the "mixing" operation. The charge that is erased by "resetting" is the residue charge after the IIR operation.

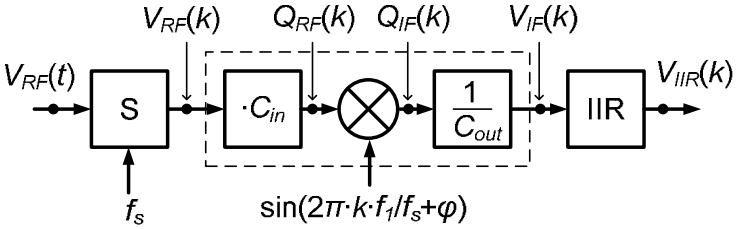

Figure 3.12 Block diagram of the SC core using
a charge-domain model for the DT mixer (in the dashed-line box)

Multiplying with a DT sine-wave $\sin(2\pi k \cdot f_1/f_s+\varphi)$ with an amplitude of 1, the loss is 0.5 since the output signal amplitude at the difference frequency is halved compared to the input. Taking this into account, the voltage CG of a DT mixer can be expressed as

$$CG = \frac{V_{IF,k}}{V_{RF,k}} = 0.5\frac{C_{in}}{C_{out}}, \tag{3.5}$$

where $V_{IF,k}$ and $V_{RF,k}$ represent the amplitude of the IF data $V_{IF}(k)$ and the sampled RF data $V_{RF}(k)$ respectively. To develop some insight, we may compare (3.5) to the voltage CG in a CT current-commutating mixer, where a transconductor g_m or a resistor R_{in} can be used for voltage-to-current conversion, and a load resistor R_L can be used for current-to-voltage conversion. The role of g_m or $1/R_{in}$ is like the role of C_{in} here for voltage-to-charge conversion, and the role of R_L is like the role of $1/C_{out}$ here for charge-to-voltage conversion.

The value of C_{in} and C_{out} in (3.5) depends on the specific implementation. But in general, C_{in} and C_{out} are defined by the sampling capacitor together with the function before and after the DT mixer respectively.

First we derive C_{out}. In our prototype shown in Fig. 3.6, the DT mixer is followed by an IIR filter, thus C_{out} is the same as the equivalent capacitor seen by the IIR filter, i.e. $C_{out}=C_{IIR}\approx(C_1+C_2)/2$ as will be derived following (3.8).

Now we derive C_{in}. Note that the amplitude of the DT sine-wave in Fig. 3.5 (b) is $\sqrt{(4+2\sqrt{2})}$. Assume p_1 and p_2 are the weighting factors in a DT sine-wave whose amplitude is 1 (so $p_1\leq 1$ and $p_2\leq 1$). Since we use the sampling capacitors to realize

these weighting factors, we need C_1:C_2=p_1:p_2. In our prototype, p_1=sin(π/8)=0.38 and p_2=sin(3π/8)=0.92, so that p_1:p_2≈2:5=C_1:C_2. Since a CG is about amplitude, we have C_{in}:C_1:C_2=1:p_1:p_2, i.e. C_{in}/1=C_1/p_1=C_2/p_2.

Substituting C_{in} and C_{out} into (3.5), the CG can be derived as

$$CG = 0.5\frac{C_{in}}{C_{out}} = 0.5\frac{C_1 / p_1}{C_{IIR}} \approx \frac{0.5C_1}{(C_1 + C_2)/2} \cdot \frac{1}{p_1} = \frac{1}{p_1 + p_2}. \tag{3.6}$$

So for our prototype, CG=1/(p_1+p_2)=0.77.

In general, for different oversampling ratio, the CG of a DT mixer can be written as

$$CG = 0.5\frac{C_{in}}{C_{out}} = 0.5\frac{C_1 / p_1}{C_{IIR}} \approx \frac{0.5C_1}{\frac{1}{n}\sum_{i=1}^{n} C_i} \cdot \frac{1}{p_1} = \frac{n/2}{\sum_{i=1}^{n} |p_i|} = \frac{1}{2}\left(\sum_{i=1}^{n} |p_i| \Big/ n\right)^{-1}. \tag{3.7}$$

In (3.7), the "n" is the ratio of the sampling frequency to the DT sine-wave frequency (n=f_s/f_1), so that n/2 is the oversampling ratio. Put in another way, the "n" is the total number of discrete points in one period of the DT sine-wave, with each discrete point representing a weighting factor. The "p_i" is the value of one of the weighting factors in the DT sine-wave (i=1, 2, …, n). There is a "1/2" factor in (3.7) since the output signal amplitude at the difference frequency is halved compared to the input, just like for a CT mixer. The periodic DT sine-wave can be described by a vector p=[p_1,p_2, …, p_n]. For example, in Fig. 3.11, for the DT sine-wave with an initial phase of π/8, its n=8 and its p_i=sin[2π·(i-1)/8+π/8], i.e. p=[0.38, 0.92, 0.92, 0.38, -0.38, -0.92, -0.92, -0.38]. According to (3.7), the CG for such a DT mixer is 0.77.

To verify the CG, we rebuild and simulate the schematic of Fig. 3.9 (a) using ideal switches and capacitors to eliminate parasitic effects which are not considered in (3.7) and without applying RFA and C_{ac}. The result of -2.3dB fits exactly what we derived above, i.e. 0.77. The overall gain of the receiver should consider the cascaded gain of RFA (6dB), voltage sampler (0dB), DT mixer (-2.3dB), IIR filter (0dB), and IF buffer (0dB), which is then equal to 6-2.3=3.7dB, without considering the 2nd-order effects such as parasitic capacitance.

The maximum achievable CG of a DT mixer is 1, the same as an ideal voltage sampler. An example of the DT mixer achieving a CG=1 is a quadrature DT mixer

using a DT cosine-wave LO [1 0 -1 0] and a DT sine-wave LO [0 1 0 -1]. Fitting into (3.7) with n=4 and p=[0, 1, 0, -1], we get CG=1.

c) IIR Filter

The charge sharing operation, between the sampling and the buffer capacitors, implements a low-pass IIR filter [5] [16]. The voltage transfer function of this IIR filter can be written as

$$H_{IIR}(Z)=\frac{1-\beta}{1-\beta Z^{-1}};\left\{\beta\approx\frac{1}{2}\left(\frac{C_b}{C_b+C_1}+\frac{C_b}{C_b+C_2}\right)\right\}. \tag{3.8}$$

The effective factor β is an average of these two charge transfer functions F_1=C_b/(C_b+C_1) and F_2=C_b/(C_b+C_2). Equivalently, β can be written as C_b/(C_b+C_{IIR}) and the IIR filter sees an effective sampling capacitor C_{IIR}≈(C_1+C_2)/2, if C_1<<C_b and C_2<<C_b. An advantage of the IIR filter is that the filter characteristic is determined by the capacitor ratios but not by their absolute values.

According to (3.8), the IIR filter has a voltage gain of 1 at DC. As an intrinsic property of DT filters, its BW scales with the sample rate f_s and the -3dB BW is determined by f_s and β. To accommodate the 5 to 8MHz channel spacing used in the TV band, the -3dB BW of this IIR filter is designed to be roughly 10MHz when f_c=0.5GHz (or equivalently f_s=4GHz), which is around the middle of the 0.2G-0.9GHz band. In simulation, the -3dB BW is 4.4MHz at 0.2GHz LO and 16.9MHz at 0.9GHz LO. Normally an IF filter BW that scales with f_s is undesired. But this effect can be compensated via a bank of selectable C_b values to adapt β to different f_s [6] [8].

Besides implementing the IIR filter, the charge sharing operation also shifts the amplitude ratio from C_1:C_2=2:5, depending on the charge transfer functions F_1 and F_2. Considering C_b=18pF, C_1=160fF, and C_2=400fF, the effective amplitude ratio is

$$\left(C_1\cdot F_1\right):\left(C_2\cdot F_2\right)=\left(C_1\cdot\frac{C_b}{C_b+C_1}\right):\left(C_2\cdot\frac{C_b}{C_b+C_2}\right)\approx 1:2.467\,. \tag{3.9}$$

Compared to the desired 1:(1+√2) ratio, the gain error is reduced from 3.6% (2:5 ratio) to 2.2% (1:2.467).

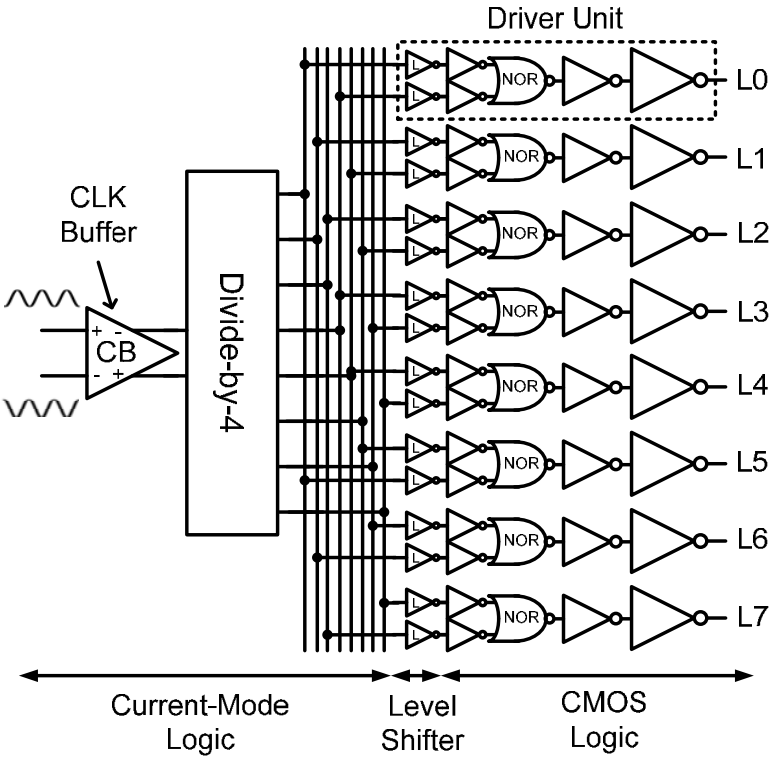

Figure 3.13 Block diagram of the 8-phase clock generator

To reduce the sample rate operated by ADC, the outputs of IIR filter can be decimated, e.g. via a moving average, to a lower sample rate and the next stages can use further DT signal processing, e.g. FIR/IIR filter and decimation [5]-[8].

3) 8-Phase Clock Generator

We need 8-phase clocks to drive the SC core described above. Such a clock generator is shown in Fig. 3.13. It can be partitioned into three parts, namely a high-frequency current-mode logic (CML) part, a level shifter, and a CMOS logic part. The CMOS logic works with full-swing signals while the CML does not, and the level shifter bridges the gap.

The input receives external differential clocks at frequency $4f_c$. An NMOS CML

buffer helps recover the clock steepness and reject possible common-mode interference. This buffer drives a divide-by-4 circuit consisting of four NMOS CML latches to generate 50%-duty-cycle 8-phase clocks at frequency f_c. The CML is chosen for its fully differential operation which has less effect and more immunity to the voltage supply than its CMOS counterpart.

The following stages are split into 8 paths each with a tapered driver unit. Each driver unit consists of level shifters, inverters and NOR gates to generate a 1/8-duty-cycle full-swing clock. The level shifter is simply implemented by an inverter with stronger driving capability in PMOS than in NMOS. CMOS logic is necessary at the final stages since full-swing clocks can improve both noise and linearity of the sampling circuitry via minimizing the switch-on resistance.

3.4 Experimental Results

Fig. 3.14 shows the micrograph of the chip fabricated in a baseline 65nm CMOS process. The active area of the chip is about 0.4mm^2, most of which is occupied by capacitors (C_{ac}, C_{su} and C_b) and signal/clock distribution networks. The chip is packaged in a 32-pin Heat-sink Very-thin Quad Flat-pack No-leads (HVQFN) package and measured on PCB. Since the RFA input is the gate of inverter, a 100Ω SMD resistor for impedance matching is soldered on PCB, close to the package and across the differential RF input traces. Both the receiver inputs and the clock inputs are differential and wideband hybrids (balun) were used to interface to single-ended 50Ω measurement equipment. The IF-output voltage is sensed by a differential active probe that performs differential to single-ended conversion and impedance conversion to 50Ω. The characteristics of all components and cables for testing are de-embedded from the results.

3.4.1 Conversion Gain and Noise Figure

Fig. 3.15 shows the simulated and measured conversion gain (CG) over the 0.2 to 0.9GHz RF band. The results are obtained at 1MHz IF, well within the -3dB IF BW for the whole band. The simulation was carried out on schematic level. The trend of the measured gain fits well with the simulated gain. The CG drops by about 3dB from 0.2 to 0.9GHz, indicating the -3dB RF BW. Analyses and

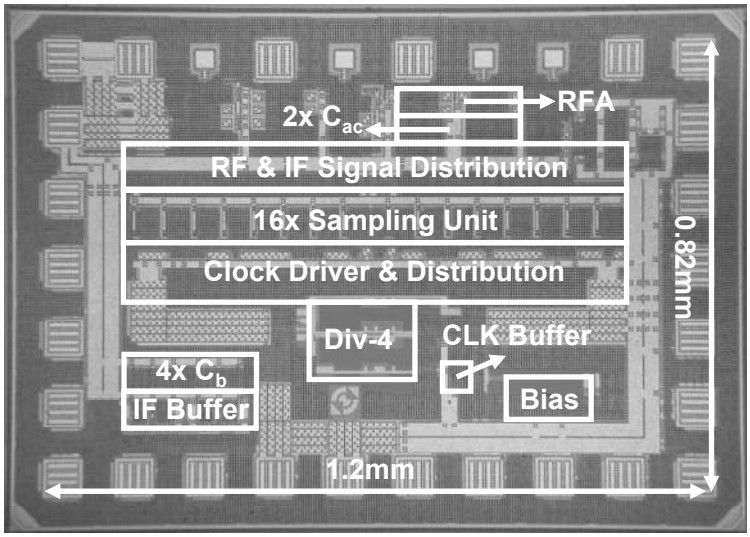

Figure 3.14 Micrograph of the chip fabricated in 65nm CMOS with key blocks indicated

simulations indicate that this strong low-pass filtering behavior is mainly due to the parasitic capacitance associated with the AC coupling capacitor C_{ac}. To improve the RF BW, the AC coupling capacitor can be moved from the signal path to the clock path, as done in Chapter 5. In layout, long interconnecting wires between the AC coupling capacitor and the sampling units, as shown in Fig. 3.14, introduce extra parasitic resistance and capacitance. Also the loss of a few centimeter PCB traces for the RF inputs was not de-embedded. These are the major causes of the gap between the simulated and measured CG.

Fig. 3.15 also presents the simulated and measured DSB NF, both referred to the matched 50Ω source noise. Two curves show similar trend but the measured NF is about 3~4dB worse, due to the degraded gain and the extra noise contributed by the wiring resistance for RF signal distribution (Fig. 3.14). Simulation shows the SC core contributes most noise. Theoretically larger gain should bring lower NF, but Fig. 3.15 shows an opposite trend. In fact, more noise folding at a lower sampling frequency (f_s) raises the NF, even with a higher gain, because: 1) at lower f_s the folding of switch noise is more, assuming a fixed RC time constant; 2) at lower f_s

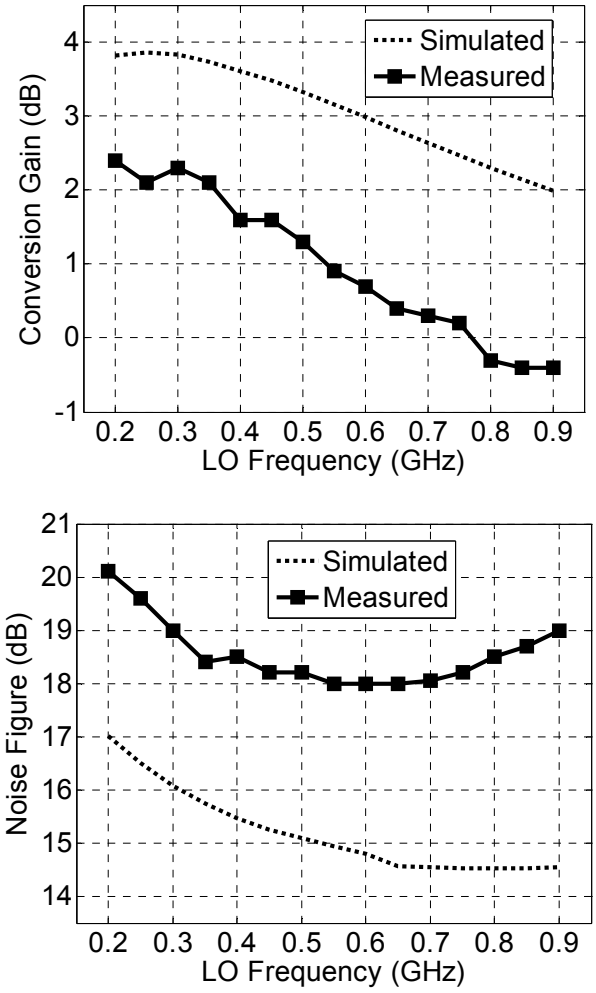

Figure 3.15 Simulated and measured (on PCB)
conversion gain and DSB NF versus LO frequency (IF=1MHz)

the folding of source noise and RFA noise is more due to the limited RF BW as indicated by the CG. Simulation shows the RFA 1/*f* noise has a negligible effect to the NF rise at low band. The measured NF also rises when RF is close to the upper-side limit, where the clock swing is insufficient to fully turn on the switches. As a result, less signal can pass through to IF and also the switches become noisier, so SNR is degraded at the output.

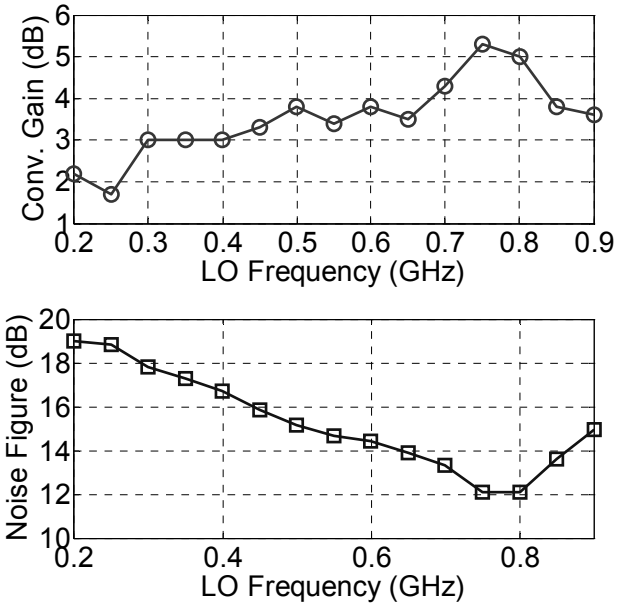

Figure 3.16 Measured (on wafer) conversion gain and DSB NF versus LO frequency (IF=1MHz)

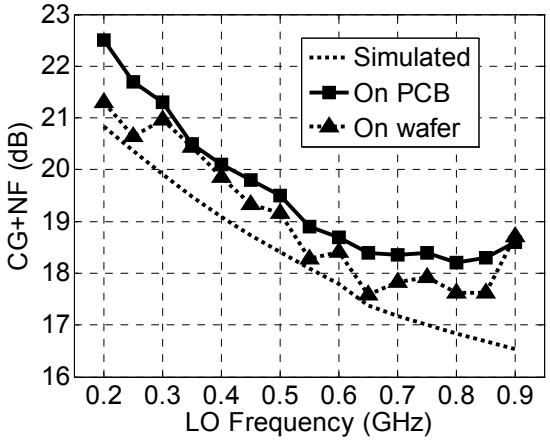

Figure 3.17 Normalized output noise (CG+NF) versus LO frequency: comparing simulation and measurements based on PCB and wafer probing

The CG and DSB NF in [1][3] were measured on wafer via probing, which showed a different trend (see Fig. 3.16). It's very likely due to the different way of installing the off-chip matching resistors. During wafer probing, two 50Ω resistors for input matching were screwed on top of the probe and thus these 50Ω resistors are further away from the chip (~4cm) and this will introduce a transmission-line effect leading to the trend shown in Fig. 3.16, as being verified by simulations. Nevertheless, since the noise from the chip is much larger than the noise from the source as indicated by the large NF, we may compare the normalized output noise (Fig. 3.17), via the sum of CG and NF in dB, which can get rid of the transmission-line effect and indicates mainly the circuit-generated noise at its output. Then three cases, i.e. simulated, measured on PCB and measured on wafer, show a similar trend and their discrepancy is within 1.5dB.

Compared to other voltage sampling downconverters, this work shows a superior NF, thanks to the reduced noise folding by employing oversampling and harmonic rejection. Even the measured worst-case NF (20dB) is still 20dB better than [3] and is better than all voltage sampling mixers discussed in [4].

3.4.2 Harmonic Rejection

Fig. 3.18 compares the HR ratio using two different techniques to reject harmonics: DT mixing and conventional FIR filtering [15]. As predicted by theory, the HR ratio of a sampling downconverter using FIR filtering drops significantly over the channel (simulation), while the proposed DT mixing architecture gives wideband HR without channel BW limitation (both simulation and measurement). For DT mixing, the trend of measured results (one typical sample) fits well with the simulated results. However, phase and amplitude mismatches, which are not included in both simulated curves, degrade the HR ratio in measurement.

Fig. 3.19 shows the measured HR ratio over the RF band of 10 samples. The worst case 3^{rd} and 5^{th} HR ratios are around 25dB and typically they are between 35dB and 45dB. To investigate whether phase or amplitude error is dominating, we did simulations for three configurations: only amplitude error, only phase error, and both. The results are shown in Fig. 3.20, for 2^{nd} to 6^{th} harmonics of a 0.35GHz LO.

[3] The NF shown in [1] should be DSB NF instead of SSB NF.

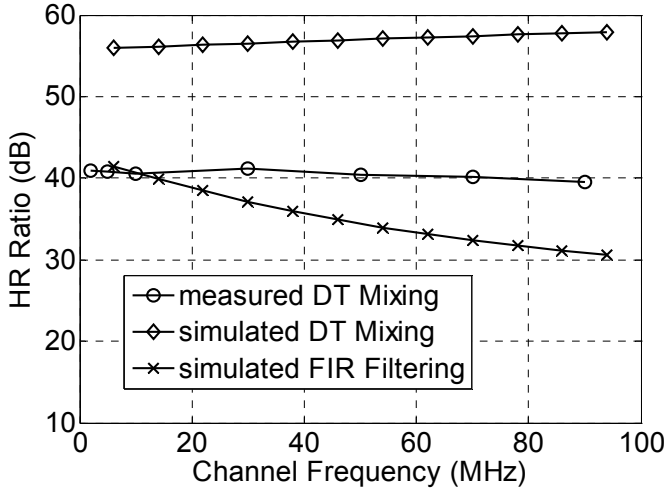

Figure 3.18 Simulated (no mismatch) and measured (a typical sample with mismatch) 3rd-order harmonic-rejection (HR) ratio versus channel frequency (LO@0.5GHz) [measured on wafer]

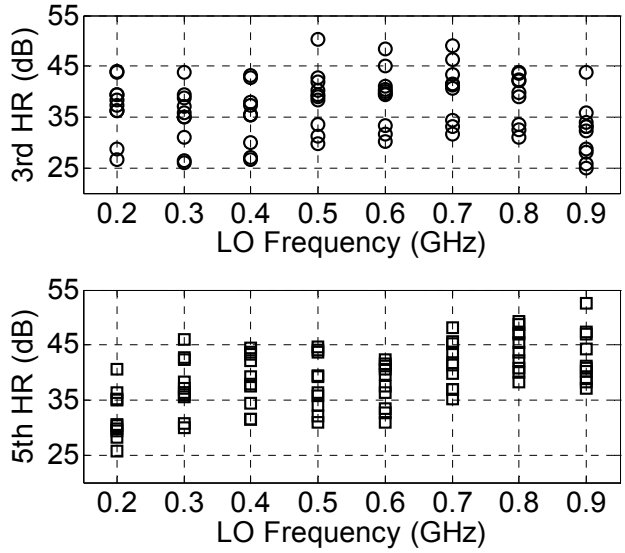

Figure 3.19 Measured 3rd and 5th HR ratio versus LO frequency (10 samples) [measured on wafer]

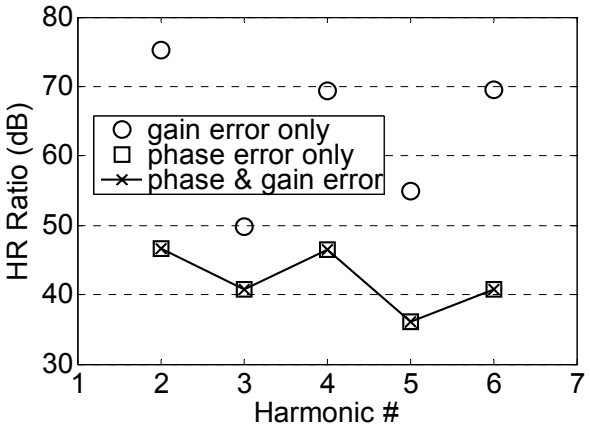

Figure 3.20 Simulated 2nd to 6th HR ratio at 0.35GHz LO
(averaged in dB for 10 Monte Carlo runs, mismatch only)

The results indicate that phase error is dominating, which affects not just the 3rd and 5th HR but also the even-order HR. We also did simulations at 0.7GHz LO, and the same conclusion holds. The relatively large phase error is mainly due to many buffer stages used after the divider (Fig. 3.13), leading to large accumulated mismatch. Nevertheless, the HR ratio can be improved via techniques that we will present in Chapter 5, for both amplitude and phase errors, or it can be improved by a tunable front-end LC filter to be presented in Chapter 4.

3.4.3 Performance Summary

Table 3.1 summarizes some of the measured parameters.

For the measured in-band linearity, the IIP3 is +10dBm and the IIP2 is +53dBm with two tones around 500MHz. There are three contributions to distortion: the RFA, the MOSFET switches and the IF buffer. The simulated IIP3 of only the SC core is +26dBm and the simulated IIP3 of only the IF buffer is +27dBm. This indicates that the measured IIP3 is dominated by the RFA whose linearity can be degraded by process spread and bondwire inductance of VDD/GND supply pins

Frequency (GHz)	0.2 to 0.9
Conv. Gain (dB)	-0.5 to 2.5
DSB NF (dB)	18 to 20
IIP3[1]	+10dBm
IIP2[1]	+53dBm
1/f noise corner	250kHz
-3dB IF BW @ 0.7GHz LO	10MHz
VDD	1.2V
DC Current	< 16mA

[1] Two tones @ 501M & 501.4MHz, LO @ 500MHz

Table 3.1 Summary of some measured parameters

[17][4]. Since a balun is used in measurement, the IIP3 of each single-ended RFA should be 3dB lower, i.e. +7dBm, which fits the result derived in [17]. Comparing to IIP3 of +11dBm shown in [1] which is based on two-tone test via wafer probing and with around 3dBm adjustment for the transmission-line effect around 500MHz RF, we may conclude that the bondwire in a packaged chip can degrade IIP3 by around 4dB at 500MHz RF.

The measured -3dB IF BW is about 10MHz at 0.7GHz LO, while the designed IF BW is 10MHz at 0.5GHz LO. Since the IIR filter BW is determined by both the sampling frequency and the capacitor ratio according to (3.8), the difference is likely due to the variation of the C_{su}-to-C_b ratio caused by process spread, as they are built by different types of capacitors, i.e. C_{su} via MOM capacitor and C_b via MOS capacitor.

For power consumption, the RFAs draw 2.3mA and the IF test buffers take 2.4mA. The current consumption of the clock is 7.8mA at 200MHz LO and 10.6mA at 900MHz LO. The overall power consumption for all blocks shown in Fig. 3.6 is less than 16mA (19mW) at 1.2V supply.

[4] In [17], the discrepancy of IIP3 results based on two-tone test and three-point method is mainly due to the inductance associated with bondwires of supply pins, as being found out later. This effect will be discussed more in Section 4.5.2.

3.5 Conclusions

A discrete-time mixing technique was defined via the classification of downconversion techniques in Section 2.2. This chapter elaborates on the receiver architecture based on DT mixing, which has some similar features as CT mixing and solves two problems in traditional RF-sampling receivers: narrowband quadrature demodulation and narrowband harmonic rejection. As a result, the DT-mixing architecture makes RF sampling more suitable to wideband SDR receivers.

In this chapter, first we presented the concept of DT mixing, which is a mixing operation in the discrete-time domain. It follows a CT-to-DT sampler to produce the DT input. Simulation shows wideband 90° phase shift for quadrature demodulation without systematic channel bandwidth limitation. Oversampling and harmonic rejection relaxes RF pre-filtering and reduces noise and interference folding. Combining voltage sampling and the DT mixing with HR, the challenges discussed in Section 2.5 can be relieved.

Then we showed that the DT-mixing concept can be realized via de-multiplexing. A proof-of-concept DT-mixing downconverter for the 200-to-900MHz RF band employing 8-times oversampling has been built in 65nm CMOS. It can reject the 2^{nd}-to-6^{th} harmonics by 40dB typically without systematic channel bandwidth limitation. Thanks to harmonic rejection which reduces aliasing, the chip also achieves better NF than other state-of-the-art voltage sampling downconverters.

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Chapter 4

Filter and Amplifier Techniques for Interference Robustness

The previous chapter demonstrated a wideband RF-sampling downconverter based on a discrete-time mixing architecture. However, without LNA, its gain is still low and NF is high, and the achieved harmonic-rejection ratio is also limited due to relatively large phase and amplitude errors. Chapter 4 describes a tunable LC filter and a linearized LNA [1] [2] applied to the DT-mixing downconverter to improve its performance with low extra power consumption and demonstrates a complete RF-sampling receiver.

An introduction in Section 4.1 is followed by an overview of the complete RF-sampling receiver in Section 4.2. The description of the tunable LC filter appears in Section 4.3, which can provide "passive" voltage gain and improve the HR ratio flexibly by tuning its center frequency. Then in Section 4.4 the design of the LNA is discussed with a focus on a linearity enhancement technique and the high (non-matched) input impedance. The complete RF-sampling receiver is implemented in 65nm CMOS, with measurement results shown in Section 4.5, demonstrating an NF as low as 0.8dB for a voltage-sampling receiver. Conclusions are drawn in Section 4.6 and references are attached in Section 4.7.

4.1 Introduction

Recently, there has been a growing research interest into RF-sampling receivers [3]-[8]. Moving the sampling closer to the antenna can be viewed as an intermediate step in the direction of a software-radio receiver with the full ADC

close to antenna which targets at greater flexibility. In addition, a direct-RF sampling can offer several other advantages as discussed in Section 2.4.2. For example, sampling exploits switches, capacitors and digital clocks which are compatible with CMOS scaling. Also it is suitable for system-on-chip (SoC) integration since the analog front-end, the ADC and the digital circuits can be clocked synchronously if integer decimation ratios are used between the RF sampling rate and the digital sample rate.

To serve software-defined radio (SDR) applications, wideband sampling receivers are desired to cover many RF bands. However, most of the reported RF-sampling receivers are dedicated to narrowband applications such as Bluetooth [5], GSM [6] [8] and WiMax [7]. In fact, compared to mixing, the traditional RF-sampling techniques present some extra challenges when used in wideband applications as described in Section 2.5, such as maintaining quadrature over a wide band and aliasing of wideband noise and interference.

Voltage sampling is known to suffer from severe aliasing because all the sampling images have equal magnitude in the ideal case. Charge sampling [5]-[8] yields reduced aliasing and gives similar harmonic downconversion as a mixer due to the SINC function in the frequency domain. The SINC function comes from charge sampling's (current to charge) integration feature in the time domain, equivalent to convolute with a widowing function [9]. However, charge sampling is not intrinsically suitable to wideband applications since its conversion gain *systematically* depends on the sampling frequency (see Section 2.5.3).

In Chapter 3, a wideband sampling technique, i.e. discrete-time (DT) mixing, has been presented which can deliver constant phase shift over a wide band for frequency-independent quadrature demodulation and wideband harmonic rejection (HR) for reduced aliasing. Thus, the combination of *voltage sampling* with frequency-independent gain and *DT mixing* with HR can be suitable to wideband SDR applications.

However, the downconverter in Chapter 3 has a few critical performance limitations. Without an LNA, the gain is low (2.5dB) and the NF is high (18dB). Furthermore, the first un-rejected harmonic is the 7^{th}, which may still cause aliasing which results in degraded NF and signal-to-interference ratio. In general, the

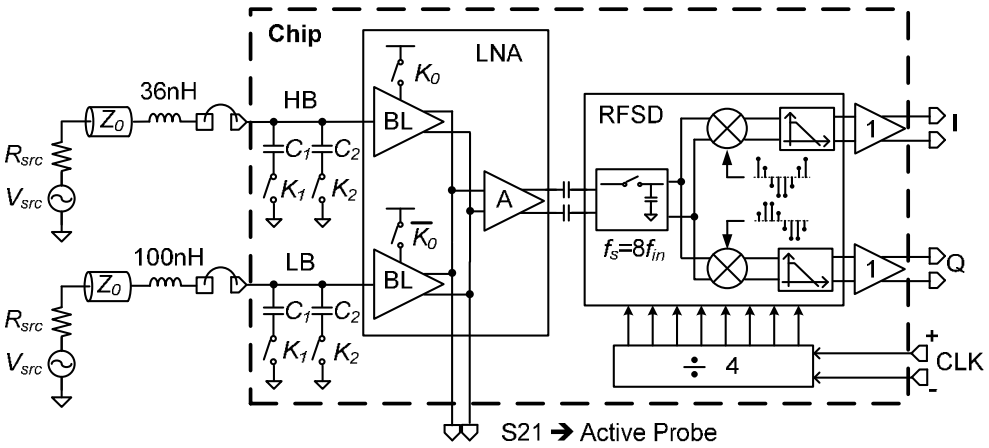


Figure 4.1 The multi-band RF-sampling receiver

number of rejected harmonics is limited by the number of LO phases, and the generation of more LO phases typically requires higher clock frequency, more complexity and more power consumption. Moreover, the HR ratio is severely affected by amplitude and phase accuracy, and the worst-case HR ratio of 25dB (among multiple samples) is not sufficient to handle strong interference in practice.

To further reduce the aliasing, in this chapter we apply a front-end tunable LC filter technique which simultaneously provides passive voltage pre-gain[1] and harmonic filtering while consuming no power. Pre-gain can improve the NF and the HR at the same time. However, it can degrade the receiver linearity. Therefore we will also present a simple voltage amplifier topology namely an enhanced voltage mirror, applied in the LNA stage, aiming at 3rd-order linearity enhancement.

Integrated with the HR downconverter presented in Chapter 3, the complete sampling receiver aims at covering the band of 300MHz to 800MHz (DVB-H band and TV bands for cognitive radio). The receiver can achieve a NF as low as 0.8dB due to the pre-gain, reduced source noise folding, and reduced LNA noise folding. The total HR is also improved from the worst case of 25dB for the basic downconverter to at least 60dB for the complete receiver. In the mean time the

[1] We refer to this voltage gain as a passive "pre-gain" meaning that it is achieved before the first active amplification stage, i.e. the LNA.

receiver achieves a moderate IIP3 of higher than -14dBm. The combination of the LC filter and the LNA can also add more than 20dB gain before downconversion thereby reducing the noise contribution from the later stages.

This chapter discusses the design of the sampling receiver with an emphasis on the filter/LNA part while the detail of the downconverter can be found in Chapter 3.

4.2 RF-Sampling Receiver Architecture

Fig. 4.1 shows the multi-band zero-IF sampling receiver architecture, in this case for 2 sub-bands. It consists of two LC filters, an LNA, and an RF-sampling downconverter (RFSD) driven by a frequency divider. Two input signal paths are used to cover a 300 to 800MHz bandwidth in two sub-bands, the High Band (HB) and Low Band (LB). These paths can be connected to different antennae as shown, *but can also be connected to a single antenna which can cover the full bandwidth.* The antennae deliver signals to a pair of LC networks which are followed by the receiver circuit. The inductors are off-chip while the rest of the components are on-chip such as two switchable capacitor banks, an LNA with two selectable single-input differential-output baluns (BL), and an RFSD with 2^{nd}-to-6^{th} order HR driven by a divide-by-4 circuit producing an 8-phase LO. For measurement purposes, after the RFSD, the quadrature baseband outputs are buffered via source followers with a voltage gain of 1. The differential S21 nodes are used to test the transfer function of the LC filter with the balun stage, via an active probe.

The RFSD in Fig. 4.1 employs the DT mixing architecture described in Chapter 3. The first stage is an oversampler with an effective sample rate of 8-times the input carrier frequency, i.e. $f_s=8f_c$. The second stage contains I/Q DT mixers which down-convert the RF signal to zero-IF with 2^{nd}-to-6^{th} order HR. Oversampling and HR relaxes RF pre-filtering and reduces noise and interference folding. The third stage consists of infinite-impulse response (IIR) low-pass filters, which remove undesired interference and serve as anti-aliasing filters before decimation to a lower sampling rate.

The DT mixing architecture can achieve *wideband* quadrature demodulation and *wideband* harmonic rejection without systematic channel bandwidth limitations,

and therefore it is more suitable for wideband SDR receivers compared to traditional sampling downconverters. The RFSD was implemented to target at the cognitive radio application recently proposed in the television broadcasting bands [10]. The wideband features of DT mixing can be useful for CR applications which might use non-contiguous segments of free spectrum distributed over a wide band. The dowconverter has a measured gain of -0.5 to 2.5dB, an NF of 18 to 20dB, and an IIP3 of +10dBm. Due to mismatches, the minimum HR ratio is around 25dB. The achieved NF is amongst the best published for voltage sampling downconverters, thanks to the reduced noise folding by employing oversampling and HR. However, the number of rejected harmonics is limited by the number of LO phases and the un-rejected harmonics (7^{th}, 9^{th} etc.) still cause noise aliasing which degrade the NF. For the rejected harmonics (e.g. 2^{nd} to 6^{th}), larger HR ratios are desired to counter strong interference.

4.3 Digitally-Controlled LC Filter

To improve the HR ratio and to reduce the noise aliasing, we apply a simple series LC filter structure as the first receiver stage, which can also provide voltage gain to reduce the NF.

4.3.1 Filter Concept

RF pre-filtering is often desired for two main reasons: 1) to attenuate strong out-of-band interferers to a level that can be handled by on-chip electronics; 2) to prevent mixer harmonic images to fold over the wanted signal.

It is well-known that a series inductor and a capacitor to ground (Fig. 4.2) define a 2^{nd}-order low-pass filter, with peaking around resonance and attenuation at high frequencies. To suppress the LO harmonics it is sufficient to just use a low-pass filter. In addition, the peaking effect of the filter can be useful to boost the desired signal before an LNA [11] [12]. Here we make the filter tunable by means of switched capacitors (see Fig. 4.3) and apply it to create a flexible sampling receiver with improved noise figure (NF) and harmonic rejection (HR). Next we will derive expressions for the (harmonic) rejection as indicated in Fig. 4.2 and the gain over the tuning range as indicated in Fig. 4.3.

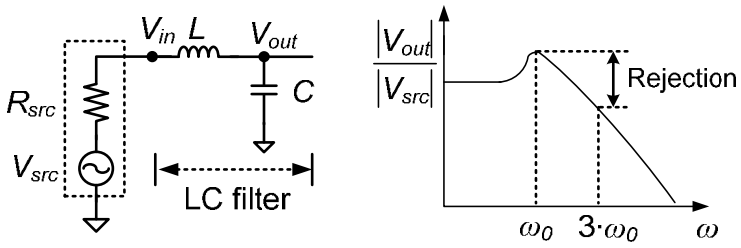


Figure 4.2 A *simple* 2nd-order LC filter with transfer function (logarithmic axis)

Assuming the source impedance is R_{src}, the magnitude of the voltage transfer function of the filter in Fig. 4.2 can be derived as

$$\left|\frac{V_{out}}{V_{src}}\right|^2 = \frac{1}{\left(1-\omega^2\cdot LC\right)^2+\left(\omega\cdot R_{src}C\right)^2} = \frac{1}{\omega^4\cdot L^2C^2+\omega^2\cdot\left(R_{src}{}^2C^2-2LC\right)+1}. \quad (4.1)$$

The peak value of (4.1) over frequency can be found via the derivative of its denominator:

$$\frac{\partial\left(\left|V_{src}/V_{out}\right|^2\right)}{\partial\omega} = 4\omega^3\cdot L^2C^2+2\omega\cdot\left(R_{src}{}^2C^2-2LC\right)=0\,. \quad (4.2)$$

Besides the trivial solution at ω=0, the other solution to (4.2) is

$$\omega_p = \sqrt{\frac{2L-R_{src}{}^2C}{2L^2C}} = \frac{1}{\sqrt{LC}}\cdot\sqrt{1-\frac{1}{2}\cdot\left(\frac{L/C}{R_{src}{}^2}\right)^{-1}} = \omega_0\cdot\sqrt{1-\frac{1}{2Q^2}}, \quad (4.3)$$

where Q is the quality factor of the series RLC network (Q=$\sqrt{(L/C)}/R_{src}$), and ω_p is the peaking frequency and ω_0 is the resonance frequency of the LC tank. From (4.3), we can see that ω_p lies below ω_0, where Q defines how much the difference is between them.

Substituting (4.3) into (4.1), the magnitude of the transfer function at ω_p can be derived as:

$$\left|\frac{V_{out}}{V_{src}}\right|_{\omega=\omega_p} = \frac{1}{\sqrt{\left(1-\omega_p{}^2\cdot LC\right)^2+\left(\omega_p\cdot R_{src}C\right)^2}} = \frac{1}{\sqrt{\frac{1}{4Q^4}+\frac{1}{Q^2}\left(1-\frac{1}{2Q^2}\right)}} = \frac{Q}{\sqrt{1-\frac{1}{4Q^2}}}. \quad (4.4)$$

Based on (4.1) we can see that the gain at the resonance frequency ω_0 is exactly Q. For high Q the difference between ω_0 and ω_p becomes small and the peak gain at ω_p is close to Q. Even for a low Q of 2, we still have ω_p=0.935ω_0 based on (4.3) and $|V_{out}/V_{src}|$=1.03Q at ω_p based on (4.4), which is only 3% larger than the gain at ω_0. Therefore, we may use the gain at ω_0 which is easier to define.

In Fig. 4.2, at the resonance frequency ω_0=1/√(LC), the LC input voltage V_{in} is equal to 0 since the series LC tank is a short circuit at ω_0. Therefore the current flowing into the LC filter is V_{src}/R_{src}, and the voltage magnitude on the capacitor can be written as

$$\left|V_{out}\right|_{\omega=\omega_0} = \frac{\left|V_{src}\right|}{R_{src}} \cdot \frac{1}{\omega_0 C} = \left|V_{src}\right| \cdot \frac{\omega_0 L}{R_{src}} = \frac{\sqrt{L/C}}{R_{src}} \cdot \left|V_{src}\right| = Q \cdot \left|V_{src}\right| = 2Q \cdot \left|V_{match}\right|, \quad (4.5)$$

where the actual source voltage $|V_{src}|$ is twice as large as the voltage $|V_{match}|$ in case of impedance matching, i.e. $V_{match}=V_{src}/2$.

To benefit from resonant peaking ($|V_{out}|>|V_{src}|$) we want Q>1. To get a coarse estimate of the required L and C, we suppose that the desired gain is $G_d=Q$ at ω_0, and then find $L=G_d \cdot R_{src}/\omega_0$ and $C=1/(G_d \cdot R_{src} \cdot \omega_0)$. For G_d=2 and R_{src}=50Ω, at frequencies below 1GHz, this leads to inductors larger than 15nH and capacitors larger than 1.5pF. Clearly, such inductors are not easily realized on chip and even if practical the Q is low. Off-chip inductors can be small, e.g. surface-mounted device (SMD), and with higher Q, and also they are relatively low-cost compared to, for instance, SAW filters. If the receiver has a single-ended RF input, only one external inductor is needed for each sub-band.

If R_{src} is defined by the antenna impedance in a radio receiver (usually 50Ω), for a sufficiently high L/C ratio, Q can be larger than 1 and thus this filter can realize "passive" voltage gain around ω_0. It can improve the receiver sensitivity, without adding noise and power consumption. This property is favorable compared to SAW filters, which often introduce significant loss.

As shown in Fig. 4.2, since inductors conduct DC signal, the attenuation on the low-frequency side is limited. A simple 2nd-order LC filter does not show a characteristic as sharp as most SAW filters, so the suppression of out-of-band interference is less. Whether this is acceptable depends on the application, the antenna characteristic and the linearity of the receiver.

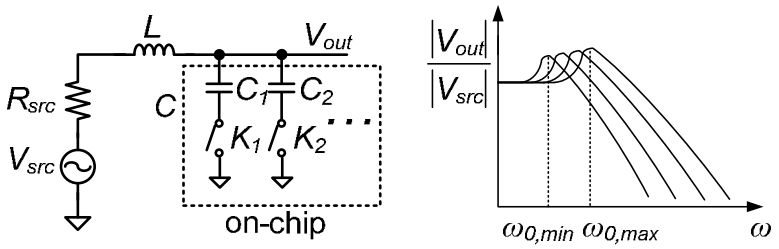


Figure 4.3 A *tunable* 2nd-order LC filter with transfer function (logarithmic axis)

Such an LC filter *does not* provide impedance matching, but *does* give useful voltage pre-gain around the resonance frequency. Moreover, the low-pass transfer function provides significant attenuation for RF signals at multiples of the sampling frequency, hence improving HR. The voltage pre-gain can boost the wanted signal and the improved HR reduces noise and interference aliasing. *Both features improve the NF of a wideband sampling receiver.*

One step further from the filter transfer function, we may quantify the improvement of HR ratio. Via (4.1), the gain for the n^{th} harmonic of the LC resonance frequency can be written as

$$\left|\frac{V_{out}}{V_{src}}\right|_{\omega=n\cdot\omega_0} = \frac{1}{\sqrt{\left(1-n^2\cdot\omega_0{}^2\cdot LC\right)^2+\left(n\cdot\omega_0\cdot R_{src}C\right)^2}} = \frac{1}{\sqrt{(n^2-1)^2+n^2/Q^2}}. \quad (4.6)$$

Since the gain at the fundamental harmonic (n=1), i.e. ω_0, is equal to Q according to (4.6). For the n^{th} harmonic (n=2, 3, 4…), we can achieve a HR improvement of

$$HR_n = 20\log_{10}\left(Q\cdot\sqrt{(n^2-1)^2+n^2/Q^2}\right) \approx 20\log_{10}\left[Q\cdot(n^2-1)\right] (\text{if } Q>>\frac{n}{n^2\text{-}1}). \quad (4.7)$$

Even for a low Q of 2, we can still get HR_3=24dB and HR_5=34dB. Please note that both the resonant peaking (Q) and the filter's 2nd-order roll-off contribute to the HR ratio, as indicated in Fig. 4.2.

The filter in Fig. 4.2 is dedicated to one resonance frequency. To cover a wider frequency range, we would like to have a tunable ω_0. In theory, an arbitrary bandpass characteristic can be made by a combination of inductors and capacitors. For a high-order filter, tuning to another frequency, while maintaining the bandpass shape involves tuning all or at least many of its components. Hence, for simplicity

of implementation it seems prudent to stick to low-order tunable filters. As inductors are not easily tunable and varactors often introduce nonlinearity, we aim to exploit MOS-switches and linear metal capacitors for tuning, which can be digitally controlled, as shown in Fig. 4.3.

Switching the capacitor to tune the filter to another frequency also changes its gain, but this gain variation can be acceptable. If we keep the frequency tuning range[2] smaller than 40%, i.e. $\omega_{0,max}/\omega_{0,min}<1.5$, the gain variation can be less than 3dB. The gain variation depends on the fact that the tuning is achieved whether via switching inductors or capacitors.

Based on (4.5), we can derive that if purely switching the capacitor, i.e. fix the inductor, the gain variation is

$$\frac{G_a}{G_b}=\frac{\omega_{0,a}}{\omega_{0,b}}=\sqrt{\frac{C_b}{C_a}}. \tag{4.8}$$

That means the gain is proportional to the resonance frequency. Yet, by switching the inductor and fixing the capacitor, the gain variation is

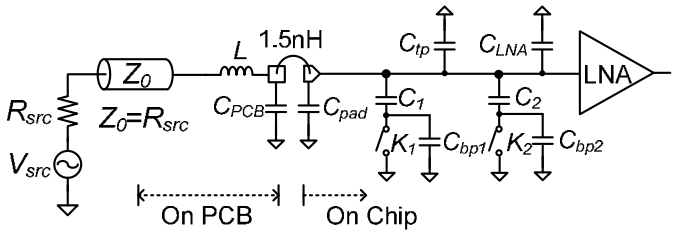
$$\frac{G_a}{G_b}=\frac{\omega_{0,b}}{\omega_{0,a}}=\sqrt{\frac{L_a}{L_b}}. \tag{4.9}$$

That means the gain is inversely proportional to the resonance frequency in case of switching inductors to tune the working band (Section 4.3.2).

4.3.2 Implementation

Fig. 4.1 shows the schematic of the implemented LC filter. Two on-board SMD inductors, 36nH for high-band (HB) and 100nH for low-band (LB), with two metal-oxide-metal (MOM) capacitors (C_1=1.2pF, C_2=0.5pF) for each inductor, are included to demonstrate the multi-band function. Which signal path in use is determined by enabling one of the balun-LNAs by setting K_0 to be 0 or 1. The band selection is achieved in two steps, a coarse selection and a fine tuning. The coarse

[2] The tuning range is defined as the ratio of the absolute tuning bandwidth to the middle frequency of the tuning band, i.e. $2(\omega_{0,max}-\omega_{0,min})/(\omega_{0,max}+\omega_{0,min})$.



$C_{fix}=C_{LNA}+C_{pad}+C_{tp}+C_{PCB}=0.17+0.1+0.17+0.25=0.69pF$

K_1K_2	C_{fix} (pF)	C_{tune} (pF)	C_{tot} (pF)
00	0.69	0.36+0.24	1.29
01	0.69	0.36+0.5	1.55
10	0.69	1.2+0.24	2.13
11	0.69	1.2+0.5	2.39

Figure 4.4 Sources of parasitic capacitance in the LC filter

selection is inherent in the LNA stage (K_0) which can be powered on/off to select which filter bank in use. The fine tuning is achieved by varying the capacitor values of the LC tank via digital bits (K_1, K_2).

Via the combination of selecting inductors and capacitors, we can set eight resonance frequency points (f_0) of the filter, i.e. controlling via three bits "$K_0K_1K_2$". These resonance frequencies are discrete points but the filter can continuously cover a large bandwidth by operating over a small bandwidth around each f_0 (Fig. 4.3).

However, the resonance frequency and the Q are heavily affected by the parasitic capacitance, as modeled in Fig. 4.4. The model includes the input capacitance of LNA C_{LNA}, the pad capacitance C_{pad}, the PCB capacitance C_{PCB}. C_{tp} indicates the top-plate parasitic capacitance of C_1 and C_2 together. C_{bp1} and C_{bp2} indicate the bottom-plate parasitics of C_1 and C_2 respectively, as well as the parasitics of their switches.

	$K_0K_1K_2$	Total L (nH)	Total C (pF)	f_0 (MHz)	Q [a)]	Gain=2Q (dB)	3rd|5th Harmonic Rejection (dB)	
HB	000	36	1.29	740	3.3	16	28	38
	001	36	1.55	670	3.0	16	27	37
	010	36	2.13	570	2.6	14	26	36
	011	36	2.39	540	2.5	14	26	35
LB	100	100	1.29	440	5.6	21	33	43
	101	100	1.55	400	5.1	20	32	42
	110	100	2.13	340	4.3	19	31	40
	111	100	2.39	320	4.1	18	30	40

[a)] Refer to a 50Ω real impedance.

Table 4.1 Calculated parameters of the implemented LC filter (Figure 4.1)

The parasitics of C_1 and C_2 are about 10% of their nominal values and the parasitics of switches are about 0.4pF due to large switches used for low on-resistance (1Ω). Via simulation and estimation, we get C_{LNA}=0.17pF, C_{pad}=0.1pF, C_{tp}=0.17pF, C_{bp1}=0.52pF, and C_{bp2}=0.45pF; C_{PCB} is about 0.25pF (fitted after experiments). The table in Fig. 4.4 summarizes the total capacitance C_{tot} in each configuration of K_1K_2.

Table 4.1 lists the resonance frequency, the Q, and the HR ratio for each of the filter 3-bit settings ($K_0K_1K_2$), calculated via (4.5) and (4.7)-(4.9). Please note that the voltage gain here is equal to 2Q, referred to V_{match} in (4.5). The lowest Q in the whole band is 2.5, for $K_0K_1K_2$=011. The bondwire of 1.5nH and the switch-on resistance of 1Ω have a negligible effect to the filter performance. Also the quality factors of the on-board inductors are in the order of 30 to 40, which also can hardly affect the filter performance. The calculated parameters in Table 4.1 have been verified by simulations.

At resonance, the LC filter input impedance is 0 (short) instead of R_{src}. Receivers without input matching have been proposed before, e.g. in [12]-[14]. Although this may complicate RF pre-filter design and may introduce issues with respect to reflections, it also has advantages. Note that for input matching there is a maximum

power transfer, but it degrades the voltage by half, i.e. $V_{match}=V_{src}/2$ as shown in (4.5). For voltage sensing devices such as a MOSFET at $f<<f_T$, the maximum voltage transfer is more of interest, and an unmatched input may have advantages, e.g. lower NF, lower power consumption, and higher Q (no extra resistance from the matching device).

The inductors are placed very close to the chip, and 50Ω transmission lines are used to connect the inductors to the antennae. If there is no impedance mismatch between the antenna and its connection lines, the voltage amplitude sensed by the LNA input is still well defined by (4.5), independent of the line length [13]. Moreover, since here we deal with frequencies below 1GHz, it is often possible to use PCB lines between the antenna and the chip which are much shorter than the wavelength. In that case, the transmission line effect can be made negligible.

The reflection due to the impedance mismatch at the input of the LC filter will create standing waves on the transmission line. If the transmission line has a negligible length or is well matched with antenna, the antenna will absorb the reflected wave and radiate it back into the air. But this reflection should not violate the radio regulation, since any obstacle in surroundings may cause the same consequence.

According to (4.5), the gain is well defined if the source impedance is well defined. However, antenna impedance is not purely resistive but involves re-active parts such as inductance and capacitance. Nevertheless, for a well-designed antenna, its impedance in the desired band can be approximated as purely resistive while the re-active parts resonate in that band. The resonant effect of the antenna can provide attenuation of interference and hence further improve the HR ratio.

In practice, the antenna impedance can also vary with the environment, e.g. due to the reflection of electromagnetic waves by surroundings. If an antenna is aimed at achieving S_{11}<-10dB referred to a 50Ω source, the real part of the antenna impedance varies in the range of 25Ω to 100Ω. This variation represents a change of Q by 0.5 to 2 times from the nominal 50Ω case.

According to (4.5), the pre-gain variation is directly proportional to the Q variation. However, for NF the variation is less because the antenna noise voltage also

changes when its impedance varies. This effect can be seen from the overall noise at the output of the LC filter:

$$\frac{\overline{v_{n,afterLC}^{\,2}}}{\Delta f} = 4kTR_{src} \cdot \left(\frac{\sqrt{L/C}}{R_{src}} \right)^2 = 4kT \cdot \frac{L/C}{R_{src}}. \tag{4.10}$$

If the antenna impedance changes by a factor of 2, the gain changes by 6dB and the NF changes by 3dB in the worst case. It happens when the antenna noise is much smaller than the noise from the receiver (the LNA and the downconverter). Generally, the NF variation should be less than 3dB, depending on how much the antenna noise is boosted by the passive pre-gain. If the antenna noise is dominating due to a high passive pre-gain, then the NF variation can be negligible. In case that the variation is not acceptable, additional measures might be taken to adaptively transform the antenna impedance. Anyhow, the variation of antenna impedance can also be problematic in a receiver *with* input impedance matching.

4.4 Amplifier based on Enhanced Voltage Mirror

Since the presented LC filter provides pre-gain before the LNA stage, the required linearity of the LNA is hence raised. Now we will propose a simple amplifier topology to construct a balun-LNA, which can provide IIP3 enhancement.

4.4.1 LNA Topology

As shown in Fig. 4.5, the balun-LNA is constructed using inverters as transconductors. Compared to common-source amplifiers with a single NMOS or PMOS as the transconductor, they can provide a large g_m/I_d ratio as the bias current of the PMOS is re-used by the NMOS, while also tolerating large voltage swings which is advantageous for handling large interference.

In fact, all inverters in Fig. 4.5 are self-biased via feedback resistors, so that no extra bias circuitry is needed. Fig. 4.6 shows the schematic of a unit amplifier used in the LNA where g_m=$g_{m,N}$+$g_{m,P}$, It includes both the feedback resistor (R_{big}) for the driving inverter and the feedback resistor (R_{fb}) for the loading inverter. The absolute value of R_{big} is not critical but is large enough (1MΩ) only for DC biasing

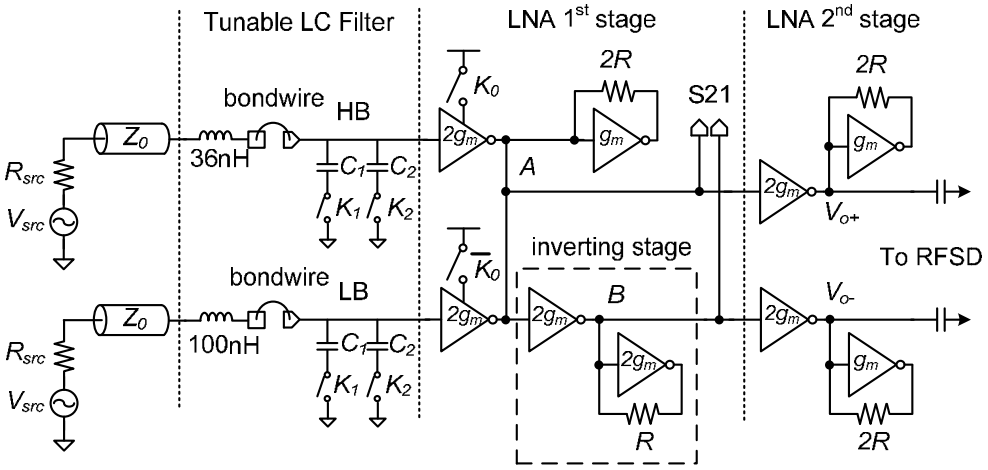


Figure 4.5 Implemented LC filter and LNA

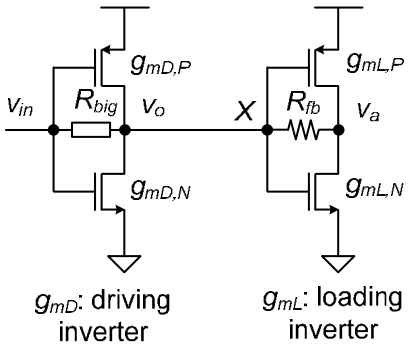


Figure 4.6 Schematic of a unit amplifier used in the LNA

purpose without affecting the transconductance function. Therefore in Fig. 4.5, R_{big} of all driving inverters are not shown for figure clarity.

To understand the basic functionality of the LNA in Fig. 4.5, let's first consider all feedback resistors of the loading inverters as shorts, realizing an impedance of $1/g_m$ or $1/(2g_m)$ where g_m is the unit transconductance in use. Driven by a transconductance of $2g_m$, an inverting gain is realized. The gain is -2 in all cases

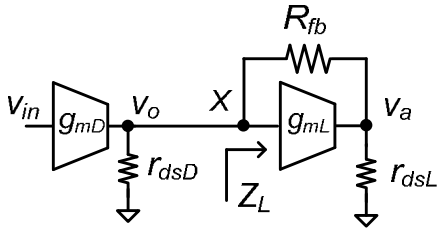


Figure 4.7 Model for the unit amplifier

except for the "inverting stage" whose gain is -1. Thus the 1st stage realizes a balun function with a 6dB gain from the input to each of the differential outputs (the single-to-differential gain is 4), and the 2nd stage is a pseudo-differential amplifier with another 6dB gain.

As can be seen from Fig. 4.5, the loading inverters have their inputs and outputs connected via a feedback resistor, either R or $2R$, for the purpose of nonlinearity compensation (Section 4.4.2). The feedback resistors and the output impedance of the inverters can affect the amplifier behavior. To analyze the gain and noise performance, we model the unit amplifier (Fig. 4.6) as Fig. 4.7, including the output resistance of the driving inverter (r_{dsD}) and the loading inverter (r_{dsL}) and the feedback resistor R_{fb}. The equivalent input impedance of the loading inverter can be written as

$$Z_L = \frac{R_{fb} + r_{dsL}}{1 + g_{mL} \cdot r_{dsL}} \approx \frac{1}{g_{mL}} (\text{if } g_{mL} \cdot r_{dsL} >> 1 \text{ and } r_{dsL} >> R_{fb}) . \quad (4.11)$$

In our design, g_{mL}=10mS, r_{dsL}=1.5kΩ, and R_{fb}=2/g_{mL}=200Ω and therefore the approximation in (4.11) holds. Then the voltage gain can be written as

$$\frac{v_o}{v_{in}} = g_{mD} \cdot \frac{r_{dsD} \cdot Z_L}{r_{dsD} + Z_L} \approx g_{mD} \cdot \frac{r_{dsD}}{1 + r_{dsD} \cdot g_{mL}} \approx \frac{g_{mD}}{g_{mL}} (\text{if } g_{mL} \cdot r_{dsD} >> 1) . \quad (4.12)$$

Traditional common-source amplifiers often rely on the product of transistor g_m and load resistance to define the gain, which can vary a lot due to process spread. The amplifier topology presented here defines its gain via the ratio between transistors' g_m, which is less sensitive to process spread especially when gain ratios via unit transconductors are used.

To gain some insight into the noise behavior of the circuit, one can idealize the transconductor output resistors, by making r_{dsD} and r_{dsL} infinite in the noise analysis. There are three noise contributors: g_{mD}, g_{mL} and R_{fb}. Ignoring r_{dsD} and r_{dsL}, the noise current of g_{mD} ($i_{nD}^2/\Delta f = 4kT\gamma \cdot g_{mD}$) can only flow through R_{fb}. As a result, a noise voltage (v_{nD}) appears at node X which generates a current via g_{mL} to match i_{nD}. The noise voltage can be written as $v_{nD} = i_{nD} \cdot Z_L \approx i_{nD}/g_{mL}$. Another noise voltage (v_{nL}) also appears at node X to generate a current via g_{mL} to cancel its own noise current ($i_{nL}^2/\Delta f = 4kT\gamma \cdot g_{mL}$), which can be written as $v_{nL} = i_{nL}/g_{mL}$. However, as R_{fb} is in series with a current source which models the noise current of g_{mD}, it does not affect the noise voltage at node X. Therefore, for a unit amplifier, the noise voltage at node X can be derived as:

$$\frac{\overline{v_n^2}}{\Delta f} = \frac{\overline{v_{nD}^2}}{\Delta f} + \frac{\overline{v_{nL}^2}}{\Delta f} = \frac{4kT\gamma \cdot g_{mD}}{g_{mL}^2} + \frac{4kT\gamma}{g_{mL}} . \tag{4.13}$$

Now consider the NF of the complete LNA shown in Fig. 4.5., According to (4.5), the voltage gain (referred to V_{src}) of the LC filter is Q, therefore the source noise voltage at the input of the LNA is $4kTR_{src} \cdot Q^2$. Applying (4.13), we can derive the total noise voltage at the LNA output as:

$$\begin{aligned} \frac{\overline{v_{n,LNAo}^2}}{\Delta f} = & \underbrace{4kTR_{src} \cdot Q^2 \cdot 8^2}_{\text{Source}} + \underbrace{\left(\frac{4kT\gamma \cdot 2}{g_m} + \frac{4kT\gamma}{g_m} \right) \cdot 4^2}_{\substack{\text{LNA 1st-Stage} \\ \text{(Exclude Inverting Stage)}}} + \underbrace{\left(\frac{4kT\gamma}{2g_m} + \frac{4kT\gamma}{2g_m} \right) \cdot 2^2}_{\text{Inverting Stage}} \\ & + \underbrace{\left(\frac{4kT\gamma \cdot 2}{g_m} + \frac{4kT\gamma}{g_m} \right) \cdot 2}_{\text{LNA 2nd-Stage}} = 4kTR_{src} \cdot 64Q^2 + 4kT\gamma \cdot \frac{58}{g_m} \end{aligned} . \tag{4.14}$$

Given R_{src}=50Ω and g_m=10mS, the NF of the LC-LNA combination is

$$NF_{LC-LNA} = \frac{v_{n,LNAo}^2}{4kTR_{src} \cdot 64Q^2} = 1 + \frac{\gamma \cdot 58/g_m}{R_{src} \cdot 64Q^2} = 1 + \frac{\gamma \cdot 58/10mS}{50\Omega \cdot 64Q^2} = 1 + \frac{1.8\gamma}{Q^2} . \tag{4.15}$$

We can see that this NF will be improved by the LC filter pre-gain defined by the Q. If Q=2 and assuming γ=1, then NF=1.6dB.

In Fig. 4.5, due to the additional stage used for inverting (marked in box) in the V_o- path, an extra delay exists therefore the balun performance can degrade at a higher frequency. Any capacitive load at node A (Fig. 4.5) affects both differential paths,

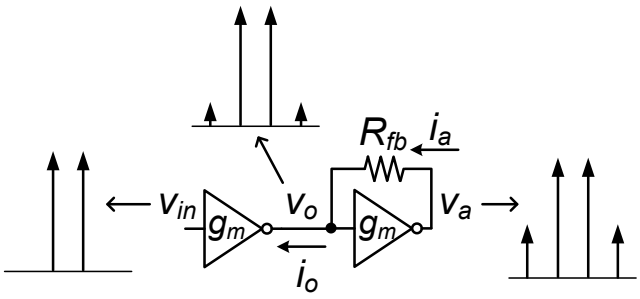


Figure 4.8 IM3 compensation mechanism in a unit amplifier

which doesn't produce imbalance. Loading at node *B* only affects the V_{o-} path and thus should be minimized. Nevertheless the extra delay on the V_{o-} path can be compensated by adding a capacitor with an appropriate value at the V_{o+} node to better balance the two paths. However, it was not included in this design.

4.4.2 Mechanism of Nonlinearity Compensation

The passive pre-gain induced by the LC filter improves receiver NF, but it can also degrade linearity. The aim of the feedback resistors in the loading inverters (Fig. 4.5 to Fig. 4.7) is to mitigate this effect by compensating the 3rd-order distortion.

To understand the compensation principle, consider first the simple case with two equally-sized inverters for a voltage gain of -1 (Fig. 4.8), and only include the linear term and the 3rd-order term in the V-I conversion.

If one models the transconductor as a nonlinear V-I converter with no v_{ds} dependence, then only g_{m1} and g_{m3} terms need to be considered:

$$\begin{cases} i_o = g_{m1}v_{in} + g_{m3}v_{in}^{\ 3} = f(v_{in}) \\ -i_a = g_{m1}v_o + g_{m3}v_o^{\ 3} = f(v_o) \end{cases}. \tag{4.16}$$

Assuming negligible gate-current, i_o and i_a are equal due to Kirchhoff's Current Law (KCL), and the solution for (4.16) is $v_o=(-1)\cdot v_{in}$ which is a perfectly linear V-V transfer function. This is because we assume the $i(v)$ function of the driving and loading inverters are equal, i.e. $v_o(i_a)$ is an *inverse function* of $i_o(v_{in})$. According to (4.16), $i_o=f(v_{in})$ and $i_a=-f(v_o)$, then we have:

$$v_o = -f^{-1}(i_a) = -f^{-1}(i_o) = -f^{-1}\left[f(v_{in})\right] = -v_{in}. \tag{4.17}$$

Although the V-I conversion does contain 3rd-order distortion, the V-V conversion can be linear, because the nonlinearity in the V-I conversion and the I-V conversion cancel each other (inverse functions). This operation with distortion compensation is sometimes referred as voltage mirror [15] [16], a counterpart to current mirror which also relies on inverse functions but with current input and output. If without v_{ds} dependence as (4.16), the V-V conversion can be linear whatever the value of the feedback resistor R_{fb} (can be a short).

However, in modern CMOS technology the output current does depend on v_{ds}, since the output impedance and the v_{gs}·v_{ds} cross-term cannot be neglected anymore [17]-[19]. If we model these effects in Fig. 4.8 via (4.18), it still appears possible to achieve 3rd-order distortion compensation:

$$\begin{cases} i_o = g_{m1}v_{in} + g_{ds1}v_o + g_{m3}{v_{in}}^3 + x_{21}{v_{in}}^2 v_o + x_{12}v_{in}{v_o}^2 + g_{ds3}{v_o}^3 \\ -i_a = g_{m1}v_o + g_{ds1}v_a + g_{m3}{v_o}^3 + x_{21}{v_o}^2 v_a + x_{12}v_o{v_a}^2 + g_{ds3}{v_a}^3 \end{cases}. \tag{4.18}$$

Traditional amplifier distortion compensation techniques such as derivative superposition [20] [21] mostly focus on the v_{gs}-related term g_{m3}, while this technique, referred as *enhanced voltage mirror*, can also take care of v_{ds}-related terms, e.g. g_{ds3}, x_{12}, and x_{21}, as explained below.

There are two equations in (4.18) but there are four unknown variables: i_o, i_a, v_o, and v_a, while v_{in} is the given input voltage. Since i_o=i_a based on KCL, the number of unknown variables is reduced to three: i_o, v_o, and v_a. Therefore, the value of v_a will affects the value of v_o now, i.e. the choice of R_{fb} does matter now as it directly affects v_a.

For a linear amplifier, we want v_o=(-1)·v_{in}, without any 3rd-order terms. Putting this condition into (4.18) and equating the two equations shows that v_a≈-v_o renders a solution. This can be realized by choosing R_{fb}≈2/g_m, so that g_m·R_{fb}≈2. Again, although the output current i_o contains 3rd-order distortion, the output voltage v_o can be quite linear.

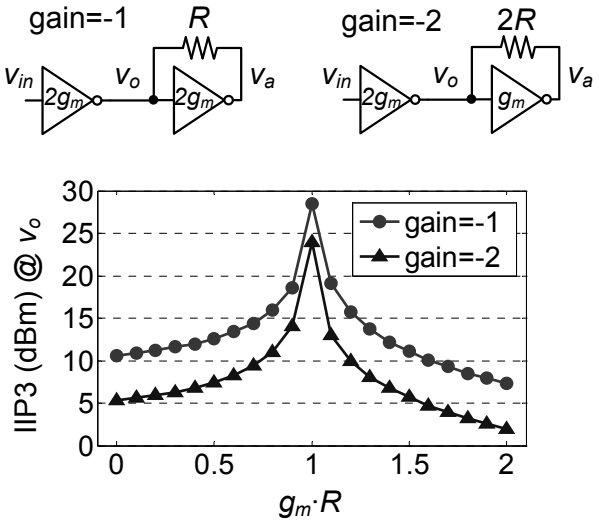


Figure 4.9 Simulated IIP3 versus $g_m \cdot R$ of two unit amplifiers (gain=-1, gain=-2) with two tones around 500MHz

The above analysis is only valid to the first order. Since v_o is linear with v_{in} and i_a is nonlinear with v_o, $v_a=v_o+i_a \cdot R_{fb}$ cannot be linear with v_{in}. Therefore v_a is only equal to $-v_o$ to the first order, and then to satisfy $i_o=i_a$, v_o must also be polluted by some distortion, but to a much lower degree than v_a, as illustrated by the two-tone-test spectra in Fig. 4.8. This is why in Fig. 4.5 all the nodes corresponding to v_a are not used. Please note that, for $v_a \approx -v_o$, the feedback resistor for g_m should be $2R$ and for $2g_m$ it should be R if $g_m \cdot R=1$, as shown in Fig. 4.5.

This technique also works for non-equal inverters but the linearity improvement will be less. Here we also use it for the stages with a gain of -2. The simulation results presented in Fig. 4.9 shows that a peak IIP3 exists at $R \approx 1/g_m$ for both gain of -1 and -2 cases. A 25% change of $g_m \cdot R$ from 1 can still give about 5dB better IIP3 compared to $g_m \cdot R=0$ (a short as feedback).

This principle is useful for the odd-order distortion but not very effective for the even-order distortion. Nevertheless, by using an inverter, the even-order distortion of the NMOS and PMOS can compensate each other nominally [22], although process spread may lead to residual distortion. A differential configuration can also

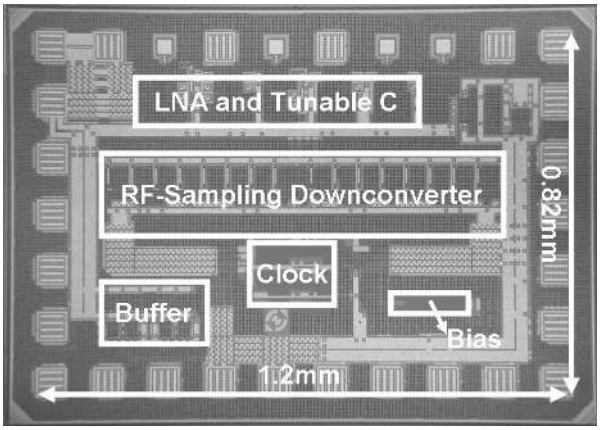


Figure 4.10 Micrograph of the chip implemented in 65nm CMOS

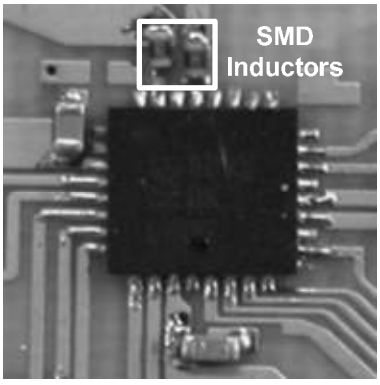


Figure 4.11 SMD inductors (36nH and 100nH) on PCB

help with even-order distortion after the balun. Moreover, the AC coupling capacitor used between the LNA and the RFSD can block the low-frequency IM2 components generated by the LNA.

4.5 Experimental Results

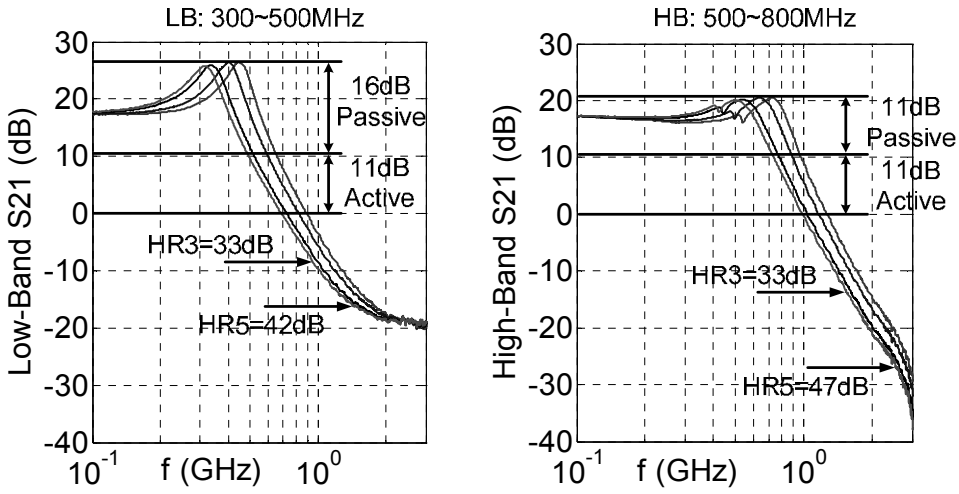


Figure 4.12 Measured S21: LC Filter plus LNA 1st-stage
(Passive: LC pre-gain; Active: LNA 1st-stage gain)

A proof-of-concept receiver was implemented in 65nm CMOS and the chip micrograph is shown in Fig. 4.10, taking an active area=0.5mm^2. The chip is packaged in a 32-pin Heat-sink Very-thin Quad Flat-pack No-leads (HVQFN) package and measured on PCB and the input port has R_{src}=50Ohm for all tests. Two inductors of value 100nH and 36nH are mounted on board, close to the chip package (Fig. 4.11). With a 1.2V supply, the current consumption is 5mA for the LNA, 10mA for the clock at 800MHz LO, and 2.4mA for the output buffer, while the RFSD consumes no power since it only contains switches and capacitors.

4.5.1 Filter Response, Gain, NF, and HR

To verify the tunability of the digitally-controlled LC filter, we measured S_{21} of the LC filter together with the 1st stage of the LNA (Fig. 4.1 & Fig. 4.5). The input of the LC filter is connected to a Vector Network Analyzer via PCB traces and co-axial cables. At the output of the LNA 1st stage, an active probe (up to 3GHz) is used to connect the S21 node (see Fig. 4.1) to the Vector Network Analyzer. The active probe performs the differential to single-ended conversion with 1x voltage gain as well as the impedance transformation to 50Ω desired for measurements.

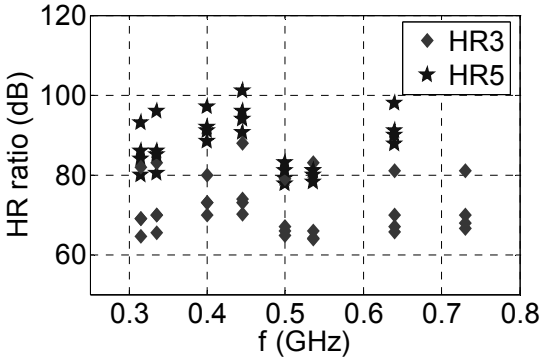


Figure 4.13 Measured 3rd and 5th order HR ratio over the RF band (4 chips)

Fig. 4.12 shows the measured S_{21} for low-band (LB) and high-band (HB) respectively, which can continuously cover 300-500MHz and 500-800MHz with less than 3dB gain variation in each band. Please note that the gain indicated here is a voltage gain referred to V_{match} in (4.5). Due to different inductor values (36nH and 100nH) used, the Q and therefore the peak gain and bandwidth are different for LB and HB. Considering the 11dB gain from LNA 1st stage (verified by measurement), the "passive" LC pre-gain is about 16dB for LB and 11dB for HB.

Comparing Fig. 4.12 and Table 4.1, we can see that the measured resonance frequencies fit the calculated ones well, via a 0.25pF excess capacitance from PCB (C_{PCB} in Fig. 4.4), e.g. due to the leadframe and the soldering pad. However, the measured gains (passive) are about 5dB lower than the calculated (and simulated) gains listed in Table 4.1. A possible reason is the deviation from 50Ω of the characteristic impedance of the connection cables and the PCB traces. Therefore the 50Ω source impedance is transformed to a higher value.

Both bands show an effective suppression of LO harmonics. The measured LB HR ratios from LC filter fit what calculated in Table 4.1, but the measured HB HR ratios are at least 7dB higher than the calculated values. We attribute this difference to the gain roll off at relatively high frequencies due to circuit parasitics of the LNA 1st stage and the sharp notch in the HB transfer function due to the inductor self-resonance. The measured 3rd and 5th HR of the complete receiver (4 chips) is shown in Fig. 4.13, where the HR ratios for the whole band are above 60dB, with roughly 30dB contribution from the LC filter and the other 30dB from the RFSD.

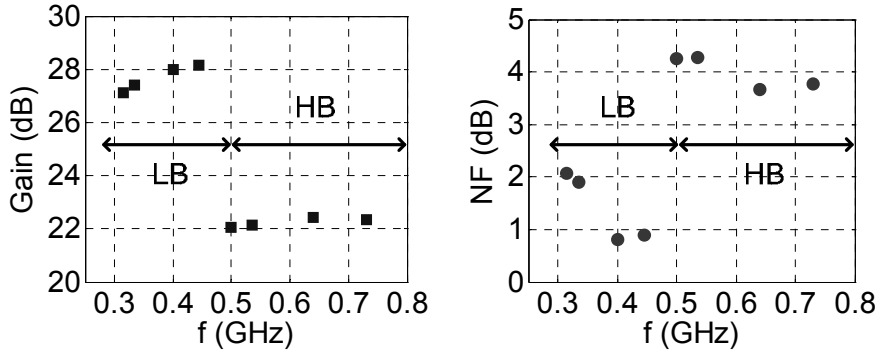


Figure 4.14 Measured gain and NF of the complete receiver over the RF band

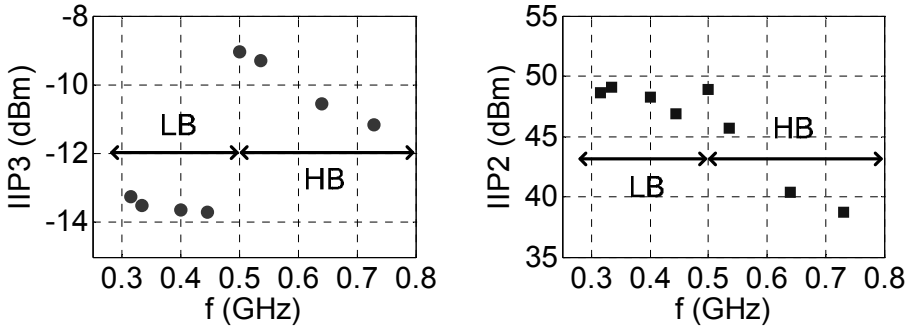


Figure 4.15 Measured IIP3 and IIP2 of the complete receiver over the RF band

Theoretically, a balanced LO with 50% duty cycle can reject all even-order harmonics. However, experiments show the 2nd-order HR can become the bottleneck, since the LC filter suppresses the 3rd and higher order harmonics more. This requires balanced LO being more accurate.

Fig. 4.14 plots the measured voltage gain and NF of the complete receiver, at the peak frequencies of both bands. The gain difference from LB to HB matches the measured S21 in Fig. 4.12. The NF is measured via the Y-factor method to read the noise voltage at the output. Fig. 4.14 shows a clear link between gain and NF, i.e. the high "passive" gain at LB also gives a better NF. The measured minimum NF is

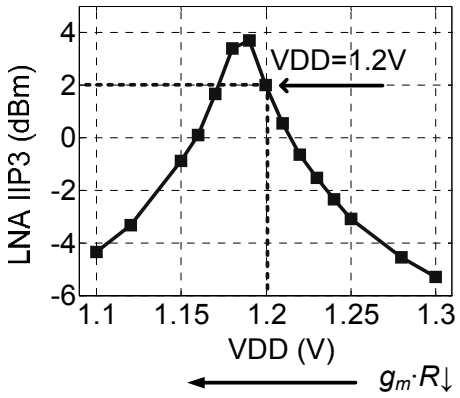


Figure 4.16 Measured LNA IIP3 at different VDD levels with two tones around 445MHz

0.8dB for the complete receiver, which shows a very low NF can be achieved with low power consumption (6mW for the LNA and downconverter), even for the voltage sampling receiver that suffers from severe noise folding. Such a low NF is achieved via a combination of sufficient "passive" pre-gain to boost the desired signal, 2^{nd}-order LC filter to prevent the source noise folding, and HR downconverter to prevent the source and the LNA noise folding.

4.5.2 Linearity

The measured in-band IIP3 and IIP2 via two-tone test are shown in Fig. 4.15.

Since the LNA is AC coupled to the RFSD (Fig. 4.1), the IIP2 is dominated by RFSD and degrades with higher frequency (worst case: +38dBm), rather independent of the gain. Most likely it is due to the degraded balun performance at the high band, since IIP2 directly relates to the matching of differential signal.

From the IIP3 plot, we see the direct effect of the "passive" pre-gain, sharing almost the same trend as NF. The worst-case IIP3 of -14dBm is moderate for a complete receiver, especially considering that this IIP3 corresponds to a very low NF of 0.8dB.

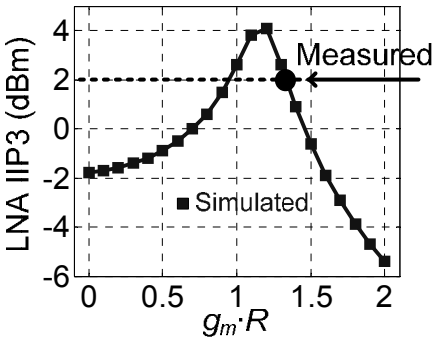


Figure 4.17 LNA IIP3: measurement versus simulation

Considering the LC pre-gain, the LNA plus RFSD combination should present an IIP3 around +2dBm. Simulation shows the LNA dominates IIP3, which means the 2-stage LNA has an IIP3 around +2dBm. To verify the effect of $g_m \cdot R$ to the IIP3, we measured and derived the IIP3 of the 2-stage LNA (Fig. 4.16) at different VDD levels, which affects the g_m value. Clearly we can see the trend of IM3 compensation which verifies the theory.

Considering VDD=1.2V, however, referred to the input of the LNA 2nd stage (S_{21} nodes in Fig. 4.5), the IIP3 should be about +7dBm, since the LNA 1st stage has a single-ended gain of 5dB. This IIP3 is far from optimum as simulated in Fig. 4.9, for the gain=-2 curve, corresponding to a 50% variation of $g_m \cdot R$ from 1. One reason is the process spread which makes the $g_m \cdot R$ value different from the designed 1. On the other hand, the measured DC linearity via a three-point method [23] is at least 4dB better than the two-tone test result. This gap of 4dB could mainly be due to the supply bondwire inductance which is not considered in the simulation of Fig. 4.9. Measurement via wafer probing (instead of packaged chips on PCB) can exclude the bondwire effect and indeed shows 4dB better IIP3 (see Section 3.4.3). The bondwire inductance disturbs the compensation mechanism since the driving inverter and the loading inverter will share the same bondwire but with different inverter sizes for the gain=-2 case (Fig. 4.9).

Simulation has been carried out to include non-ideal effects from both process spread (slow-NMOS and slow-PMOS indicated by measured DC operating point)

and supply bondwire inductance (VDD: 2nH, GND: 0.5nH, as estimated from the chip size and the specific package used). Fig. 4.17 compares the measured IIP3 and the simulated IIP3 around 500MHz RF at VDD=1.2V. The simulation agrees with the measured trend of Fig. 4.16 and it also indicates that the IIP3 improvement is about 4dB via the enhanced voltage mirror by applying R_{fb} (instead of a short) in the loading inverter (Fig. 4.6). Both Fig. 4.16 and Fig. 4.17 indicate that the distortion compensation is still effective, although additional techniques are desired to improve its robustness against process spread and bondwire inductance. For instance, techniques to change g_m to track an R or C value are well-known for filters.

4.6 Conclusions

A 300-to-800MHz multi-band RF-sampling receiver is presented, with 0.8dB minimum NF and more than 60dB HR. It is based on a discrete-time mixing harmonic-rejection downconverter in 65nm CMOS, preceded by a voltage sensing LNA which exploits a simple 2nd-order LC filter with one external inductor per sub-band. This LC filter does not provide impedance matching but does provide voltage pre-gain and also acts as a harmonic filter tunable via on-chip switchable capacitor banks which can be controlled by digital codes. The filtering significantly improves the sampling downconverter's HR ratio from 25dB to more than 60dB for 3rd and 5th harmonics, resulting in less interference aliasing. The voltage-sensing balun-LNA is built via a simple amplifier topology consisting of inverters and resistors. It reduces the 3rd-order nonlinearity due to both v_{gs} and v_{ds} related terms, via an enhanced voltage mirror technique. The compensation effect is demonstrated via measurements, although an improved robustness against process spread and supply bondwire inductance is desired.

A low NF (0.8dB) at a low power consumption (6mW for the LNA and downconverter) for a voltage sampling receiver can be achieved by a sufficient "passive" pre-gain from the LC filter, together with the reduced noise aliasing thanks to both the LC filter and the harmonic-rejection downconverter.

4.7 References

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Chapter 5

Downconversion Techniques Robust to Out-of-Band Interference

The previous two chapters mainly looked at RF-sampling SDR receivers for better compatibility with CMOS scaling and SoC integration. Although some techniques may deal with interference such as discrete-time (DT) harmonic-rejection (HR) mixing, tunable LC filtering and amplifier linearization, they either rely on external components such as high-Q inductors, or still desire more robustness to mismatch or process spread. This chapter focuses on the other aspect of our research: SDR receivers robust to out-of-band interference (OBI), and aims at more reliable techniques to tackle interference by exploiting frequency downconversion. Instead of RF sampling, this chapter will use RF mixing to demonstrate a few new concepts [1], which can be applicable to both sampling and mixing approaches.

After an introduction in Section 5.1, Section 5.2 introduces a low-pass blocker filtering technique to improve out-of-band linearity. For a low voltage gain at RF, a "mix-impedance" is exploited whose transfer function is analyzed (see Appendix *A*). Section 5.3 proposes a 2-stage polyphase HR concept to dramatically improve amplitude accuracy. Together with a proposed accurate multiphase clock, a high HR ratio robust to mismatch is obtained. To be able to quantify the achievable HR ratio, the effects of random amplitude and phase errors to HR is analyzed (see Appendix *B*). The implementation of the receiver analog front-end is discussed in Section 5.4, followed by a discussion in Section 5.5 to extend the receiver's frequency range. Section 5.6 presents the measurement results with a benchmarking which shows the highest IIP3 and the most-robust HR for this work. The conclusions are drawn in Section 5.7 with references listed in Section 5.8.

5.1 Introduction

A software-defined radio (SDR) is expected to support the reception of different communication standards. For that purpose, a wideband radio receiver seems an obvious solution. Some wideband receivers have been reported, e.g., for SDR applications [2] [3], wideband TV receivers [4] [5], and ultra-wideband receivers [6] [7]. However, *wideband receivers are not only wideband to desired signals but also wideband to undesired interference*.

In Section 1.2, we distinguished the in-band interference (IBI) and the out-of-band interference (OBI). For popular mobile communication applications, the IBI can be as strong as -30 to -20dBm while the OBI can be as strong as -10 to 0dBm [8]. An RF band-selection filter is often employed to suppress OBI to below the IBI level, requiring high quality factor and sharp roll-off. These filters are difficult to integrate on-chip and are often dedicated to one specific band. In a SDR receiver, the dedicated RF filter is undesired owing to its poor flexibility. State-of-the-art multi-band receivers [9] [10] use multiple dedicated RF filters in parallel, which increases size and cost for every band that is added. This chapter will propose techniques to improve the robustness of a radio receiver to OBI in order to relax the requirement on RF filters.

At least two mechanisms generate in-band distortion due to OBI: 1) nonlinearity related mixing of strong OBI via, e.g., intermodulation or cross-modulation; 2) harmonic mixing of interferers with LO harmonics due to hard-switching mixers and/or the use of digital LO waveforms. We will quickly review these two mechanisms and detailed discussions can be found in Section 1.2.

Without sufficient RF band-selection filtering, the out-of-band linearity can become the bottleneck since OBI is much stronger than IBI. A wideband LNA as used in [2] and [3] amplifies the desired signal and undesired wideband interference with equal gain. A low voltage gain of 6dB can already clip a 0dBm blocker to a 1.2V supply. The amplified interference also challenges the nonlinear output impedance of an LNA and the linearity of a next-stage mixer. LNA linearization techniques have been proposed via, e.g., derivative superposition

methods [11] [12]. But these techniques mostly compromise the robustness to process spread and deliver only limited benefits for strong interference [13].

Linear time-variant behavior in a hard-switching mixer, or equivalently multiplication with a square wave, not only down-converts the desired signal but also interference around LO harmonics. This harmonic mixing is of much less concern in narrowband receivers, relying on RF band-selection filters. The 8-phase harmonic-rejection (HR) mixers as described in [14] can suppress RF signals around 2^{nd} to 6^{th} LO harmonics but amplitude and phase mismatches limit the achievable HR ratio typically to 30-40dB [3]-[5] [15].

Both out-of-band nonlinearity and harmonic mixing can severely degrade signal-to-distortion ratio. Therefore, in our view *a practical SDR should not just be a wideband receiver, but should also have enhanced out-of-band linearity and enhanced harmonic rejection*. This chapter will propose a low-pass (LP) blocker filtering technique to improve the wideband receiver's linearity, especially its IIP3 for OBI and its tolerance to blockers, without requiring additional feedforward signal paths as used in [16]. Moreover, a 2-stage polyphase HR technique is proposed to improve HR by rejecting harmonics in two successive steps ("iterative") and make HR mixers more robust to mismatch. Via these techniques, we aim at dramatically relaxing the requirements of RF pre-select filters.

5.2 Low-Pass Blocker Filtering

Traditionally, narrowband receiver front-ends use LNA-mixer combinations which can deliver good enough linearity, typically an IIP3<0dBm, for in-band (IB) interference while an RF band-selection filter takes care of out-of-band (OB) interference. However, in a wideband receiver, since OBI is much stronger than IBI, the required OB IIP3 is much higher than the required IB IIP3 and even desensitization can occur due to strong OB blockers. Therefore, frequency selective amplification or attenuation is desired. Tunable band-pass filtering (BPF) is in principle a solution, but it is difficult to provide sufficient selectivity and tunability simultaneously with good noise and linearity, using CMOS on-chip filters. Here we approach the problem from another angle.

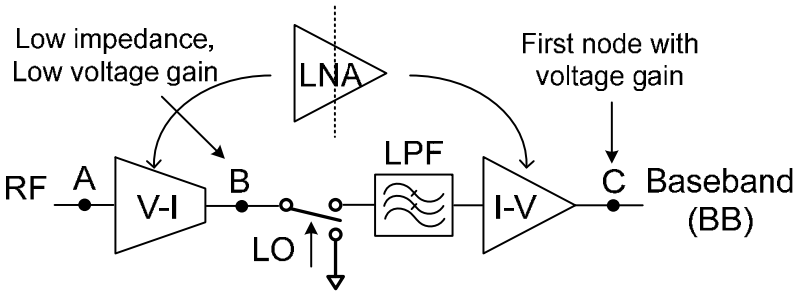

Figure 5.1 Conceptual diagram of the low-pass blocker filtering.

5.2.1 Concept

To guarantee low NF, we need amplification early in the receiver chain. Voltage amplification in an LNA is usually realized via V-I conversion using, e.g. the transconductance of a transistor, followed by I-V conversion via some impedance or transimpedance. We can separate the two functional blocks, V-I and I-V, and insert a passive zero-IF mixer and a low-pass filter (LPF) in between, as shown in Fig. 5.1. The LPF drawn is conceptually current-in current-out and internally with no voltage swing. However in practice, the functions of the LPF and the I-V conversion can be merged by using a frequency-dependent impedance, such as a parallel *R* and *C*.

It is crucial to present a low impedance over a wide band to the output of V-I block, i.e. node B, so that little voltage gain occurs before filtering, leading to less distortion in the mixer and the nonlinear output impedance of the V-I block[1]. Therefore the 1st voltage gain occurs only at baseband after low pass filtering, which provides selectivity to mitigate OBI.

To quantify the blocker filtering effect, we may compare the 1dB compression point (P_{1dB}) for desired signals to the 1dB desensitization point (B_{1dB}) for blockers[2],

[1] Another motivation for low impedance at RF nodes is to widen the receiver's RF bandwidth as exploited in [6].

[2] P_{1dB} thus defines the desired input signal power at which the receiver gain drops by 1dB without applying blockers, while B_{1dB} defines the undesired input interference (single-tone blocker) power where the receiver gain drops by 1dB.

both input referred. Assume a 3rd-order Taylor series for nonlinearity with α_1 and α_3 for the 1st and 3rd order coefficients respectively. Without any blocker filtering, it can be derived from [17] that P_{1dB}=10·log(0.145·|α_1/α_3|) and B_{1dB} = 10·log(0.0725·|α_1/α_3|), if both in amplitude. Therefore, B_{1dB} can be calculated based on P_{1dB}, and if without blocker filtering, B_{1dB} = (P_{1dB}-3dB).

The LPF in Fig. 5.1 can mitigate blockers, and its bandwidth (BW) and order (n) determines the blocker filtering effect. If desensitization happens after I-to-V conversion, which is often the case due to a high voltage gain and limited voltage headroom, the suppression of blockers in dB by the LPF corresponds to the improvement of B_{1dB}.

However, for a wideband receiver the situation is more complicated, as one RF-blocker can be downconverted by different LO harmonics. For instance, a square-wave LO of 400MHz converts a 1250MHz RF signal to 850MHz and 50MHz via the 1st and 3rd harmonic of the LO, respectively. The strongest downconverted signal depends on the blocker frequency (f_B) and the LO frequency (f_{LO}), i.e. which LO harmonic the blocker is closer to. Also it depends on the relative gain of the m^{th} harmonic compared to the fundamental (1st) harmonic, i.e. the m^{th} harmonic rejection ratio (HR_m).

Assume for simplicity that one blocker component dominates after downconversion and determines B_{1dB}. If $|f_B - m \cdot f_{LO}| \leq$BW, i.e. the blocker is within the LPF BW after downconversion by the m^{th} harmonic, we find:

$$B_{1dB} \approx \left(P_{1dB} - 3dB\right) + \min\left[HR_m\right]. \tag{5.1}$$

If $|f_B - m \cdot f_{LO}| >$BW, i.e. the blocker is outside the LPF BW after downconversion by the m^{th} harmonic, assuming an asymptotic filter characteristic, we find:

$$B_{1dB} \approx \left(P_{1dB} - 3dB\right) + \min\left[n \cdot 20\log\left(\frac{\left|f_B - m \cdot f_{LO}\right|}{BW}\right) + HR_m \right]. \tag{5.2}$$

From (5.2) we can expect smaller bandwidth (BW) and higher order (n) of the LPF gives higher B_{1dB}, if f_B, f_{LO} and HR_m are fixed. Besides, we can also improve B_{1dB} via improving P_{1dB}, e.g. if compression happens at the receiver output, a lower receiver voltage gain or a larger output voltage headroom can improve the input referred P_{1dB}, and hence a higher B_{1dB}.

The LPF can help to relax the OB linearity of the I-V conversion, however *not* for the V-I conversion. Therefore, the maximum achievable B_{1dB} is ultimately limited by the P_{1dB} of the V-I conversion minus 3dB. Via a similar mechanism, the OB IIP3 can also be enhanced compared to the IB IIP3. Thus linearity of the V-I conversion is very important and we will return to that point in Section 5.4.1.

5.2.2 Realization

A specific realization of the general concept (Fig. 5.1) is presented in Fig. 5.2. Zero-IF receivers commonly use an LNA followed by a mixer with current output loaded by a LPF to suppress interference. We carry this approach *one step further* by entirely removing the voltage-gain LNA before the mixer and instead use a Low Noise Transconductance Amplifier (LNTA) as the first RF stage for the V-I conversion with input impedance matching. As mentioned before, maintaining a low impedance at node B over a wide band is important. This is realized by using low-ohmic switches in the passive mixers followed by transimpedance amplifiers (TIA) built via negative feedback around operational transconductance amplifier (OTA). The feedback network consists of R & C in parallel to form a LPF. At high frequency, the feedback-loop gain drops so the virtual-ground impedance rises. By putting a capacitor C_{VG} to ground or across the differential virtual-ground nodes, the impedance at high frequency is reduced. Both C_{VG} and C_{FB} contribute to the total LPF function.

Fig. 5.2 also shows, qualitatively, the impedance relationship between node B (Z_B) and node D (Z_D), i.e. Z_B is roughly equal to a certain scaling factor times Z_D plus the mixer switch-on resistance (R_{mixer}) and shifted in frequency. This is because, if the mixer switches work in linear region, the mixer can effectively transfer the impedance at baseband frequency to an impedance at RF, a so-called "*mix-impedance*" that has a property of frequency translation. Applying an RF current input, it can be derived that (see Appendix *A*), for an N-phase mixer driven by $1/N$-duty-cycle (non-overlapping) LO, the impedance Z_B at an RF around m^{th}-LO-harmonic frequency (m=1, 2, 3…), i.e. with an offset frequency Δf from $m \cdot f_{LO}$ ($|\Delta f| \leq f_{LO}/2$), can be written as:

$$Z_B(m \cdot f_{LO} + \Delta f) \approx R_{mixer} + \frac{N}{m^2 \cdot \pi^2} \cdot \sin^2\left(\frac{m \cdot \pi}{N}\right) \cdot Z_D(\Delta f), \qquad (5.3)$$

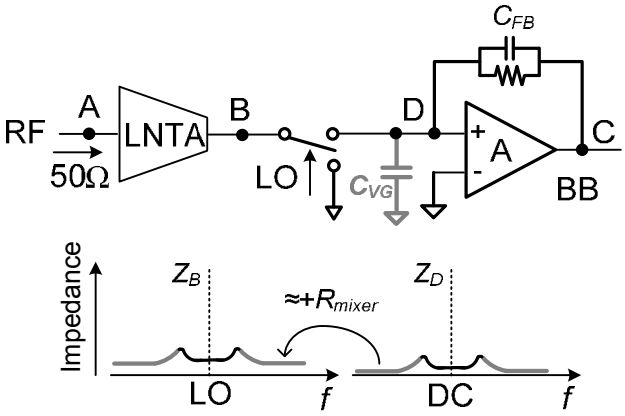

Figure 5.2 Realization of the low-pass blocker filtering and illustration of the impedance transfer effect (from Z_D to Z_B)

given that Z_D presents strong filtering effect, e.g. a pole at a much lower frequency than f_{LO}, which is normally the case for a down-mixer. Consider m=1: for N=2 or 4 the coefficient of Z_D is about 0.2, and it is about 0.12 for N=8 and about 0.06 for N=16, showing R_{mixer} actually plays a much larger role in determining Z_B. For m>1, the coefficient of Z_D is even smaller. On the other hand, if R_{mixer} is negligible, having a bigger N may give a lower Z_B which is good for linearity.

Besides delivering low impedance, this topology (Fig. 5.2) can also bring two other advantages exploited in some *narrowband* receivers [18]-[20]: 1) good *in-band* linearity in the I-V conversion due to the negative feedback; 2) low 1/*f* noise from the mixer switches working in the linear region which carry little DC current. To our knowledge, this work [21] is the first to exploit this topology in a *wideband* receiver to enhance *out-of-band* linearity. If the LPF suppresses the OBI well, the main contributor to the OB nonlinearity will come from the V-I conversion of the LNTA, which can be quite linear as we will see later.

Although voltage amplification is avoided at RF, if the transconductance of LNTA is big, the receiver-input referred noise of the following stages, i.e. mixer and TIA, can be relatively small, so that the overall receiver NF can still be good and

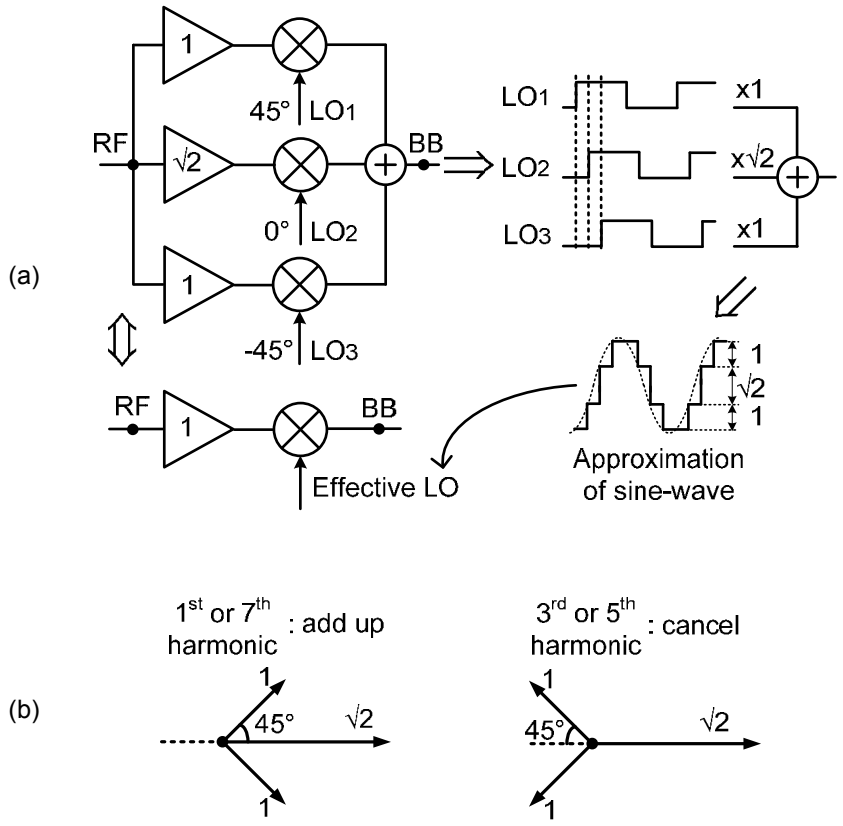

Figure 5.3 (a) Block diagram of a traditional HR mixer; (b) its vector diagram

dominated by LNTA itself. As an example, the whole receiver in [20] achieves a NF of 2.2dB based on a similar topology but in a narrowband configuration.

5.3 2-stage Polyphase Harmonic Rejection

The low-pass blocker filtering technique presented in Section 5.2 acts after mixing, so it cannot prevent the harmonic mixing already occurring in the mixer stage. It is known that using balanced LO can suppress all even-order harmonics. To also suppress odd-order harmonics, harmonic-rejection (HR) mixers using multi-phase

square-wave LOs driving parallel operating mixers have been proposed before [14]. Fig. 5.3 (a) shows an example, where the weighted current outputs add up to approximate mixing with a sine-wave LO. The combination of an amplitude ratio of 1:√2:1 and an 8-phase LO[3] (equidistant 45°) can reject the 3rd and 5th harmonics, as shown in the vector diagram of Fig. 5.3 (b). The 7th harmonic is not rejected and still needs to be removed by filtering, but the filter requirement is strongly relaxed compared to the case of a normal double-balanced I/Q mixer whose first un-rejected harmonic is the 3rd order. However, the achievable HR ratio is limited by the accuracy of the amplitude ratios and the LO phases.

To achieve high HR ratio we need to accurately implement the desired weighting ratios, in this case the irrational ratio 1:√2 accurately on chip. There are at least two challenges here: 1) realizing the right nominal (average) ratio; 2) keeping random variations due to mismatch small enough. To address these issues we propose a 2-stage polyphase HR concept (see Fig. 5.4) in which 2-stage *iterative* weighting and summing results in much higher HR than traditional HR mixers with only 1-stage. We will show that this iterative weighting results in a small product of relative errors for random variations, whereas the use of suitably chosen integer ratios results in sufficient accuracy to achieve a HR well above 60dB.

5.3.1 Block Diagram

Fig. 5.4 shows the block diagram of the 2-stage polyphase HR system, implemented on chip. The irrational ratio 1:√2:1 is realized in two iterative steps with integer ratios: a first step with 2:3:2 and a second step with 5:7:5. The 1st-stage weighting is realized via 7 unit-LNTAs interconnected in 3 parallel groups to form the 2:3:2 ratio. The 2nd-stage weighting is realized via a baseband resistor network "R-net" between the TIA1 and TIA2 stages. The 5:7:5 amplitude ratio corresponds to the 7:5:7 resistance ratio. The passive mixer array is driven by 8-phase 1/8-duty-cycle (non-overlapping) LO. Via the combination of the LNTA, mixer and TIA with LPF, the 1st voltage gain occurs at baseband after LPF for good OB linearity. Since harmonics can be as strong as blockers, it is important to have significant HR before the first voltage gain, especially because the anti-blocker filtering doesn't reduce harmonic images close to harmonics of the LO, as

[3] More LO phases can reject more harmonics, but complicating the LO generation.

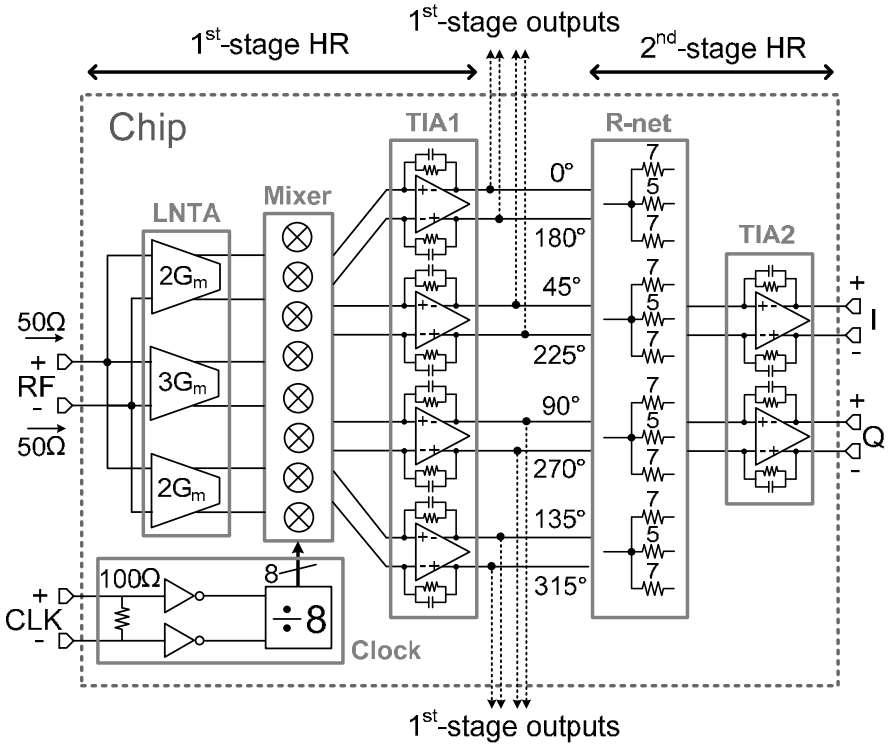

Figure 5.4 Block diagram of the chip implementing
the 2-stage polyphase HR and the low-pass blocker filtering

shown in (5.1). The additional more accurate HR follows in the 2nd stage, aiming to bring residual harmonic images below the noise floor.

5.3.2 Working Principle

We will now show how to accurately approximate 1:√2:1 via 2:3:2 and 5:7:5. A key point is that the output of the TIA1 stage has 8 IF-outputs with equidistant phases, i.e. 0° to 315° with 45° step, instead of the conventional 4 phases, i.e. quadrature. This enables iterative HR by adding a 2nd stage. Fig. 5.5 shows the weighting factor for the 8 outputs of the 1st-stage HR versus time (t) for one complete period of the LO (T). If we weight and sum three adjacent-phase outputs of the 1st-stage HR via the 2nd-stage weighting factors 5:7:5, as shown in Fig. 5.6,

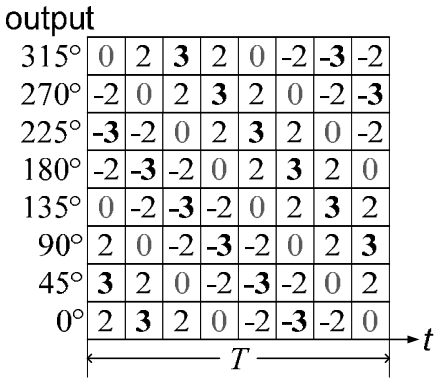

Figure 5.5 Weighting factors for the 1st-stage HR outputs versus time (t) in one period (T)

$$
\begin{array}{r}
[\,2 \quad \mathbf{3} \quad 2 \quad 0 \quad -2 \quad \mathbf{-3} \quad -2 \quad 0] \cdot 5 \\
+\,[\,0 \quad 2 \quad \mathbf{3} \quad 2 \quad 0 \quad -2 \quad \mathbf{-3} \quad -2] \cdot 7 \\
+\,[-2 \quad 0 \quad 2 \quad \mathbf{3} \quad 2 \quad 0 \quad -2 \quad \mathbf{-3}] \cdot 5 \\
\hline
[\,0 \;\; 29 \;\; 41 \;\; 29 \;\; 0 \;\; -29 \;\; -41 \;\; -29]
\end{array}
$$

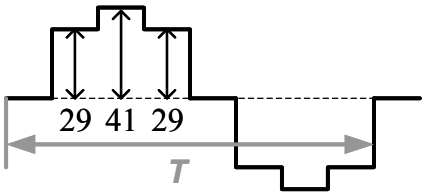

Figure 5.6 Approximation of 1:√2:1 as 29:41:29 via integer ratios

we find 29:41:29. The ratio 41:29 is equal to 1.4138, which represents only a 0.028% error from √2. This amplitude error corresponds to a HR ratio of more than 77dB, if no phase error.

The 2-stage polyphase HR not only can approximate 1:√2:1 very closely, but it is also robust to amplitude mismatch, as illustrated in Fig. 5.7 via vector diagrams of the two stages. It shows how, for the desired signal, polyphase contributions from three paths add up, while for the 3rd and 5th harmonics, they cancel nominally.

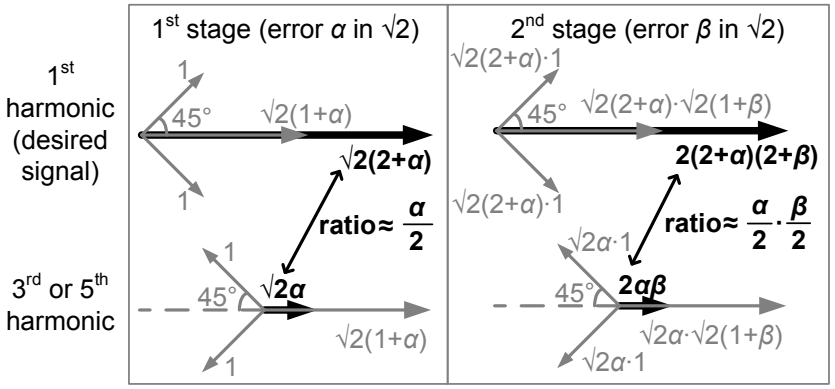

Figure 5.7 Error reduction principle in the 2-stage polyphase HR (error $\alpha/2$ becomes a much smaller product of errors: $\alpha\beta/4$)

Assume now that the error in realizing √2 dominates and model it as a relative error α for the 1st stage and β for the 2nd stage. Also for simplicity, assume that the desired signal and the 3rd and 5th harmonics are equally strong at the receiver input and neglect the relative strength of different LO harmonics due to a certain LO duty cycle. After the 1st stage, the desired signal is multiplied by $\sqrt{2}\cdot(2+\alpha)$ and the 3rd and 5th harmonics by $\sqrt{2}\cdot\alpha$, leading to a relative error (interference-to-signal ratio) of $\alpha/2$ if $\alpha<<2$. For the second stage the same derivation holds. As the two stages are cascaded, the product of the gains determines the result, i.e. the total gain for the desired signal becomes $[\sqrt{2}\cdot(2+\alpha)]\cdot[\sqrt{2}\cdot(2+\beta)]$ and for the 3rd and 5th harmonics it is $[\sqrt{2}\cdot\alpha]\cdot[\sqrt{2}\cdot\beta]$. This renders a total relative error (interference-to-signal ratio) of

$$\frac{2\alpha\beta}{2\cdot(2+\alpha)\cdot(2+\beta)} \approx \frac{\alpha}{2}\cdot\frac{\beta}{2}. \tag{5.4}$$

if $\alpha<<2$ and $\beta<<2$. Therefore, the total relative error is the *product* of the relative errors for the two stages, $\alpha/2$ and $\beta/2$. If the 2nd stage has an error β=1%, ideally this improves HR by $(\beta/2)^{-1}$, i.e. 46dB, which has also been confirmed by simulation.

Please note that the product of errors, as shown in (5.4), holds for both 3rd and 5th harmonics. Moreover, it not just works for mismatch induced errors but for any

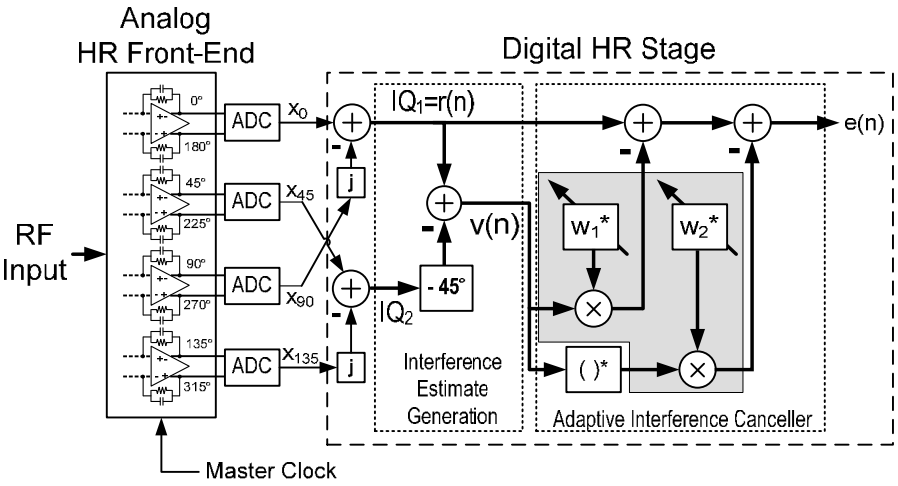

Figure 5.8 A system-level overview of the analog HR front-end connected with the digital HR stage

amplitude errors, e.g. errors introduced by parasitic capacitance or finite LNTA output impedance.

Theoretically, more than 2 stages can achieve even better amplitude accuracy, but practically phase accuracy will often dominate. To also address the phase error, a HR concept that exploits digital adaptive interference cancelling techniques [22] [1] can be applied to improve the HR for one dominant harmonic, either of 3rd or 5th order. The digitally-enhanced HR concept has been verified based on the analog front-end 1st-stage presented in Fig. 5.4. It provides 8-phase (4 differential) baseband outputs to a digital processor. The extra outputs deliver extra information compared traditional quadrature baseband signals, enabling digital enhancement of HR. An overview of the whole system is shown in Fig. 5.8. It uses the power of digital techniques to solve analog problems and can be a useful alternative to the 2-stage polyphase HR technique. Both techniques improve HR by rejecting harmonics in two successive steps ("iterative"). They use a second stage, either analog or digital, to dramatically improve the HR from the first stage. Details of the digital HR technique can be found in [1] but will not be described further in this thesis. Next we will look at the implementation of the receiver's analog front-end.

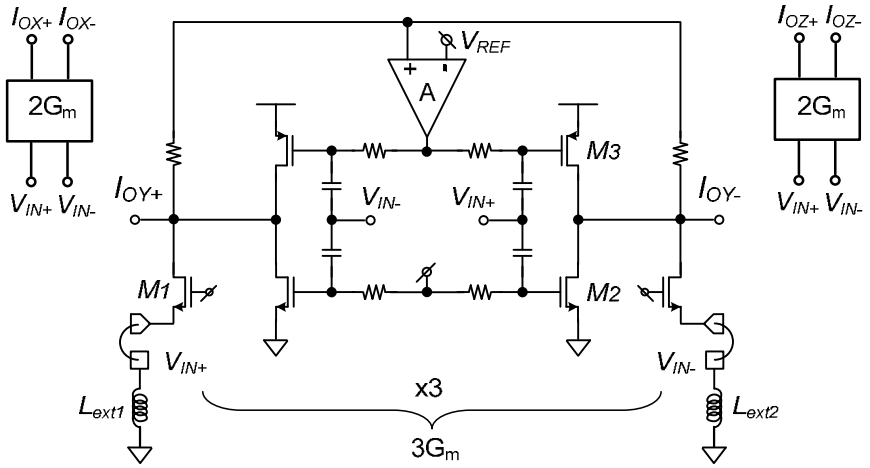

Figure 5.9 The low-noise transconductance amplifiers (LNTA) implementing $3G_m$ (shown on transistor level) and two blocks of $2G_m$ (identical schematic)

5.4 Chip Implementation

A SDR receiver chip has been implemented in 65nm CMOS to verify the two concepts proposed in the previous sections. The block diagram of the chip has been shown in Fig. 5.4. The signal path consists of LNTAs, passive mixers, and 2-stage TIAs with 2nd-stage HR-weighting via a resistor network (R-net). The first voltage gain should be at baseband after LPF for good OB linearity, as discussed in Section 5.2, and the realization of 2-stage polyphase HR has been described in Section 5.3. The 8-phase LO is derived via a divide-by-8 from an off-chip signal CLK, i.e. the master clock. The receiver can be reconfigured to deliver either 8-phase outputs from TIA1 or I/Q outputs from TIA2. The 8-phase outputs interface to off-chip ADCs for digitally-enhanced HR measurements [1] while the TIA2 stage is switched off. To better understand the implementation, a more detailed description for some key blocks follows.

5.4.1 Linear LNTA

Fig. 5.9 shows the schematic of a pseudo-differential unit-LNTA, of which there are 7 units in parallel to form three LNTAs with 2:3:2 ratio, sharing the same external (large-value) inductor to GND for DC bias. The common-gate (CG) transistor *M1* provides input matching while the input is also connected to the AC-coupled inverter consisting of common-source (CS) transistors *M2* and *M3*. For each single-ended half, all 7 unit-LNTAs together deliver an impedance matching with the source impedance R_S=50Ω and a total transconductance $g_{m,tot}$=100mS ($g_{m,CG}$=20mS, $g_{m,CS}$=80mS). A common-mode feedback (CMFB) loop using high-ohmic resistors and an amplifier "A" controls the PMOS transistors and ensures all three LNTA outputs are biased around V_{REF}=600mV. In total the three differential LNTAs draw 14mA from a 1.2V supply.

The noise behavior of the LNTA can be understood by studying a single-ended half, which consists of a CG transistor *M1* and two CS transistors *M2*/*M3*, sharing the same input V_{in+}. Considering the LNTA output noise in the current domain, the noise factor can be written as

$$F = 1 + \frac{kT\gamma g_{m,CG} \cdot (1 - R_S \cdot g_{m,CS})^2}{kTR_S \cdot g_{m,tot}{}^2} + \frac{4kT\gamma g_{m,CS}}{kTR_S \cdot g_{m,tot}{}^2}. \tag{5.5}$$

The 2nd term considers the partial noise cancelling of the CG transistor noise [23] and the 3rd term considers the noise from the CS transistors. If take R_S=50Ω, $g_{m,CG}$=20mS, g_{mCS}=80mS, and $g_{m,tot}$=100mS into (5.5), we get F=1+9γ/25+16γ/25 =1+γ. If γ is in the range of 2/3 to 1, the noise figure (NF) would be 2.2 to 3dB.

For wideband operation, minimum-length transistors are used to achieve S_{11}<-10dB to more than 6GHz RF (simulation). Since the input impedance of a CG transistor depends on its drain impedance [24], a wideband low impedance at its output, i.e. node B in Fig. 5.2, is desired for wideband input matching. This fits well to what is desired for linearity as discussed in Section 5.2.

Since the LPF improves the OB linearity of I-V conversion (Fig. 5.1), the V-I linearity sets the ultimate limit of OB linearity. To obtain a good V-I linearity, high (V_{GS}-V_{TH}) and high V_{DS} is desired. In our VDD=1.2V design, (V_{GS}-V_{TH}) is larger than 250mV and V_{DS} is 600mV.

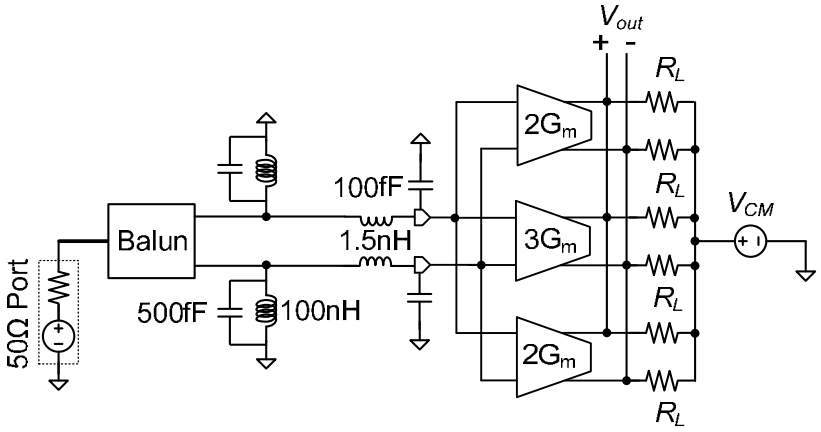

Figure 5.10 LNTA simulation setup, modeling pad and bondwire parasitics (100fF and 1.5nH)

A simulation setup is built as shown in Fig. 5.10, using an ideal balun and external big inductors L=100nH with parasitic capacitance[4] of 500fF. It also models the pad capacitance of (100fF) and bondwire inductance (1.5nH). *Each* of the three LNTAs is loaded by a pair of resistors R_L to model the input impedance of the next stage mixers. To average out the effect of different LNTA transconductance (2:3:2), the simulation is carried out with all three LNTAs combined together as well as their individual R_L. These resistors (R_L) are biased at V_{CM}=600mV to emulate the baseband DC voltage in the actual design.

Simulation shows S_{11}<-10dB from 100MHz to 6GHz for R_L between 1Ω and 1kΩ. For linearity test, the two input tones are at 801MHz and 802MHz. Fig. 5.11 shows the IIP3 simulation results, considering process spread. Simulations predict an IIP3 of more than +15dBm if R_L<100Ω and only ±1dB variation over different process corners, indicating that high LNTA linearity robust to process spread is possible if we keep voltage gain low (small R_L).

[4] This parasitic capacitance is also exploited to provide bandwidth extension for the input impedance matching, in combination with the bondwire inductance and the pad capacitance [3].

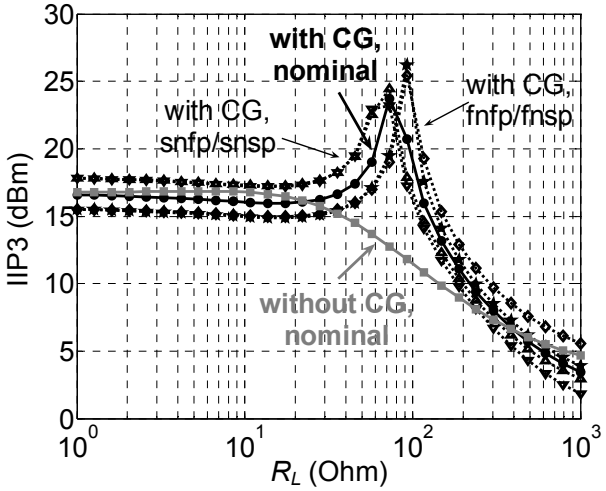

Figure 5.11 Simulated LNTA IIP3 versus load impedance (R_L) for different process corners (sn: slow-NMOS, sp: slow-PMOS, fn: fast-NMOS, fp: fast-PMOS)

Actually, it turns out that the addition of the CG-stage in parallel to the inverters has a nonlinearity cancellation effect that improves IIP3 for R_L between about 20Ω and 200Ω, which determines the V_{ds}-related distortion terms (for the case without a CG-stage, see the grey curve in Fig. 5.11). Simulation and analysis indicate that it is mainly the pre-distortion at the inverter inputs introduced by the CG-stage via its source current, to cancel the distortion generated by inverter itself. Nevertheless, since we are interested in using a low R_L value, produced by mixer switches, to deliver signal current into the TIA stage, here we don't discuss this effect further.

A differential LNTA requires an off-chip balun if a single-ended antenna or RF filter is used. Compared to an LNTA with single-ended input, although the differential one may double the power consumption [25], it can render better IIP2. Besides, the input voltage swing on each of the differential inputs is lowered by 3dB, which improves LNTA IIP3 and P_{1dB} by 3dB.

Using the same setup as Fig. 5.10, simulations with R_L=50Ω (the designed input impedance of the mixer) show input referred P_{1dB}=+4dBm, NF<3dB (only including noise from LNTA), and voltage gain=-1dB for each single-ended output

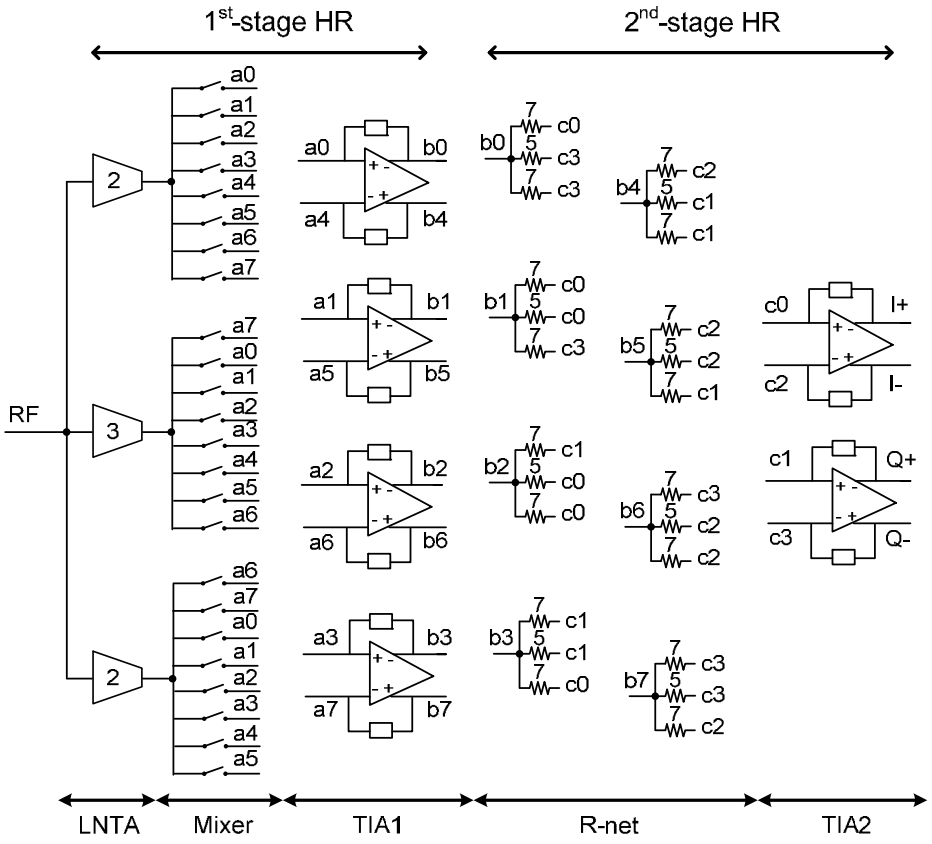

Figure 5.12 Complete connection of
the 1st-stage HR (single-ended RF input shown) and the 2nd-stage HR

(low voltage gain as desired for good linearity) with -3dB bandwidth >7GHz. This wide RF bandwidth benefits from the low impedance (real part) at the output of LNTA, which means the dominant pole is located at a very high frequency given a certain capacitance.

5.4.2 Passive Mixer

Each of the three LNTAs with 2:3:2 ratio connects to 8 passive current-commutating mixer arrays driven by 8-phase LO, as shown in Fig. 5.4. The mixers are DC-coupled to the LNTAs for wider bandwidth compared to AC-coupled,

which introduces parasitic capacitance. Each mixer array receives 3 differential inputs from LNTAs and all mixer arrays together deliver 4 differential outputs to TIA1, i.e. 8-phase signals with 45° interval. The complete connection from LNTA to TIA1 via passive mixer switches can be found in Fig. 5.12, with single-ended RF input for figure clarity.

The passive mixer simply consists of NMOS switches, with bulk tied to source to reduce the body effect, for a minimized R_{mixer} at a certain V_{GS}. The bulk and source joint node is at the baseband side of the switch, to reduce the effect of parasitic capacitance from substrate. The gate of the mixer switch is AC-coupled to a clock driver and biased so that the maximum V_{GS}=VDD.

The mixer switch-on resistance R_{mixer} is in the order of 50Ω and all mixer switches have the same dimension for good phase accuracy. Besides, the same R_{mixer} and different LNTA output impedance (3:2:3) also introduce a current division effect which brings the actual 1st-stage weighting ratio different from 2:3:2 but closer to the ideal 1:√2:1 ratio, good for the overall amplitude accuracy.

For good NF, we need to minimize clock overlap to avoid a low-ohmic path between TIA inputs that will amplify TIA noise [18]. For the case with 8 TIA inputs this leads to a maximum LO duty cycle of 1/8. Both sides of the mixer, i.e. the output of LNTA and the input of TIA, are biased at the same DC level (around half VDD) ensuring that little DC current flows for a low 1/f noise from the mixer switches.

As an alternative to mixer switches working in the linear region when turned on, using switches in the saturation region (e.g. switches in a Gilbert mixer) may also provide low impedance as $1/g_m$. However, working in the saturation region would require DC current flowing through those switches, degrading $1/f$ noise.

5.4.3 Accurate Multiphase Clock

Since the amplitude accuracy can be ensured by the 2-stage polyphase HR, the phase inaccuracy is likely to dominate. Based on Appendix *B*, if the LO duty cycle is "*d*", the resulting 3rd HR (1σ) is:

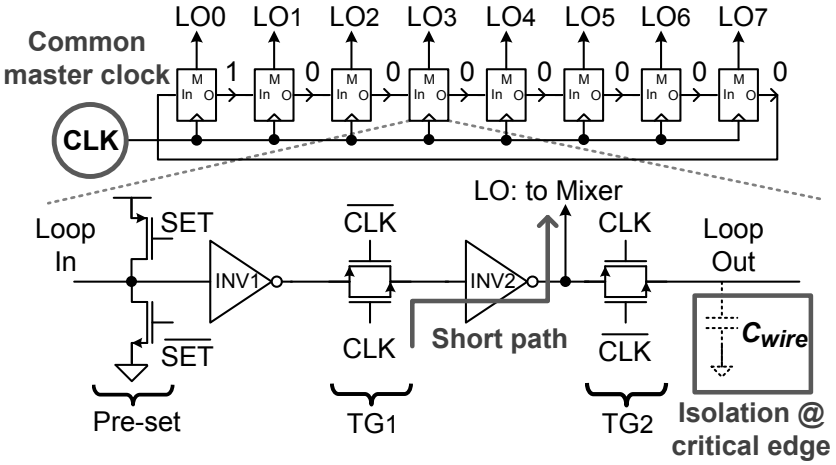

Figure 5.13 An 8-phase clock generator with small phase mismatch (one flip-flop unit is shown on transistor level)

$$HR3 = 10\log\left(\frac{\sin^2(\pi\cdot d)}{\sin^2(3\pi\cdot d)}\cdot\left[\left(\frac{\sigma_A}{12}\right)^2+\left(\frac{\sigma_\varphi}{4}\right)^2\right]^{-1}\right), \tag{5.6}$$

where σ_A and σ_φ are the standard deviation in the amplitude and phase respectively. For d=1/8 and negligible amplitude error ($\sigma_A \rightarrow 0$) due to the 2-stage technique as in (5.4), to reach 60dB HR (3σ), the required phase error is σ_φ=0.03°.

To build a multiphase clock generator with low phase mismatch, two design principles are applied: 1) to use a common master clock to derive all phases; 2) to minimize the path from the common master clock to the mixer switches therefore to minimize mismatch accumulation.

Fig. 5.13 shows a divide-by-8 ring counter using eight dynamic transmission-gate (TG) flip-flops (FF). The same master clock (CLK), with 8-times the LO frequency, drives all FFs. Only one inverter (INV2) is used as a buffer to minimize the path from CLK to mixer.

A preset data pattern is required to deliver the desired 1/8 duty cycle. Each LO phase controls 6 mixer switches connecting to differential outputs of three LNTAs.

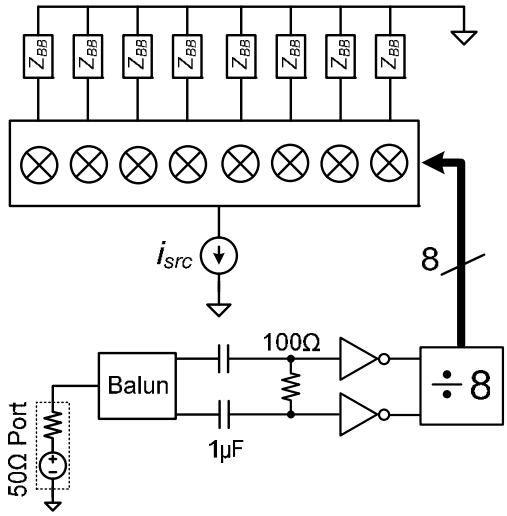

Figure 5.14 Simulation setup for LO phase mismatch, including the effect of real mixer switches

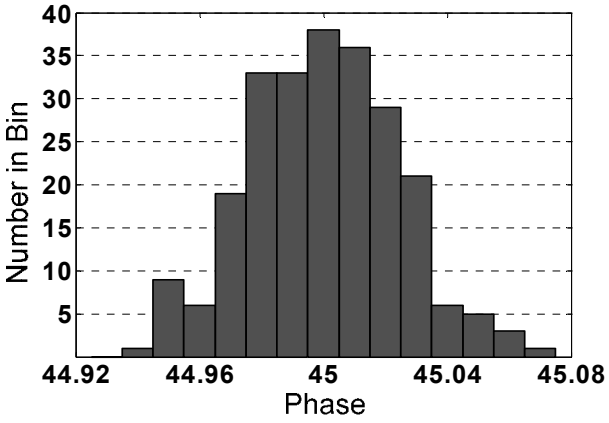

Figure 5.15 Histogram of the simulated phase difference between two adjacent LO outputs (240 Monte Carlo simulation results)

The gates of all the 6 switches are connected together and driven by the same buffer, i.e. INV2, to minimize buffer mismatch.

In a ring counter, all flip-flops "see" the same environment. However, a loop is not convenient in layout and it may need different wiring lengths between each two flip-flops, degrading phase accuracy. A careful layout strategy is adopted to minimize the wiring differences. Moreover, when the critical LO edges occur, the largest part of the wiring (C_{wire}) is isolated from the output of INV2 via TG2, decreasing rise and fall times and reducing the effect of wiring mismatch.

The phase error reported in [21] is found to be too pessimistic due to an incorrect simulation test-bench. The new simulation setup is shown in Fig. 5.14. It uses an ideal balun, 1μF AC-coupling capacitors, and a 100Ω matching resistor. The sine-wave input is converted to square-wave via the on-chip buffers. The divide-by-8 block drives the 8-phase mixers with an ideal input current source. The phase error is checked at baseband, which is loaded by 10Ω and 10pF in parallel to emulate the baseband impedance Z_{BB} in the actual design.

Fig. 5.15 presents the simulated phase deviation from 45° between two adjacent 0.8GHz LO phases due to mismatch, including the contribution from mixer switches. The histogram shows a maximum phase error of only 0.07° and it yields σ=0.024°, i.e. 0.08ps for 0.8GHz. This clock performance is hence compatible with HR>60dB (3σ).

The master clock CLK comes from an off-chip generator followed by a pair of inverters as on-chip buffer. Simulation shows, at 0.8GHz LO, the power consumption of the divider is 5.4mA at 1.2V supply and the input buffers consume 8.9mA driven by 6.4GHz differential input clock.

In simulation, the divide-by-8 can work up to 1.25GHz LO (10GHz CLK) in nominal case although it can vary with process corners. The up-side LO frequency is mainly limited by the large division ratio, i.e. 8. If a higher LO frequency is wanted, a divide-by-2 may be used to generate 4-phase (quadrature) LO instead of the divide-by-8, and then the receiver in Fig. 5.4 can be reconfigured to a quadrature wideband receiver without HR, as will be described in Section 5.5, when harmonic mixing is less to be a problem at higher bands.

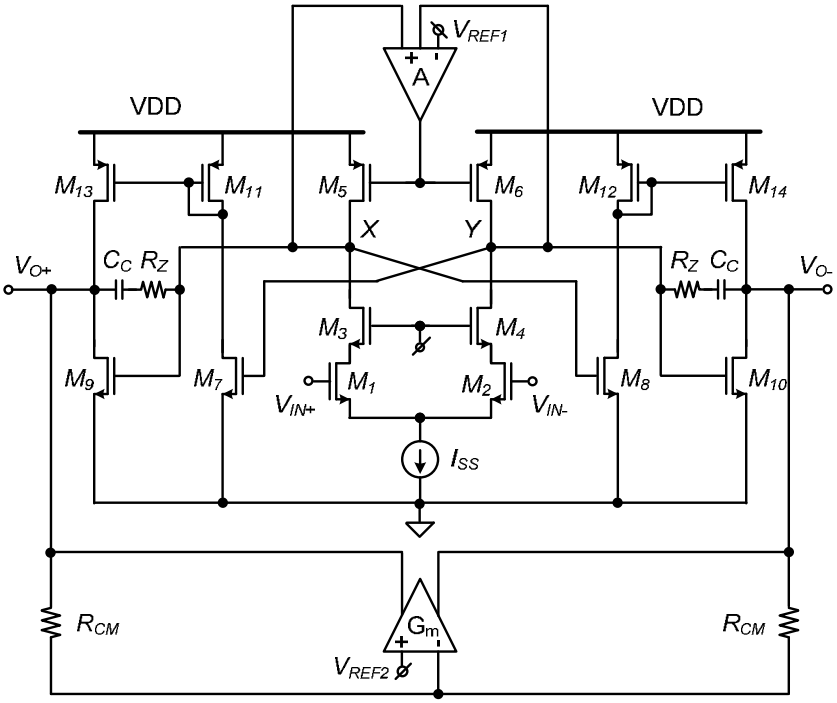

Figure 5.16 The OTA schematic with class-AB push-pull output stage and two common-mode (CM) feedback loops

5.4.4 High-Swing TIA

Since the voltage gain occurs at the outputs of the TIA1 stage where interference is only partly suppressed, we chose an OTA topology able to handle large voltage swing, which helps tolerate large blockers. It is a two-stage class-A/AB OTA based on [26] but with modifications. The main feature of this OTA is the class-AB push-pull output stage, which can achieve large output voltage swing. The circuit schematic is shown in Fig. 5.16.

Start from looking at the first stage (M_1-M_6). The input pair M_1-M_2 uses NMOS transistors in weak inversion for a high g_m/I_{DC} ratio leading to low thermal noise and high gain and a big size leading to low $1/f$ noise. The cascode transistors M_3-M_4 are applied for three purposes: 1) to isolate the 1st-stage output high-impedance nodes (X/Y) from the drain capacitance of big M_1-M_2 to improve the speed; 2) to

improve the output impedance of first stage and therefore to improve the OTA voltage gain, which is crucial for a high closed-loop in-band linearity; 3) to prevent the relatively high voltage swing at the X/Y nodes from seeing the drain of M_1-M_2, so to reduce the effect of channel-length modulation. The PMOS loads M_5-M_6 use a large V_{GS} and V_{DS} and a large length, which lead to low thermal and $1/f$ noise and a high output impedance comparable to R_{out} from the NMOS side M_1-M_4. At nodes X/Y, enough voltage headroom is reserved to handle more than 250mV peak-to-peak voltage swing on each side.

For the OTA's second stage (M_7-M_{14}), a class-AB push-pull output stage is used, which can handle more than 2V peak-to-peak differential output voltage swing at VDD=1.2V. This push-pull capability is obtained via the current mirrors M_{11}-M_{14}, whose DC current can be well defined by the common-mode level of the first-stage outputs. To ensure a low overdrive voltage for high output voltage swing and at the same time to accommodate the relatively high common-mode level at the X/Y nodes due to the cascode transistors M_3-M_4, high-V_{TH} NMOS transistors M_7-M_{10} are used, which are naturally available in the standard digital CMOS process without adding any extra cost.

For the differential-mode feedback (DMFB) loop, Miller compensation via resistor R_Z and capacitor C_C guarantees 55° minimum phase margin over all process corners. Due to the use of a current mirror, the common-mode output voltage of the second stage is not influenced by that of the first stage. Therefore, two common-mode feedback (CMFB) loops are required in this OTA, i.e. a voltage-sense voltage-control loop for the first stage and a voltage-sense current-control loop for the second stage respectively, as shown in Fig. 5.16.

In our design, the difference from what was presented in [26] are mainly two points: 1) the input pair is changed from PMOS to NMOS (M_1-M_2) to accommodate the DC voltage at the virtual-ground node, which is defined by LNTA to be half VDD for maximum voltage swing (Fig. 5.4); 2) the addition of cascode transistors M_3-M_4 for improved performance as discussed before.

Each OTA draws 3.2mA from 1.2V supply, with 2mA in the first stage and 1mA in the second stage while two CMFB loops and bias circuitry together consume

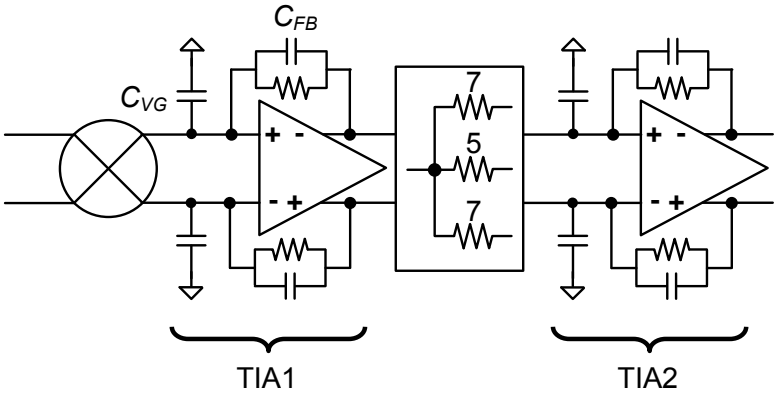

Figure 5.17 Two-stage fully-differential TIA configuration

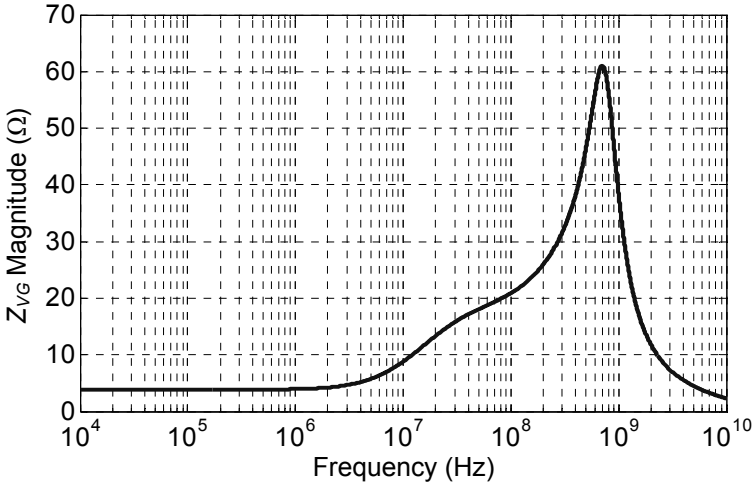

Figure 5.18 TIA1 virtual-ground node impedance (Z_{VG}) versus frequency

0.2mA. Simulations of the OTA for the nominal case show 63dB open-loop gain and 3.5GHz unity-gain bandwidth, with only slight difference over process corners.

When applying the OTA into the TIA (Fig. 5.17), a parallel RC feedback network as well as C_{VG} implements a 1st-order LPF to perform blocker filtering. Each of the two TIA stages has a LPF -3dB bandwidth of 20MHz and together they determine

the receiver IF bandwidth of 12MHz, which may accommodate most mobile communication standards.

The virtual-ground impedance (Z_{VG}) of the TIA1, as shown in Fig. 5.18, has a magnitude of about 4Ω around DC and peaks to 60Ω around 700MHz due to a lowered loop gain while a 5pF C_{VG} brings impedance down at higher frequencies. Applying (5.3) to multiply Z_{VG} with a coefficient of 0.12 and consider R_{mixer}=50Ω, we know that R_{mixer} will dominate the mix-impedance value at node *B* of Fig. 5.2.

The two TIA stages use the same OTA design but different component values in the RC feedback. The feedback resistor of the TIA1 stage is 1kΩ and that of the TIA2 stage is 2kΩ. The simulated gain of the receiver after the TIA1 stage is 27dB and after the TIA2 stage the gain is 34dB.

5.4.5 Baseband R-net

The resistor network (R-net) provides the 2nd-stage weighting for HR. It also converts 8-phase outputs of the TIA1 stage into quadrature inputs of the TIA2 stage. To form a 5:7:5 amplitude ratio, 19 unit-resistors form a resistance ratio of 7:5:7 in 3 paths. As shown in Fig. 5.12, the R-net consists of weighted resistor groups each with a ratio of 7:5:7 and there are 8 groups in total to interface the 8 outputs of TIA1 stage. Harmonic rejection at baseband (via R-net) can also reduce errors due to parasitic capacitance compared to at high frequency.

5.5 Receiver Frequency Range Extension

The divide-by-8 is used to generate accurate LO phases for HR, which requires the common master clock frequency to be 8-times the LO frequency. Indeed the LO path limits the receiver frequency range to 1.25GHz (simulation). However, the signal-path bandwidth should be much wider as mentioned in Section 5.4.1 because: 1) minimum-length transistors (65nm) are used in the LNTA which guarantees S_{11}<-10dBm up to 6GHz as simulated; 2) a low real impedance is presented to the output of the LNTA so that the RC time constant is small, which allows a -3dB bandwidth of 7GHz in simulation. To explore the wideband property, we should extend the LO frequency range.

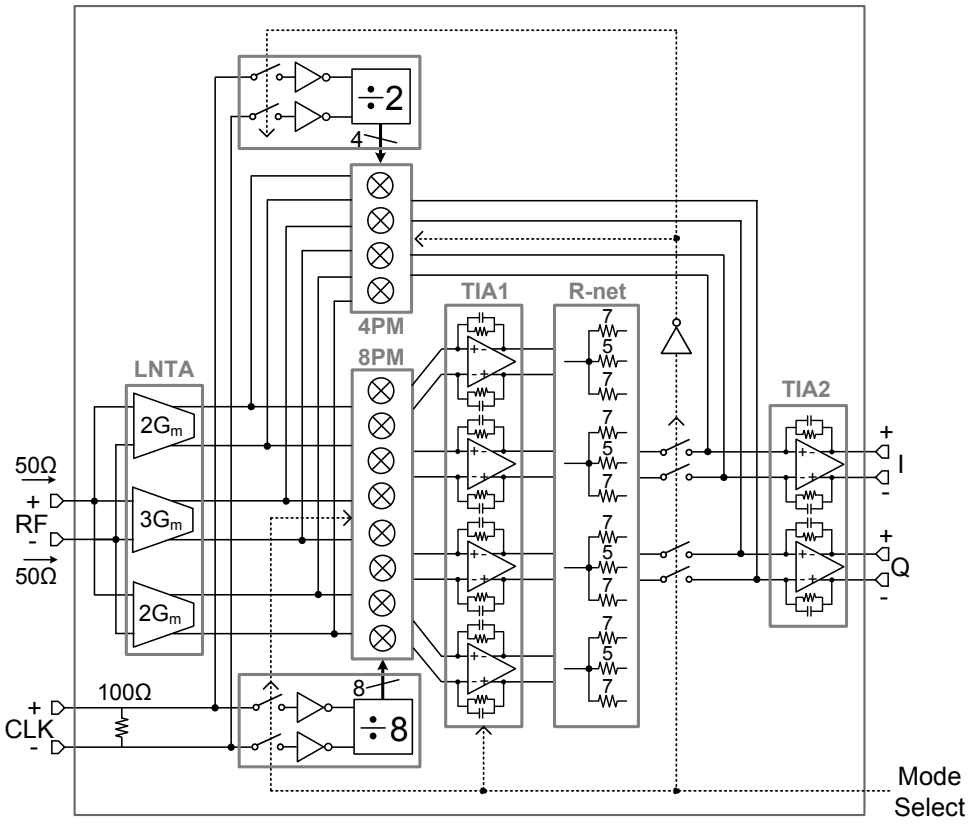

Figure 5.19 Reconfigurable 0.4-to-5GHz receiver block diagram

If a higher LO frequency is wanted, a divide-by-2 may be used to generate 4-phase (quadrature) LO, instead of the divide-by-8, which can be expected to extend the LO frequency by 4 times assuming the same maximum speed of the master clock. Since harmonic mixing is mainly problematic for relatively low LO frequencies, e.g. <1GHz, as observable from Fig. 1.1 of spectrum allocation, the 4-phase LO can be used as an alternative at high bands. Then the 2-stage polyphase HR architecture (Fig. 5.4) can be made reconfigurable by adding a quadrature 4-phase mixer driven by a 4-phase LO in parallel to the presented 8-phase mixer to extend the receiver's frequency range.

Fig. 5.19 shows the block diagram of the extended receiver with a 4-phase mixer added, driven by a 25%-duty-cycle LO generated via a divide-by-2, which can still

generate accurate balanced LO to reject the even-order harmonics. Which divider is enabled (via Mode Select) determines either the 4-phase mixer (4PM) or the 8-phase mixer (8PM) in use. In case of the 4-phase mixer, the divide-by-2 is enabled while the divide-by-8 is disabled and the gate bias voltages are set to GND for all 8-phase mixer switches. Both mixers share the same switch size.

The 4-phase mixer consists of 4 mixer arrays in parallel each driven by an LO phase. Each mixer array consists of 6 NMOS switches which receive 3 differential inputs from LNTAs and all mixer arrays together deliver I/Q differential outputs to the virtual ground nodes of the TIA2 stage while the TIA1 stage can be shut down to save power. Big-sized NMOS switches are applied between the R-net and the TIA2 stage, which only turn on when the 8-phase mixer is in use.

When the receiver is configured to the 4-phase mode, the feedback resistor of the TIA2 stage is set to 1kΩ to keep about the same receiver gain (~34dB) while 2kΩ was used in the 8-phase mode and extra capacitors are connected to maintain the IF bandwidth of 20MHz. Still, the low-pass blocker filtering is effective since the 1st voltage gain occurs at baseband after the LPF of the TIA2 stage.

The whole reconfigurable 4/8-phase receiver including the divide-by-2/8 has been realized in schematic transistor-level and simulation has been done using all real components. In simulation, the divide-by-2 works up to 5GHz LO (master clock at 10GHz). The gain is consistently around 33dB and the NF is around 4dB up to 5GHz RF while the IIP3 is +5dBm. Please note that the power consumption in the 4-phase mode can be 12mA lower than the 8-phase mode since the TIA1 stage is turned off. These results show the promise to reconfigure the 2-stage polyphase HR system to achieve a broader RF range.

Unfortunately, due to limited time, the reconfigurable receiver was only ready in schematics but was not integrated into the final chip layout. Nevertheless, the basic ideas of building SDR receivers robust to OBI, via the low-pass blocker filtering and the 2-stage polyphase HR techniques, can already be demonstrated via the 8-phase receiver path. The wideband property of the receiver signal-path can also be proved by measurement, as to be shown in Section 5.6.1.

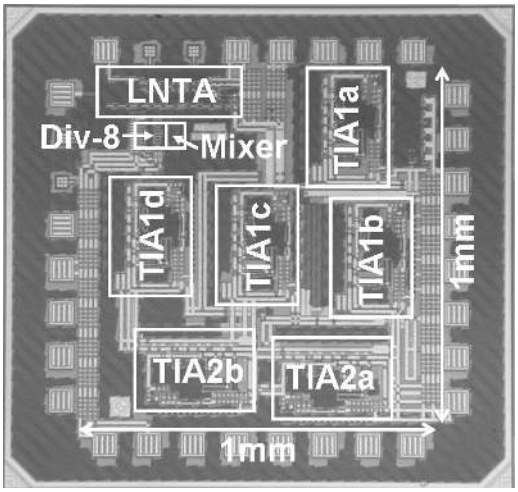

Figure 5.20 65nm-CMOS chip micrograph indicating functional blocks

5.6 Experimental Results

The circuit shown in Fig. 5.4 is fabricated in 65nm CMOS and the micrograph is shown in Fig. 5.20. The total area, excluding bond-pads, is about 1mm^2. Capacitors (C_{FB} and C_{VG} in Fig. 5.17) take a large portion of area in the TIA, and also the OTA input pair is big to achieve a low 1/f noise corner. With 1.2V supply, the analog power consumption is 33mA (LNTA: 14mA, TIA1-stage: 12.8mA, TIA2-stage: 6.4mA) while the clock power consumption is 8mA at 0.4GHz LO and 17mA at 0.9GHz LO, including the clock input buffers.

The chip is packaged in a 32-pin Heat-sink Very-thin Quad Flat-pack No-leads (HVQFN) package. To prove the receiver is robust to OBI, all measurements are performed on PCB without any external filter. Two SMD inductors are mounted on the PCB to bias the LNTA (Fig. 5.9). Both the receiver inputs and clock inputs are differential and wideband hybrids (balun) were used to interface to single-ended 50Ω measurement equipments. The IF-output voltages are sensed by a differential active probe that performs differential to single-ended conversion and impedance conversion to 50Ω. The characteristics of all components and cables for testing are de-embedded from the results.

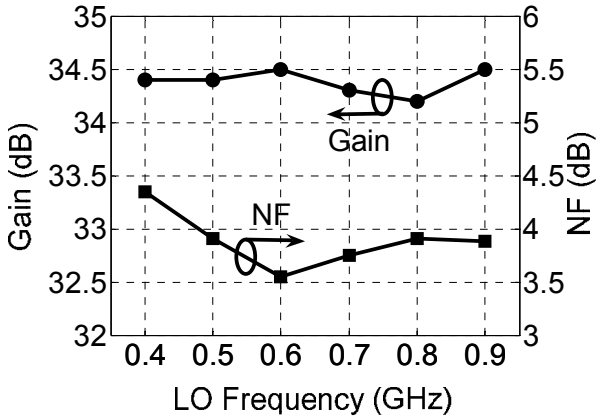

Figure 5.21 Measured voltage gain and NF of the 2-stage receiver versus LO frequency

The divide-by-8 works up to 0.9GHz LO, and the measured S_{11} is lower than -10dB up to 5.5GHz. This means the HR measurement is valid for 0.9GHz LO up to its 6th harmonic. The measured IF bandwidth is 12MHz and the baseband 1/*f* noise corner is 30kHz thanks to the passive mixer with little DC current and the OTA with a large-sized input pair.

5.6.1 Gain, NF, in-band IIP2/IIP3, and RF bandwidth

Fig. 5.21 shows the measured voltage gain and DSB NF over an LO frequency of 0.4 to 0.9GHz. The voltage conversion gain, measured for an IF of 1MHz from the input of the balun to the differential outputs of receiver, is above 34dB over the whole band and is quite flat (±0.2dB variation), indicating a much wider RF bandwidth. The NF is measured for an IF of 10MHz since the available NF analyzer (Agilent N8973A) starts from that frequency. The DSB NF is below 4dB except for 0.4GHz where 1/*f* noise from the LNTA starts to dominate.

Fig. 5.22 shows the measured in-band (IB) IIP2 and IIP3 over LO frequency, with two tones close to the LO frequency f_{LO} so that they are not affected by IF filtering (IIP2: f_{LO}+3MHz and f_{LO}+6.01MHz; IIP3: f_{LO}+3MHz and f_{LO}+3.01MHz). After

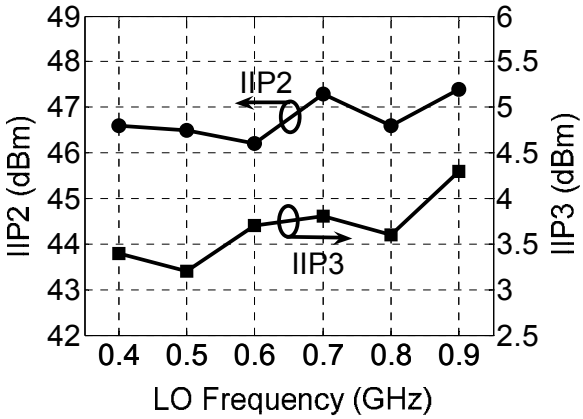

Figure 5.22 Measured in-band IIP2 and IIP3 versus LO frequency

downconversion, the IM2 component at 3.01MHz and the IM3 component at 2.99MHz are measured. The IB IIP3 is around +3.5dBm, which is good given the high gain of 34dB, thanks to only voltage gain at baseband with negative feedback. The IB IIP2 is above +46dBm.

The divide-by-8 limits the LO frequency range up to 0.9GHz (master clock @ 7.2GHz), but the signal-path -3dB RF bandwidth is much wider, up to 6GHz. To verify it, we conducted a gain measurement for the 7^{th} harmonic, i.e. the first non-canceled high-order harmonic. Ideally, using 1/8 duty-cycle LO, the strength of the 7^{th} harmonic should be 1/7 of the fundamental harmonic, so we expect the 7^{th} harmonic should ideally have a gain that is 16.9dB (1/7) lower from 34dB, i.e. 17.1dB. Indeed, as shown in Fig. 5.23, the gain drops from 17dB at 0.7GHz RF to 14.3dB at 6GHz RF (LO: 0.1 to 0.85GHz), which means the OBI will only be attenuated a little by the frequency roll-off at RF. It also indicates that the receiver can be readily expanded to cover higher bands by extending the LO range as discussed in Section 5.5.

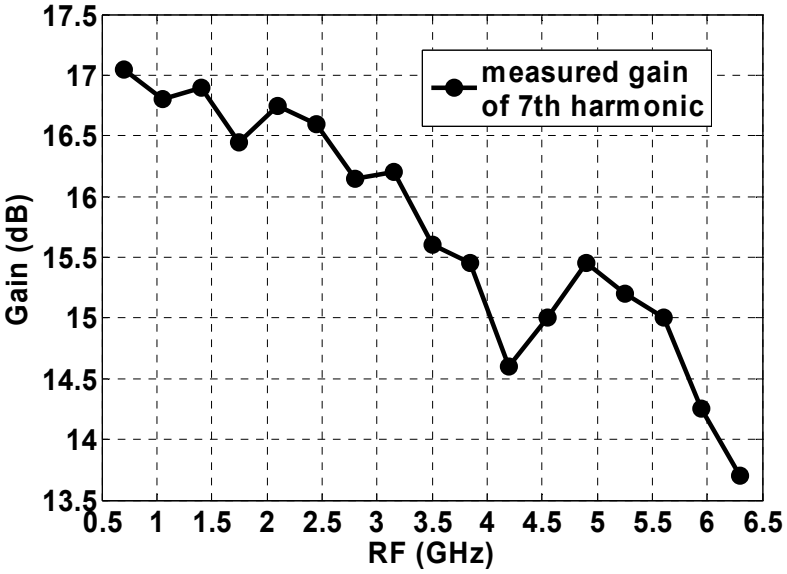

Figure 5.23 Measured voltage gain of 7th harmonic indicating a signal-path -3dB bandwidth of 6GHz (IF=1MHz, RF=7·f_{LO}+1MHz)

5.6.2 Out-of-Band IIP2/IIP3

We also measured the out-of-band (OB) IIP2 and IIP3. Due to the LPF behavior, the measured OB linearity depends on the distance from f_{LO} to the two RF tones used. For sufficient distance, the LPF will suppress the downconverted two-tone interference so the OB nonlinearity is mainly contributed by the V-I of the LNTA.

The OB IIP3 is tested via two tones at 1.61GHz and 2.40GHz with an LO at 819MHz, so that the IM3 is at 820MHz RF and 1MHz IF. The results of both IB (0.8GHz LO) and OB IIP3 are shown in Fig. 5.24. Without fine tuning, the measured OB IIP3 is +16dBm, which agrees with the simulated results in Fig. 5.11. Compared to the IB IIP3 of +3.5dBm, the OB IIP3 is dramatically improved because the TIA was dominating the IB IIP3, due to the high voltage gain at the output. As shown in the figure, the range for which IM3 follows the extrapolation line is also improved by almost 20dB (upper limit of -30dBm for IB versus -10dBm for OB). This is crucial to tolerate large OB interference.

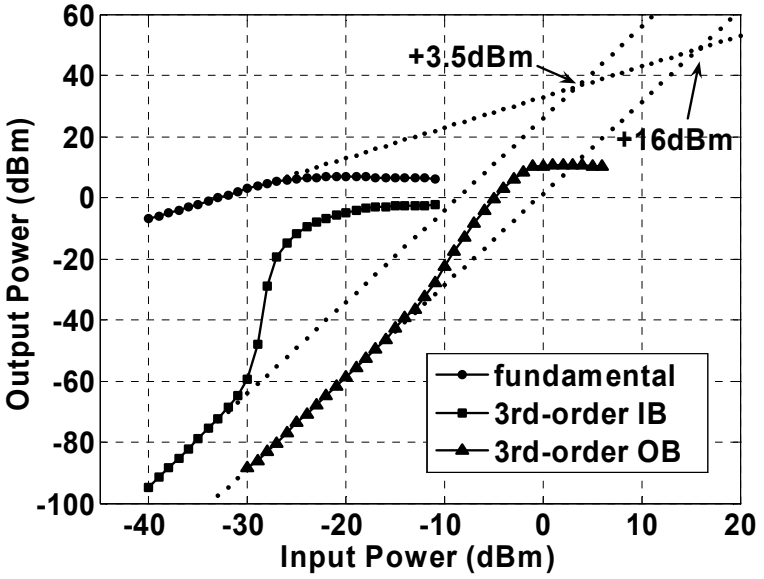

Figure 5.24 Measured in-band (IB) and out-of-band (OB) IIP3 demonstrating the OB linearity improvement (LO around 800MHz)

The OB IIP2 is +56dBm, tested via two tones at 1.80GHz and 2.40GHz while LO at 601MHz, so that the IM2 is at 600MHz RF and 1MHz IF.

5.6.3 1dB Compression Point and Blocker Filtering

To quantify the effect of the blocker filtering, we measured the 1dB compression point (P_{1dB}) and the 1dB desensitization point (B_{1dB}), both input referred.

First we measured the P_{1dB} without applying any blockers, which is -22dBm. The result is reasonable since -22dBm input power plus 34dB gain is equal to 12dBm output power (referring to 50Ω), differentially. The single-ended voltage swing is about 1.27V peak to peak, just exceeding the 1.2V supply. This means the limitation is at the receiver output and the P_{1dB} can be improved by automatic gain control (AGC).

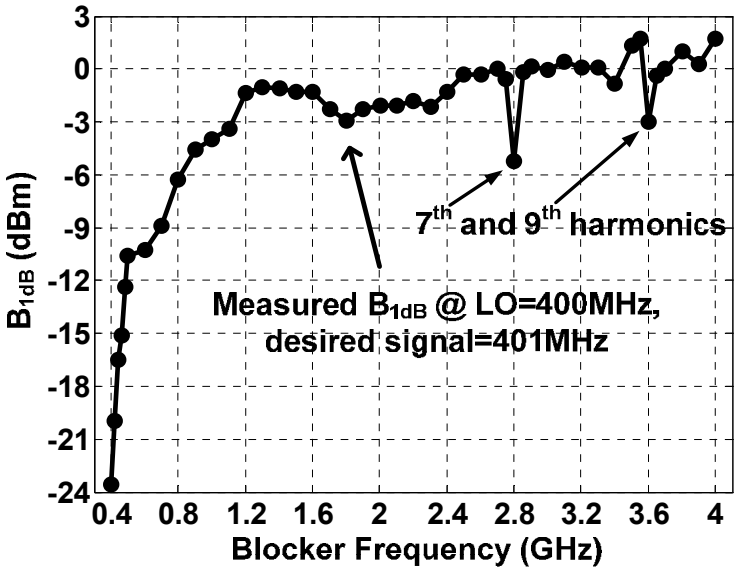

Figure 5.25 Measured 1dB desensitization point (B_{1dB}) versus blocker frequency

A more serious problem is to receive a weak signal at the same time with a strong interferer: a so-called blocker test. In this situation AGC doesn't help since the maximum gain is required to maintain sensitivity. The measurement was carried out with the LO at 400MHz and the desired RF signal at 401MHz with -50dBm input power. The blocker frequency is varied from 402MHz to 4.002GHz. Fig. 5.25 shows B_{1dB} versus the blocker frequency. As predicted by (5.1) and (5.2), we see two effects in the figure: 1) the tolerable blocker power depends on the frequency distance between the LO and the blocker, due to the LPF behavior[5]; 2) HR also plays a role in blocker filtering, as two dips occur around 7th and 9th harmonics of the LO frequency, both of which are not rejected well by the 8-phase HR. From the figure, we can observe that B_{1dB} is better than P_{1dB} (-22dBm) except very close-by blockers (402MHz) and the maximum B_{1dB} is more than 0dBm, showing the blocker filtering is indeed effective.

[5] The actual behavior of the LPF is more complicated than (5.2), since our baseband filter is cascaded in two stages, which does not follow a simple 1st-order or 2nd-order filtering behavior.

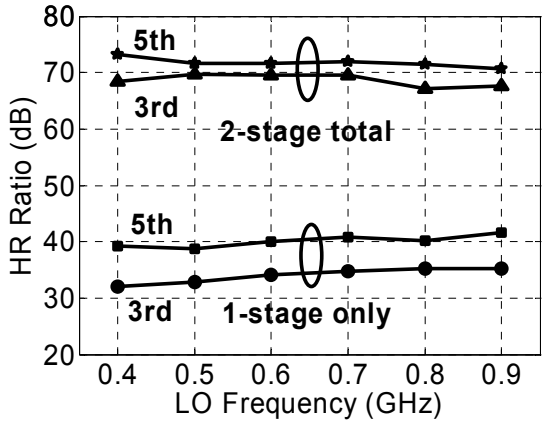

Figure 5.26 Measured HR ratio versus LO frequency: comparison between HR with only 1-stage and total 2-stage

5.6.4 Harmonic Rejection

First we look at the 2-stage polyphase HR. The HR ratio can be measured by comparing the gain difference between the desired signal and the harmonic image. At the receiver input, the desired signal power was -50dBm while the harmonic image power was -30dBm.

Fig. 5.26 shows, for one chip, the HR of 1-stage, at the outputs of the TIA1, and the total 2-stage HR, at the outputs of the TIA2, versus LO frequency. The HR of 1-stage is between 30 and 40dB and the HR of 2-stage is around 70dB, which represents a 30dB improvement for both 3rd and 5th HR thanks to the 2-stage polyphase HR technique. Generally, the HR improvement from 1-stage to 2-stage is in the range of 20 to 40dB as observed from multiple chips. The large improvement also shows that it is the amplitude error dominating the 1st-stage HR.

To identify the effect of mismatch, we measured the HR of 2-stage for 40 chips at 0.8GHz LO, as shown in Fig. 5.27. The minimum 3rd order HR is 60dB and the minimum 5th order HR is 64dB. The 2nd, 4th, and 6th HR is also measured, over 20 chips. The minimum 2nd-order HR is 62dB, while the minimum 4th and 6th order

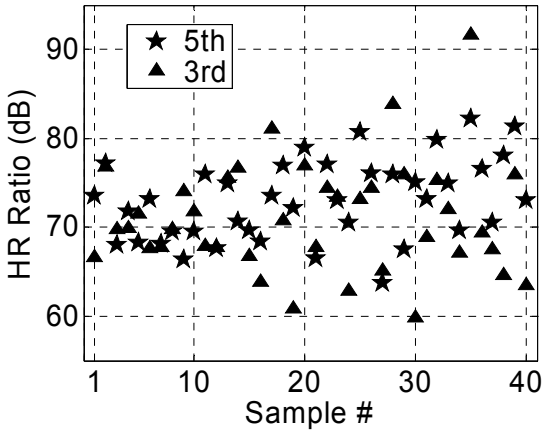

Figure 5.27 Measured HR ratio of 40 chips at 800MHz LO

HR are both 67dB. These results are achieved without calibration, trimming, or RF filtering.

Since the signal-path -3dB RF bandwidth has been characterized to be up to 6GHz, the contribution of the frequency roll-off to the HR result should be small. According to (5.6), the simulated phase error $\sigma=0.024°$ means a minimum HR (3σ) of 62dB if the amplitude error is eliminated, fitting well with the measured HR as well as the Monte Carlo simulation results. This also suggests that phase error can indeed be the limitation now.

As mentioned at the end of Section 5.3. To further correct phase error, digitally-enhanced HR can be applied, whose measurement results will be briefly mentioned here as a comparison (Table 5.1).

	Analog 2-stage	Digital AIC
Rej. strongest	>60 dB	>80 dB [a)]
Rej. other odd	>64 dB	>36 dB
Rej. even	>62 dB	>64 dB
Power front-end	50 mA @ 1.2 V (excl. ADCs)	44 mA @ 1.2 V (excl. ADCs)
Power DSP (100 MS/s)	N/A	<8.5 mA @ 1.2 V (simulated)
# ADCs	2	4

[a)] If one harmonic interference image band is dominating.

Table 5.1 Comparison of two alternative HR techniques robust to mismatch

The 2-stage polyphase HR implemented in analog approach helps both 3rd *and* 5th HR via improved amplitude accuracy and achieves a minimum rejection of 60dB and 64dB respectively. The digitally-enhanced HR based on AIC algorithm consistently shows more than 80dB of HR for a single harmonic image (either the 3rd *or* the 5th) by correcting both amplitude and phase of that harmonic image. The other harmonic image is rejected by at least 36 dB, not improved from the analog 1st stage. They share a similar limitation on even-order HR. An interesting and advantageous feature of digitally-enhanced HR is that when interferer is stronger the HR ratio is also larger, benefiting from the adaptive algorithm [1].

On the implementation level, compared to the 2-stage polyphase HR, the digitally-enhanced HR architecture requires two additional A/D converters (Fig. 5.8), which may increase the power considerably. Nevertheless, they may be switched off when the analog HR stages can provide enough harmonic rejection.

5.6.5 Performance Summary and Benchmark

Table 5.2 summarizes the measured performance. As a benchmark, Table 5.3 shows a comparison to other recently published wideband receivers with HR.

LO Frequency		0.4 to 0.9GHz
Gain		34.4dB± 0.2dB
DSB NF		4dB± 0.5dB
S_{11} < -10dB		80MHz to 5.5GHz
-3dB RF Bandwidth		Up to 6GHz
In/Out-of-band IIP3		+3.5dBm / +16dBm
In/Out-of-band IIP2		+46dBm / +56dBm
-3dB IF Bandwidth		12MHz
1/f noise		30kHz corner
Harmonic Rejection	Analog 2-stage	2^{nd}-6^{th}: >60dB
	Digital AIC	1 strongest: >80dB
Technology		65nm CMOS
Supply Voltage		1.2V
DC Current		50mA max.

Table 5.2 Summary of some measured key performance

Benchmark	CMOS Tech.	Freq. (MHz)	Gain (dB)	NF (dB)	IIP3 (dBm)	HR3 (dB)	HR5 (dB)	Chip #	Cal.	Power (mW)
This Work	65nm	400-900 [a]	34	4	**+3.5**	**60**	**64**	**40 min.**	**No**	**60**
			LNA + Mixer + Divider							
Bagheri, JSSC06 [3]	90nm	800-5000	36	5	-15 [b]	38	40	1	No	51
			LNA + Mixer + Divider, performance at 900MHz							
Lerstaveesin, JSSC08 [5]	180nm	48-860	83	4 to 7	-14	42 [c]	?	1	No	468 [c]
			LNA + Mixer + BB filter + VGA + ADC + PLL							
Ru, ISSCC08 [15]	65nm	200-900	2	19	+11	41	44	10 av.	No	19
			No LNA, only mixer & multiphase clock							
Maxim, ISSCC08 [27]	130nm	40-1000	?	16	+20	63	64	1	No	450
			No LNA, only mixer & multiphase clock							
Cha, MWCL08 [28]	180nm	48-862	35	8	-15	72	45	10 min.	Yes	189
			LNA + Mixer + Divider							

[a] Only LO frequency range, while the measured RF bandwidth is up to 6GHz.
[b] IIP3 is derived for the full-gain setting which is required to match the 5dB NF.
[c] Both the HR3 and the power data exclude the contribution of RF tracking filter.

Table 5.3 Benchmark with other recent work

There are two outstanding parameters of this work, i.e. linearity and harmonic rejection. Comparing all work including an LNA, [3], [5], and [28] shows an IIP3 around -15dBm while this work shows an IIP3 of +3.5dBm and a competitive NF. The OB IIP3 of our work is even higher (+16dBm), but we didn't find a good way to benchmark it. For HR, only [27] and [28] reported numbers comparable to this work. However, [27] only reported results from one chip while consuming large power due to a different structure of the HR mixer. [28] reported results for 10 chips, but relying on hand calibration, and the calibration is only effective for either 3rd or 5th HR but not for both at the same time. Thus we conclude that our design has both good linearity and good HR at moderate power consumption, thanks to the proposed techniques.

5.7 Conclusions

This chapter has addressed two main problems for *out-of-band interference* (OBI): out-of-band (OB) nonlinearity and harmonic mixing. First, OB nonlinearity can be improved by low-pass (LP) blocker filtering, i.e. making voltage gain only at baseband simultaneously with LP filtering to improve the OB IIP3 and the desensitization point due to blockers. We have also presented a comprehensive analysis of mix-impedance (see Appendix *A*) which can deliver a low impedance at RF by transferring the baseband impedance through passive mixers. Second, an "iterative" HR technique, i.e. a 2-stage polyphase HR concept, is proposed. It realizes HR in cascaded stages which can greatly enhance the amplitude accuracy for both 3rd and 5th HR so that the total amplitude error becomes the product of errors from each stage. To guarantee a small phase error, a simple but accurate ring counter is presented to generate the multiphase clocks driving the HR mixer. Together they provide mismatch-robust HR. To quantify the achievable HR with certain mismatch, the effects of random amplitude and phase errors to HR are also analyzed (see Appendix *B*).

We have verified the proposed techniques via a SDR receiver in 65nm CMOS, with RF bandwidth up to 6GHz and 8-phase LO frequency up to 0.9GHz (master clock up to 7.2GHz). The 1dB compression point is -22dBm while the maximum 1dB desensitization point is more than 0dBm, showing the LP blocker filtering is

effective. In terms of IIP3, +16dBm for OBI is measured without fine tuning for sufficient frequency spacing, e.g. LO at 819MHz while two-tone at 1.61G and 2.40GHz, versus an in-band IIP3 of +3.5dBm. Without any trimming or calibration, the 2-stage polyphase HR technique achieves 60dB minimum HR ratio at 0.8GHz LO for both 3rd and 5th harmonics over 40 randomly-selected chips. All even-order HR ratios are measured to be above 60dB as well. The benchmarking shows that this work achieves the highest IIP3 and the most-robust HR without compromising other performance such as NF and power consumption.

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Chapter 6

Conclusions

This final chapter summarizes the work being described in Chapter 1 to Chapter 5, and it also provides an outlook to future work on software-defined radios. Section 6.1 presents the summary and conclusions of this thesis and Section 6.2 highlights the original contributions of this work. Section 6.3 suggests some future work. The references are listed in Section 6.4.

6.1 Summary and Conclusions

This thesis is dedicated to two aspects of realizing software-defined radio (SDR) receivers: 1) the challenge of realizing SDR receivers compatible with CMOS scaling and SoC integration; 2) the challenge of realizing SDR receivers robust to out-of-band interference (OBI). We have mainly focused on frequency translation techniques to address these challenges and have also investigated some filter and amplifier techniques to support the receivers' robustness to OBI. We have contributed to the theory of frequency translation (FT) in radios and have also proposed and verified several new concepts in deep-sub-micron CMOS technology.

Chapter 1

We started from describing the *origins* of the terms "software radio" (SWR) and "software-defined radio" (SDR) which were not always clear. Based on literature review, we have clarified these two terms and suggested that SWR can be regarded as *software-intensive* SDR, illustrated by a phase space of radio evolution towards greater programmability.

Being aware of the fact that a SDR should preferably be implemented in CMOS together with digital hardware on the same chip, for feasibility at this moment we still need the *analog front-end* (AFE) in a SDR receiver to ease the requirements of ADC. After setting our thesis scope on the AFE, we have recognized four specific *challenges* of a SDR receiver compared to a traditional receiver. For each point of these challenges, discussions are expanded to clarify their implications and some *state-of-the-art* solutions are briefly reviewed to present the progress towards SDR.

Two challenges, i.e. wideband receivers and flexible channel-selection filters, appear close to be solved by other work. Then concrete research objectives are defined mainly in line with the other two challenges: 1) *compatibility with CMOS scaling and SoC integration*; 2) *robustness to out-of-band interference*. Specifically, we conclude that *frequency translation* (FT) techniques deserve attention.

Chapter 2

An overview of different FT techniques for radio receivers has been given by means of *classification*, based on downconversion principles (mixing or sampling) and input signal domains (continuous or discrete in both time and amplitude). A comparison of the mixing and sampling principles reveals their fundamental differences: in the time domain, for sampling the *information rate* changes while for mixing it keeps the same; in the frequency domain, mixing always performs frequency translation while sampling may or may not, depending on the relationship between the input and the sampling frequency. A mathematical derivation of the sampling process proves the importance of the step of conversion from continuous-time (CT) domain with an infinite information rate to discrete-time (DT) domain with a finite information rate.

Furthermore, based on various FT techniques, three *receiver architectures* come up. All architectures have been evaluated for their suitability to SDR receivers and it can be argued that both *RF-mixing* and *RF-sampling* receivers are suitable, each with their own advantages and drawbacks. The advantages of RF-sampling receivers include the compatibility with CMOS scaling and SoC integration. The drawback is the implementation complexity due to the clock generation/routing and the RF-related baseband processing. To explore the potential of RF sampling for *wideband* SDR receivers, three specific *challenges* are identified and analyzed

quantitatively: frequency-dependent phase shift, aliasing of noise and interference, and frequency-dependent conversion gain of charge sampling.

Chapter 3

The classification of FT techniques also leads to the definition of a new FT technique: *DT mixing*, which is based on the mixing principle with an analog-DT input signal. It is a variation of RF-sampling receivers but *more suitable for wideband applications* as it features wideband phase shift and wideband harmonic rejection (HR). Preceded by voltage sampling whose conversion gain is *not* systematically dependent on sampling frequency, the DT mixing architecture can relieve the three challenges mentioned in the previous paragraph.

The DT mixing concept has been verified by a 200-to-900MHz downconverter chip built in 65nm CMOS, employing an 8-times oversampler realized via time-interleaved sampling followed by an I/Q DT HR mixer realized via *de-multiplexing*. The chip consumes less than 20mW power including a multiphase clock generator. It achieves a best-in-class NF (18 to 20dB) compared to other voltage sampling based RF downconverters, thanks to oversampling and rejection of noise folding by HR. It can reject the 2^{nd}-to-6^{th} harmonic mixing, however the worst-case HR is limited to around 25dB in the current design, due to amplitude errors and especially severe phase mismatches.

Chapter 4

To improve the NF and the HR of the downconverter chip as well as to build a complete RF-sampling receiver, a *tunable LC filter* and a *linearized LNA* are added as pre-stages. To obtain a high Q and to save chip area, SMD inductors are employed on a PCB. The 2^{nd}-order series LC filter is tunable by an on-chip capacitor bank over the 300-to-800MHz RF range. It provides a low-pass characteristic which can suppress harmonics simultaneously with a peaking around the desired-signal frequency. This *"passive" pre-gain* due to resonance with a well-defined Q improves the gain and NF of the follow-up downconverter without adding noise and power consumption. As the LNA receives an amplified voltage signal, its design focuses on the *IIP3 enhancement*. It is constructed by two stages of an amplifier topology (*enhanced voltage mirror*) which is based on two inverters

acting as transconductors, one as driver and the other as load. We have found out the IIP3 can be improved by adding a resistor in the feedback path of the loading inverter which was otherwise shorted as a diode connection in a traditional design.

Measurements of the complete RF-sampling receiver show dramatic improvements of performance from the downconverter alone. The gain is improved from maximum 2.5dB to more than 22dB. The NF is improved from 18-to-20dB to 0.8-to-4.3dB. The 3rd and 5th HR ratios are improved from minimum 25dB to above 60dB. The 2-stage LNA alone presents around +2dBm IIP3 which is degraded by process spread and supply bondwire inductance. The extra power consumption is only 2.7mA, consumed by the balun stage of the LNA.

Via the above work, we have proved that a wideband RF-sampling receiver at a low NF and a low power is feasible, using a new DT-mixing architecture. This may open the door to implement SDR receivers based on RF-sampling techniques, which are compatible with CMOS scaling and SoC integration as suggested by some previous industrial work [1]-[3].

Chapter 5

Another aspect of our research has been focused on making receivers more *robust to out-of-band interference (OBI)*. In Chapter 1 we have identified that out-of-band nonlinearity and harmonic mixing are two major mechanisms of how OBI generates in-band distortion. Two new FT techniques are then proposed.

To tackle out-of-band nonlinearity, a *low-pass (LP) blocker filtering* technique can be used, which circumvent the difficulty of making tunable band-pass filters in CMOS. Traditional wideband receivers use a wideband LNA which amplifies both desired signal and undesired interference with an equal gain. However, OBI can be very strong and supply voltage is much limited in advanced CMOS. Therefore, the amplified OBI at RF is likely to limit the linearity since it is difficult to achieve bandpass selectivity. We have proposed to avoid voltage gain at RF, and instead only to amplify signal in voltage at baseband *simultaneously or after LP filtering* which already attenuates some OBI. The amount of attenuation depends on the filter bandwidth and order as well as the distance of the interference to the desired

signal on spectrum. The ultimate limitation of linearity is the RF transconductance stage if the OBI is well suppressed by the LP blocker filtering.

To tackle harmonic mixing, we have proposed a *2-stage polyphase HR* technique, bringing enhanced amplitude accuracy against mismatch. To emulate a sine-wave LO often involves irrational amplitude ratios such as 1:√2:1, which is not easy to make accurately via integer ratios on chip. By distributing the HR function in two stages, an overall highly accurate amplitude ratio can be achieved via simple integer ratios in each stage such as 2:3:2 and 5:7:5. Also the 2-stage HR is robust to amplitude mismatches since *total error becomes product of errors* by cascading two HR stages. For example, errors of 1% and 1% in each stage become 0.01% in total. Since a good HR ratio also relies on accurate LO phases. To improve the phase accuracy, we have presented an accurate yet power-efficient *frequency divider* topology.

The two aforementioned techniques have been applied to an RF-mixing SDR receiver prototype. The chip implemented in 65nm CMOS is measured to have a 34dB gain, a 4dB NF and a +3.5dBm in-band IIP3 while consuming 60mW in total. The LO frequency is up to 900MHz generated from a divide-by-8 and the -3dB RF bandwidth is up to 6GHz, which shows the receiver can be easily extended to cover a higher RF range via extending the LO frequency. For OBI with sufficient frequency spacing from the desired signal, a 1dB desensitization point of 0dBm and an IIP3 of +16dBm are measured, showing the LP blocker filtering is effective. The 2^{nd}-to-6^{th} order HR is characterized to be more than 60dB for 40 randomly selected chips without requiring calibration or trimming, which indicates the 2-stage polyphase HR concept is robust to mismatch. The chip can also be reconfigured for a digitally-enhanced HR by producing additional baseband signal paths to a digital processor. The digitally-enhanced HR can achieve more than 80dB HR for one dominant harmonic by correcting both amplitude and phase errors. The benchmarking shows that this work achieves the highest IIP3 and the most-robust HR without compromising other performance such as NF and power consumption.

This part of work shows that, via new frequency-translation techniques, a wideband SDR receiver with enhanced robustness to out-of-band interference is

feasible. Therefore, the RF pre-filtering requirements can be relaxed which is a key to obtain higher flexibility at a small size and a low cost.

Overall, this thesis has made contributions towards flexible radio receivers via both theoretical study of FT techniques and proposing and verifying new FT techniques, based on which the CMOS-and-SoC-compatible SDR and the interference-robust SDR can become possible.

6.2 Original Contributions

Theory and Analysis:

- A classification has been proposed to clarify different FT techniques. They can be classified based on input-signal domains (analog CT, analog DT, or digital) and FT principles (sampling or mixing). In addition, we have identified a criterion to fundamentally distinguish between sampling and mixing in all three signal domains: information-rate conversion. (Chapter 2)
- The importance of changing the information rate for sampling has been mathematically proven. Basically there are two steps for a CT-to-DT sampling function: 1) multiplying an input analog-CT signal with a Dirac comb; 2) changing the result of multiplication from the CT to the DT domain. Classic textbooks and other literature only explain the first step. However, the result from the first step is still a CT signal with a magnitude factor proportional to the sampling frequency, which can only be removed by changing the information rate, i.e. getting into the DT domain. (Chapter 2)
- The challenges of RF sampling for wideband applications have been identified. There are four challenges found: 1) RF-related baseband processing, which makes baseband filtering characteristic proportional to RF; 2) frequency-dependent phase shift, which means that the phase shift is systematically proportional to the input signal frequency; 3) aliasing of wideband noise and interference, which degrades signal to noise and interference ratio; 4) frequency-dependent conversion gain of charge sampling, which means its gain is systematically proportional to sampling frequency. In addition, the conversion gain of charge sampling considering some parasitic effects has also been derived and verified. (Chapter 2)

- The mix-impedance, i.e. the "impedance transfer function" of passive mixers, has been analyzed. Regarding the low-pass blocker filtering topology, it is important to implement a wideband low impedance at RF to lower the voltage gain. This can be done via a mixer to transfer a baseband impedance on one side of the mixer to an RF impedance on the other side. However it's not straightforward to quantify this impedance transfer function. We have derived and verified this transfer function, for both real and imaginary parts and considering mixer switch-on resistance, LO phase number, LO harmonic number, and LO initial phase. (Appendix *A*)
- The required amplitude and phase accuracy for a certain HR ratio has been quantified analytically. Previous derivations in literature were based on simple deterministic models for the amplitude and the phase errors. We have comprehensively analyzed the actual effects of these errors on HR ratio, considering the statistical nature of random mismatches, the effect of LO duty cycle, and the case of a double-balanced mixer which is commonly used in practice. (Appendix *B*)

Circuits and Systems Design:

- On the conceptual level, a DT mixing architecture has been proposed. It makes RF sampling more suitable for wideband SDR receivers, as it provides wideband phase shift and wideband harmonic rejection. The conversion gain of a DT mixer is derived analytically. On the implementation level, we have realized the DT mixing function via de-multiplexing and also realized 8-times oversampling for RF up to 900MHz via a time-interleaved sampling technique. (Chapter 3)
- The use of a tunable 2^{nd}-order series LC filter as a pre-stage of a flexible receiver has been proposed. It can simultaneously provide a "passive" pre-gain without adding noise and power consumption while also improve HR. The filter is tunable via an on-chip capacitor bank. We have verified its feasibility by applying it to a receiver with high (non-matched) input impedance. (Chapter 4)
- A simple amplifier topology, namely an enhanced voltage mirror, with IIP3 enhancement has been proposed. A slightly different version was known for its possibility to cancel some nonlinearity, by forming an inverse function via a first transconductor loaded by a second transconductor in diode connection.

However that is not effective in advanced CMOS technology due to the V_{ds}-related distortion terms. Most previous nonlinearity-cancellation work focused on improving the distortions in g_m only. We find that adding a resistor (R) in the feedback path of the second transconductor (g_m) can improve IIP3 in a certain $g_m \cdot R$ range by compensating both the distortions in g_m and the V_{ds}-related distortions. However, additional techniques are desired to make it more robust to process spread and supply-bondwire inductance. (Chapter 4)

- A low-pass blocker filtering technique has been proposed. Voltage gain is avoided at RF but is only made at baseband simultaneously with low-pass filtering to attenuate out-of-band interference such as blockers. Traditional narrowband receivers mostly rely on external RF pre-filters to remove strong out-of-band blockers. The blocker filtering technique here is based on low-pass filters which can be more easily integrated on chip. This technique requires less complexity than a previously published technique based on high-pass filtering which requires an additional feedforward path. Therefore, it is also free of the noise and power consumption otherwise added by the feedforward path. (Chapter 5)
- A 2-stage polyphase HR concept has been proposed. It realizes HR in cascaded stages to achieve HR robust to amplitude mismatch. Its total error becomes the product of the individual errors of the cascaded stages, which can reduce the amplitude error by a few orders of magnitude. Since it doesn't rely on any circuit-level or device-level property, in principle this concept can be applied to different process technologies using different components. (Chapter 5)
- The possibility of employing additional baseband signal paths is suggested, to provide extra information for digital systems to compensate amplitude and phase errors caused by the analog circuitry. This leads to the development of the digitally-enhanced HR concept in cooperation with Niels Moseley. (Chapter 5)
- An accurate yet power-efficient frequency divider topology has been proposed to achieve high phase accuracy for a high HR ratio. The divider is constructed by combining three key techniques to minimize phase mismatch: 1) using a single master clock to derive all LO phases, i.e. re-clocking, to avoid mismatch from the master clock; 2) applying a minimum number of buffer stages after re-clocking to reduce mismatch accumulation; 3) isolating wiring parasitics during LO transitions, to reduce LO rise and fall times and the effect of wiring mismatch. (Chapter 5)

6.3 Future Work

Software-defined radio is a work in progress. This thesis hopefully will inspire more ideas, not limited to those related to FT techniques, to enable practical and affordable software-defined radios.

The presented *RF-sampling* downconverter (Chapter 3) is based on voltage sampling and it achieves better NF compared to other previous voltage-sampling based downconverters. However, voltage sampling still suffers from noise folding of switches and some noise folding of RF amplifiers due to higher-order harmonics not being rejected by HR. In another implementation, the NF could be improved by realizing the DT mixing after *charge sampling* [4]. Charge sampling may render similar noise folding as a CT mixer and it has been implemented in some narrowband RF-sampling receivers [1]-[3] which showed an NF as low as 2dB and has been applied in cellular products. Its main disadvantage, the frequency-dependent gain, can be relieved by some suggestions given in Section 2.5.3 although the solutions can be complex. Via the combination of charge sampling and DT mixing, *wideband low-noise* RF-sampling receivers (without requiring the passive pre-gain technique introduced in Chapter 4) would be possible, producing competitive noise performance to wideband RF-mixing receivers.

The presented *RF-sampling* downconverter (Chapter 3) measures a -3dB RF *bandwidth* up to 900MHz. To support more standards, it is desired to extend the frequency range. As identified by simulation, a major limitation of the bandwidth comes from the parasitics of the *AC coupling* capacitor following the RF amplifier. In another implementation, the AC coupling capacitor can be moved from the signal path to the clock path, where the bandwidth limitation is less of a problem if the clock buffer is designed to be able to drive switches at the highest frequency. This approach has been adopted in the other design (Chapter 5) where the RF bandwidth is measured to be 6GHz (partly this is also because voltage gain is avoided at RF so the dominant pole is located at a very high frequency). The LO frequency (Chapter 3) is also up to 900MHz, but in principle it shouldn't be a bottleneck since multi-GHz LO generation in advanced CMOS is readily available. The LO frequency was limited by the specific divider design, relatively large

division ratio of 4, and small duty cycle of 1/8. Any modification on one of the three factors can extend its frequency range, e.g. when only a 4-phase quadrature LO (instead of 8-phase) is desired if HR is not necessary.

As derived in Section 1.2, a *HR ratio* of 100dB is *sometimes* desired to address interference as strong as 0dBm. The achievable HR ratio is determined by the amplitude and phase accuracy together. The 2-stage polyphase HR concept (Chapter 5) can significantly improve the amplitude accuracy, but not for phase. More investigation into the phase accuracy is clearly valuable. On the other hand, digitally-enhanced HR (Chapter 5) seems to be a good candidate as 80-to-90dB minimum HR has been demonstrated and probably the actual number is even higher if not limited by the measurable dynamic range. However, it requires additional baseband signal paths which may add extra power. One possibility to reduce this cost is to *reconfigure* between analog and digital HR. The additional baseband signal paths are only required to be active when interference is extra-ordinarily strong, which might not be often the case.

Other than HR, the other out-of-band challenge is related to *nonlinearity*. The low-pass blocker filtering technique (Chapter 5) can improve the linearity at the output of the receiver by attenuating out-of-band interference. However, the prototype has only demonstrated a 1st-order filter with a fixed bandwidth while a higher-order filter with a flexible bandwidth would be better. In addition, the distortion occurring in the *RF-transconductance* stage, which is often required for low noise, cannot be helped by the LPF and therefore sets the ultimate limitation to the achievable out-of-band IIP3. As indicated by [5], the required receiver IIP3 for some standards can be as high as +30dBm while the demonstrated IIP3 is +16dBm. For *frequency-division duplex (FDD)* standards, the required receiver linearity due to strong transmitting power without dedicated duplexers can be even higher. It is worth more investigation to explore possibilities to further improve the out-of-band linearity and especially the limitation set by the RF-transconductance stage.

To handle the *strong interference* is very challenging and probably also power consuming due to the high dynamic range requirement. Nevertheless, the chance is low that very weak desired signal (e.g. at sensitivity level) and very strong interference (e.g. at 0dBm) appear at the same time. If that situation does happen, it is most likely to happen only for a short period of the whole operation time of a

receiver. Therefore it doesn't make sense to have the receiver always working in the mode with maximum dynamic range. To save power, the receiver can *reconfigure* its mode by detecting the relative strength of desired signal and undesired interference. However, this approach also has a risk of degrading the quality-of-service during the mode switching, since the detecting-reconfiguring procedure will add some latency which has to be minimized to a tolerable level. This concept actually can be part of the function of a future *cognitive radio* [6], which adds more intelligence based on a software-defined radio.

6.4 References

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Appendix A

Analysis of the "Mix-Impedance"

As shown in Fig. 5.2, via a passive mixer operating in the linear region when turned on, the impedance at the baseband side strongly affects the impedance seen at the RF side. The RF impedance can be obtained by translating the baseband impedance in frequency. We refer to this impedance as the "*mix-impedance*", since the frequency-translation property distinguishes it from a conventional impedance. This section will derive the mathematical description of a mix-impedance.

A.1 Derivation

To quantify the impedance seen into the mixer from the RF side, we may apply an ideal current source $i_{src}(f)$, as shown in Fig. A.1, to drive the mixer switches and check its corresponding voltage $v_{src}(f)$, so to derive the RF impedance $Z_{RF}(f)=v_{src}(f)/i_{src}(f)$, which depends on the baseband impedance (Z_{BB}).

First, consider two mixer switches in parallel driven by a 50% duty-cycle balanced LO, as shown in Fig. A.1 (a). Since the differential mixer switches conduct alternatively, the i_{src} always sees a Z_{BB}. If Z_{BB} is frequency independent, e.g. only resistive (R_{BB}), since there is no memory effect in a pure resistance, Fig. A.1 (a) is equivalent to Fig. A.1 (b) which means

$$Z_{RF} = R_{BB} . \tag{A.1}$$

However, Z_{BB} is often frequency dependent with LPF characteristic, e.g. R_{BB} in parallel with C_{BB}, to mitigate interference. This case is more complicated since Z_{BB} may present memory effect. But we will try to clarify the transfer function from Z_{BB} to Z_{RF} step by step, for a general-case Z_{BB} which can be any impedance (combination of R, L or C).

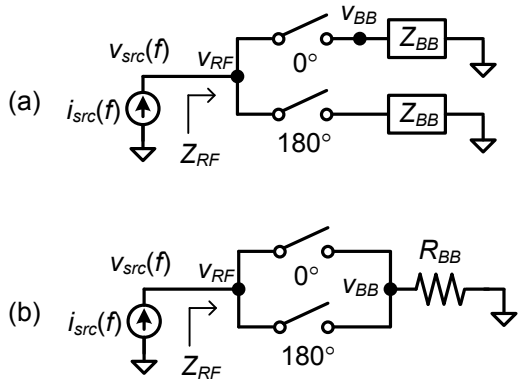

Figure A.1 (a) A balanced-LO switching system;
(b) Equivalent model of (a) if Z_{BB} is purely resistive (Z_{BB}=R_{BB})

For a current signal at frequencies around f_{LO}, e.g. $f_{LO}+\Delta f$, it can be represented as $i_{src}(f_{LO}+\Delta f)$. After the mixer, the current is down-converted to Δf with an amplitude of $(1/\pi)\cdot i_{src}(f_{LO}+\Delta f)$ at each branch of the mixer, which creates a voltage v_{BB} across Z_{BB}:

$$v_{BB}(\Delta f) = \frac{1}{\pi} \cdot i_{src}(f_{LO} + \Delta f) \cdot Z_{BB}(\Delta f) . \tag{A.2}$$

If the mixer switch has 0 on-resistance, i.e. R_{mixer}=0, the input of the mixer sees an up-converted v_{BB} (BB-to-RF voltage conversion) to create v_{RF} via the same mixer switch as down-conversion (RF-to-BB current conversion). Since the down-conversion and the up-conversion are controlled by the same clock signal, any phase shift due to the clock signal is removed. Therefore the RF voltage contributions from each branch add up in phase:

$$v_{RF}(f_{LO} + \Delta f) = 2 \cdot \frac{1}{\pi} \cdot v_{BB}(\Delta f) = \frac{2}{\pi^2} \cdot i_{src}(f_{LO} + \Delta f) \cdot Z_{BB}(\Delta f) . \tag{A.3}$$

This RF voltage stands at the same frequency as the original current signal $i_{src}(f_{LO}+\Delta f)$. The reason is that $i_{src}(f_{LO}+\Delta f)$ was first down-converted by $(-1)^{st}$ LO harmonic and then the resulted BB voltage signal $v_{BB}(\Delta f)$ is up-converted by $(+1)^{st}$ LO harmonic, resulting in a total equivalent LO-harmonic order of 0^{th}, i.e. no spectrum shift.

The BB-to-RF voltage upconversion will also create an *image* signal at $|f_{LO}-\Delta f|$:

$$v_{RF}(|f_{LO}-\Delta f|) = 2\cdot\frac{1}{\pi}\cdot v_{BB}(\Delta f) = \frac{2}{\pi^2}\cdot i_{src}(f_{LO}+\Delta f)\cdot Z_{BB}(\Delta f)\,. \qquad \text{(A.4)}$$

This image voltage stands at a different frequency from the original current signal, because $i_{src}(f_{LO}+\Delta f)$ was first down-converted by $(-1)^{st}$ LO harmonic and then again up-converted by $(-1)^{st}$ LO harmonic. Therefore, the total equivalent LO harmonic order is $(-2)^{nd}$, leading to a spectrum shift from $f_{LO}+\Delta f$ to $|\Delta f-f_{LO}|$.

In the above derivation, only the fundamental LO harmonic is considered. In fact, more spectrum components emerge as we include the higher-order LO harmonics as well, e.g. 3rd, 5th etc. In general, an RF current signal $i_{src}(f_{RF})$ with $f_{RF}\geq 0$ can be down-converted[1] by $(-m)^{th}$ LO harmonic (m=…-1, 0, 1, …) to create $v_{BB}(f_{RF}-m\cdot f_{LO})$ which can then be up-converted by n^{th} LO harmonic (n=…-1, 0, 1, …) resulting in $v_{RF}(|f_{RF}+[n-m]\cdot f_{LO}|)$, so that the total equivalent LO harmonic order is $(n-m)^{th}$.

If $n=m$, the result does not involve spectrum shift at the RF side (node B in Fig. 5.2). For $n\neq m$, spectrum shift does happen at the RF side. That means an RF current signal at a certain frequency may create a voltage signal at another frequency if loaded by the time-variant impedance such as Fig. A.1.

In the following derivation, we first focus on the total equivalent LO harmonic order of 0^{th}, i.e. $n=m$.

A.1.1 Impedance without Spectrum Shift

Consider a more general case as shown in Fig. A.2, the mixer consists of N switches in parallel driven by N-phase 1/N-duty-cycle LO. Such a configuration guarantees there is always a switching path at the on state to conduct the current and there is no overlap between any paths.

For signal $i_{src}(f_{RF})$ with $f_{RF}\geq 0$ down-converted by $(-m)^{th}$ LO harmonic, the voltage at baseband (each path) can be written as:

[1] We use "down-converted" to mean a conversion from the RF side to the BB side, but effectively the frequency may be up- or down-converted, depending on the sign of m. A similar remark holds for "up-converted" which refers to a conversion from the BB to the RF side but may be up- or down-converted in frequency.

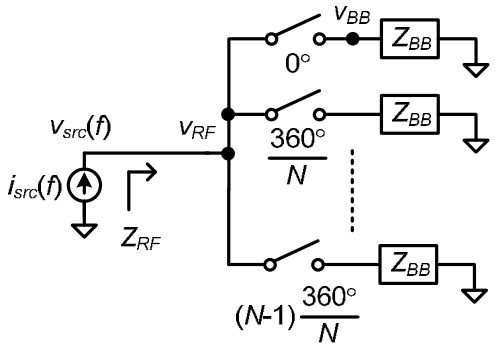

Figure A.2 A general *N*-phase switching system

$$v_{BB}(f_{RF} - m \cdot f_{LO}) = H(-m) \cdot i_{src}(f_{RF}) \cdot Z_{BB}(f_{RF} - m \cdot f_{LO}) . \tag{A.5}$$

$H(-m)$ is the Fourier coefficient of $(-m)^{\text{th}}$ LO harmonic. For 1/*N*-duty-cycle square-wave LO with a delay of t_0, it can be written as:

$$H(m)\big|_{m \neq 0} = \frac{1}{m \cdot \pi} \cdot \sin(\frac{m \cdot \pi}{N}) \cdot e^{-j \cdot m \cdot 2\pi \cdot \frac{t_0}{T}}, H(0) = \frac{1}{N} . \tag{A.6}$$

The corresponding voltage at RF after up-conversion by m^{th} LO harmonic can be written as:

$$v_{RF}(f_{RF}) = N \cdot H(-m) \cdot H(m) \cdot i_{src}(f_{RF}) \cdot Z_{BB}(f_{RF} - m \cdot f_{LO}) . \tag{A.7}$$

The factor of N comes because signals from N paths add up in phase at the RF side, since each path goes through down-and-up-conversion by the same LO signal which means the total phase shift is zero. Besides, it is well-known that currents can easily add up. However, it is also possible for voltages from different paths to add up at a joint node, if these paths conduct with no overlap.

Also for each individual path, voltage signals can add up at one frequency after being converted from different frequencies, e.g. harmonic mixing. As a result, the total RF voltage is the sum of contributions from all LO harmonics (m=…-1, 0, 1, …):

$$v_{RF}(f_{RF}) = i_{src}(f_{RF}) \cdot \sum_{m=-\infty}^{\infty} \left[N \cdot H(-m) \cdot H(m) \cdot Z_{BB}(f_{RF} - m \cdot f_{LO}) \right] . \tag{A.8}$$

Now the impedance Z_{RF} can be derived as:

$$Z_{RF}(f_{RF}) = \frac{v_{src}(f_{RF})}{i_{src}(f_{RF})} = \frac{v_{RF}(f_{RF})}{i_{src}(f_{RF})} = N \cdot \sum_{m=-\infty}^{\infty} \left[H(-m) \cdot H(m) \cdot Z_{BB}(f_{RF} - m \cdot f_{LO}) \right] . \tag{A.9}$$

Suppose N=2, i.e. the case of Fig. A.1, and if Z_{BB} is frequency independent, e.g. Z_{BB}=R_{BB}, applying (A.6) we can write (A.9) as

$$\begin{aligned} Z_{RF}(f_{RF}) &= R_{BB} \cdot \left(\frac{1}{2} + \sum_{m=-\infty, m\neq 0}^{\infty} \left[\frac{2}{m^2 \cdot \pi^2} \cdot \sin^2\left(\frac{m \cdot \pi}{2}\right) \right] \right) \\ &= R_{BB} \cdot \left(\frac{1}{2} + \frac{2}{\pi^2} \cdot 2 \cdot \left[1 + \left(\frac{1}{3}\right)^2 + \left(\frac{1}{5}\right)^2 + \ldots \right] \right) = R_{BB} . \end{aligned} \tag{A.10}$$

It fits exactly what we got from (A.1).

Now include the finite switch-on resistance which can be modeled as a single R_{mixer} in front of the mixer, as shown in Fig. A.3. It generates the same effect as having R_{mixer} within each of the mixer switches since the on states of any switches do not overlap. Then we have $v_{src}(f_{RF})$:

$$v_{src}(f_{RF}) = v_{RF}(f_{RF}) + i_{src}(f_{RF}) \cdot R_{mixer} . \tag{A.11}$$

Therefore the impedance is:

$$Z_{RF}(f_{RF}) = \frac{v_{src}(f_{RF})}{i_{src}(f_{RF})} = R_{mixer} + N \cdot \sum_{m=-\infty}^{\infty} \left[H(-m) \cdot H(m) \cdot Z_{BB}(f_{RF} - m \cdot f_{LO}) \right] . \tag{A.12}$$

If Z_{BB} presents LPF effect to strongly suppress the high-frequency components, e.g. a pole at a much lower frequency than the LO frequency, which is often the case in practice for a down-mixer, (A.12) can be simplified since the contributions of $Z_{BB}(f_{RF}$-$m \cdot f_{LO})$ at frequencies around DC are likely to dominate. That means, the impedance Z_{RF} at an RF around m^{th}-LO-harmonic frequency (m=0, 1, 2, 3…), i.e. with an offset frequency Δf from $m \cdot f_{LO}$, with $|\Delta f| \leq f_{LO}/2$ and $(m \cdot f_{LO} + \Delta f) \geq 0$, can be written as:

$$Z_{RF}(m \cdot f_{LO} + \Delta f) \approx R_{mixer} + N \cdot H(-m) \cdot H(m) \cdot Z_{BB}(\Delta f) . \tag{A.13}$$

Substituting (A.6) into (A.13) can obtain (5.3) which does not include the m=0 case for simplicity.

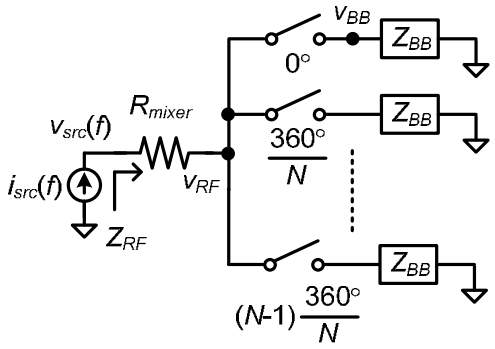

Figure A.3 A general N-phase switching system modeling switch-on resistance (R_{mixer})

A.1.2 Impedance with Spectrum Shift

In the above derivation we focused on the case of total equivalent LO harmonic order of 0th, i.e. n-m=0. For the other orders which lead to spectrum shift at the RF node, similar procedure can be followed. Generally, for a total k^{th} order (n-m=k≠0), we can first derive the transfer function of down-conversion by $(-m)^{th}$ LO harmonic and then up-conversion by $(m+k)^{th}$ LO harmonic. As a result, the source voltage can be derived as:

$$\begin{aligned}&\left[v_{src}(|f_{RF}+k\cdot f_{LO}|)\right]_{k\neq 0}=\left[v_{RF}(|f_{RF}+k\cdot f_{LO}|)\right]_{k\neq 0}\\&=i_{src}(f_{RF})\cdot\sum_{m=-\infty}^{\infty}\left[c\cdot N\cdot H(-m)\cdot H(m+k)\cdot Z_{BB}(f_{RF}-m\cdot f_{LO})\right],\end{aligned}\quad (A.14)$$

where c is defined as

$$c=\begin{cases}1, \text{if } (k/N)=\text{integer}\\0, \text{otherwise}\end{cases}, \quad (A.15)$$

because only when k/N=integer, the contributions from all N paths add up at the RF side and otherwise they cancel each other due to different phases.

There is no R_{mixer} term in (A.14), i.e., for the case of k≠0, v_{src} and v_{RF} shares the same voltage. The reason is that effectively R_{mixer} only conducts the RF current signal without spectrum shift (k=0), as it can be modeled before the mixer switches (Fig. A.3).

From (A.14), we can also see which interference may affect the desired signal due to spectrum shift in a mix-impedance. Suppose the resulted voltage signal falls on top of a desired signal at $f_{LO}+\Delta f$, i.e. $|f_{RF}+k\cdot f_{LO}|=f_{LO}+\Delta f$. Then we get

$$f_{RF} = \left\{ \left[(-k+1)\cdot f_{LO} + \Delta f \right] \text{ or } \left[(-k-1)\cdot f_{LO} - \Delta f \right] \right\} \text{ and } f_{RF} \geq 0 . \quad \text{(A.16)}$$

If k=-2, we have signal originally at $3f_{LO}+\Delta f$ and $f_{LO}-\Delta f$ to overlap with the desired signal at $f_{LO}+\Delta f$, which are the 3rd harmonic interference and the image interference respectively.

The impedance resulted from (A.14) involves spectrum shift, i.e. a current signal at f_{RF} creates a voltage signal at $|f_{RF}+k\cdot f_{LO}|$, and it is named as Z_{shift} to distinguish from Z_{RF} for k=0 case. Z_{shift} can be written as:

$$\left[Z_{shift}\left(\left|f_{RF}+k\cdot f_{LO}\right|\right) \right]_{k\neq 0} = \frac{\left[v_{src}\left(\left|f_{RF}+k\cdot f_{LO}\right|\right) \right]_{k\neq 0}}{i_{src}\left(f_{RF}\right)}$$

$$= \sum_{m=-\infty}^{\infty} \left[c\cdot N\cdot H(-m)\cdot H(m+k)\cdot Z_{BB}\left(f_{RF}-m\cdot f_{LO}\right) \right] . \quad \text{(A.17)}$$

A few interesting points can be discovered from (A.17). If N=4, i.e. quadurature mixer driven by 25%-duty-cycle LO, since c=0 if $k/4$ is not an integer, Z_{shift} is zero for k=-3, -2, -1, 1, 2, 3. That means the 3rd harmonic and image interference will not make trouble according to (A.16). However, the 5th harmonic and the image of 3rd harmonic can still overlap with the desired signal since Z_{shift} for k=-4 is not zero. If N=8, i.e. 8-phase mixer driven by 12.5%-duty-cycle LO, since c=0 if $k/8$ is not an integer, Z_{shift} is zero for k=-7…-1, 1…7. That means the image interference and 2nd to 6th harmonic interference with their images will not overlap with the desired signal.

Intuitively explained, for a 4-phase mixer, since the RF-to-BB current conversion creates quadrature baseband signal, the BB-to-RF voltage conversion driven by four phase LO is equivalent to a single-sideband up-conversion mixer which can eliminate the image signal at the RF side. For more phases, we may apply polyphase multipath principle [1]. For N mixer switches in parallel driven by N-phase LO, the RF-to-BB current conversion creates N-phase baseband signal. Then

the BB-to-RF voltage conversion is equivalent to a polyphase multipath up-converter, which adds all N paths in phase at RF and may cancel up to $(N\text{-}2)^{th}$ LO harmonics [2].

A.2 Simulation

To verify the theory presented above, we may compare the simulation results with the calculated results via (A.12) and (A.17), which is general for different LO waveforms. For a specific square-wave LO with 1/N duty-cycle, substituting (A.6) into (A.12) and (A.17) respectively, we get:

$$Z_{RF}(f_{RF}) = R_{mixer} + \frac{1}{2}\cdot Z_{BB}(f_{RF}) + N\cdot \sum_{m=-\infty}^{\infty, m\neq 0}\left[\frac{1}{m^2\cdot\pi^2}\cdot \sin^2(\frac{m\cdot\pi}{N})\cdot Z_{BB}(f_{RF}-m\cdot f_{LO})\right], \tag{A.18}$$

and

$$\left[Z_{shift}(|f_{RF}+k\cdot f_{LO}|)\right]_{k\neq 0} = \sum_{m=-\infty\ldots\infty}^{m\neq 0, m\neq -k}\left[\frac{c\cdot N}{m\cdot(m+k)\cdot\pi^2}\cdot \sin(\frac{m\cdot\pi}{N})\cdot\sin(\frac{[m+k]\cdot\pi}{N})\cdot e^{-j\cdot k\cdot 2\pi\cdot\frac{t_0}{T}}\cdot Z_{BB}(f_{RF}-m\cdot f_{LO})\right]. \tag{A.19}$$

We can see that Z_{RF} is independent of the initial phase (t_0) of the LO, while Z_{shift} *is* dependent. If only to consider the magnitude, t_0 makes no difference, but it does change the real and imaginary parts of Z_{shift}.

A simulation setup same as Fig. A.2 has been built up with ideal components (current source, switches with internal R_{mixer}, and baseband impedance) to eliminate the effect of parasitic elements which are not considered in the equations. The comparison is carried out with N=8, i.e. an 8-phase system, and a maximum m=51, i.e. considering up to the 51st LO harmonic. The LO frequency (f_{LO}) is at 1GHz with 1/8 duty-cycle and the RF range (f_{RF}) is from DC to 5GHz. The LO harmonic strength is determined by the LO waveform which is affected by the rise and fall time. To be precise, a small rise and fall time of 1fs is used to match, as close as possible, the amplitude of the Fourier coefficients described by (A.6). Two different LO initial phases of t_0=0 or t_0=T/9 are tested to check the effect of initial LO delay. The baseband impedance consists of a resistor R_{BB}=1kΩ and a capacitor C_{BB}=10pF in parallel to ground, corresponding to a pole at 16MHz, and the mixer

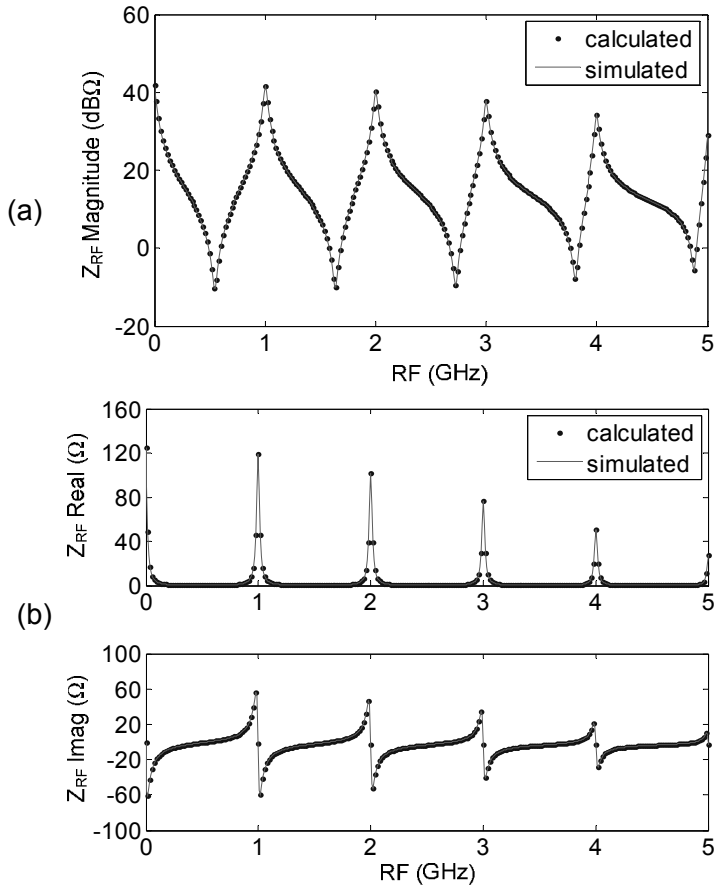

Figure A.4 Calculated via (A.18) and simulated Z_{RF} with R_{mixer}=1mΩ: (a) magnitude in dB; (b) real and imaginary parts

switch-on resistance is either R_{mixer}=50Ω or R_{mixer}=1mΩ to demonstrate different scenarios with or without mixer resistance.

First we look at (A.18). With R_{mixer}=1mΩ, the magnitudes of simulated and calculated Z_{RF} (k=0) are plot in Fig. A.4 (a), and they show an exact match. Since impedance may consist of real and imaginary parts, we compared these two separately as well. Fig. A.4 (b) gives both simulated and calculated results which match very well too. Fig. A.5 shows the case for R_{mixer}=50Ω where the real part shows an offset value of R_{mixer} as expected. The same results hold for different t_0

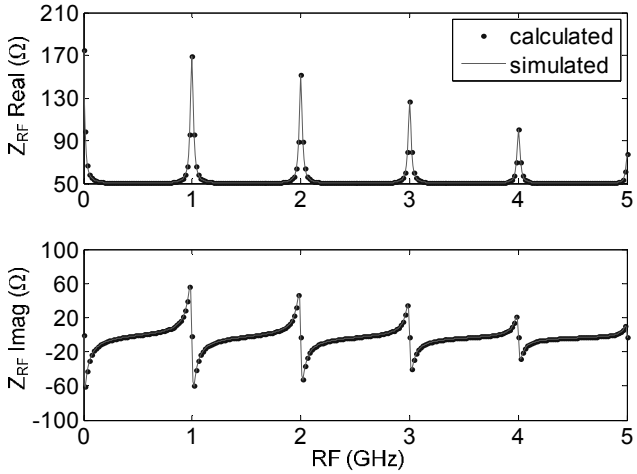

Figure A.5 Calculated via (A.18) and simulated Z_{RF}: real and imaginary parts with R_{mixer}=50Ω

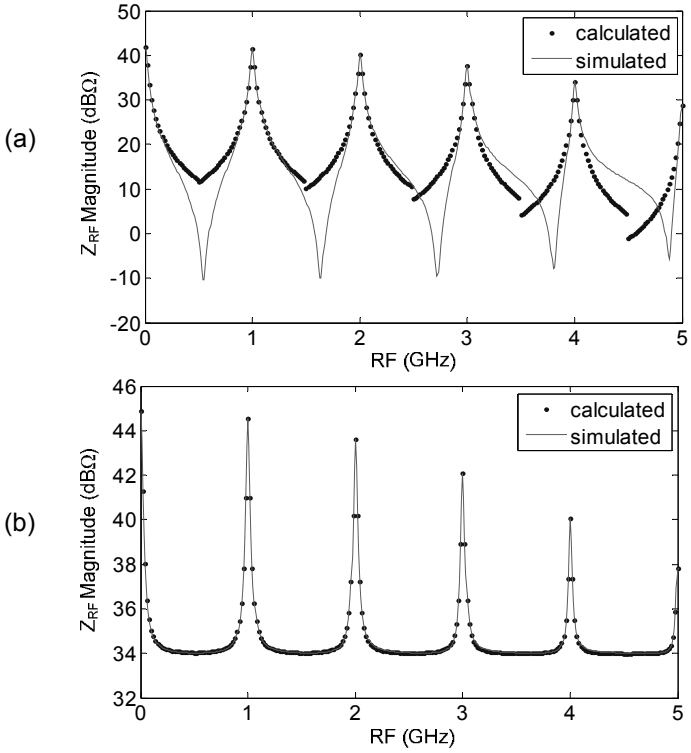

Figure A.6 Calculated via simplified equation (A.13) and simulated Z_{RF}: magnitude in dB with (a) R_{mixer}=1mΩ (b) R_{mixer}=50Ω

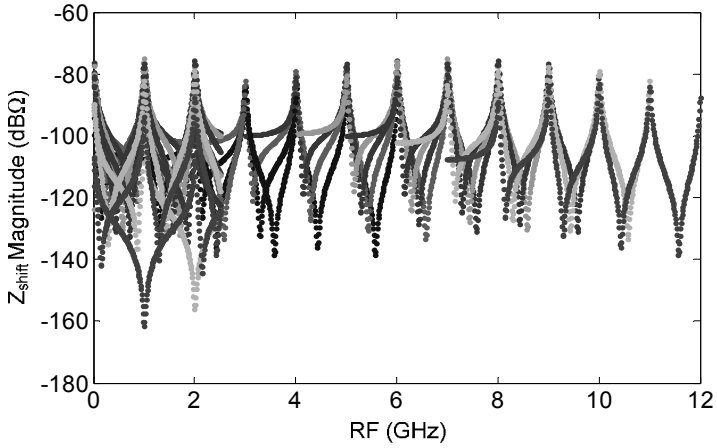

Figure A.7 Simulated Z_{shift}: magnitude in dB with k=-7…-1, 1…7

values. These results prove our derivation for Z_{RF}, via (A.12) in general and (A.18) for the specific LO waveform.

To check the accuracy of the simplified equation (A.13), or (5.3) without considering spectrum around DC, we plotted in Fig. A.6, the simulated magnitude and calculated magnitude via (A.13). If R_{mixer}=1mΩ as in Fig. A.6 (a), the approximation is good around peak values but less accurate when Z_{RF} drops low. Nevertheless, in practice, R_{mixer} is often in the order of tens of Ohms. For our design (Fig. 5.4), R_{mixer}=50Ω, and Fig. A.6 (b) shows that then the approximation is pretty good for all values since R_{mixer} now dominates low Z_{RF} values.

Then, we look at (A.19). In simulation, we checked k=-7…-1, 1…7, which should give Z_{shift}=0 since c=0 according to (A.15). The simulated Z_{shift} magnitudes are shown in Fig. A.7, independent of R_{mixer}. All results are below -70dBΩ which means a negligible impedance, confirming the theory.

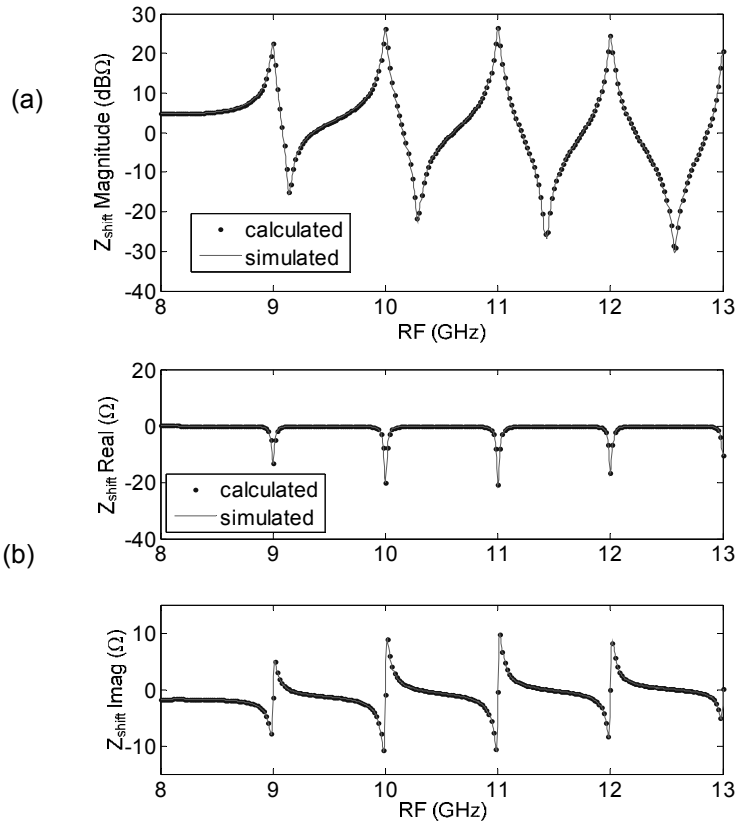

Figure A.8 Calculated via (A.19) and simulated Z_{shift} with k=8 and t_0=0: (a) magnitude in dB; (b) real and imaginary parts

Further, we compare a non-canceled Z_{shift} with k=8, so that c=1 according to (A.15). The simulated and calculated Z_{shift} in magnitude and real/imaginary parts are shown in Fig. A.8 (a) and (b), respectively, for the t_0=0 case. A very good fit is found again. We also checked $t_0=T/9$, and the comparisons for magnitude and real/imaginary parts are plotted in Fig. A.9 (a) and (b), showing no difference. However, it shows the effect of t_0, which does not affect magnitude but does change the real and imaginary parts compared to Fig. A.8. All these simulation results are independent of R_{mixer}. Therefore, we may conclude that the derived Z_{shift}, via (A.17) in general and (A.19) for the specific LO waveform, is verified.

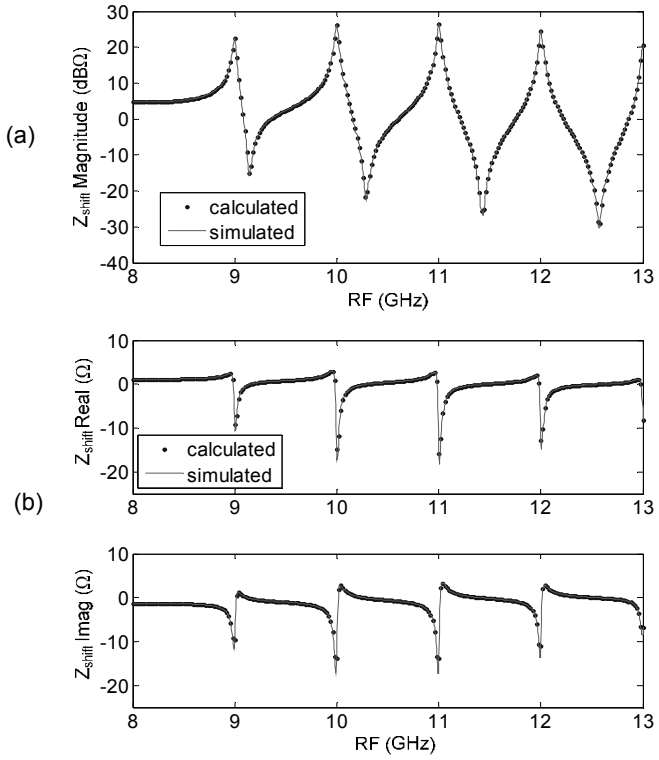

Figure A.9 Calculated via (A.19) and simulated Z_{shift} with k=8 and t_0=T/9: (a) magnitude in dB; (b) real and imaginary parts

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Appendix B

Effect of Random Amplitude and Phase Errors to Harmonic Rejection

This appendix aims at estimating the HR ratio and its sensitivity to amplitude and phase errors. These effects have been partly considered in [1] and [2], however, the statistical nature of mismatch and the effect of using balanced RF or balanced LO have not been included so far. We will also consider the effect of LO duty cycle "*d*".

B.1 Derivation

Suppose we have three signal paths to the output (as in Fig. 5.3 to Fig. 5.7) and the signals are represented by vectors as in Fig. B.1. The resulted 1st and 3rd harmonics can be respectively written as:

$$\begin{aligned} H_1 &= R_{H1} \cdot \left[A_1 \cos\varphi_1 + \sqrt{2}\cos 0^\circ + A_2 \cos\varphi_2 \right] \\ H_3 &= R_{H3} \cdot \left[A_1 \cos(3\varphi_1) + \sqrt{2}\cos 0^\circ + A_2 \cos(3\varphi_2) \right], \end{aligned} \tag{B.1}$$

where R_{H1} and R_{H3} are the Fourier series coefficients of a pulse-wave LO with duty cycle "*d*":

$$\begin{aligned} &R_{H1} = \frac{2}{\pi}\sin(\pi \cdot d), R_{H3} = \frac{2}{3\pi}\sin(3\pi \cdot d), \\ &A_1 = (1 + \Delta A_1), A_2 = (1 + \Delta A_2), \\ &\varphi_1 = (45^\circ + \Delta\varphi_1), \varphi_2 = (-45^\circ + \Delta\varphi_2) \end{aligned} \quad . \tag{B.2}$$

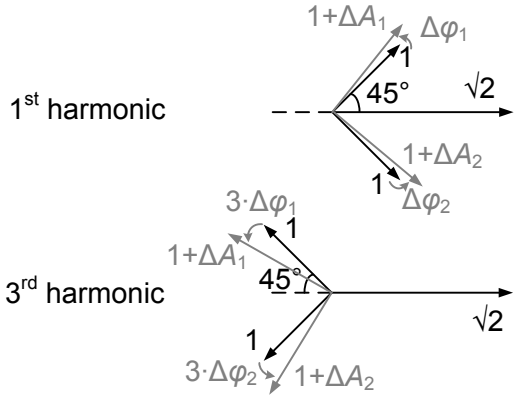

Figure B.1 Vector diagram modeling amplitude and phase errors for 8-phase harmonic rejection

If ΔA_1, ΔA_2, $\Delta\varphi_1$, $\Delta\varphi_2$ are small and uncorrelated, we can approximate the variance in H_3 as:

$$\sigma_{H3}{}^2 \approx R_{H3}{}^2 \cdot \left[\left(\frac{\partial H_3}{\partial A_1} \right)^2 \cdot \sigma_{A1}{}^2 + \left(\frac{\partial H_3}{\partial A_2} \right)^2 \cdot \sigma_{A2}{}^2 + \left(\frac{\partial H_3}{\partial \varphi_1} \right)^2 \cdot \sigma_{\varphi 1}{}^2 + \left(\frac{\partial H_3}{\partial \varphi_2} \right)^2 \cdot \sigma_{\varphi 2}{}^2 \right]. \quad \text{(B.3)}$$

If $\sigma_{A1}=\sigma_{A2}=\sigma_A$ and $\sigma_{\varphi 1}=\sigma_{\varphi 2}=\sigma_\varphi$, then:

$$\sigma_{H3}{}^2 \approx R_{H3}{}^2 \cdot \left[2\cos^2\left(3\cdot 45^\circ\right)\cdot \sigma_A{}^2 + 18\sin^2\left(3\cdot 45^\circ\right)\cdot \sigma_\varphi{}^2 \right] = R_{H3}{}^2 \cdot \left[\sigma_A{}^2 + 9\sigma_\varphi{}^2 \right]. \quad \text{(B.4)}$$

Since $H_1 \approx 2\sqrt{2}\cdot R_{H1}$, taking the ratio, we obtain:

$$\left(\frac{\sigma_{H3}{}^2}{H_1{}^2} \right) \approx \frac{R_{H3}{}^2 \cdot \left[\sigma_A{}^2 + 9\sigma_\varphi{}^2 \right]}{8R_{H1}{}^2} = \frac{\sin^2(3\pi\cdot d)}{\sin^2(\pi\cdot d)} \left[\left(\frac{\sigma_A}{6\sqrt{2}} \right)^2 + \left(\frac{\sigma_\varphi}{2\sqrt{2}} \right)^2 \right]. \quad \text{(B.5)}$$

Please note that σ_A is the standard deviation of amplitude error in percentage and σ_φ is the standard deviation of phase error in radians.

For a double-balanced HR mixer, which creates the output during one half period from 0 to $T/2$ with the positive-sign RF-LNTA path then the other half from $T/2$ to T with the negative-sign RF-LNTA path, the 1st harmonic adds up in amplitude while the 3rd harmonic adds up in power (as the error is uncorrelated between twohalf periods for both amplitude and phase). Therefore, the ratio is improved by 3dB for a double-balanced HR mixer compared to (B.5), i.e.

$$\left(\frac{\sigma_{H3}{}^2}{H_1{}^2}\right)_{diff} \approx \frac{\sin^2(3\pi\cdot d)}{\sin^2(\pi\cdot d)}\left[\left(\frac{\sigma_A}{12}\right)^2+\left(\frac{\sigma_\varphi}{4}\right)^2\right]. \tag{B.6}$$

If the duty cycle of the LO is 50% or 25%, i.e. d=0.5 or 0.25, we get

$$\left(\sigma_{H3}{}^2/H_1{}^2\right)_{diff,50\%} \approx \left(\sigma_A/12\right)^2+\left(\sigma_\varphi/4\right)^2. \tag{B.7}$$

If there is no amplitude error, 50% or 25% duty cycle results in a 3σ-HR3 of 70dB if σ_φ=0.024°.

If the duty cycle is 1/8, i.e. d=0.125, as in our case, we get:

$$\left(\sigma_{H3}{}^2/H_1{}^2\right)_{diff,12.5\%} \approx 5.8\cdot\left[\left(\sigma_A/12\right)^2+\left(\sigma_\varphi/4\right)^2\right]. \tag{B.8}$$

Without amplitude error, the 3σ-HR3 is now 62dB.

A similar derivation for 5th order HR of a double-balanced HR mixer renders:

$$\left(\frac{\sigma_{H5}{}^2}{H_1^2}\right)_{diff} \approx \frac{\sin^2\left(5\pi\cdot d\right)}{\sin^2\left(\pi\cdot d\right)}\cdot\left[\left(\frac{\sigma_A}{20}\right)^2+\left(\frac{\sigma_\varphi}{4}\right)^2\right]. \tag{B.9}$$

where the phase term σ_φ would have been multiplied by 5 in (B.5) due to the 5-times phase shift of H_5 compared to H_1. Nevertheless, without amplitude errors, this leads to the same numerical result (σ_φ=0.024°): a 3σ-HR5 of 62dB for 1/8 duty cycle LO.

B.2 Simulation

Fig. B.2 plots the 3rd-order HR (HR3) and 5th-order HR (HR5) versus amplitude and phase errors with 1/8 duty cycle, based on (B.6) and (B.9) respectively. In the figure, Psigma means σ_φ and Asigma means σ_A. The HR results in dB correspond to 3-sigma errors. We can see that when $\sigma_A \geq 0.5\%$, phase error hardly affects HR ratio. While if $\sigma_A \leq 0.1\%$, phase error can easily dominate with $\sigma_\varphi \geq 0.02°$.

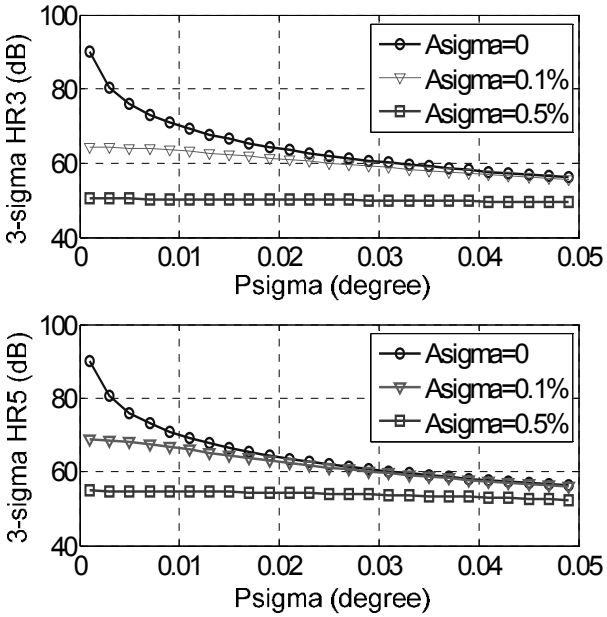

Figure B.2 Effect of amplitude error (Asigma= σ_A) and phase error (Psigma=σ_φ) to HR with 1/8 duty-cycle LO

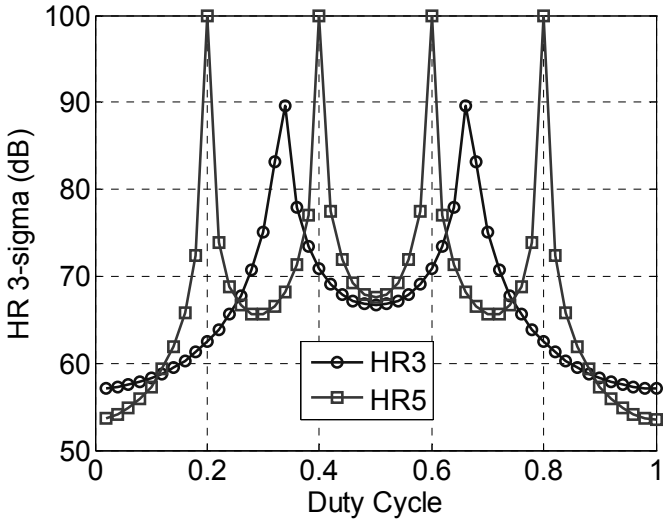

Figure B.3 Effect of duty cycle (*d*) to HR, with σ_A=0.1% and σ_φ=0.03°

Fig. B.3 plots the 3-sigma HR3 and HR5 versus duty cycle (d) with σ_A=0.1% and σ_φ=0.03°. We can see that the duty cycle effect is symmetrical around d=0.5 as can be understood, and presents a few narrow peaks for both HR3 and HR5. These HR peaks are due to the facts that $\sin(3\pi \cdot d)$ in (B.6) is close to 0 when d is around 1/3 and 2/3, and $\sin(5\pi \cdot d)$ in (B.9) is close to 0 when d is around 1/5, 2/5, 3/5 and 4/5. For the convenience of illustration, the upper limit of the peaking values in the figure is set to 100dB while in theory an exact 0 value for $\sin(3\pi \cdot d)$ or $\sin(5\pi \cdot d)$ can lead to infinite HR ratio. From Fig. B.3 we can also see that around d=0.5, the 3rd and 5th HR ratios are generally larger than the cases when d approaches 0 or 1. This is because the relative strength of harmonic components in a square-wave clock can vary for different duty cycles.

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Zhiyu Ru
Enschede, October 2009

Samenvatting

Er is een toenemende vraag naar draadloze communicatie en er zijn in de loop van de tijd diverse communicatiestandaarden ontwikkeld voor dit doel, bv. voor GSM, Bluetooth, Wi-Fi, etc. Vanwege het gebruiksgemak wil gebruikers graag een universele radio die overal werkt voor alle standaarden. Een "software-defined radio" (SDR) met programmeerbare radio functionaliteit kan aan deze vraag voldoen. Er zijn echter een aantal technische uitdagingen om een SDR-ontvanger praktisch realiseerbaar te maken.

Dit proefschrift richt zich op radio-frequentie (RF) frequentie translatie technieken, met nadruk op twee belangrijke SDR-ontvanger uitdagingen: de robuustheid voor out-of-band interferentie (OBI) en de compatibiliteit met CMOS en system-on-chip integratie. Dit proefschrift bestudeert de principes en prestatiebeperkingen van bestaande frequentie translatie technieken en stelt nieuwe circuit- en systeemtechnieken voor die betere SDR-ontvangers mogelijk maken.

Fundamentele verschillen tussen diverse frequentie translatie technieken worden aan het licht gebracht door middel van een classificatie van mixer and sampler technieken. Dit leidt tot de definitie van een nieuwe discrete-time (DT) mixer techniek. Verder worden RF-mixen en RF-samplen vergeleken met betrekking tot hun geschiktheid voor SDR. RF-samplen lijkt daarbij in het voordeel qua compatibiliteit met CMOS en system-on-chip integratie. Bestaande RF sampling ontvangers zijn echter smalbandig en zijn niet direct geschikt voor breedbandige SDR toepassingen.

Om dit probleem aan te pakken wordt een nieuwe discrete-time mixer techniek voorgesteld, die een mixer operatie in het DT-domein uitvoert na RF-sampling. Deze techniek maakt RF-samplen meer geschikt voor breedbandige SDR-ontvangers doordat DT-mixen zowel een breedbandige faseverschuiving als een breedbandige harmonische rejectie (HR) geeft. DT-mixen kan eenvoudig worden

gerealiseerd met behulp van de-multiplexen van samples. De praktische werking van het concept wordt gedemonstreerd door een 200-900MHz DT-mixer ontwerp met 8-voudige RF-oversampling en 2e-tot-6e HR, geïmplementeerd op een chip in 65nm CMOS technologie. Om hiermee een complete RF-ontvanger te realiseren, is een afstembare LC filter en een gelineariseerde ruisarme voorversterker op de chip toegevoegd, voorafgaand aan de DT-mixer. Het LC-filter gebruikt één externe spoel en schakelbare condensatoren op chip voor de frequentie afstemming. De ruisarme voorversterker bestaat uit een cascade van CMOS-inverters, gelineariseerd via een “spannings-spiegel” concept. De totale RF-sampling ontvanger heeft een minimale Noise Figure van 0.8dB, terwijl deze de HR met 30dB verbetert.

Om RF mixers beter bestand te maken tegen OBI worden voorts twee technieken voorgesteld: een techniek die de “out-of-band lineariteit” verbetert en een andere die de HR robuust maakt voor bij productie optredende component ongelijkheden. Daarbij wordt spanningsversterking niet op hoge frequenties gerealiseerd, maar uitgesteld tot na de conversie naar basisband, alwaar laagdoorlaat filtering in combinatie met versterking plaatsvindt om de OBI te onderdrukken. De lage spanningsversterking bij hoge frequenties wordt bereikt via een "mix-impedantie", die kwantitatief geanalyseerd wordt. Om de HR aanzienlijk te verbeteren en ongevoelig te maken voor amplitude fouten, wordt een 2-traps polyfase HR-techniek voorgesteld. Om tevens een goede fasenauwkeurigheid te bereiken, is een nauwkeurige frequentiedeler ontworpen. De effecten van random amplitude en fase fouten op de HR worden ook geanalyseerd. Om aan te tonen dat de concepten werken, is in 65nm CMOS technologie een ontvanger geïmplementeerd die een “in-band” IIP3 van +3.5dBm heeft en +16dBm “out-of-band IIP3”. Meer dan 60dB HR is gemeten over 40 willekeurig gekozen chips. De multifase klok generator werkt tot 0.9GHz, terwijl de -3dB RF-bandbreedte meer dan 6GHz is.

Publications

Journal Papers

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Patents

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