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Full 3D Quantum Transport Simulation of Interface Roughness in Nanowire FETs[1] SUNGGEUN KIM, ABHIJEET PAUL, MATHIEU LUISIER, GERHARD KLIMECK, Purdue University, TIMOTHY BOYKIN, University of Alabama — Silicon-silicon dioxide interface roughness has been identified as a critical device characteristic in MOS devices a long time ago. Down-scaling the diameter of silicon nanowires increases the relative importance of the details on their surfaces. In this work, we numerically investigate the effects of surface roughness in ultra-scaled silicon nanowire field-effect transistors (NWFETs) using a full 3D quantum transport simulator based on the atomistic $sp^3d^5s^*$ tight-binding model. The interface roughness between the silicon and the silicon dioxide atoms is generated in a real-space atomistic representation using an experimentally derived autocovariance function. Through statistical evaluations of different atomistic nanowire configurations, it is found that interface roughness alters the conduction band edge throughout the nanowire structure leading to resonance peaks in the transmission probability and localization of the density-of-states . These effects cause a reduction of the drain current in the ON-state of the NWFETs. A threshold voltage fluctuation is also observed in rough nanowire samples. The reduction and the fluctuation of the ON-current and of the threshold voltage caused by interface roughness increase as the diameter of the NWFETs decreases. This behavior is illustrated for NWFETs with a diameter of 2 and 3nm.

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