Available online at www.sciencedirect.com
ScienceDirect
INTEGRATION, the VLSI journal 40 (2007) 226–234
INTEGRATION the VLSI journal
www.elsevier.com/locate/vlsi

Full-chip multilevel routing for power and signal integrity ☆

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Received 28 June 2004; received in revised form 14 November 2005; accepted 15 November 2005

Abstract

Conventional physical design flow separates the design of power network and signal network. Such a separated approach results in slow design convergence for wire-limited deep sub-micron designs. In this paper, we present a novel design methodology that simultaneously considers global signal routing and power network design under integrity constraints. The key part to this approach is a simple yet accurate power net estimation formula that decides the minimum number of power nets needed to satisfy both power and signal integrity constraints prior to detailed layout. The proposed design methodology is a one-pass solution to the co-design of power and signal networks in the sense that no iteration between them is required in order to meet design closure. Experiment results using large industrial benchmarks show that compared to the state-of-the-art alternative design approach, the proposed method can reduce the power network area by 19.4% on average under the same signal and power integrity constraints with better routing quality, yet use less runtime.

Keywords: Extended global routing; Power and signal network co-design; Power integrity; Signal integrity

1. Introduction

Power distribution network and signal network are two major resource consumers for wire-limited deep sub-micron (DSM) designs. In a conventional physical design flow, they are designed separately. The power network is designed first to respect the power integrity constraint, then signal network is routed under the remaining routing resource budgets.

As the minimum feature size keeps shrinking, signal integrity becomes more and more critical due to the higher operating frequency and closer proximity between interconnects. Two major facts that contribute to signal integrity problems are the increasing capacitive coupling and inductive coupling. In addition to sizing, spacing, and buffering, shielding has been proven to be effective to improve signal integrity for DSM designs. Because shields are interconnects connected to the power network directly through vias instead of devices, they can not only reduce the capacitive coupling between signal nets, but also provide a closer current return paths for signals [1]. Shields are usually inserted into the layout after/during signal routing, hence they contend for the same scant routing resources left for signal routing.

Note that in the final layout, shields indeed form part of the power network. Therefore, it makes sense for us to include shielding into the power network design loop and account the area consumed by shielding into power network's resource budgets. However, as the accurate shielding information is only known after detailed signal routing, it is impossible to consider shielding during the power network design stage in the conventional separated design flow. To make it even worse, in such a separated design flow, the power network tends to over-design to have power network area more than necessary to satisfy power integrity constraints because of the lack of knowledge about the following signal routing and shielding. The consequence is that the remaining resource budgets after power network

☆This work is supported in part by an NSF CAREER award CCR-0093273, in part by an SRC grant 1100, in part by a UC MICRO grant sponsored by Analog Devices, Fujitsu Laboratories of America, Intel Corporation, and LSI Logic, and in part by a Faculty Partner Award by IBM. We used computers donated by Intel and Sun Microsystems.

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doi:10.1016/j.vlsi.2005.11.001

design may be too restrictive for a routing algorithm to find a feasible signal routing solution in one pass. Iterations between signal routing and power network design are seldom avoidable and design closure suffers. Therefore, an integrated resource management and co-design of both power network and signal routing are in great demand.

However, there are very limited previous works on this subject. The reason is that both signal routing and power network design are computationally intensive, and combining them results in a problem with even higher complexity. To the best of our knowledge, there are only two works in literature that have addressed such a similar problem [2,3]. Ref. [2] is the first work in literature that proposed to manage power and signal routing resources simultaneously by adding a feedback loop between the conventional power network design and signal routing flow to resolve the resource contention problem between them. To accurately capture the power integrity constraints, Su et al. [2] employed the detailed RLC model for the power network with SPICE simulation. Very promising experiment results have been reported. However, because of the detailed SPICE simulation used for power network design and the iterative nature of feedback, the computation cost of such an approach is high. Moreover, Su et al. [2] has not considered shielding for signal integrity yet. Recognizing that shielding requirement is only known after signal routing, the authors in [3] proposed to solve the power and signal network co-design problem in the following manner: they first rout part of the signal nets along with their required shielding; then they synthesize the power network, considering the shielding resource from step one; and finally they rout the rest of signal nets under the remaining routing resources. The novelty of their approach is that their power network synthesis in step two can take signal shielding into consideration because of the early shielding insertion from step one. However, because their first step routing was not aware of the following power routing, iterations may still be possible. Nevertheless, Saxena and Gupta [3] did provide a new perspective to the conventional physical design flow, and such a three-step solution has been successfully applied to real industrial practices.

In this work, we propose a one-pass solution to the co-design of power network and signal routing under integrity constraints by using a high abstract level integrity models. The major motivation for this work is our awareness of that the design convergence problem can only be solved by a correct-by-construction methodology rather than a trial-and-error approach. Moreover, to handle the high complexity of co-design, we have to employ high abstract level power integrity and signal integrity models for the purpose of computation efficiency. The rest of the paper is organized as follows: we discuss the preliminary and design constraints in Section 2 and our problem formulation in Section 3. We develop the power net estimation formula in Section 4, present algorithm details and experiment results in Sections 5 and 6, respectively. We conclude this paper with discussion of our future work in Section 7.

2. Preliminary and design constraints

Both power and signal integrity constraints are closely related to timing and noise problems [4,5]. However, timing and noise constraints are generally defined in electrical domain and are difficult to be directly used in physical layout synthesis. One way to bridge the gap between electrical constraints and physical layout is to convert these electrical constraints into physical layout "wiring rules" [6,7]. Under this spirit, we employ two high abstract level yet efficient integrity models in this work, namely, the power pitch model to address the power integrity constraints, and the signal net shielding model to address the signal integrity constraints.

2.1. Power pitch constraints

The goal of global power network design is to satisfy the power integrity constrains with minimum routing area. IR-drop and $Ldi/\mathrm{d}t$ noise are two of the major factors contributing to power integrity problems. A power network is usually designed as a mesh to provide a low impedance current return path for signals. *Power pitch* is the separation between two adjacent power lines in a mesh structure as shown in Fig. 1 (a). To ensure power integrity in the mesh structure, it is preferable to have a small power pitch. Because the smaller the power pitch, the smaller the power network's effective resistance and inductance, hence the smaller the IR-drop and $Ldi/\mathrm{d}t$ noise. However, the smaller power pitch also implies more routing area for power network design. Therefore, a maximum power pitch should be carefully chosen such that the low impedance current return paths are still maintained at the full-chip level but with reasonable routing area.

According to [9], the relation between the maximum power pitch and the maximum IR-drop constraint can be established based upon the following first order approximation, i.e., each power bonding pad is responsible for supplying current draws for circuits located within its vicinity area. As shown in Fig. 1 (b), the area supplied by a given power bonding pad can be modeled as a circle with radius as $p/2$, where p is the power pitch in a mesh structure. Within the circle, each unit area draws a constant current, i.e., the constant current density σ, and the total current is supplied through the power bonding pad with a diameter as w. Denote ρ as the effective sheet resistance of the global power distribution network. Assuming constant voltage at each power supply pad, the worst case IR-drop happens at the peripheral of the area serviced by the power bonding pad. Such an IR-drop can be estimated by the following equation:

$$\begin{aligned}\Delta V &= \int_{w/2}^{p/2} \mathrm{d}V_r = \int_{w/2}^{p/2} I \cdot \mathrm{d}R \\ &= \int_{w/2}^{p/2} \pi\left(\frac{p^2}{4} - r^2\right)\sigma \cdot \rho \, \frac{\mathrm{d}r}{2\pi r}\end{aligned}$$

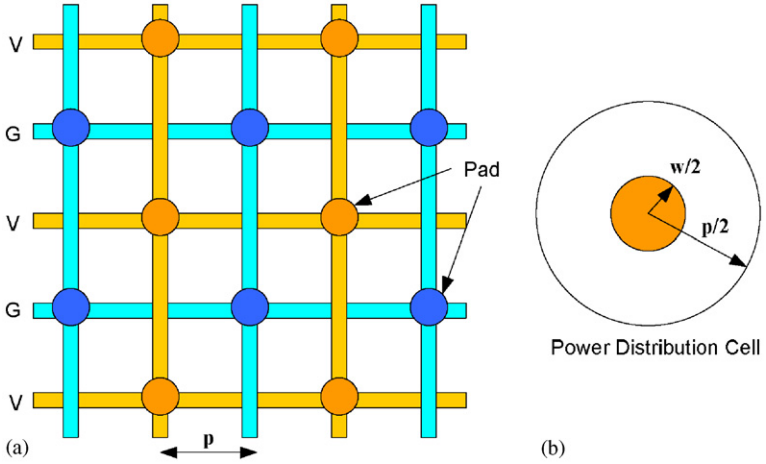

Fig. 1. Illustration of power network modeling (not on scale): (a) power network; and (b) worst case IR-drop modeling.

$$= \frac{1}{2}\sigma\rho\left(\frac{p^2}{4}\ln(r) - \frac{1}{2}r^2\right)\Big|_{w/2}^{p/2}$$
$$= \frac{1}{8}\sigma\rho p^2\left(\ln\frac{p}{w} + \frac{w^2}{2p^2} - \frac{1}{2}\right). \quad (1)$$

Given the required IR-drop constraints (ΔV), we can obtain the required maximum power pitch (p) by solving (1) numerically. If Ldi/dt noise is of a concern, we refer readers to [1,10,11] for the details on how to choose such a maximum power pitch. Therefore, at high abstract level, a power network can be designed with a maximum power pitch constraint ($\overline{PGP}$) such that as long as its power pitch is less than $\overline{PGP}$, the resulting power network is guaranteed to satisfy the required IR-drop, Ldi/dt and electro-migration constraints.[1] Such a power pitch model has been used successfully in real designs by Saxena and Gupta [3]. Because of its simplicity and high abstraction, we employ the power pitch model in this paper. The benefit of using power pitch model is two-fold: avoiding the expensive numerical-based power network analysis [5,12] and making it possible to check the power integrity constraints on-the-fly during signal routing.

2.2. Signal shielding constraints

As we have discussed in Section 1, shielding is effective to reduce crosstalk. The following two types of crosstalk reduction model via shielding have been studied in literature [3,13,14]. The first one is to reduce the crosstalk for every signal net in a routing region via simultaneous shield insertion and net ordering (SINO) under an effective inductive coupling coefficient model [13]. The second one is to reduce the crosstalk for critical signal nets by putting shields adjacent to those critical signal nets [3,14]. In this work, we employ the second crosstalk reduction model, as such a model has been used successfully in industry practices for modern micro-processor designs [3]. According to [3], signal nets are characterized into three categories according to their criticality in the timing graph: the most critical nets are shielded on both sides, which we call $s2$-nets; the next most critical nets are shielded on only one side, which we call $s1$-nets; and the rest of nets are non-critical nets and require no shielding, which we call $s0$-nets. The definition of signal nets' criticality can be obtained via either static timing analysis or noise optimization as shown in [3] and [15].

2.3. Routing model

We tessellate the routing area into rectangular partitions as *routing tiles*, and all cells along with their connection pins are placed at the center of routing tiles.

The circuit layout can be formally modeled by an undirected graph $G(V, E)$, as shown in Fig. 2, where each vertex $v \in V$ represents a routing tile, and each edge $e \in E$ represents the routing area between two adjacent tiles. To model the limited routing resources, we associate each edge in $G(V, E)$ with a *capacity*, which is defined as the maximum number of tracks available for routing. The capacity is decided by the geometry of the design and the technology used. In multilayer designs, an edge may consist of more than one layer. We assume that each layer is composed of equally spaced tracks and each track can be used by only one net segment. Therefore, we can accommodate multilayer designs by increasing the capacity of each edge. An edge in the routing graph is also called a *routing region*. A *track assignment solution* in a routing region is the sequence of track numbers for all signal nets and power nets in that region. Similar to [16], an *extended global routing solution* not only decides the regions that every signal net is routed through, i.e., the set of edges to connect all nodes (global bins) that contain pins for the net,

[1]Such an approach is in accordance with designers' common practice. Nevertheless, for power network sign-off, a detailed power network simulation may still be necessary.

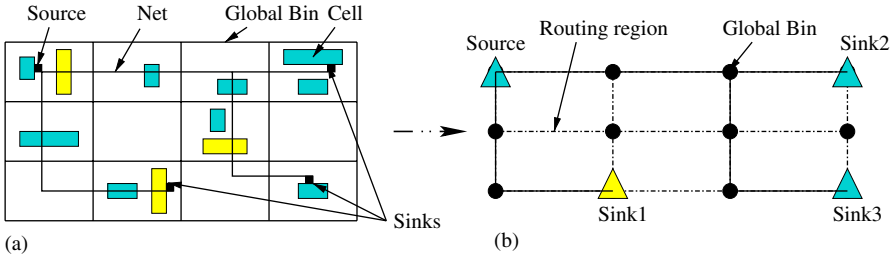

Fig. 2. (a) Layout. (b) The corresponding routing graph.

but also determines the track assignment solutions for all regions.

Because shields are part of the power network, we do not distinguish shields and power nets specifically in this paper. Assuming uniform wire sizing for all power nets and uniform length for all finest routing tiles, we can model the total power network area in terms of the total number of power nets (or shields) in the final layout:

$$PG_{\text{area}} = \sum_{\forall t} S_t \tag{2}$$

where S_t is the number of power nets used in R_t. For a given routing region R_t, its routing density is defined as $Den_t = (G_t + S_t)/C_t$, where C_t is the routing capacity, G_t and S_t are the number of signal nets and power nets in R_t, respectively. When $Den_t > 1$, overflow occurs in R_t; otherwise, there is no overflow. Same as in [2,17], we measure the overall routing congestion by the maximum density over all routing regions, i.e., $\max Den = \max_{\forall t \in E} Den_t$.

3. Problem formulation

As we discussed in Section 1, shields are effective to improve signal integrity but introduces routing area overhead. As the clock frequency continues to increase, the proportion of nets that require shielding is also growing. This trend implies that more and more routing area will be used solely for shielding purpose. In order to achieve design closure for both power network design and signal network design, we not only need to minimize the power network area, but also accurately allocate routing resources for shielding purpose. This is only made possible by a unified approach to the co-design of power and signal networks simultaneously. We formulate the co-design of power and signal network problem as follows:

Formulation 1 (*GSPR Problem*). *Given the power pitch constraint* ($\overline{PGP}$), *a placement solution*, *a net list*, *and the shielding requirements for all signal nets*, *the GSPR*[2] *problem synthesizes a power network and an extended global routing solution*, *such that the power network has a power pitch less than* $\overline{PGP}$, *the extended global routing solution satisfies the required shielding constraints for all nets*, *and the total power network area as defined in* (2) *is minimized*.

[2]GSPR stands for Global Signal and Power co-Routing.

The GSPR problem has very high complexity as even its sub-problem global routing (minimum rectilinear Steiner tree problem) per se is already NP-hard. In order to solve it, we propose a novel design methodology in this paper. Instead of synthesizing the power network first as a conventional physical design flow does, we now synthesize a global routing solution first with power net estimation and minimization considering both the power pitch and signal shielding constraints. After global routing, we then synthesize a power network to satisfy the power pitch constraint, and at the same time decide track assignment solutions for all signal nets to satisfy their shielding requirements. The key to this approach is a simple yet accurate power net estimation formula that decides the minimum number of power nets needed to satisfy both power pitch and signal shielding constraints without knowing the exact power network design. We develop the power net estimation formula in Section 4, and discuss the algorithmic details in Section 5.

4. Power net estimation

A *valid* track assignment solution in R_t is a track assignment solution that satisfies both power pitch and signal shielding constraints. To find valid track assignment solutions for all net segments in all routing regions, we may need to insert many power nets. The exact number of power nets is only known after we have fixed the track assignment solution in each region. But at that time, it is often too late to correct a "bad" routing solution in case we could not find a feasible routing solution within the routing resource budgets. Therefore, in the following we develop a closed formula to estimate the minimum number of power nets in R_t without knowing its exact track assignment solution.

Lemma 1. *Given a routing region* R_t *with capacity* C_t, *in order to satisfy the power pitch constraint* $\overline{PGP}$, *the minimum number of power nets needed in* R_t *is given by* $p_t = \lceil C_t/\overline{PGP} \rceil$.

Therefore, knowing the power pitch constraint is equivalent to knowing p_t, such that the resulting power pitch in R_t is less than $\overline{PGP}$.

Lemma 2. *Given a routing region R_t with m_2 number of $s2$-nets, m_1 number of $s1$-nets, and m_0 number of $s0$-nets, in order to satisfy the signal shielding requirements, the minimum number of power nets S_t^{si} is given as follows*:

$$S_t^{si} = \begin{cases} m_2 + 1, & m_2 > 0, m_1 < 2 \\ m_2 + \left\lceil \frac{m_1}{2} \right\rceil, & m_1 \geqslant 2 \end{cases} \quad (3)$$

Proof. The minimum number of power nets in R_t is obtained when every power net is contributing two-side shielding effects for either $s1$-nets or $s2$-nets, i.e., there are either $s1$-nets or $s2$-nets on the two sides of every power net, while the signal shielding requirements are still satisfied. In this case, we cannot reduce any power net without violating signal nets' shielding constraints, therefore, the obtained number of power nets is minimum. Such a solution can be obtained by (1) alternating all m_2 $s2$-nets with power nets, and putting two $s1$-nets adjacent to the two outermost power nets; (2) sharing one power net between every remaining $s1$-net pair. As all $s0$-nets do not need any shields, the total power net number is the sum of the above two procedures: i.e., $(m_2 + 1) + \lceil (m_1 - 2)/2 \rceil = m_2 + \lceil m_1/2 \rceil$. To accommodate special cases, like there is no $s1$-net or s2-net, we could obtain the more general equation as shown in (3). □

Lemmas 1 and 2 give the minimum number of power nets to satisfy the power pitch constraint and signal shielding constraints, respectively. In order to satisfy both constraints, we have the following Theorem:

Theorem 1. *For a routing region R_t with two edge power nets, given the routed m_2 $s2$-nets, m_1 $s1$-nets, m_0 $s0$-nets, and the minimum number of power nets p_t for power integrity constraints, then among all valid track assignment solutions, the tight upper bound on the minimum number of power nets is given as follows*:

$$S_t = \begin{cases} m_2 + \left\lceil \frac{m_1}{2} \right\rceil, & m_1 \geqslant 2 \cdot (p_t + 1), \\ p_t + m_2 + 1, & m_1 < 2 \cdot (p_t + 1), \left\lceil \frac{m_1}{2} \right\rceil + m_2 \geqslant p_t, \\ p_t + m_2, & m_1 < 2 \cdot (p_t + 1), \left\lceil \frac{m_1}{2} \right\rceil + m_2 < p_t. \end{cases} \quad (4)$$

Proof. We first prove that the Eq. (4) is indeed an upper bound on the minimum number of power nets. We then prove that this upper bound is also very tight compared to the known lower bound in most cases.

The first part can be proved by constructing a valid track assignment solution for every possible scenario, and the so obtained valid track assignment solution gives an upper bound on the minimum number of power nets for that scenario. For example, in the scenario where the number of $s1$-nets m_1 is great than $2 \cdot (p_t + 1)$, we can construct a valid track assignment solution as follows: (1) according to Lemma 1, we uniformly layout $(p_t - 1)$ power nets in R_t to satisfy the power pitch constraint, as the two edge power nets are counted as one in S_t because they are shared between adjacent routing regions; (2) we then put as many as $2 \cdot p_t$ $s1$-nets adjacent to the already layout p_t power nets to satisfy these $s1$-nets' shielding constraint. Note that each of the two edge power nets only contribute one-side shielding effect for these $s1$-nets; (3) after step (2), we have $m_1' = m_1 - 2 \cdot p_t$ $s1$-nets left, which is greater than 2, i.e., $m_1' \geqslant 2$. Then according to Lemma 2, we need additional $m_2 + \lceil \frac{m_1'}{2} \rceil$ power nets to satisfy the remaining signal nets' shielding constraints. Moreover, the above procedures are always feasible provided that the routing region has no overflow. Therefore, the total number of power nets S_t is the summation of power nets used in the above three steps in obtaining a valid track assignment solution, which is $p_t + m_2 + \lceil (m_1 - 2 \cdot p_t)/2 \rceil = m_2 + \lceil m_1/2 \rceil$. By taking similar procedures for all other scenarios, we can obtain the formulae given by Eq. (4) accordingly. Therefore, (4) indeed gives an upper bound on the minimum number of power nets in order to satisfy both power and signal integrity constraints.

We now prove that (4) is also a very tight upper bound compared to the known lower bound. It is obvious that Lemmas 1 and 2 are two known lower bounds on the number of power nets for any valid track assignment solution in R_t. The maximum of the two, i.e., $\max(p_t, S_t^{si})$, results in a tighter lower bound. If a valid track assignment solution can achieve this tighter low bound, then it must also have the minimum number of power nets. The gap between the upper bound (4) and this tighter lower bound indicates how tight our upper bound is. For example, for the same scenario we discussed above, the tighter lower bound is given by $\max(p_t, S_t^{si}) = S_t^{si} = m_2 + \lceil m_1/2 \rceil$, which is exactly what (4) gives. Therefore, in this scenario, the upper bound is also the tightest (optimal) upper bound. For all other scenarios, we can similarly show that the upper bound is also very tight.[3] □

One example obtained by the above procedures is shown in Fig. 3, where solid squares are power nets and others are signal nets, and the numbers above signal nets are their shielding requirements.

5. GSPR algorithm

The overall GSPR algorithm is illustrated in Fig. 4. The algorithm is composed of two major parts: (1) power integrity aware multilevel signal routing; (2) power network synthesis and track assignment to satisfy both power and signal integrity constraints. The essence of our GSPR algorithm is to pre-allocate routing resources for power network design during the signal routing stage, while finalize the power network design after signal routing. Below we discuss each part in detail.

[3]Note that the power net estimation Eq. (4) will be used in our following power and signal network co-design framework, and it is sufficient for (4) to give a tight upper bound, not necessary the tightest upper bound. Moreover, we have assumed that the minimum power pitch is less than the routing tile pitch in Theorem 1. But it is straightforward to extend the results to the case when the minimum power pitch is larger than the routing tile pitch by following similar arguments as shown in the proof.

Fig. 3. A valid track assignment solution with a minimum number of power nets ($p_t = 3$).

```
//Power integrity aware multilevel signal routing
Construct routing Graph;
For each level at the coarsening stage
  For each local critical net N_i
    Pattern routing N_i;
    If not possible, mark it as failed;
For each level at the uncoarsening stage
  For each un-routed/failed net N_i
    Global maze routing N_i;
    Refine routed nets if necessary;
Rip-up and reroute;
//Power network synthesis and track assignment
Global power network synthesis;
For each routing region
  Synthesis local power network;
  Track assignment for power and signal nets;
```

Fig. 4. The GSPR algorithm overview.

5.1. Introduction to multi-level routing

Routing techniques have been studied in [18] for congestion minimization, in [17,19] for performance optimization, and in [20,21] for crosstalk minimization. However, all of these algorithms run directly on a flat routing models, and may suffer the scalability problems for large designs. Moreover, all of these works have not consider power integrity constraints yet. In the following, we present a novel multilevel power integrity aware signal routing algorithm by utilizing the estimation formula developed in Theorem 1.

To better understand the multi-level routing algorithm, we have to mention the hierarchical routing algorithms [22–24]. The hierarchical routing algorithm was proposed to address the scalability problem for large designs. Instead of running the routing algorithms directly on a flat routing models, i.e., finding paths for all nets on the finest tiles, the hierarchical routing algorithm builds the routing graph hierarchically. At the highest level, a coarsest routing graph is used to find routing paths for nets that only appear in that coarsest level while all nets below the current level are not considered. At the next level, the original routing problem is broken down into a set of sub-routing problems that work on different routing graphs expanded from the upper level coarse grids. For each individual sub-routing problems, the same procedure can be repeated hierarchically. Therefore, at each hierarchical routing level, only a constant size routing graph needs to be considered for routing, and the problem size will not grow as much as the design does. However, because the hierarchical algorithm ignores all lower level nets' congestion effect when it works at the higher level routing graph, it may make a wrong routing decision to route a high level net into routing regions that might become very congested due to those neglected lower level nets. As there is only one pass that goes from the highest level to the lowest level, there is no way for the hierarchical routing algorithm to correct such a mistake later on.

The multi-level routing algorithm [25–27] remedies this problem by introducing an additional planning pass that goes from the lowest level to the highest level at the beginning. To distinguish itself from the hierarchical routing, the multi-level routing algorithm calls the newly introduced planning pass as "coarsening", while the original hierarchical pass as "uncoarsening" borrowing terms from the multi-grid method, a numerical method that accelerates the solution of partial differential equations [28]. In the coarsening process, fine routing tiles are recursively merged into coarser tiles. At each coarsening stage, the routing resources for tiles defined in the current level are estimated. The coarsening process stops when the number of tiles in the coarsest level is less than a certain threshold. The purpose of coarsening is to obtain a relatively accurate congestion estimation for higher level routing decision. The uncoarsening process is to determines a tile-to-tile global routing solution hierarchically based upon the congestion information obtained from coarsening.

5.2. Power integrity aware multilevel signal routing

According to Fig. 4, after building the routing graph, we start our power integrity aware multilevel routing algorithms from coarsening the finest tile at level 0. At each coarsening level, only critical nets belonging to the current level are routed. Pattern routing [29] is employed in coarsening stage for speed consideration. To choose a pattern among all L-shaped and Z-shaped patterns, we define the following cost function for each path P_e:

$$cost(P_e) = \sum_{\forall t \in P_e} \alpha_t \cdot (G_t + S_t - C_t), \tag{5}$$

where G_t is the number of nets, S_t is the number of power nets, and C_t is R_t's capacity. A dynamic amplification factor (α_t) is used to dynamically adjust the cost function so that we penalize more for a path that tends to cause overflow

[18]. The path cost is the sum of edge costs along the route. A path is *overflow* if any edge in P_e has overflow. We choose a pattern that minimizes the cost function (5) without overflow. If we cannot find such a pattern during coarsening, we mark it as *failed net* and it will be refined during the uncoarsening stage. When we compute the cost function (5), we apply the power net estimation equation from Theorem 1 for each routing region. By doing this, we reserve an appropriate number of tracks for power nets during routing, and take into consideration the shielding requirements for both signal shielding and power pitch constraints. Because of this, our routing algorithm is power integrity aware.

The uncoarsening stage refines each local failed nets and all other un-routed nets starting from the coarsest level. For better routability, the routed nets from coarsening procedures can also be modified if such a modification results in less congestion. In our current implementation, maze routing algorithm is employed to route local nets belonging to the current level during uncoarsening. The same cost function as in (5) is employed, and we confine the maze search scope within the tile defined by the current level and do not allow overflow.

If after uncoarsening, there are still un-routed nets, rip-up and reroute will be used to find a minimum cost route. Maze routing with the searching space defined in the whole chip is used and we allow overflow at this stage. We shall point out that our multilevel framework does not depend on what specific routing algorithms are used. Pattern routing and maze routing are two possible choices chosen for our current implementation.

5.3. Power network synthesis and track assignment

We propose to synthesize the global power network by a hierarchical two-step procedure. We first synthesize a coarse level global power network such that there are two power nets along the two edges of every routing region. By synthesizing the coarse level global power network this way, we decouple the whole chip power network design problem into a series of independent fine level power network synthesis problems; and more importantly, we satisfy the pre-condition of Theorem 1, which is used in the cost function for our power integrity aware signal routing. We then synthesize the fine level power network and track assignment within each routing region simultaneously. As track assignment is performed within each routing region, and the number of power nets used is no more than what we have reserved, iteration is not required. The optimal fine level power network and track assignment solution in each routing region is decided by Theorem 1. The algorithmic implementation of this step is the same as the constructive proof procedures of Theorem 1.

6. Experiment results

The proposed co-design of power network and signal network has been implemented in C++ on Linux. Ten large industrial benchmarks from the ISPD'98 IBM benchmark suite [30] are employed to show the applicability of our algorithm to real designs. The benchmarks are placed by DRAGON [31]. In our current implementation, two preferred routing directions are assumed for all regions, one for horizontal wires and the other for vertical wires. Because there is no shielding information about nets in the original benchmark, we assume that 10% nets are $s2$-nets and 10% nets are $s1$-nets for all benchmarks. We assume the required power pitch ($\overline{PGP}$) for all benchmarks is 10 according to a typical industrial design. The characteristics of the benchmarks are shown in Table 1.

Table 1
Benchmark settings

Ckts	Net #	Pin #	Grid
IBM01	13 056	44 266	64 × 64
IBM02	19 291	78 171	80 × 64
IBM03	26 104	75 710	80 × 64
IBM04	31 328	89 591	96 × 64
IBM05	29 647	124 438	128 × 64
IBM06	34 935	124 399	128 × 64
IBM07	46 885	244 369	192 × 64
IBM08	49 228	198 180	192 × 64
IBM09	59 454	187 872	256 × 64
IBM10	72 760	269 000	256 × 64

As we pointed out in Section 1, there are very limited work on power and signal network co-design in literature. Therefore, a direct comparison between our work and an existing work is not possible. Nevertheless, to show the effectiveness of our approach, we implemented a three-step algorithm similar to [3] as our comparison base. The three-step algorithm is as follows: route the critical signal nets along with their required shields, synthesize a power network considering shield sharing, and then route the non-critical nets. The track assignment solution in step one is decided in a greedy fashion and explicit power nets are inserted whenever the power-pitch constraint is violated in step two. Because our GSPR algorithm can optimize the shield sharing in each region while the three-step algorithm cannot, the latter is expected to consume more power nets than the former. Moreover, because of more shields, step three might obtain a routing solution with many detours. Routing detours is equivalent to more routing bends or longer routing lengths. A bend in a routing path indicates that a via may be introduced during detailed routing. Vias not only cause congestion for detailed routing, but also deteriorate chips' reliability. Therefore, in a routing solution, the smaller the bend number, the better.

We compare the experiment results between our GSPR algorithm and the three-step algorithm in Table 2. Columns 5 and 10 of Table 2 are the final power network area (PG_{area}) given by (2). According to the results, we observe that under the same power and signal integrity constraints, the GSPR algorithm consumes less power network area for all benchmarks than the three-step

Table 2
Experiment results, where numbers in parentheses are reductions of the GSPR algorithm over the three-step algorithm in percentage

1	2	3	4	5	6	7	8	9	10	11
Test	Three-step algorithm					GSPR algorithm				
Ckts	max *Den*	*Bend #*	*Seg #*	PG_{area}	Time	max *Den*	*Bend #*	*Seg #*	PG_{area}	Time
IBM01	0.83	28 478	63 955	33 563	63.2	1.00	26 227 (−7.9%)	62 255 (−2.7%)	22 921 (−31.7%)	37.5
IBM02	0.82	94227	177 657	67 911	127.1	0.87	87 999 (−6.6%)	173 693 (−2.2%)	54 476 (−19.8%)	73.8
IBM03	0.82	81 148	153 735	66 381	120.1	0.84	75 329 (−7.2%)	150 995 (−1.8%)	51 450 (−22.5%)	68.6
IBM04	0.82	79 337	171 601	79 856	114.6	0.80	72 241 (−8.9%)	168 387 (−1.9%)	61 315 (−23.2%)	66.4
IBM05	0.83	409 305	653 752	191 661	451.6	0.82	381 037 (−6.9%)	646 994 (−1.0%)	167 198 (−12.8%)	246.7
IBM06	0.82	174 652	295 150	112 642	177.1	0.88	163 990 (−6.1%)	289 980 (−1.8%)	92 965 (−17.5%)	102.8
IBM07	0.86	216 602	385 113	147 832	173.2	0.92	202 349 (−6.6%)	378 045 (−1.8%)	116 095 (−21.5%)	102.9
IBM08	0.90	229 288	427 669	154 048	207.9	0.94	214 366 (−6.5%)	421 483 (−1.4%)	122 825 (−20.3%)	123.3
IBM09	0.82	257 902	437 863	190 499	197.3	0.92	241 648 (−6.3%)	427 519 (−2.4%)	147 738 (−22.4%)	115.8
IBM10	0.79	326 648	607 843	240 002	255.7	0.81	305 568 (−6.5%)	597 621 (−1.7%)	198 729 (−17.2%)	150.6
Average							−6.7%	−1.7%	−19.4%	

algorithm. Take benchmark *IBM*03 for an example, the three-step algorithm needs 66 381 power nets, while the GSPR algorithm only needs 51 450 power nets, and the relative saving is 22.5%. On average, GSPR can reduce power net area by 19.4% when compared to the three-step algorithm. This observation is expected, and it convincingly shows us that the GSPR algorithm can utilize the limited routing resource more economically than the three-step algorithm.

We further compare the signal routing quality in terms of the maximum density (max *Den*), total number of bends (*Bend*), and total number of segments (*Seg*) (or equivalently, normalized routing length) in Table 2. According to columns 2 and 7 of Table 2, all benchmarks have max $Den \leqslant 1$, therefore, both algorithms can complete routing without causing overflow. However, when compared to the three-step algorithm, the GSPR algorithm always achieves less number of bends and smaller routing length. The reduction of number of bends and routing length on average are 6.7% and 1.7%, respectively. This observation shows that because of the earlier power net estimation and reservation, the GSPR algorithm cannot only reduce the final power net area, but also improve the final routing quality.

We also compare the runtime in seconds in column 6 and 11 of Table 2. According to the runtime results, the GSPR algorithm uses less runtime than the three-step algorithm, and the overall speedup is about 2x.

7. Conclusion and discussion

We have presented a novel design methodology to the co-design of power and signal networks under integrity constraints. Experiment results using large industrial benchmarks have shown that compared to the best alternative design methodology [3], the proposed method can reduce the power network area by 19.4% on average with better routing quality but use less runtime.

To handle the high complexity resulted from combining the power and signal network designs, we employed the high abstract yet effective power integrity model (power pitch model) and signal integrity model (shielding requirements for nets) [1,3]. However, we recognize that these models are conservative for real designs. For example, to reduce crosstalk, it is not necessary to shield critical nets from the source to the sinks. In the future, we will develop similar high abstract level but more accurate models for both power integrity and signal integrity, and apply them to our multilevel routing framework. Moreover, in this paper, we only synthesized an extended global routing with track assignment for both signal and power networks, but not detailed signal routing and power network design. In the future, we will develop detailed routing algorithms for both signal and power networks with accurate parasitic extraction, and present experiment results on the comparison between the high abstract level integrity model and the SPICE simulation.

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